ELECTRICAL ENGINEERING

A RADIATION-HARDENED-BY-DESIGN CHARGE PUMP FOR PHASE-LOCKED LOOP CIRCUITS

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Thesis under the direction of Professor Lloyd Massengill

Single-event transients (SETs) due to terrestrial or space radiation exposure have become a growing concern in modern high-speed analog and mixed-signal electronics. Recent work with computer circuit-level simulation techniques has enabled the understanding of SET effects in mixed-signal and radio-frequency (RF) applications such as the phase-locked loop (PLL). Furthermore, a PLL radiation sensitivity weak point has been identified as the conventional current-based charge pump (CP), with ion strikes in the CP resulting in at least two orders of magnitude higher output phase displacement than any other module within the PLL.

This thesis presents a CP topology as a novel method to solving this critical SET problem with the potential of significantly improving overall PLL resistance to SET effects. A method of PLL design employing a tri-state, voltage-based charge pump (V-CP) circuit has been implemented that significantly hardens the PLL to SET effects. Simulations and experimental testing have been performed on PLL circuits designed and fabricated in the IBM 130nm CMRF8RF CMOS technology available through the MOSIS foundry system. Analysis of the measured PLL output error signatures is used to

quantify the relative hardness of PLL circuits implementing a V-CP stage over a conventional CP module, demonstrating a maximum of 2.3 orders of magnitude improvement in the SET response. The design effectively eliminates the charge pump as the most susceptible element in the PLL; as a result, this hardened design technique, which can be applied to other PLL topologies, provides SE performance that is orders of magnitude better than typical PLL designs.

Approved by:

Dr. Lloyd Massengill

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CHAPTER I

INTRODUCTION

Single-event effects (SEEs) for many space and military environments have been a growing concern for electronics, especially in modern integrated circuits (ICs) where increased susceptibilities to SEEs have been reported as device feature sizes decrease and operating frequencies increase [1, 2]. A single-event (SE) occurs when a high energy ionizing particle, such as a heavy ion, bombards with the circuit. As the particle penetrates the semiconductor material it looses energy through Coulombic interactions with the lattice structure and leaves a dense track of electron-hole pairs in the material. These excess carriers can be collected on circuit nodes and result in undesirable circuit responses which can vary depending on the circuit topology, the amount of charge deposited, and the amount of charge collected on the circuit node [3, 4].

One type of effect resulting from SEs in an IC is a single-event transient (SET). SETs are undesirable asynchronous signals that can propagate through signal paths and result in a variety of circuit responses. In digital circuits, an SET can result in a single-event upset (SEU), that is, an alteration of the state of memory circuits (e.g. a memory cell can be changed from a “0” state to a “1” state). The SEU can lead to a circuit error if the corrupted data propagates throughout the circuit and is visible at the output. In analog and mixed-signal applications, however, the definition of a SEU is dependant on the topology and type of circuit. Over the years a wide variety of experimental procedures [5-10] and computer simulation techniques [11-15] have been utilized to further the

understanding of the SET phenomenon in digital, analog, and mixed-signal applications. Furthermore, the combination of experimental testing and simulation efforts has enabled an understanding of SEEs that experimental testing alone did not provide [16]. Recent work with computer circuit-level simulation techniques has enabled the understanding of SET effects in mixed-signal and radio-frequency (RF) applications such as the voltage-controlled oscillator (VCO) and the phase-locked loop [17-19].

Phase-locked loops (sometimes termed bit synchronization circuits, or clock-recovery circuits) are widely used in commercial and space-deployed electronics systems to reduce the phase delay associated with the distribution of clock signals, to generate high-speed clock signals, and to synchronize data transfer [20, 21]. Since PLLs have been identified as SE vulnerable circuits in space-deployed electronics, there is a growing interest on the impacts SETs in the PLL can have on circuit designs that utilize PLLs for clock signals [22]. Furthermore, previous work has identified a PLL radiation sensitivity weak point as the conventional current-based charge pump (CP), with ion strikes in the CP resulting in at least two orders of magnitude higher output phase displacement than any other module within the PLL [18, 19].

Charge pump circuits are used to convert the phase difference between the generated clock signal and the reference signal into an electrical current. Simulations show that a single ion strike in the output stage of the CP can deposit enough charge to significantly alter the frequency of the generated clock signal [18]. Furthermore, the maximum number of erroneous (missing or additional) clock pulses on the output of the PLL resulting from strikes in the CP is at least one order of magnitude greater than strikes occurring in any of the other modules of the PLL [19].

This thesis presents a CP topology as a novel method to solving this critical SET problem with the potential of significantly improving overall PLL resistance to SET effects. A method of PLL design employing a tri-state, voltage-based charge pump (V-CP) circuit [23] has been implemented that significantly hardens the PLL to SET effects. Simulations and experimental testing have been performed on PLL circuits designed and fabricated in the IBM 130nm CMRF8RF CMOS technology available through the MOSIS foundry system. Analysis of the measured PLL output error signatures is used to quantify the relative hardness of PLL circuits implementing a V-CP stage over a conventional CP module, demonstrating a maximum of 2.3 orders of magnitude improvement in the SET response. The design effectively eliminates the charge pump as the most susceptible element in the PLL; as a result, this hardened design technique, which can be applied to other PLL topologies, provides SE performance as measured by the output phase displacement that is orders of magnitude better than typical PLL designs. In addition, the significant improvement in the overall SE performance of the PLL has exposed the vulnerability of other PLL components, such as the voltage-controlled oscillator (VCO), that have previously been thought of as having an insignificant impact on the overall susceptibility of the PLL to SETs.

CHAPTER II

THE PHASE-LOCKED LOOP

Circuit Topology Description

The phase-locked loop (PLL) considered in this work is an all-CMOS variant designed in the IBM 130 nm CMRF8RF process available through the MOSIS foundry system and consists of four main components: the phase-frequency detector (PFD), the charge pump (CP), the low-pass filter (LPF), and the voltage-controlled oscillator (VCO), displayed in Figure 1. Detailed schematics of the PFD and VCO components can be found in Appendix A. In addition, the PLL was designed for a range of operation between 150 MHz and 1 GHz with a 400 MHz center frequency of operation (frequency at which $V_{inVCO} = V_{dd}/2$).

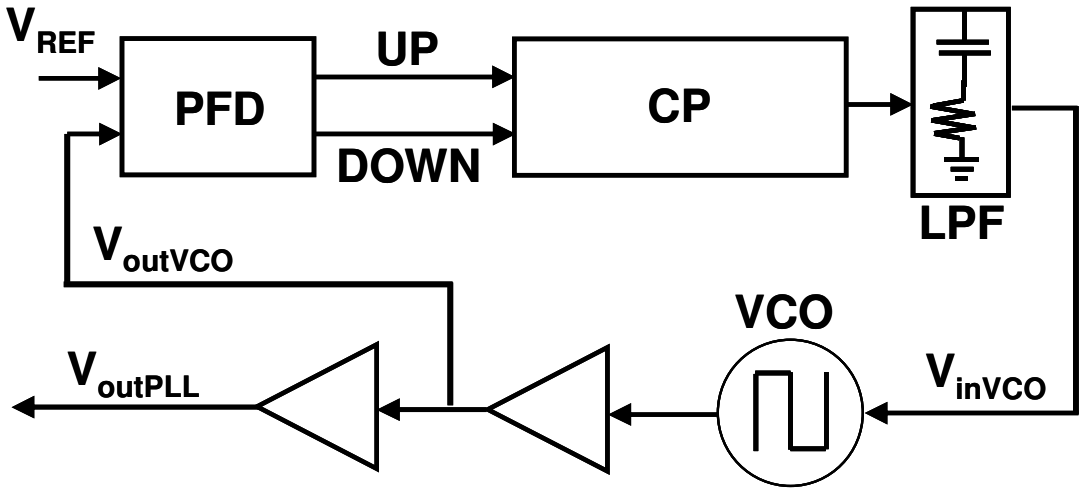

Figure 1. Block diagram of the PLL, consisting of a phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), and voltage-controlled oscillator (VCO). An "e-graded" buffer was implemented in order to account for loading effects.

The PLL is a closed loop system that implements negative feedback in order to synchronize an output signal (V_{outVCO}) to a reference signal (V_{REF}) as shown in Figure 1. On start-up the PFD compares the phase and the frequency of the input reference signal (V_{REF}) to the output signal of the VCO (V_{outVCO}). When V_{outVCO} is lagging (leading) V_{REF} in phase and frequency, an output pulse will be generated on the UP (DOWN) output of the PFD. This leads the CP module to source (sink) charge to (from) the LPF, thus changing the LPF output voltage (V_{inVCO}) and adjusting the output frequency of the VCO [17, 18].

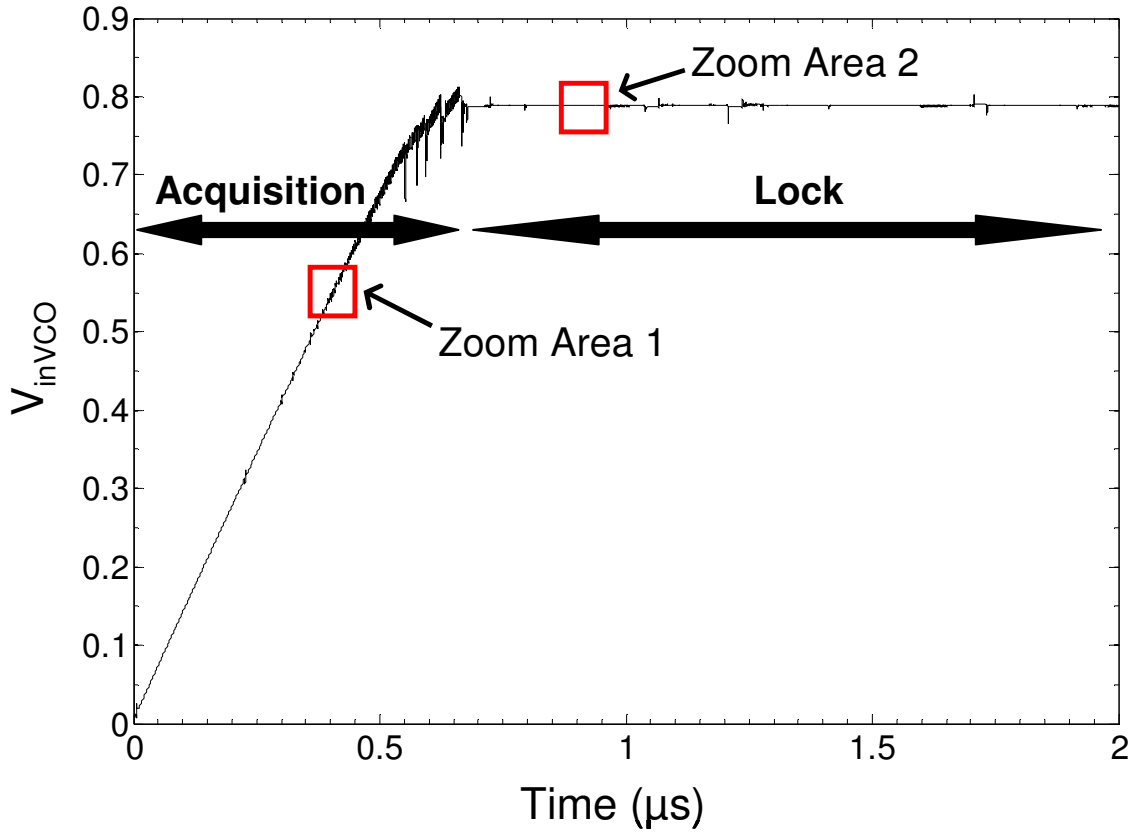

Figure 2. Acquisition and lock curve: V_{inVCO} vs. time for 700 MHz operation. The reference and output signals represented by the highlighted boxes (*Zoom Area 1* and *Zoom Area 2*) are displayed in Figures 3 and 4.

PLL Electrical Characteristics and SET Sensitivity

When analyzing the electrical performance of the PLL, the input of the VCO (V_{inVCO}) can be a useful metric. Figure 2 shows the acquisition curve of the PLL for 700 MHz operation. The acquisition or tracking period denotes the time period when V_{outVCO} is lagging (leading) in frequency and phase when compared to the input reference signal, V_{REF} (Figure 3). The voltage at the input of the VCO changes with every clock cycle as the PFD continues to compare the leading edges of the signals, and the CP continues to source (sink) current to (from) the LPF. Once the phase and frequency of V_{outVCO} and V_{clock} are identical, V_{inVCO} should ideally remain constant indefinitely as the PLL is in the lock state (Figure 4).

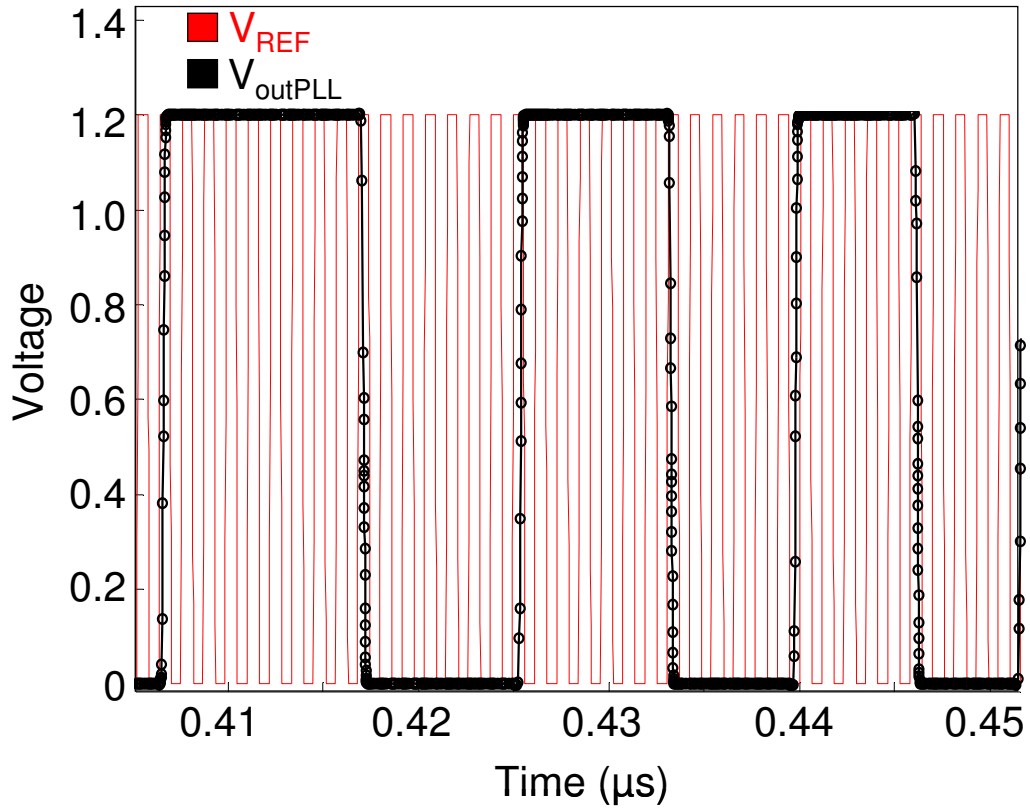

Figure 3. V_{REF} and V_{outPLL} during the acquisition period as indicated in *Zoom Area 1* of Figure 2.

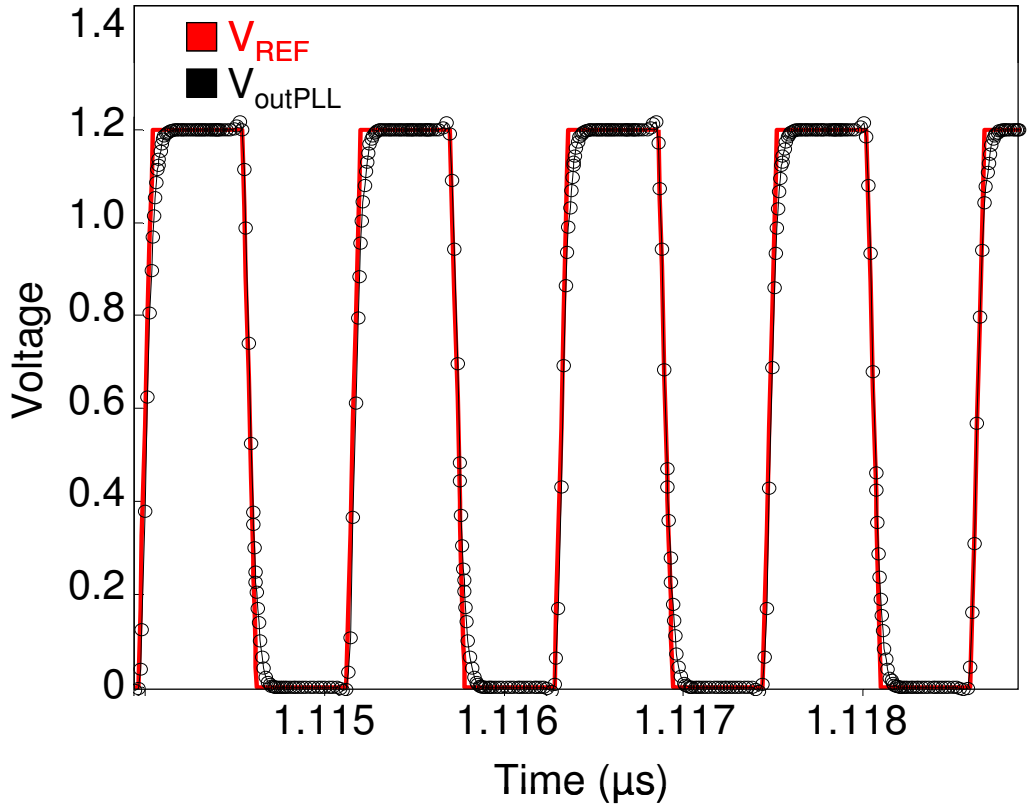

Figure 4. V_{REF} and V_{outPLL} during the lock period as indicated in *Zoom Area 2* of Figure 2.

Recent work has identified the CP module as the most sensitive component of the PLL to SEs [18]. Figure 5 displays the schematic representation of the CP and notes the six vulnerable transistors in the output stage. As the output stage of the CP is directly connected to the capacitive node of the LPF (V_{inVCO}) a SE strike in this sector will either deplete or deposit charge on the LPF capacitors, thus directly affecting V_{inVCO}. The rate at which this deposited charge is removed by the CP determines the SE response of the PLL. Most modern CPs are current-based (the sourcing and sinking of charge is carried out by current-sources) and current-based charge pumps are primarily used over voltage-based charge pumps to reduce the phase jitter associated with power supply fluctuations.

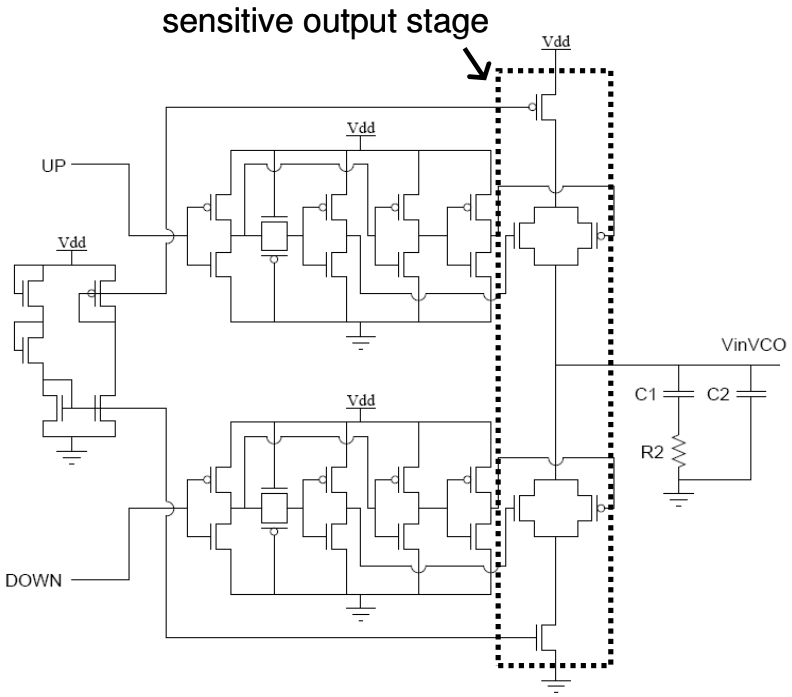

Figure 5. Schematic representation of the charge pump and low-pass filter module. Sensitive nodes are in the output stage consisting of two current sources and two transmission gates [18].

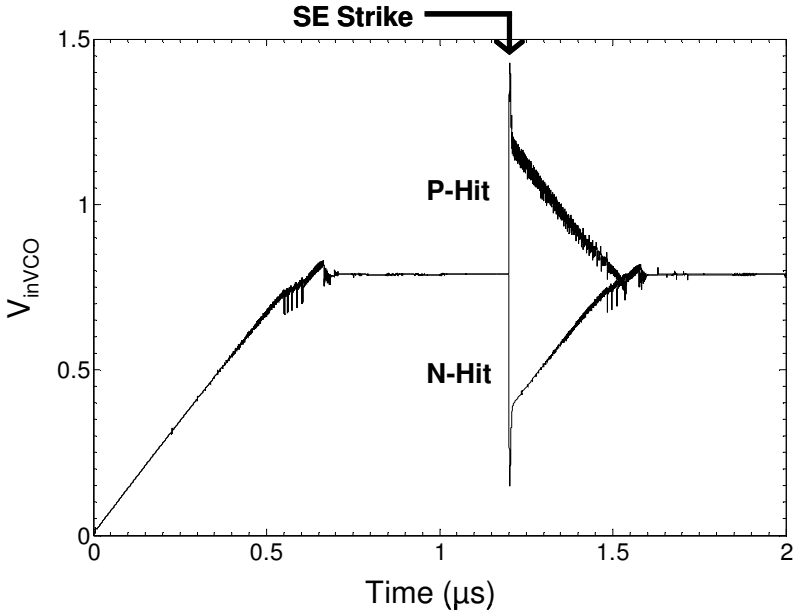

Figure 6. V_{inVCO} vs. time for 700 MHz operation. SETs occur at 1.2 µs and span over approximately 280 clock cycles, resulting in approximately 120 erroneous clock pulses [19].

Figure 6 illustrates an example of the voltage perturbations that occur on V_{inVCO} as a result of ion strikes depositing 200 fC of charge for 700 MHz of operation [19]. A P-Hit is a strike on a PMOS transistor whereas an N-Hit is a strike on an NMOS transistor. The simulated strikes result in a maximum voltage perturbation of 0.64 V and a maximum time of recovery of 0.4 μs. The illustrated SET spans approximately 280 clock cycles and results in approximately 120 erroneous clock pulses in the output of the PLL. A P-Hit will result in an increase in the frequency of operation, thus additional pulses and an N-Hit will result in missing clock pulses as it will temporarily decrease the frequency of the VCO.

The current sources determine the rate at which the charge is removed from the hit node in the CP. Bigger current sources have a better SE response as the restoring current drive will be greater and the overall response time of the PLL will be less. The response time of the PLL can be described by the natural frequency (ω_{nCP}), represented by equation (2.1) where K_{VCO} is the gain of the PFD (radians/V-s), and C_1 is the LPF capacitance [20]. PLLs are customarily designed such that ω_{nCP} is as large as possible such as to minimize the response time of the loop, maximize the pull-in and lock-ranges of the PLL, and minimize the pull-in and lock-in times. Thus increasing the charge pump current, I_{ch}, will also result in an increased natural frequency.

$$\omega_{nCP} = \sqrt{\frac{I_{ch} \cdot K_{VCO}}{2\pi \cdot C_1}} \quad \text{(radians/s)} \tag{2.1}$$

As increasing I_{ch} will result in an increased natural frequency, adjusting ω_{nCP} will subsequently modify the damping ratio, ξ, given by equation (2.2) [20].

$$\zeta_{CP} = \frac{\omega_{nCP}}{2} \cdot RC_1 \tag{2.2}$$

Typically, the damping ratio is designed to be approximately 1 such that the system is critically damped. Decreasing the damping ratio will result in increased ringing and overshoot in the loop's transfer characteristics, thus resulting in increased jitter and unstable PLL operation. Alternatively, increasing the damping ratio will result in a roll-off of the loop's transfer equation and diminish the bandwidth of the PLL.

CHAPTER III

THE TRI-STATE VOLTAGE-BASED CHARGE PUMP

Introduction

The basic premise behind the proposed tri-state voltage-based CP (V-CP) and LPF design, schematically represented in Figure 7, is to reduce the number of vulnerable nodes present in the CP, increase the rate of charge sourcing and sinking, improve operational performance of the PLL, and provide a mechanism to isolate the vulnerable nodes from the SE sensitive capacitive nodes of the LPF. The V-CP is implemented using two transmission gates that are controlled by "dead-zone" circuitry to ensure simultaneous switching. In addition, a series resistance, R_1, is used to isolate V_{lpf} in the V-CP from V_{inVCO} in the LPF.

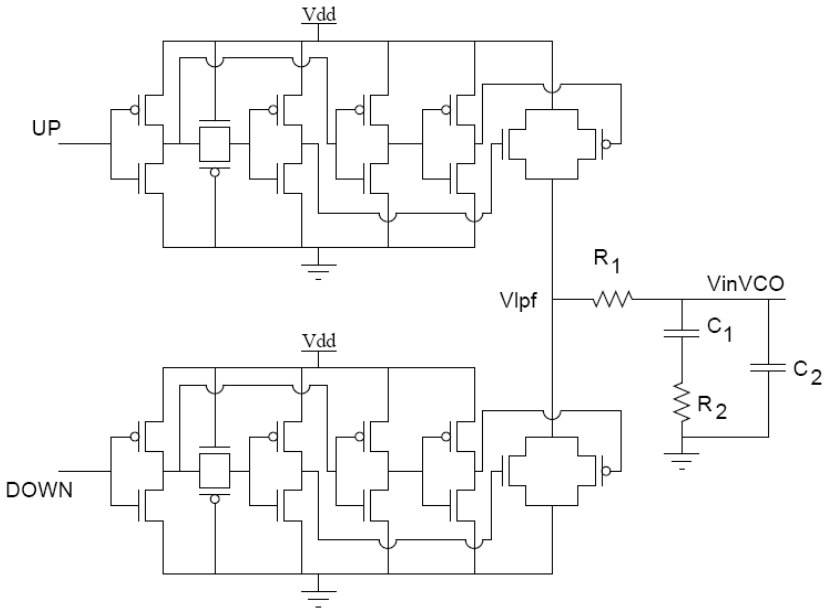

Figure 7. Schematic representation of the tri-state voltage-based charge pump and LPF [19].

Electrical Characteristics, Closed-Loop Requirements, and LPF Design

A V-CP can improve the speed of the acquisition since the current is not limited to a fixed value set by current sources, provided an appropriate resistor value for R_1 is chosen. Upon start-up, a large amount of current can flow from the V-CP into the LPF to quickly raise the voltage applied to the VCO. However, as the current magnitude depends strongly on the voltage on the LPF capacitors, a voltage increase on V_{inVCO} will decrease the current flow, resulting in a non-linear response in the acquisition period. This large initial current may cause voltage spikes in the power supply node, and care must be taken to ensure safe operation against it.

An analytical model has been developed to determine the electrical parameters (pull-in and lock-in times, pull-in and lock-in ranges, settling speed, phase margin, and jitter) of the proposed design. The natural frequency, which represents the response time of the loop, can then be used to derive the lock and pull-in times, and the lock and pull-in ranges of the PLL. Appendix B presents the corresponding equations for the electrical parameters. It is customary to design a PLL with as large a natural frequency as possible, thus gaining a greater improvement in lock and pull-in time, and lock and pull-in ranges. Equation (3.1) represents the natural frequency of the PLL implementing the V-CP.

$$\omega_{nVCP} = \frac{1}{2}\sqrt{\frac{V_{DD} \cdot K_{VCO}}{\pi \cdot (R_1 + R_2) C_1}} \quad \text{(radians/s)} \tag{3.1}$$

The parameter, K_{VCO}, is the gain of the VCO module and R_1, R_2, C_1, and C_2 are the components in the LPF as shown in Figure 7. As the CP is limited by the amount of current from the fixed current sources, the RC time constant must be small in order to achieve a large natural frequency. However, by implementing a V-CP, more flexibility in

the RC time constant can be achieved while still maintaining a large natural frequency. A large RC time constant is necessary in order to limit the amount of initial current flow upon PLL start-up and will also provide for further SET mitigation, as will be explained in Chapter IV.

Furthermore, the design of the loop filter has a major influence on the stability of the PLL's electrical performance. The damping factor, noted as equation (3.2), represents the loop's stability. By choosing a damping factor, ξ, of approximately 1 and using equation (3.1) for the natural frequency, the capacitors C_1 and C_2, and resistors R_1 and R_2 can be selected. In addition, the capacitors C_1 and C_2 are designed such that C_1 is ten times larger than C_2 in order to minimize the jitter [18, 21].

$$\zeta_{VCP} = \frac{\omega_{nVCP}}{2} R_2 C_1 = \frac{R_2 C_1}{4} \sqrt{\frac{V_{DD} \cdot K_{VCO}}{\pi \cdot (R_1 + R_2) C_1}} \tag{3.2}$$

The LPF parameters in this design were chosen by selecting C_1, C_2, and R_2 from the previously published work [18] and by choosing R_1 in order to achieve the desired damping factor. Additionally, the PLLs were designed with the IBM 130nm CMRF8RF process available through the MOSIS foundry system. The acquisition curve for the PLL implementing the V-CP is compared to the curve for the CP in Figure 8. In the selected figure, the acquisition time was improved by 50 % by implementing the V-CP over the CP at 700 MHz, indicating an approximate doubling of the natural frequency [19].

Conclusion

The tri-state or voltage-based charge pump (V-CP) and corresponding LPF was utilized in order to improve fundamental PLL design parameters. By implementing the V-CP the locking time was decreased by 50 %. The decreased lock time is an effect of the increased natural frequency and the improvement in the rate of charge sourcing and sinking. An additional advantage is the flexibility gained in designing the RC time constant of the loop filter. As the RC time constant is less of a limiting factor in achieving a high natural frequency in V-CP PLLs, the RC time constant can be increased significantly in order to limit the effects of power supply spikes and SEs while still maintaining an improvement in the PLL's lock time.

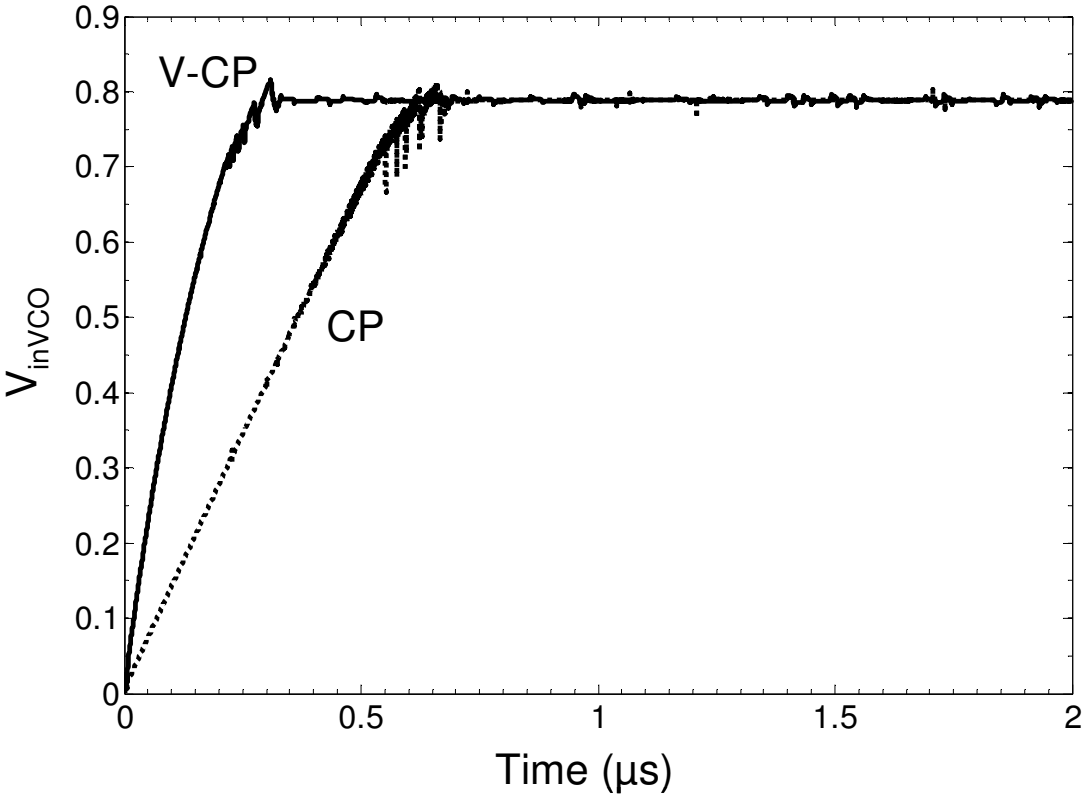

Figure 8. V_{inVCO} vs. Time. The acquisition curves illustrating the improved lock-in time of the PLL implementing the V-CP over the CP [19].

CHAPTER IV

SET SIMULATION RESULTS

Single-event transient (SET) simulations were performed on the PLL circuits using the CADENCE EDA tool suite, the SPECTRE environment, and calibrated IBM CMRF8RF 130nm MOSIS device models. Charge collection from heavy-ion strikes were simulated using a double-exponential current source injected into the circuit with time constants calibrated to the drift and diffusion processes affecting the free-carriers in the technology nodes of study [18] (Appendix D). The PLL circuits were simulated at 160 MHz, 400 MHz, 700 MHz, and 850 MHz for deposited charges of 50 fC, 100 fC, 200 fC, and 500 fC. The maximum voltage perturbations of V_{inVCO} were recorded for all cases. In addition, the outputs of the PLLs were recorded in order to examine the phase displacement and the number of erroneous clock pulses as a result of the voltage perturbation encountered on V_{inVCO}. Four metrics were considered in the SET analysis of the PLL: the amount of voltage perturbation on V_{inVCO}, the time for V_{inVCO} to recover to its locked voltage, the phase displacement of V_{outPLL}, and the maximum number of erroneous pulses (missing or additional) in the output of the PLL.

The voltage perturbations resulting from P-Hits depositing 200 fC of charge on comparable nodes for the V-CP and CP are shown in Figure 9. The voltage perturbation (ΔV) of V_{inVCO} from a strike in the CP was 640 mV, while the ΔV from a strike in the V-CP was 42 mV, resulting in approximately 93% improvement. Simulations were also completed for strikes depositing 50 fC, 100 fC, 200 fC, and 500 fC for frequencies

ranging from 160 MHz to 850 MHz. The responses of strikes depositing 500 fC in the V-CP for the above stated frequency range is shown in Figure 10. The maximum ΔV observed for strikes in the V-CP was 55 mV while the current-based CP displayed a worst case ΔV of 1.54 V when 500 fC was deposited. In addition to the voltage perturbation of V_{inVCO}, the maximum time to recovery (Δt) for the V-CP was 162 ns as compared to 1.03 μs for the CP – an 84 % improvement in recovery time [19].

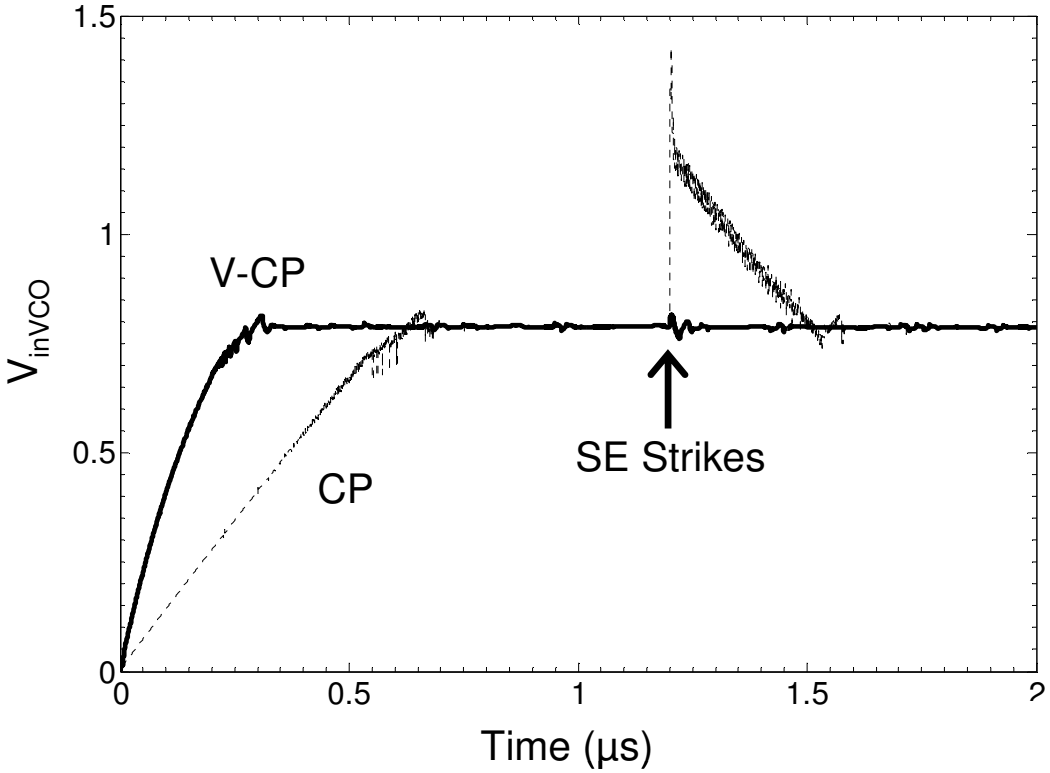

Figure 9. V_{inVCO} vs. Time: The acquisition curves illustrating the voltage perturbation resulting from SE strikes depositing 200 fC of charge in the V-CP and the CP for 700 MHz operation [19].

The improved hardness of the PLL implementing a V-CP derives from the implementation of the resistance R_1 to isolate the deposited charge from V_{inVCO}. Two mechanisms occur following a strike to allow for fast recovery of V_{inVCO}. First, the

change in V_{inVCO} is fed back to the V-CP activating the current sourcing/sinking mechanism. As the current dissipation is not limited by the current source transistors as in the CP, a large amount of charge may be transferred per clock cycle, and the time to recovery is decreased. Another single-event mechanism for deep-sub-micron technology is the (V_{dd} + V_{DIODE}) voltage resulting at the hit node. This increased potential creates a forward biased junction between the drain and the substrate of the struck device, creating a current path, thus sinking/sourcing additional charge and improving the time to recovery.

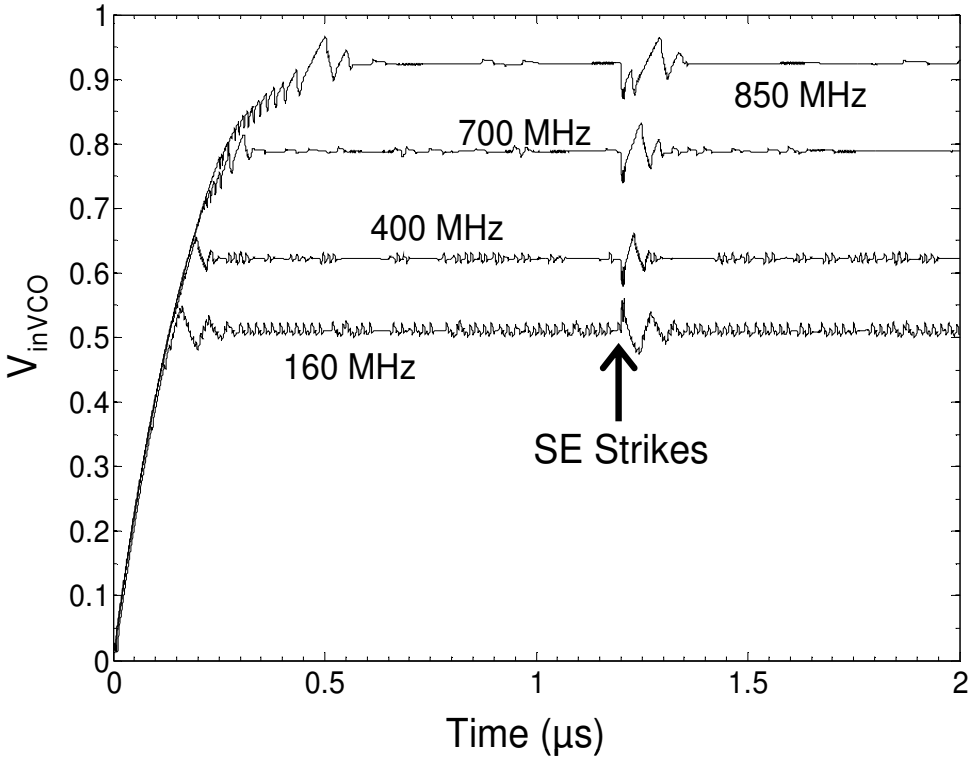

Figure 10. V_{inVCO} vs. Time for 160 MHz, 400 MHz, 700 MHz, and 850 MHz operation. SE strikes depositing 500 fC of charge in the V-CP occur at 1.2 µs. The worst-case voltage perturbation is 55 mV and time to recovery is 162 ns [19].

Additional metrics that can be useful in examining the response of the PLL to SEs in the V-CP are the number of erroneous pulses and the amount of phase displacement present in V_{outVCO}. The number of erroneous pulses is defined as either missing or additional pulses and the phase displacement is the amount of phase shift that occurs in the rising edge of the PLL's output signal. For the SE strike to cause an erroneous pulse a phase displacement of at least 2π radians (360 degrees) must occur.

Figure 11 shows an example of V_{outPLL} and the input reference signal for a P-Hit in the V-CP depositing 200 fC. During the entire event, V_{outPLL} did not lead the reference signal in phase by more than 90 degrees. Full recovery of the locking condition occurs at 98 ns and there are no erroneous pulses observed.

The maximum phase displacement versus frequency resulting from strikes in the CP, V-CP, and the VCO is shown in Figure 12. For 500 fC of deposited charge in the CP approximately 418 erroneous pulses were observed at 850 MHz, corresponding to a phase displacement of approximately 2626 radians. The lowest number of erroneous pulses occurred at 400 MHz with 274 pulses (approximately 1722 radians) [19].

Approximately 2 orders of magnitude improvement in maximum phase displacement was achieved when implementing the V-CP/LPF. Only 1 erroneous pulse – 6.28 radians of phase displacement – was observed at 850 MHz and no erroneous pulses were observed at 160 MHz, 400 MHz, and 700 MHz operation. In addition, for 500 fC of deposited charge, the maximum phase displacement and the number of erroneous clock pulses resulting from strikes in the V-CP is approximately one order of magnitude lower than those resulting from strikes in the VCO [19].

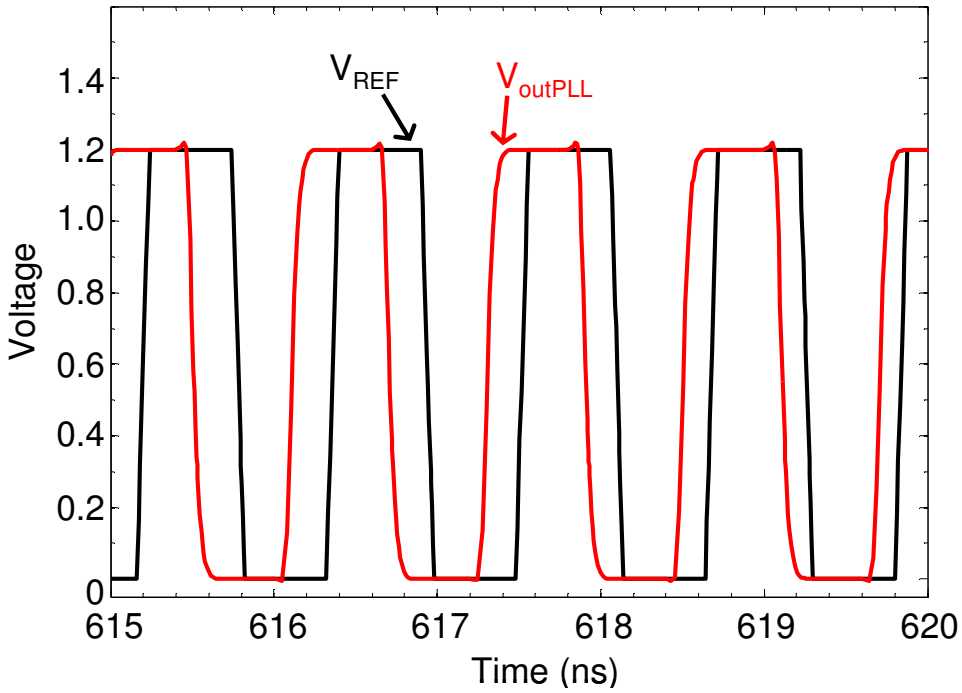

Figure 11. V_{outPLL} and V_{REF} vs. Time: V_{outPLL} leads in phase by a maximum of 90 degrees for a strike of 200 fC at 700 MHz. Full recovery of the lock condition occurs at 98 ns.

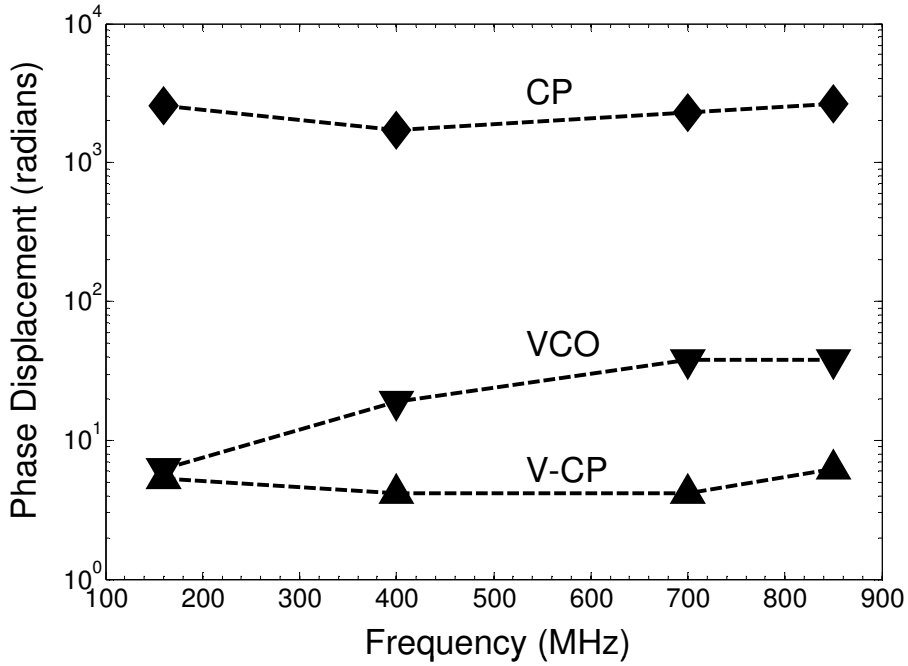

Figure 12. The maximum phase displacement vs. frequency for SE strikes depositing 500 fC of charge in the CP, VCO, and V-CP. At least 2 orders of magnitude improvement is achieved by the V-CP over the CP [19].

CHAPTER V

TWO-PHOTON LASER EXPERIMENTAL RESULTS

Introduction

Two phase-locked loop (PLL) topologies were designed and fabricated for SET testing with the two-photon absorption (TPA) technique. Both PLLs consisted of the four primary components as stated in Chapter II and displayed in Figure 1: the phase-frequency detector (PFD), charge pump, low-pass filter (LPF), and voltage-controlled oscillator (VCO). Furthermore, the first PLL was implemented with a standard current-based charge pump module (CP) while the second PLL was implemented with a voltage-based charge pump (V-CP).

The VCO circuits for the experiments were designed to achieve a center frequency (frequency at which $V_{inVCO}=V_{dd}/2$) of approximately 200 MHz. The maximum frequency for the VCO in the PLL implementing the CP (CPLL) was measured to be approximately 530 MHz whereas the maximum frequency measured for the PLL implementing the V-CP (VPLL) was measured to be approximately 600 MHz. For both PLL circuits, the locking range was between approximately 40 MHz and 350 MHz. Figure 13 illustrates the measured transfer characteristics (frequency versus V_{inVCO}) of the VCO circuits and indicates the PLLs' locking range. Although the maximum frequencies of the VCO circuits varied slightly, the operating ranges of the PLLs were closely matched, thus a direct comparison between the circuits can be made.

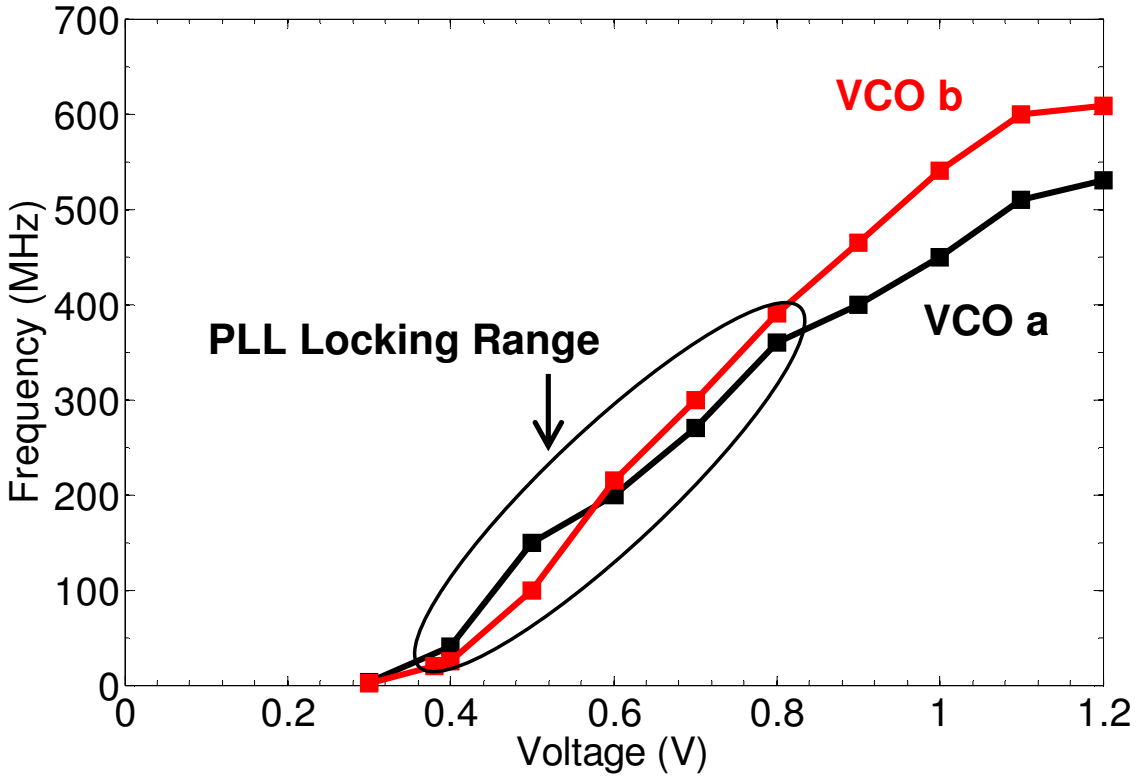

Figure 13. Transfer curves of the VCO circuits. The center frequencies were approximately 200 MHz and the maximum frequencies were between 500 MHz and 600 MHz. The PLLs' locking ranges were between approximately 40 MHz and 350 MHz.

Experimental Details

Recently, a new method of laser-induced carrier generation for SEE applications based on two-photon absorption (TPA) using high peak power femtosecond pulses at sub-bandgap optical wavelengths has been demonstrated [10, 24]. For excitation by two-photon absorption, the laser wavelength is chosen to be less than the bandgap of the semiconductor material, such that no carriers are generated (no optical absorption) at low light irradiances. At sufficiently high irradiance, however, the material can absorb two photons simultaneously to generate a single electron-hole pair [25, 26]. Because carrier

generation in the two-photon process is proportional to the square of the laser pulse irradiance (I), significant carrier generation occurs only in the high-intensity focal region of the focused laser pulse [10, 25, 26].

A primary motivation for the development of the TPA SEE technique is its ability to interrogate SEE phenomena through the wafer using backside irradiation. This eliminates interference from the metallization layers that are prevalent in modern devices, and circumvents many of the testing issues associated with flip-chip-mounted parts. In this thesis the through-wafer TPA SEE technique is utilized to investigate the SET response of PLL circuits.

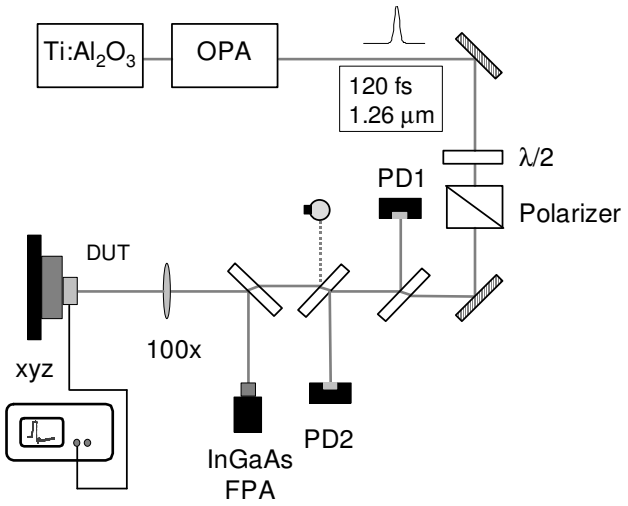

Figure 14. TPA SEE experimental setup. Ti:Al_2O_3; amplified, modelocked titanium-sapphire laser; OPA: optical parametric amplifier; λ/2: half-wave plate; PD1, PD2: large-area calibrated InGaAs photodiodes; FPA: focal plane array [10, 24].

The TPA SEE experimental setup is illustrated in Figure 14 [10, 24]. The SET experiments at wavelengths below the silicon bandgap were performed using an amplified titanium sapphire laser system that pumps a tunable optical parametric amplifier and produces 120 fs optical pulses at 1.26 µm with about 10 µJ of energy per

pulse. The strong IR beam is attenuated by a waveplate-polarizer combination to precisely control the pulse energy incident on the device under test (DUT). The pulse energy is monitored with a calibrated large area InGaAs photodiode (PD2).

The DUT is mounted on a motorized *xyz* translation platform with 0.1 µm resolution, and the optical pulses are focused through the wafer onto the front surface of the DUT with a 100x microscope objective, resulting in a near-Gaussian beam profile with a diameter of 1.6 µm at focus [10]. Because the carrier deposition varies as I^2, this corresponds to a Gaussian carrier density distribution with a 1.1 µm diameter (full-width-at-half-maximum). All experiments were performed at room temperature. The DUT was imaged through the wafer using near-infrared (NIR) imaging optics in conjunction with an InGaAs focal plane array (Indigo Alpha NIR).

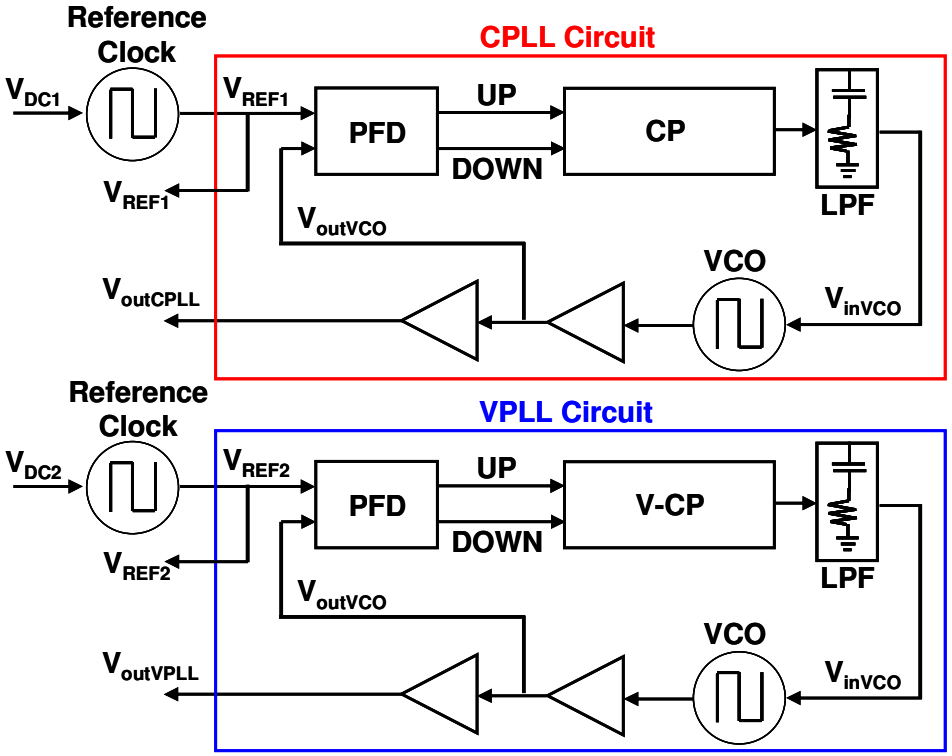

Figure 15. General block diagram of the DUT.

The DUT, illustrated in Figure 15, included two PLL circuits (the CPLL and VPLL) and two additional VCO circuits to serve as the reference signals. For both PLLs the reference signals (V_{REF1} and V_{REF2}) and the outputs ($V_{outCPLL}$ and $V_{outVPLL}$) were bonded to output pads. Five additional n-diffusions with a minimum area of 1µm x 1µm were included in the layout of the PLL designs to provide targets for the laser irradiation and had minimal effects on the circuits' operation. The diffusion areas were tied to nodes within the circuits that were pre-determined through simulations [19] to be the most sensitive nodes in each component. Figure 16 illustrates the circuit schematic of the VCP and indicates the node of the strike location. Appendix A displays the circuit schematics of the VCO and CP and similarly indicates the strike locations. One target was included for each VCO; two were provided for the CP module, and one for the V-CP component. Furthermore, Figure 17 displays an image of the VCO circuit for the CPLL captured by the Indigo Alpha NIR imaging optics and indicates a strike location connected to the output of an inverter stage within the VCO.

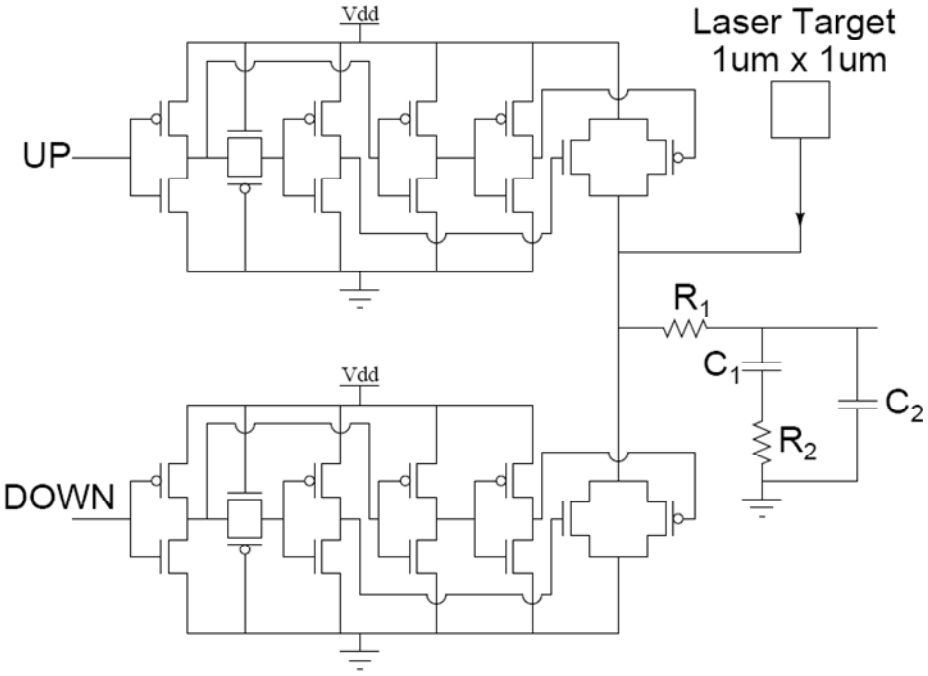

Figure 16. Schematic of the V-CP circuit indicating the location of the 1µm x 1µm diffusion area used for the laser strikes.

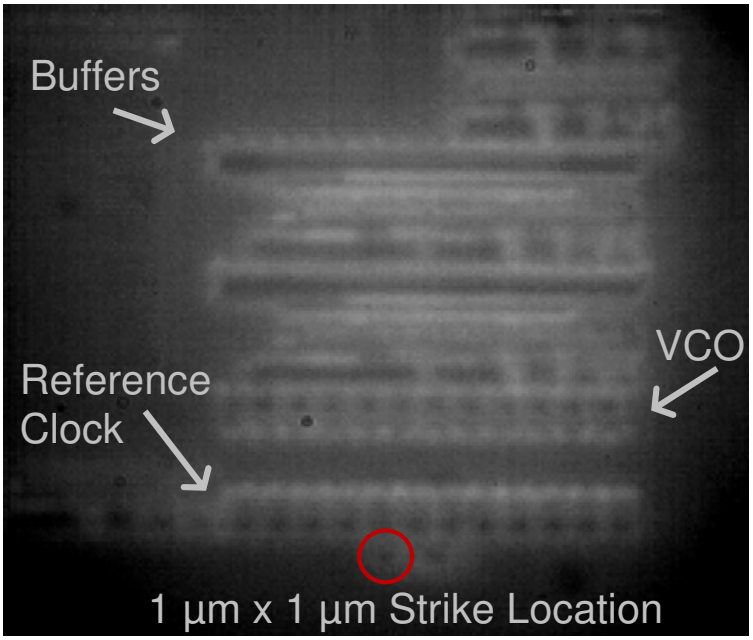

Figure 17. Die photo of one strike location tied to a node in the VCO circuit located in the CPLL. Also indicated is the reference VCO and output buffers.

Experimental Results

During steady-state operation, the output of the PLL was locked to the phase and frequency of the reference signal. As explained in Chapter IV, a SE occurring within the PLL was expected to cause either a frequency modulation of the output signal or an oscillation failure [17-19]. By monitoring and comparing both the reference signal and the PLL output signal, the number of erroneous (missing or additional) pulses present in the output of the PLL following a strike could be extracted.

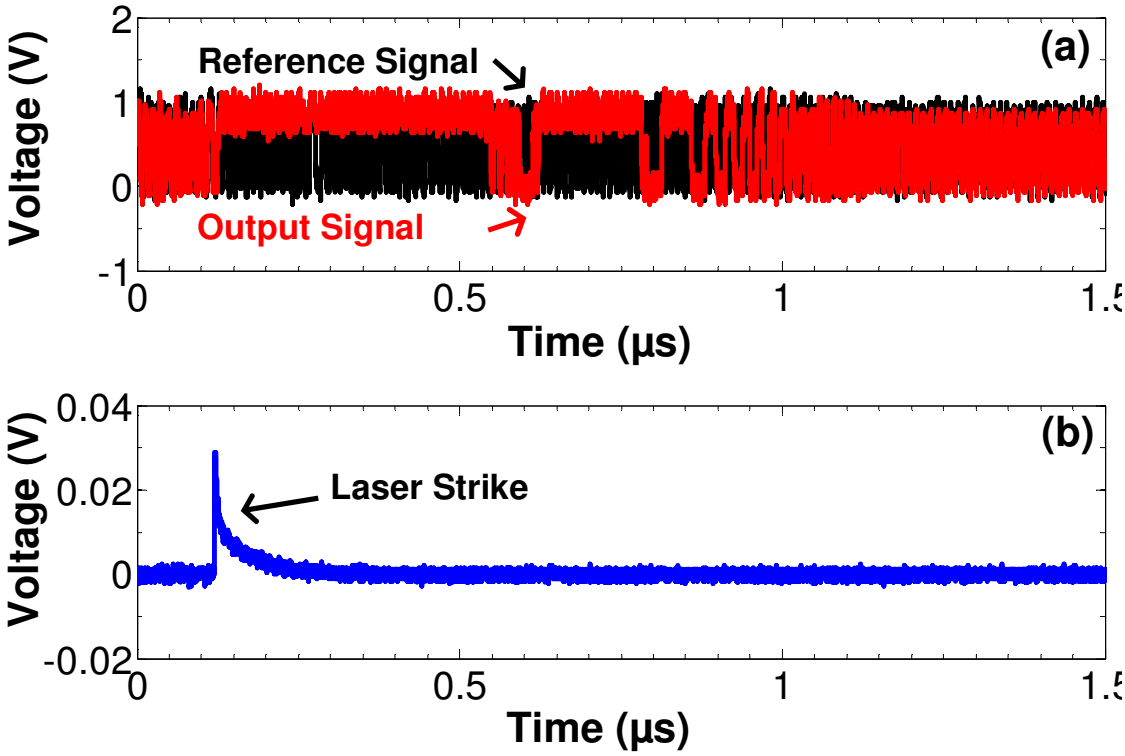

Figure 18. (a) The reference and output signals versus time following a laser strike of energy 30 nJ in the CP component of the CPLL at 200 MHz. (b) Voltage representation of the laser strike. The voltage can be converted to energy using the following relationship: 1.2 nJ/mV.

Data was collected for a total of ten laser strikes per strike location for varying input bias conditions (V_{DC1} and V_{DC2}) representing various frequencies of PLL operation. For all strikes the reference signal and the PLL's output signal were recorded following the strike until the PLL returned to its locked state. Figure 18 illustrates an example of the reference and output signals following a laser strike with energy 30 nJ in the CP component of the CPLL. The PLL looses lock as the output frequency is reduced following the strike. Subsequently, the frequency gradually increases until the PLL returns to the locked state.

The maximum number of erroneous pulses in the outputs of the CPLL and VPLL following strikes in the CP, VCO, and V-CP modules are displayed in Figure 19 versus the frequency of operation on a semi-log scale. Strikes in the CP resulted in a maximum of 2.3 orders of magnitude more erroneous pulses than strikes in the V-CP, and between 1 to 2 orders of magnitude more erroneous pulses than strikes in the VCO. This result illustrates the reduced vulnerability of PLL implementing the V-CP over the CP. For the CP, the maximum number of erroneous pulses (3745 missing pulses) occurred at 140 MHz and resulted from strikes on the output node. The maximum in the VCO and V-CP circuits occurred at 200 MHz with 54 erroneous pulses and 290 MHz with 35 missing pulses, respectively. The average number of erroneous pulses versus frequency is plotted in Figure 20. In agreement with the results in Figure 19 the mean number of erroneous pulses was approximately 2 orders of magnitude lower for strikes occurring in the V-CP over the CP. Error bars represent 1 standard deviation from the mean.

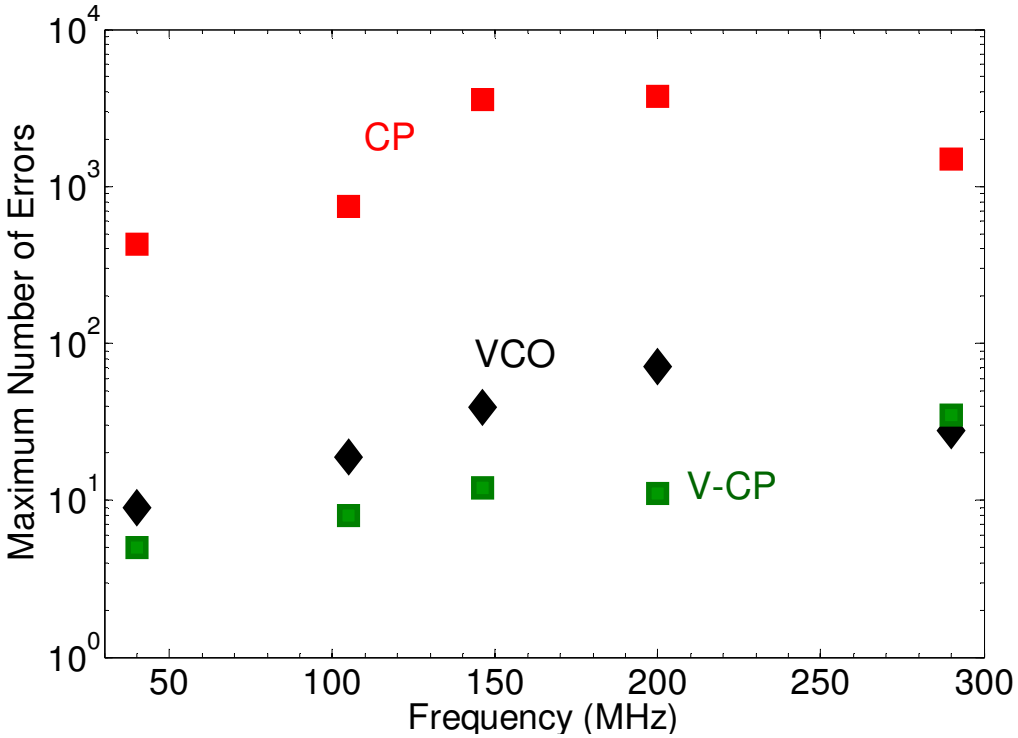

Figure 19. Maximum number of erroneous pulses resulting from strikes of energy 30 nJ in various PLL components.

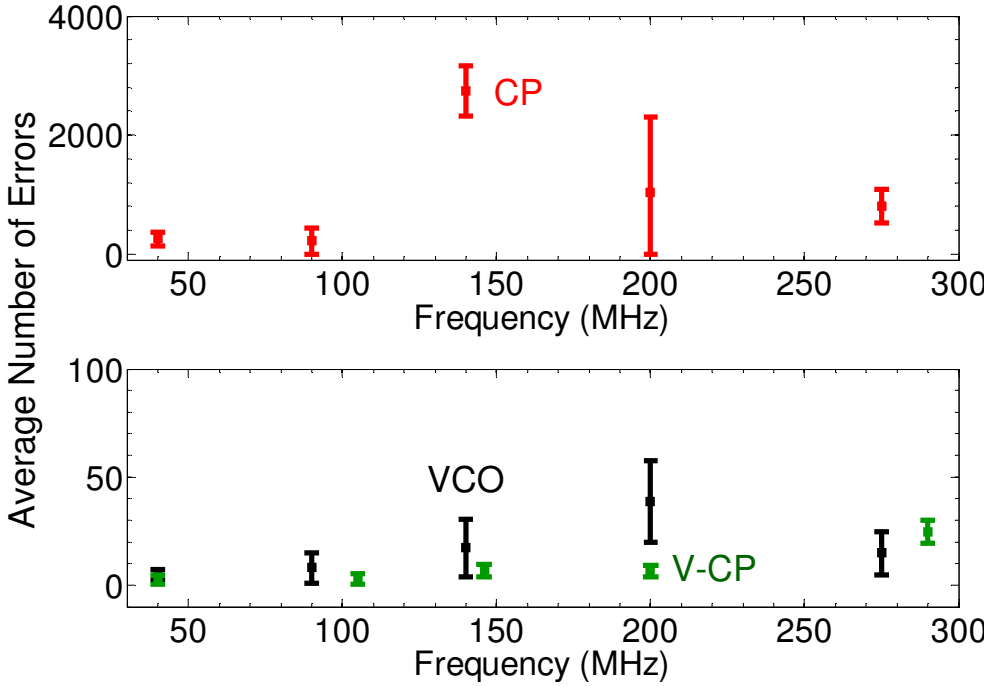

Figure 20. Average number of erroneous output pulses versus frequency for 10 laser strikes of energy 30 nJ in various PLL components. Error bars represent 1 standard deviation away from the mean.

Furthermore, the effects of power supply reduction on the SET sensitivity of the PLL circuits were examined. Figure 21 illustrates the average number of erroneous pulses for the VCO and V-CP in the VPLL circuit when operating at two different supply voltages. For the VCO, the reduction in the power supply resulted in an increased vulnerability to SEs. Although the frequency of oscillation decreased due to the lower drive current, the restoring drive of the VCO responsible for the SET recovery also decreased, resulting in an overall increase in the number of errors. This result is consistent with previous studies that show an increased sensitivity to SEs with power supply reductions [27].

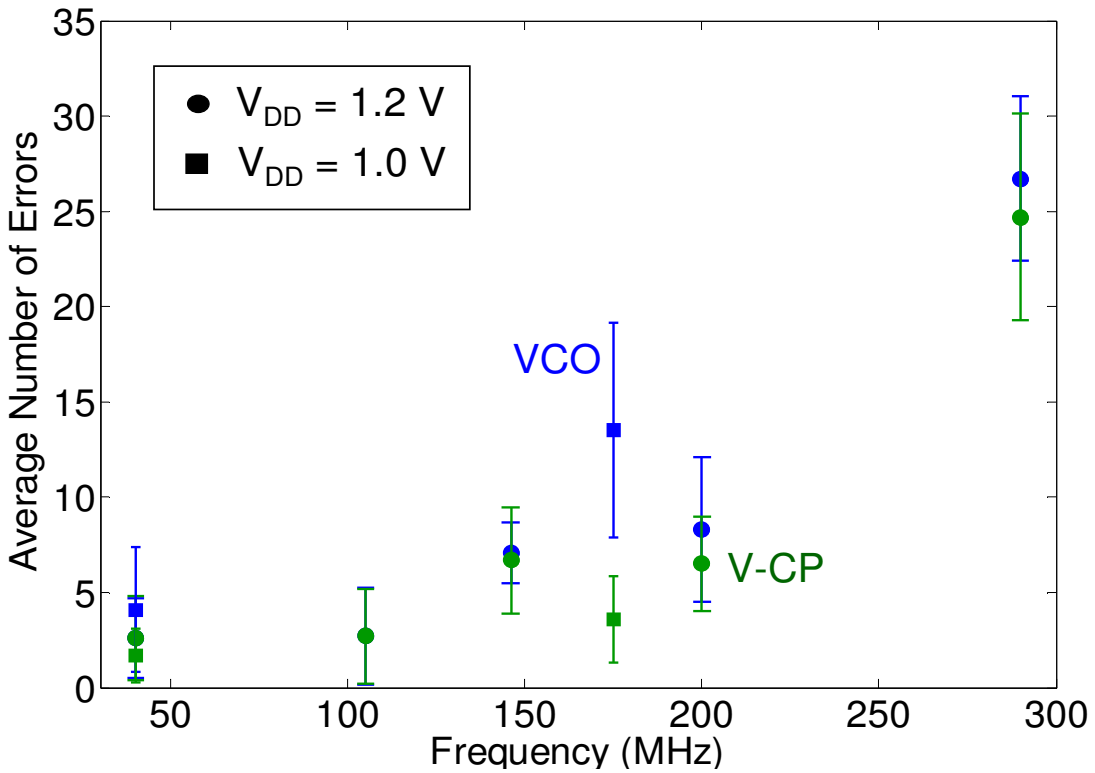

Figure 21. Average number of erroneous pulses versus frequency for various power supply voltages in the VCO and V-CP of the VPLL circuit.

Conversely, the response of the PLL to strikes in the V-CP was a slight decrease in the overall susceptibility to SEs. This result indicates that the reduction in the power supply has a minimal effect on the response of the PLL to strikes in the V-CP module. Although the natural frequency was reduced due to the reduction of the power supply voltage, the frequency of operation was also reduced. The minimal effects of the power supply reduction suggest that the reduction in frequency is the dominant contributor to the change in the SET response of the PLL for strikes in the V-CP component.

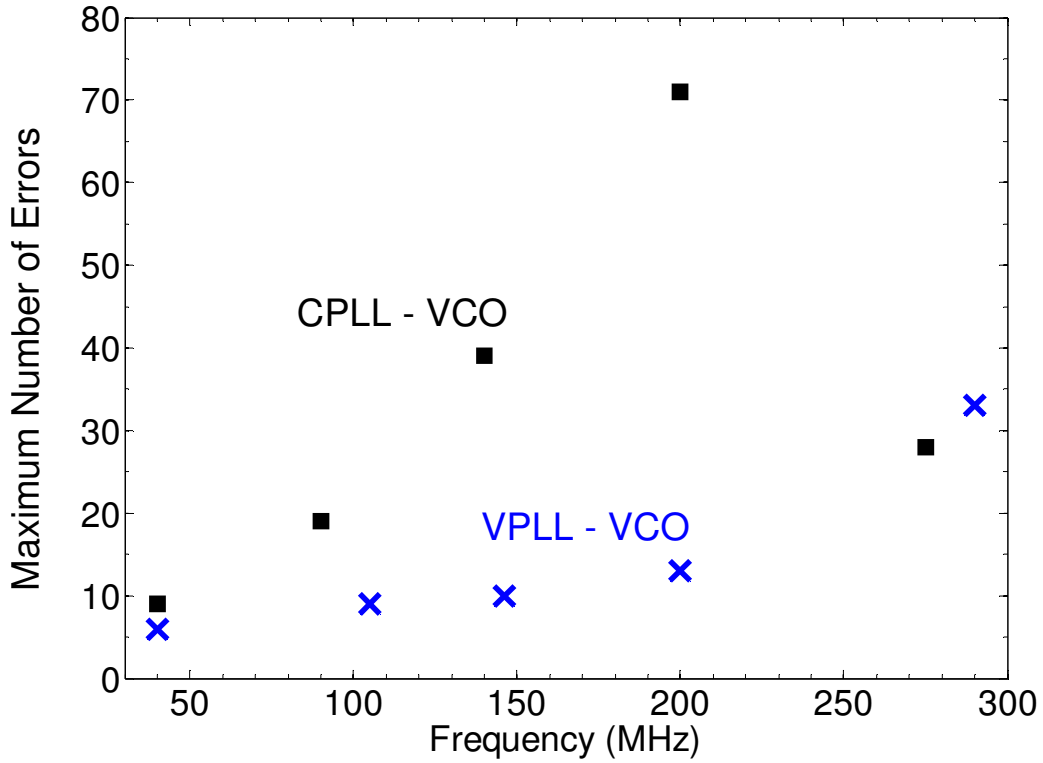

Figure 22. Maximum number of erroneous pulses versus frequency in the outputs of the CPLL and VPLL for strikes in the VCOs.

An additional effect observed is illustrated in Figure 22 where the number of erroneous pulses in the PLLs' outputs was compared for strikes in the VCOs. Although the VCOs were identical, the slope of the number of erroneous pulses versus frequency

was greater for the CPLL than the VPLL. This result indicates the improved response time of the PLL implementing the V-CP over the CP. As a strike in the VCO will directly affect the output frequency, thus activating the PFD and charge pump components in attempt to counteract the effects of the SE, an improved response time of the loop will decrease the amount of time for the PLL to recover. The decreased slope of the VPLL is due to the increased natural frequency and improved damping when implementing the V-CP over the CP [19] and confirms the improved SE performance of the voltage-based charge pump.

Conclusion

Two phase-locked loop (PLL) topologies were designed and fabricated for SET testing with the two-photon absorption (TPA) technique. The first PLL was implemented with a standard current-based charge pump module (CP) whereas the second PLL was implemented with a voltage-based charge pump (V-CP). Analysis of the SE error signatures shows a maximum improvement of 2.3 orders of magnitude as measured by the number of erroneous clock pulses resulting from laser strikes in the V-CP over the CP. The significant improvement in the response of the V-CP to SETs reduced the number of erroneous clock pulses due to strikes in the V-CP below those generated by strikes in the VCO module.

Furthermore, the improvement in the electrical parameters, such as natural frequency and damping, of the PLL implementing the V-CP over the CP were illustrated by examining the number of erroneous clock pulses resulting from strikes in the VCO modules of each PLL. The lower vulnerability of the VCO module implemented in the

V-CP PLL results from the improved response time, thus the increased natural frequency of the PLL.

CHAPTER VI

DESIGN TRADEOFFS AND CONSIDERATIONS

Introduction

Though implementing a V-CP instead of a CP can result in a significant improvement in SET susceptibility, certain electrical performance and design tradeoffs such as phase jitter, resistor design tolerances, and area must be considered before implementing the V-CP in the PLL. In addition, a redundancy technique was examined as a hardening approach. The redundancy technique uses multiple copies of the charge pump and low-pass filter to reduce the effects of an ion hit on a single node. This technique increases the area and power requirements significantly over the original design and the proposed V-CP design. The following section examines in detail the tradeoffs for the V-CP design for important PLL parameters. For all parameters, the proposed V-CP design was superior to the redundancy technique.

Phase Jitter Definition

Phase jitter is a fundamental PLL parameter that represents the amount of phase fluctuation that the PLL's output signal encounters while in the lock state. Many components within the PLL can result in phase jitter (e.g., power supply fluctuations, unmatched current sources in the CP, noise coupled into the LPF), and jitter has been quantified many different ways using numerous techniques [28, 29]. This work quantifies phase jitter as the maximum amount of time variation the rising edge of V_{outPLL}

encounters while in the lock state. We attempt to only separate jitter caused by power supply fluctuations; all other sources of jitter are grouped together into one quantity. A graphical example of our definition of phase jitter is represented in Figure 23.

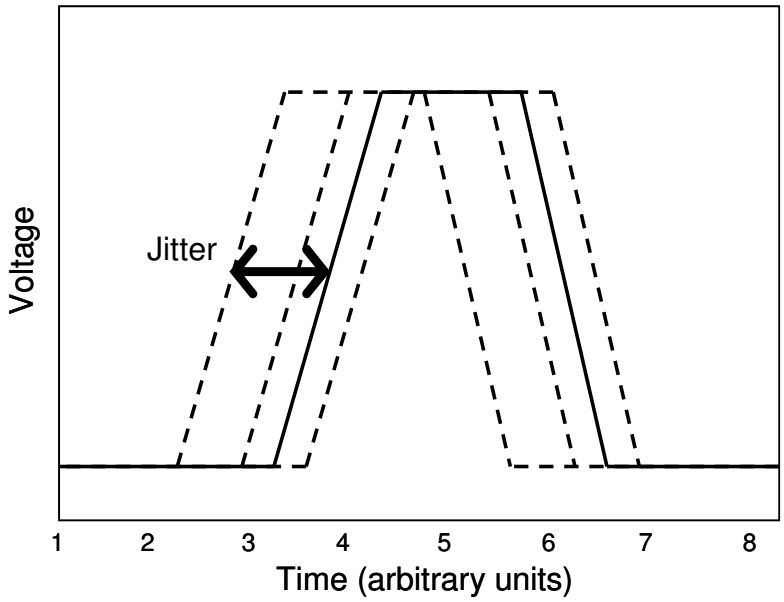

Figure 23. A graphical representation of the phase jitter in the output of the PLL quantified by the maximum amount of time variation in the rising edge of the PLL's output pulse.

CP versus V-CP Phase Jitter Comparison

The primary tradeoff in electrical performance of the PLL is the phase jitter of the output signal. We developed a script that determined the maximum amount of phase jitter that was encountered in the CP and the V-CP during a specified time window. The phase jitter induced by power supply fluctuations was calculated by introducing a 200 mV, 100 kHz oscillating power supply in series with V_{dd}. The maximum jitter of the V-CP (1.07 ns) was determined to be 10 times greater than that of the CP at 400 MHz.

The increased sensitivity of the V-CP to power supply variations is expected and results from the direct connection between the power supply and the LPF capacitors.

The Impacts of Passive Resistance Tolerances on the Electrical Performance of the V-CP

The LPF resistor tolerances are of particular concern to the electrical performance and the SET susceptibility of the PLL. The resistors R_1 and R_2 have a major influence on the natural frequency and locking time of the PLL, as illustrated by equations 2.1, 2.2, 3.1, and 3.2 in Chapters II and III. A larger value of resistance will result in a slower locking time and an increased damping factor. In addition, the value of resistor R_1 has an impact on the SET susceptibility of the PLL. A larger value of R_1 will result in a smaller voltage perturbation of V_{inVCO} and a smaller phase discrepancy at the output of the PLL.

A set of simulations was performed to examine the effects of resistor tolerances on the electrical performance and SET vulnerability of the PLL. The values of resistors R_1 and R_2 were varied by 25 % and every combination of resistor values were simulated for a given set of capacitor values in the LPF. For each simulation, the acquisition time (T_L) and the voltage perturbation (ΔV) resulting from a SE strike depositing 200 fC of charge in the V-CP were recorded for an operating frequency of 700 MHz. Table 1 displays the values of the resistors chosen for this study in addition to the T_L and ΔV resulting from each combination. For all resistor combinations C_1 was 2.4 pF and C_2 was 210 fF.

Results indicate that a 25 % increase (decrease) in R_1 resulted in a maximum of 38 % increase (decrease) in lock time (214.4 ns) and a maximum of 47 % decrease (increase) in voltage perturbation (11.2 mV). The resistor R_2 had a minimal effect on the locking time with a maximum variation within a given value of R_1 of 23.8 %. As the damping factor

depends strongly on the value of R_2 the variation in the locking time resulted primarily from a decrease in the damping factor when R_2 was decreased. The decreased damping factor resulted in an increase in the oscillations of V_{inVCO} before the PLL entered its locked state. Furthermore, the variation of R_2 had a negligible effect on the SET susceptibility of the PLL with a maximum increase in ΔV of 8.2 mV (43 %) when R_2 was decreased by 25 %.

TABLE 1
Effects of Resistance Tolerances on the Electrical and SE Performance of the PLL

R_1(kΩ)	R_2 (kΩ)	T_L (ns)	ΔV (mV)
94 (-25%)	1.8 (-25%)	462.2	30.8
94 (-25%)	2.4 (0%)	443.5	35.5
94 (-25%)	3.0 (+25%)	400.6	31.9
125 (0%)	1.8 (-25%)	697.7	23.2
125 (0%)	2.4 (0%)	563.3	24.2
125 (0%)	3.0 (+25%)	610.2	29.1
156 (+25%)	1.8 (-25%)	886.4	27.2
156 (+25%)	2.4 (0%)	777.7	19.0
156 (+25%)	3.0 (+25%)	654.1	22.1

Figure 24 shows the acquisition and lock curves for all combinations of resistors. The three distinct sets of curves correspond to the different values of R_1. Within each set of curves the fluctuations of R_2 had minimal impacts on the lock time of the PLL. Additionally, the variations in ΔV resulting from the SE strikes were negligible.

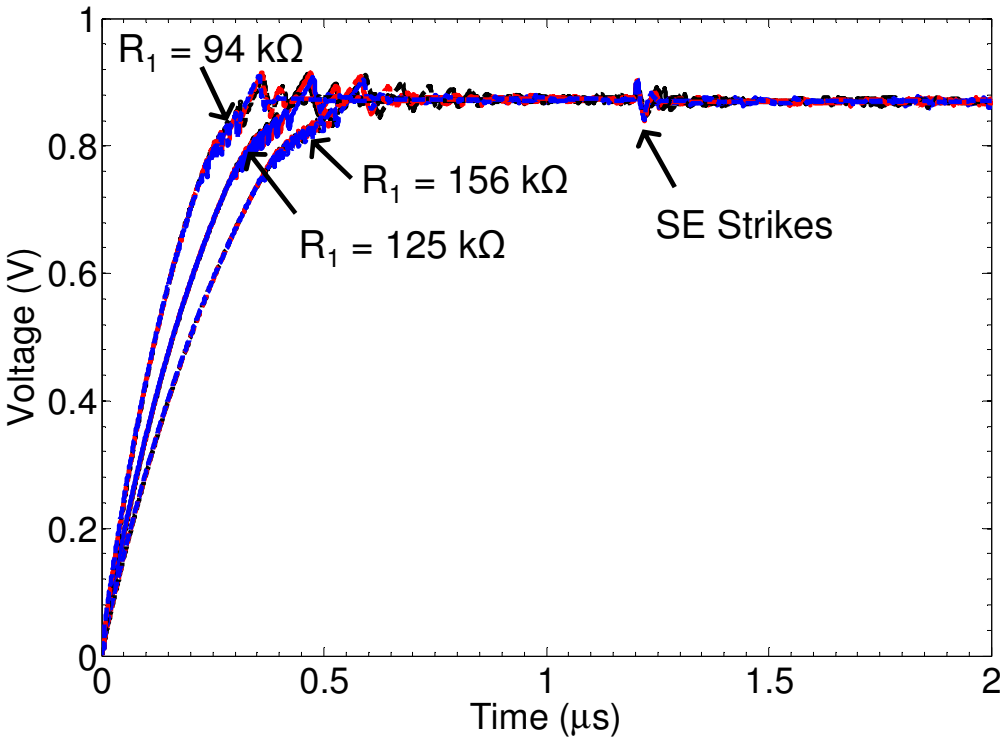

Figure 24. V_{inVCO} versus time: Effects of resistance tolerances on the electrical and SET performance of PLLs.

Area, Resistive Tolerances, and Power Design Tradeoffs

Finally, the area, resistive tolerances, and power design tradeoffs between the PLLs implementing the V-CP over the CP were examined. The V-CP and LPF design considered in this work implements the same passive components, C_1, C_2, and R_2, as the PLL design implementing the CP [18]. The resistor R_1 was chosen large in order to improve the tracking time and to minimize the effect of a SE strike. Furthermore, as the fixed current sources were removed from the CP, and a minimum width resistor was implemented in the LPF, a total PLL area decrease of 10% was achieved. However, the required area is highly dependent on the chosen values in the LPF and should be weighed against the effects of resistor value fluctuations due to the fabrication process.

In order to minimize the area, minimum width *p*+ doped poly resistors were implemented. However, such a resistor does result in maximum fluctuation of the final resistance value due to process variation. Since simulations showed a minimal impact on overall PLL performance due to resistor value fluctuations, this was not a concern. However, if the designer wishes to further decrease this fluctuation, an area tradeoff will be encountered. As the size of the resistors is increased to achieve a smaller tolerance, the total area of the PLL will begin to be dominated by the area of the LPF resistors.

The final concern examined was the impact implementing a V-CP over a CP in the PLL has on power consumption. By monitoring the current flow from the power supply, the average operating current for the two designs was observed to be approximately equivalent. The power consumption of the PLL is dominated by the VCO due to the continuous oscillations and subsequent transistor switching.

Conclusion

Although a V-CP instead of a CP can result in a significant improvement in SET susceptibility, certain electrical performance and design tradeoffs such as phase jitter, resistor design tolerances, and area were examined. The primary disadvantage of the V-CP is the increase in phase jitter that results from the connection of the power supply to the VCO's control voltage. The phase jitter resulting from power supply variations was approximately 10 times greater for the PLL implementing the V-CP over the CP.

Additionally, the impacts of resistor design tolerances on the electrical and SET performance of the PLL were examined. Simulations showed that a 25 % increase (decrease) in R_1 resulted in a maximum of 38 % increase (decrease) in lock time

(214.4 ns) and a maximum of 47 % decrease (increase) in the voltage perturbation (ΔV) of V_{inVCO}. Fluctuations in R_2 had little to no effect on the lock time or ΔV.

Finally, the area and power design tradeoffs were considered for both PLLs. By implementing minimum width *p*+ doped poly resistors the total area of the PLL implementing the V-CP was reduced by 10 % over the PLL implementing the CP. Additionally, the power consumption was determined to be approximately equivalent for both PLLs.

CHAPTER VII

CONCLUSIONS

Because of the high sensitivity of the charge pump (CP) to single-events (SEs) a tri-state voltage-based charge pump (V-CP) and low-pass filter has been presented to eliminate the CP as the most vulnerable module within the phase-locked loop (PLL), to improve the locking time, and to decrease the overall PLL area. The major design tradeoff when implementing the V-CP over the CP is the increase in phase jitter due to close coupling of the power supply and the VCO's control voltage. Simulations were performed using the IBM 130nm CMRF8RF process available through the MOSIS foundry system with SE strikes represented by the double-exponential current pulse model for charges up to 500 fC. Additionally, two PLL circuits, the first implementing the CP and second implementing the V-CP, have been designed, fabricated, and tested for SE sensitivity and the effectiveness of RHBD mitigation.

Simulations show that the V-CP can significantly reduce the voltage perturbation on the input of the voltage-controlled oscillator (VCO) and reduce the amount of phase displacement in the output of the PLL by approximately 2 orders of magnitude, reducing the number of erroneous pulses below those resulting from strikes in the VCO. Additionally, results from a through-wafer TPA technique performed on the PLL circuits show that a maximum of 2.3 orders of magnitude improvement in the number of erroneous pulses present in the output of the PLL following a SE was achieved by the PLL implementing the voltage over the current charge pump. Our findings show that a

novel SE RHBD hardening technique effectively reduces the sensitivity of the charge pump sub-circuit below the upset level of the voltage-controlled oscillator. Further improvements are possible by addressing upsets in the VCO. These results show that RHBD is effective for high-speed, mixed-signal circuits using unconventional analog design techniques and targeted single-event circuit simulations.

APPENDIX A

PLL CIRCUIT SCHEMATICS

The logic-level schematic of the phase-frequency detector (PFD) designed and fabricated is illustrated in Figure 26 [18].

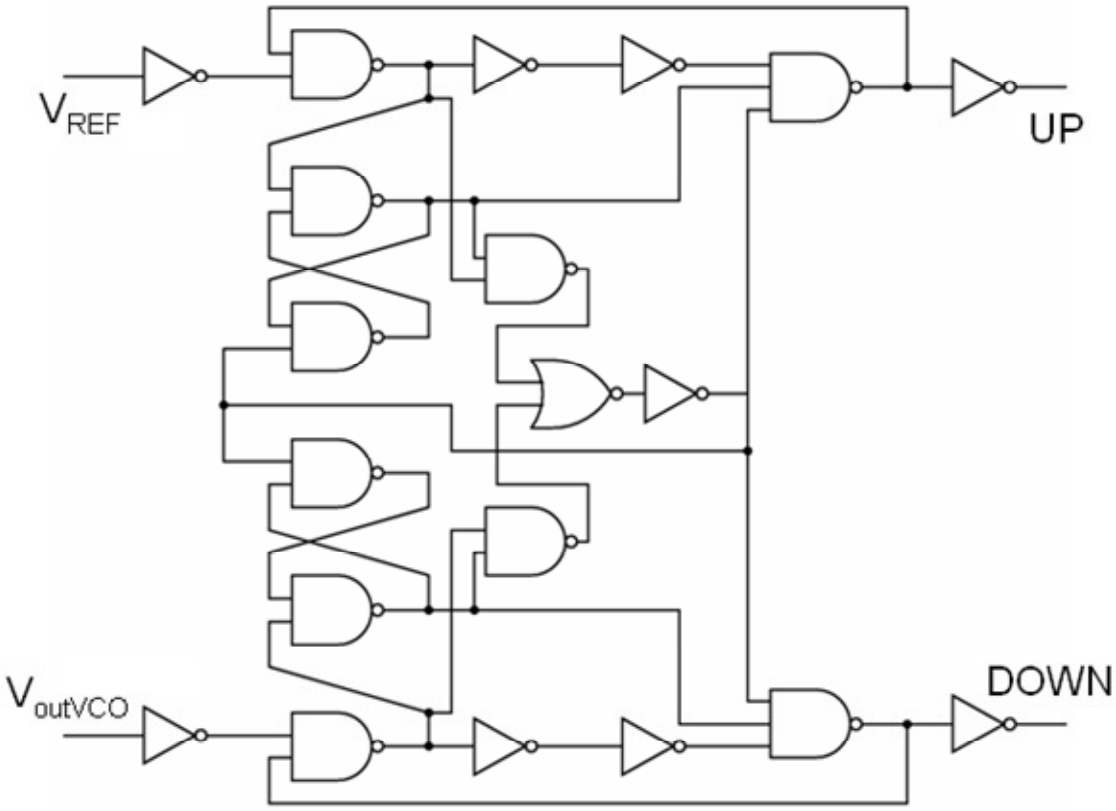

Figure 25. Circuit schematic of the PFD module [18].

The circuit schematics for the VCO and CP modules indicating the locations of the laser targets for the TPA experimentation are displayed in Figures 27 and 28, respectively.

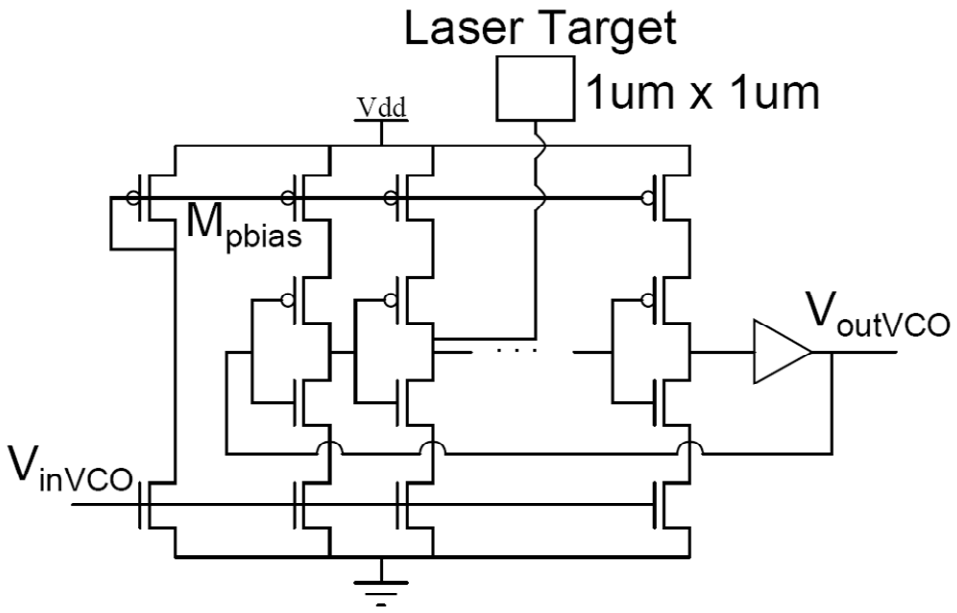

Figure 26. Schematic of the VCO circuit indicating the location of the 1µm x 1µm diffusion area used for the laser strikes.

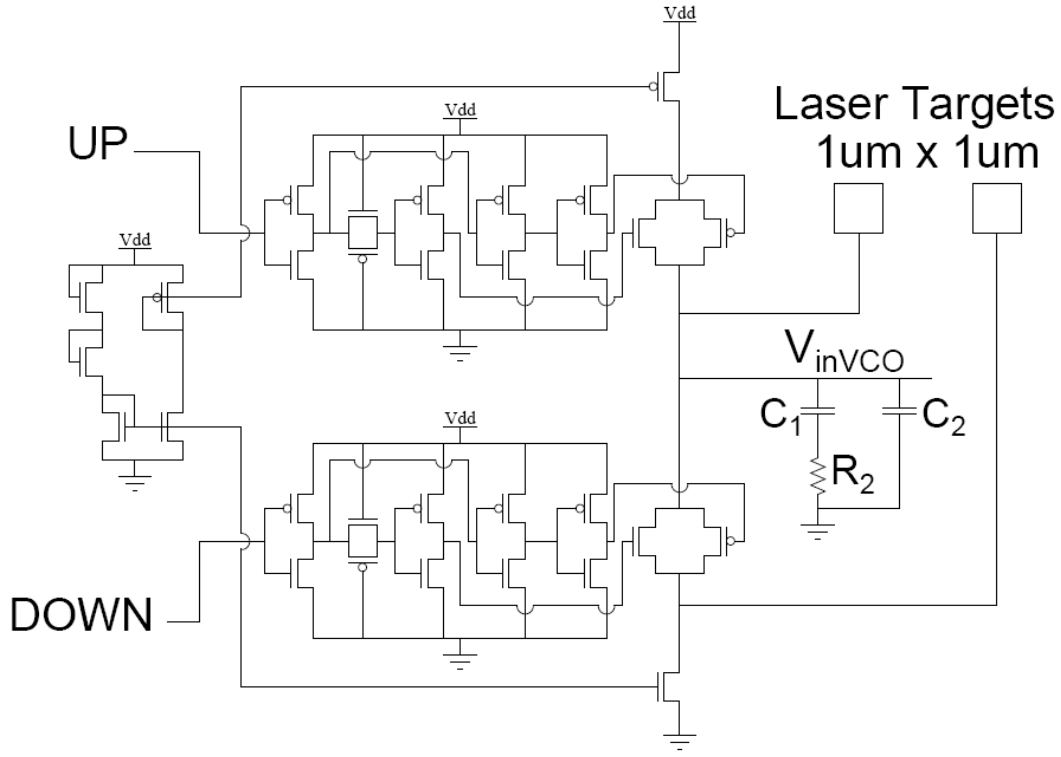

Figure 27. Schematic of the CP circuit indicating the locations of the 1µm x 1µm diffusion area used for the laser strikes.

APPENDIX B

V-CP DESIGN EQUATIONS

This appendix displays the design equations for the PLL implementing the V-CP. Equation B.1 represents the phase transfer function, H(s) [20], where K_{PFD} is the gain of the PFD module, K_F is the LPF transfer equation, and K_{VCO} is the gain of the VCO.

$$H(s) = \frac{\phi_{REF}}{\phi_{PLL}} = \frac{K_{PFD}K_FK_{VCO}}{s + K_{PFD}K_FK_{VCO}} \quad \text{B.1}$$

By letting $K_{PFD}= V_{dd}/4\pi$ for the voltage-based charge pump and PFD, by approximating K_F with equation B.2, and by rearranging H(s), the loop transfer equation can be represented by equation B.3.

$$K_F = \frac{1 + sR_2C_1}{s(R_1 + R_2)C_1} \quad \text{B.2}$$

$$H(s) = \frac{\phi_{REF}}{\phi_{PLL}} \approx \frac{(\frac{V_{dd}}{4\pi})K_{VCO}[\frac{1 + sR_2C_1}{s(R_1 + R_2)C_1}]}{s^2 + s\frac{(\frac{V_{dd}}{4\pi})K_{VCO}R_2C_1}{(R_1 + R_2)C_1} + \frac{(\frac{V_{dd}}{4\pi})K_{VCO}}{(R_1 + R_2)C_1}} \quad \text{B.3}$$

Then, by setting equation B.3 to equation B.4, equations B.5 and B.6 can be calculated.

$$H(s) = \frac{\omega_n^2}{s^2 + 2s\delta\omega_n + \omega_n^2} \quad \text{B.4}$$

Specifically, equations B.5, B.6, B.7, B.8, and B.9 represent the natural frequency, the damping ratio, the pull-in time, the lock-range, and the lock time, respectively.

$$\omega_{nVCP} = \frac{1}{2}\sqrt{\frac{V_{DD} \cdot K_{VCO}}{\pi \cdot (R_1 + R_2)C_1}} \quad \text{(radians/s)} \tag{B.5}$$

$$\zeta_{VCP} = \frac{\omega_{nVCP}}{2} R_2 C_1 = \frac{R_2 C_1}{4}\sqrt{\frac{V_{DD} \cdot K_{VCO}}{\pi \cdot (R_1 + R_2)C_1}} \tag{B.6}$$

(NOTE: Equations B.1 and B.2 are equivalent to equations 3.1 and 3.2)

$$T_{pVCP} = 2R_1 C_1 \cdot \ln \frac{K_{VCO}(\frac{V_{DD}}{2})}{K_{VCO}(\frac{V_{DD}}{2}) - \Delta\omega} \quad \text{(s)} \tag{B.7}$$

(Δω is the input frequency step)

$$\Delta\omega_{LVCP} = 4\pi \cdot \zeta \cdot \omega_{nVCP} = \frac{V_{DD} K_{VCO} \cdot R_2 C_1}{2(R_1 + R_2)C_1} \quad \text{(radians/s)} \tag{B.8}$$

$$T_{LVCP} = \frac{2\pi}{\omega_{nVCP}} \quad \text{(s)} \tag{B.9}$$

APPENDIX C

SPICE NETLIST

This appendix displays the detailed netlist, created using CADENCE and the SPECTRE environment, describing the PLL implementing the V-CP. The sub-circuits for V-CP and V-LPF can be replaced with the sub-circuits for CP and C-LPF in order to implement the standard current-based charge pump. Additionally, the top-level statements in the implementation must be corrected in order to implement the CP and C-LPF modules.

```
// Generated for: spectre
// Design cell name: DPLL_VoltagePump
// Design view name: schematic
simulator lang=spectre
global 0 vss! vdd!
include
"/gpfs0/local/x86/cadence/IBM_PDK/cmrf8sf/V1.3.0.2LM/Spectre/models/all
Models.scs"

////////////////////// Beginning of V-LPF ////////////////////////////
// Cell name: V_LPF
// View name: schematic
subckt V_LPF lpf_in lpf_out
  C1 (lpf_out net11 vss!) vncap w=146.68u l=146.000000u botlev=1 \
    toplev=2 setind=-2 est=1 m=1 par=1 rsx=50 dtemp=0
  C0 (lpf_out 0 vss!) vncap w=39.16u l=40u botlev=1 toplev=3 setind=-2 \
    est=1 m=1 par=1 rsx=50 dtemp=0
  I0 (0 vss!) subc l=4u w=2u dtemp=0
  OPppc1 (net11 0 vss!) opppcres w=200.0n l=880.0n r=2.41K sbar=1 m=1 \
    par=1 bp=3 dtemp=0.0 rsx=50
  OPppc0 (lpf_out lpf_in vss!) opppcres w=200.0n l=7.14u r=15.00355K \
    sbar=4 m=1 par=1 bp=3 dtemp=0.0 rsx=50
ends V_LPF
// End of subcircuit definition.
////////////////////////// End of V-LPF ////////////////////////////////

////////////////////// Beginning of VCO ////////////////////////////////
// Cell name: VCO_stage
// View name: schematic
subckt VCO_stage in n_in out p_in
  I2 (0 vss!) subc l=4u w=2u dtemp=0
  T34 (out in net8 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
```

```
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T36 (net8 n_in 0 vss!) nfet l=120.0n w=320.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.76e-13 as=1.76e-13 pd=1.74u ps=1.74u nrd=0.5625 nrs=0.5625 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T47 (net10 p_in vdd! vdd!) pfet l=120.0n w=1.11u nf=1 m=1 par=1 \
    ngcon=1 ad=6.105e-13 as=6.105e-13 pd=3.32u ps=3.32u nrd=0.1622 \
    nrs=0.1622 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
  T31 (out in net10 vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1\
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends VCO_stage
// End of subcircuit definition.

// Cell name: VCO_input_stage
// View name: schematic
subckt VCO_input_stage in out
  I2 (0 vss!) subc l=4u w=2u dtemp=0
  T59 (out out vdd! vdd!) pfet l=120.0n w=1.11u nf=1 m=1 par=1 ngcon=1 \
    ad=6.105e-13 as=6.105e-13 pd=3.32u ps=3.32u nrd=0.1622 nrs=0.1622 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T58 (out in 0 vss!) nfet l=120.0n w=320.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.76e-13 as=1.76e-13 pd=1.74u ps=1.74u nrd=0.5625 nrs=0.5625 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends VCO_input_stage
// End of subcircuit definition.

// Cell name: VCO_500M
// View name: schematic
subckt VCO_500M n_bias o11
  I30 (o9 n_bias o10 p_bias) VCO_stage
  I23 (o2 n_bias o3 p_bias) VCO_stage
  I24 (o3 n_bias o4 p_bias) VCO_stage
  I33 (o10 n_bias o11 p_bias) VCO_stage
  I22 (o1 n_bias o2 p_bias) VCO_stage
  I25 (o4 n_bias o5 p_bias) VCO_stage
  I26 (o5 n_bias o6 p_bias) VCO_stage
  I27 (o6 n_bias o7 p_bias) VCO_stage
  I2 (o11 n_bias o1 p_bias) VCO_stage
```

```
  I29 (o8 n_bias o9 p_bias) VCO_stage
  I28 (o7 n_bias o8 p_bias) VCO_stage
  I18 (n_bias p_bias) VCO_input_stage
ends VCO_500M
// End of subcircuit definition.
```
////////////////////////// End of VCO ////////////////////////////////

////////////////////// Beginning of V-CP ////////////////////////////

```
// Cell name: p_switch_final
// View name: schematic
subckt p_switch_final SW0 SW1 in
  T10 (i3 i2 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T9 (i4 t1 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T6 (i2 i1 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T4 (SW0 i4 SW1 vss!) nfet l=240.0n w=1.6u nf=1 m=1 par=1 ngcon=1 \
    ad=8.8e-13 as=8.8e-13 pd=4.3u ps=4.3u nrd=0.1375 nrs=0.1375 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T2 (t1 vdd! i1 vss!) nfet l=120.0n w=1.28u nf=1 m=1 par=1 ngcon=1 \
    ad=7.04e-13 as=7.04e-13 pd=3.66u ps=3.66u nrd=0.1406 nrs=0.1406 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (i1 in 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T11 (i3 i2 vdd! vdd!) pfet l=120.0n w=980.0n nf=1.0 m=1 par=1 ngcon=1\
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T8 (i4 t1 vdd! vdd!) pfet l=120.0n w=980.0n nf=1.0 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
```

```
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T7 (i2 i1 vdd! vdd!) pfet l=120.0n w=980.0n nf=1.0 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T5 (SW0 i3 SW1 vdd!) pfet l=240.0n w=5.6u nf=1 m=1 par=1 ngcon=1 \
    ad=3.08e-12 as=3.08e-12 pd=12.3u ps=12.3u nrd=0.0393 nrs=0.0393 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T1 (i1 in vdd! vdd!) pfet l=120.0n w=980.0n nf=1.0 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T3 (t1 0 i1 vdd!) pfet l=120.0n w=4.48u nf=1 m=1 par=1 ngcon=1 \
    ad=2.464e-12 as=2.464e-12 pd=10.06u ps=10.06u nrd=0.0402 \
    nrs=0.0402 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
  I0 (0 vss!) subc l=4u w=2u dtemp=0
ends p_switch_final
// End of subcircuit definition.

// Cell name: V_Ch_pump_final
// View name: schematic
subckt V_Ch_pump_final ChDown ChUp Vcap
  I1 (Vcap 0 ChDown) p_switch_final
  I0 (vdd! Vcap ChUp) p_switch_final
ends V_Ch_pump_final
// End of subcircuit definition.
//////////////////////////// End of V-CP ////////////////////////////////

///////////////// Beginning of Output Buffer ////////////////////////////
// Cell name: BufferX6_final
// View name: schematic
subckt BufferX6_final in out
  I3 (0 vss!) subc l=4u w=2u dtemp=0
  T11 (out net036 0 vss!) nfet l=120.0n w=41.48u nf=68.0 m=1 par=1 \
    ngcon=1 ad=7.4664e-12 as=7.6433e-12 pd=65.96u ps=67.15u nrd=0.2951 \
    nrs=0.2951 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
  T10 (net036 net055 0 vss!) nfet l=120.0n w=15.25u nf=25.0 m=1 par=1 \
    ngcon=1 ad=2.6962e-12 as=2.9707e-12 pd=24.09u ps=25.6u nrd=0.2951 \
    nrs=0.2951 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (net4 in 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
```

```
 ad=2.8e-14 as=1.54e-13 pd=480.0n ps=1.66u nrd=0.6429 nrs=0.6429 \
 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
 panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
 sb=5.5e-07 sd=3.6e-07 dtemp=0
T3 (net8 net4 0 vss!) nfet l=120.0n w=760.0n nf=2.0 m=1 par=1 ngcon=1\
 ad=1.368e-13 as=2.47e-13 pd=1.48u ps=2.44u nrd=0.4737 nrs=0.4737 \
 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
 panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
 sb=5.5e-07 sd=3.6e-07 dtemp=0
T7 (net055 net16 0 vss!) nfet l=120.0n w=5.6u nf=10.0 m=1 par=1 \
 ngcon=1 ad=1.008e-12 as=1.1704e-12 pd=9.2u ps=10.34u nrd=0.3214 \
 nrs=0.3214 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
 panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
 sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T4 (net16 net8 0 vss!) nfet l=120.0n w=2.04u nf=4.0 m=1 par=1 ngcon=1\
 ad=3.672e-13 as=5.151e-13 pd=3.48u ps=4.57u nrd=0.3529 nrs=0.3529 \
 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
 panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
 sb=5.5e-07 sd=3.6e-07 dtemp=0
T9 (out net036 vdd! vdd!) pfet l=120.0n w=146.000000u nf=100.0 m=1 \
 par=1 ngcon=1 ad=2.628e-11 as=2.67034e-11 pd=182.000000u \
 ps=184.04u nrd=0.1233 nrs=0.1233 rf_rsub=1 plnest=-1 plorient=-1 \
 pld200=-1 pwd100=-1 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p \
 panw2=0p panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p \
 panw9=0p panw10=0p sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T8 (net036 net055 vdd! vdd!) pfet l=120.0n w=53.58u nf=38.0 m=1 par=1\
 ngcon=1 ad=9.6444e-12 as=1.00533e-11 pd=67.26u ps=69.25u \
 nrd=0.1277 nrs=0.1277 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 \
 pwd100=-1 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p \
 panw3=0p panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p \
 panw10=0p sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T1 (net4 in vdd! vdd!) pfet l=120n w=980n nf=2.0 m=1 par=1 ngcon=1 \
 ad=1.764e-13 as=3.185e-13 pd=1.7u ps=2.77u nrd=0.3673 nrs=0.3673 \
 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
 panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
 sb=5.5e-07 sd=3.6e-07 dtemp=0
T6 (net055 net16 vdd! vdd!) pfet l=120.0n w=19.6u nf=14.0 m=1 par=1 \
 ngcon=1 ad=3.528e-12 as=3.934e-12 pd=24.64u ps=26.62u nrd=0.1286 \
 nrs=0.1286 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
 panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
 sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T5 (net16 net8 vdd! vdd!) pfet l=120.0n w=7.2u nf=4.0 m=1 par=1 \
 ngcon=1 ad=1.296e-12 as=1.818e-12 pd=8.64u ps=11.02u nrd=0.1 \
 nrs=0.1 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
 panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
 sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
T2 (net8 net4 vdd! vdd!) pfet l=120.0n w=2.67u nf=3.0 m=1 par=1 \
 ngcon=1 ad=4.094e-13 as=8.099e-13 pd=3.59u ps=5.38u nrd=0.2022 \
 nrs=0.2022 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
 lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
```

```
   panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
   sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
ends BufferX6_final
// End of subcircuit definition.
```
////////////////////// End of Output Buffer ////////////////////////////

////////////////////// Beginning of PFD ////////////////////////////////

```
// Cell name: Nor2_X1
// View name: schematic
subckt Nor2_X1 A B out
  I3 (0 vss!) subc l=4u w=2u dtemp=0
  T3 (net7 A vdd! vdd!) pfet l=120.0n w=1.96u nf=1 m=1 par=1 ngcon=1 \
    ad=1.078e-12 as=1.078e-12 pd=5.02u ps=5.02u nrd=0.0918 nrs=0.0918 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T2 (out B net7 vdd!) pfet l=120.0n w=1.96u nf=1 m=1 par=1 ngcon=1 \
    ad=1.078e-12 as=1.078e-12 pd=5.02u ps=5.02u nrd=0.0918 nrs=0.0918 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T1 (out B 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (out A 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Nor2_X1
// End of subcircuit definition.

// Cell name: Nand3_X1
// View name: schematic
subckt Nand3_X1 A B C out
  I3 (0 vss!) subc l=4u w=2u dtemp=0
  T4 (out C vdd! vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T3 (out A vdd! vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T2 (out B vdd! vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
```

```
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T5 (net039 C 0 vss!) nfet l=120.0n w=840.0n nf=1 m=1 par=1 ngcon=1 \
    ad=4.62e-13 as=4.62e-13 pd=2.78u ps=2.78u nrd=0.2143 nrs=0.2143 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T1 (net15 B net039 vss!) nfet l=120n w=840n nf=1 m=1 par=1 ngcon=1 \
    ad=4.62e-13 as=4.62e-13 pd=2.78u ps=2.78u nrd=0.2143 nrs=0.2143 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (out A net15 vss!) nfet l=120.0n w=840.0n nf=1 m=1 par=1 ngcon=1 \
    ad=4.62e-13 as=4.62e-13 pd=2.78u ps=2.78u nrd=0.2143 nrs=0.2143 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Nand3_X1
// End of subcircuit definition.

// Cell name: Nand2_X1
// View name: schematic
subckt Nand2_X1 A B out
  I2 (0 vss!) subc l=4u w=2u dtemp=0
  T3 (out A vdd! vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T2 (out B vdd! vdd!) pfet l=120.0n w=980.0n nf=1 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T1 (net15 B 0 vss!) nfet l=120.0n w=560.0n nf=1 m=1 par=1 ngcon=1 \
    ad=3.08e-13 as=3.08e-13 pd=2.22u ps=2.22u nrd=0.3214 nrs=0.3214 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (out A net15 vss!) nfet l=120.0n w=560.0n nf=1 m=1 par=1 ngcon=1 \
    ad=3.08e-13 as=3.08e-13 pd=2.22u ps=2.22u nrd=0.3214 nrs=0.3214 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Nand2_X1
// End of subcircuit definition.

// Cell name: Inv_X1
// View name: schematic
```

```
subckt Inv_X1 in out
  I0 (0 vss!) subc l=4u w=2u dtemp=0
  T1 (out in vdd! vdd!) pfet l=120n w=980n nf=1.0 m=1 par=1 ngcon=1 \
    ad=5.39e-13 as=5.39e-13 pd=3.06u ps=3.06u nrd=0.1837 nrs=0.1837 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (out in 0 vss!) nfet l=120.0n w=280.0n nf=1 m=1 par=1 ngcon=1 \
    ad=1.54e-13 as=1.54e-13 pd=1.66u ps=1.66u nrd=0.6429 nrs=0.6429 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Inv_X1
// End of subcircuit definition.

// Cell name: Inv_X3
// View name: schematic
subckt Inv_X3 in out
  I2 (0 vss!) subc l=4u w=2u dtemp=0
  T1 (out in vdd! vdd!) pfet l=120.0n w=2.94u nf=1 m=1 par=1 ngcon=1 \
    ad=1.617e-12 as=1.617e-12 pd=6.98u ps=6.98u nrd=0.0612 nrs=0.0612 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (out in 0 vss!) nfet l=120.0n w=840.0n nf=1 m=1 par=1 ngcon=1 \
    ad=4.62e-13 as=4.62e-13 pd=2.78u ps=2.78u nrd=0.2143 nrs=0.2143 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Inv_X3
// End of subcircuit definition.

// Cell name: PDF_BuffX3
// View name: schematic
subckt PDF_BuffX3 Data Dclock Down Up
  I23 (net028 net096 net050) Nor2_X1
  I14 (net0121 net089 net5 net079) Nand3_X1
  I12 (net22 net14 net5 net9) Nand3_X1
  I18 (net079 net0136 net084) Nand2_X1
  I15 (net089 net084 net096) Nand2_X1
  I16 (net089 net5 net085) Nand2_X1
  I17 (net084 net085 net089) Nand2_X1
  I11 (net14 net5 net20) Nand2_X1
  I10 (net11 net20 net14) Nand2_X1
  I9 (net9 net49 net11) Nand2_X1
  I13 (net14 net11 net028) Nand2_X1
  I24 (net050 net5) Inv_X1
  I20 (net084 net0117) Inv_X1
  I19 (net0117 net0121) Inv_X1
  I5 (net26 net22) Inv_X1
  I4 (net11 net26) Inv_X1
  I22 (Dclock net0136) Inv_X3
  I21 (net079 Down) Inv_X3
```

```
  I2 (net9 Up) Inv_X3
  I0 (Data net49) Inv_X3
ends PDF_BuffX3
// End of subcircuit definition.
//////////////////////////// End of PFD ////////////////////////////////

/////////////////////// Beginning of VPLL ////////////////////////////
// Cell name: DPLL_500M_VoltagePump
// View name: schematic
  I26 (v_lpf v_in_vco) V_LPF
  I20 (v_in_vco vco_out) VCO_500M
  V0 (clk_in 0) vsource type=pulse val0=0.0 val1=1.2 period=1.25n \
    delay=5n rise=80p fall=80p width=545.000p
  V1 (vdd! 0) vsource dc=1.2 type=dc
  C0 (pll_buff_out 0) capacitor c=2p
  I13 (DOWN UP v_lpf) V_Ch_pump_final
  I27 (vco_out pll_buff_out) BufferX6_final
  I17 (clk_in vco_out DOWN UP) PDF_BuffX3
  ic v_in_vco=0 v_lpf=0 vco_out=0
//////////////////////////// End of VPLL ////////////////////////////////

/////////////////////// Beginning of CP ////////////////////////////
// Cell name: Ch_pump_2uA_final
// View name: schematic
subckt Ch_pump_2uA_final ChDown ChUp Vcap
  I11 (net24 Vcap ChUp) p_switch_final
  I12 (Vcap net20 ChDown) p_switch_final
  I15 (0 vss!) subc l=4u w=2u dtemp=0
  T12 (vdd! vdd! net2 vss!) nfet l=900n w=900n nf=1 m=1 par=1 ngcon=1 \
    ad=4.95e-13 as=4.95e-13 pd=2.9u ps=2.9u nrd=0.2444 nrs=0.2444 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T11 (net2 net2 net053 vss!) nfet l=900n w=900n nf=1 m=1 par=1 ngcon=1\
    ad=4.95e-13 as=4.95e-13 pd=2.9u ps=2.9u nrd=0.2444 nrs=0.2444 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T10 (net053 net053 net11 vss!) nfet l=900n w=900n nf=1 m=1 par=1 \
    ngcon=1 ad=4.95e-13 as=4.95e-13 pd=2.9u ps=2.9u nrd=0.2444 \
    nrs=0.2444 rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 \
    lstis=1 lnws=0 rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p \
    panw4=0p panw5=0p panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p \
    sa=5.5e-07 sb=5.5e-07 sd=3.6e-07 dtemp=0
  T7 (0 net11 net11 vss!) nfet l=720.0n w=720.0n nf=1 m=1 par=1 ngcon=1\
    ad=3.96e-13 as=3.96e-13 pd=2.54u ps=2.54u nrd=0.3056 nrs=0.3056 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T3 (net25 net11 0 vss!) nfet l=3u w=3.5u nf=1 m=1 par=1 ngcon=1 \
    ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 nrs=0.0629 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
```

```
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T2 (net20 net11 0 vss!) nfet l=3u w=3.5u nf=1 m=1 par=1 ngcon=1 \
    ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 nrs=0.0629 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T4 (net24 net25 vdd! vdd!) pfet l=3u w=3.5u nf=1 m=1 par=1 ngcon=1 \
    ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 nrs=0.0629 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
  T0 (net25 net25 vdd! vdd!) pfet l=3u w=3.5u nf=1 m=1 par=1 ngcon=1 \
    ad=1.925e-12 as=1.925e-12 pd=8.1u ps=8.1u nrd=0.0629 nrs=0.0629 \
    rf_rsub=1 plnest=-1 plorient=-1 pld200=-1 pwd100=-1 lstis=1 lnws=0 \
    rgatemod=0 rbodymod=0 panw1=0p panw2=0p panw3=0p panw4=0p panw5=0p \
    panw6=0p panw7=0p panw8=0p panw9=0p panw10=0p sa=5.5e-07 \
    sb=5.5e-07 sd=3.6e-07 dtemp=0
ends Ch_pump_2uA_final
// End of subcircuit definition.
//////////////////////////// End of CP ////////////////////////////////

/////////////////////// Beginning of C-LPF ////////////////////////////
// Cell name: C_LPF
// View name: schematic
subckt C_LPF Vlpf
  C1 (Vlpf net16 vss!) vncap w=79.48u l=79.0u botlev=1 toplev=2 \
    setind=-2 est=1 m=1 par=1 rsx=50 dtemp=0
  C0 (Vlpf 0 vss!) vncap w=27.64u l=27.0u botlev=1 toplev=2 setind=-2 \
    est=1 m=1 par=1 rsx=50 dtemp=0
  I0 (0 vss!) subc l=4u w=2u dtemp=0
  OPppc1 (net16 0 vss!) opppcres w=200n l=880n r=2.40947K sbar=1 m=1 \
    par=1 bp=3 dtemp=0.0 rsx=50
ends C_LPF
// End of subcircuit definition.
//////////////////////////// End of C-LPF ////////////////////////////////

/////////////////////// Beginning of CPLL ////////////////////////////
// Cell name: DPLL_500M_CurrentPump_sim_noinputVCO
// View name: schematic
  V1 (PLLin 0) vsource type=pulse val0=0 val1=1.2 period=2.5n delay=5n \
    rise=80p fall=80p width=1.17n
  I13 (net033 net032 net030) Ch_pump_2uA_final
  I33 (PLLout net021) BufferX6_final
  C0 (net021 0) capacitor c=2p
  V0 (vdd! 0) vsource dc=1.2 type=dc
  I28 (net030) C_LPF
  I20 (net030 PLLout) VCO_500M
  I17 (PLLin PLLout net033 net032) PDF_BuffX3
  ic net030=0 PLLout=0
//////////////////////////// End of CPLL ////////////////////////////////
```

APPENDIX D

DOUBLE-EXPONENTIAL PARAMETERS

The equation representing the double-exponential pulse representative of the SE induced current is represented in equation D.1 [30], or by an equivalent piecewise model representative of a SPICE model in equation D.2 [3].

$$I(t) = I_0[e^{-\alpha t} - e^{-\beta t}] \tag{D.1}$$

$$I(t) = \begin{cases} I_0(1 - e^{\frac{-t}{\tau_R}}) & ; t < t_D \\ I_0(1 - e^{\frac{-t_D}{\tau_R}})e^{\frac{-(t-t_D)}{\tau_F}} & ; t > t_D \end{cases} \tag{D.2}$$

The time constants, τ_R and τ_F, were 1 ns and 2 ns, respectively. In order to vary the amount of charge deposition the peak current, I_0 was varied according to TABLE 1.

TABLE 2
Peak current required for various charge deposition values.

Q (fC)	**I_0 (mA)**
50	0.25
100	0.5
200	1.0
500	2.5

The SPICE command used to insert the double-exponential pulse depositing into the circuit is as follows:

```
I# (0 NMOS_node) isource type=exp val0=0 val1=I0m td1=d1u tau1=αn \
        td2=(d1+d2)u tau2=βn
```

-or-

```
I# (PMOS_node vdd!) isource type=exp val0=0 val1=I0m td1=d1u tau1=αn \
        td2=(d1+d2)u tau2=βn
```

NMOS_node is the drain of a desired NMOS device whereas *PMOS_node* is the drain of a desired PMOS device. The parameters I_0, d_1, d_2, α, and β should be filled in appropriately.

APPENDIX E

DATA ANALYSIS SCRIPTS

The following are the primary scripts used to analyze the PLL error signatures. All of the scripts were developed in MATLAB. The function, getPLLData(), is used to analyze the output signals. The function must be initiated using a separate file listing the data file names. Additionally, getPeriod(), determines the period of the output signal. The data analyzed must be a signal unperturbed by a SE strike.

```
%% function getPLLData()
% Author: Daniel Loveless
% Last Updated: 10/19/2006
%
% Description:
% This function analyzes the output clock signal with respect to a
% reference signal. The output pulses are counted and the phase
% displacement between the rising edges of the output signal with
% respect to the reference signal is calculated. This function
% generates a text file including an index, the name of the file
% analyzed, the number of errors determined, and the phase
% displacement.
%
% Input Variables:
%       filename:       name of file to be analyzed (char)
%       PER:            the period of the signal under normal operation
%                       (getPeriod () may be used to determine)
%       compFilename:   name of reference file
%       filecount:      the number of the file called to be analyzed
%       fileflag:       1 - begin a new data file
%                       0 - continue with last data file
%       chrg:           LET code: eg. 'LET80' or '500fC'
%       stageNum:       the number of inverter stages in VCO: eg. '11'
%       vin:            the input bias applied to circuit: eg. '300mV'

% Output Variables
%       Text files (.txt) will be created in the directory that the
%       script is called from with the following naming convention:
%           pll_data_(freq)_(chrg).txt
%
%       Each file will include the index of the file, the name of the
%       file analyzed, the number of errors recorded, and the phase
%       displacement in degrees
```

```
function
getPLLData(filename,PER,compFilename,filecount,fileflag,chrg,freq)
%%  Load the file to be analyzed and assign columns to arrays
pll_hit = load(filename);
%%% Time
t1 = pll _hit(:,2);     % NOTE: The columns are specific to the
%%% Output voltage      % formatting of the data files
v1_2 = pll_hit(:,4);

%% Other Data Nodes In File (optional)
% v1_1 = pll_hit(:,3);      %Current Pulse
% v1_3 = pll_hit(:,5);      %Node Voltage

%%  Load the reference file and assign columns to arrays
pll_nohit = load(compFilename);
%%% Time
t2 = pll_nohit(:,2);
%%% Output
v2_1 = pll_nohit(:,3);

%% Initialize variables for data analysis
threshold = .5;
flag = 0;
count = 0;
count2 = 0;
time_check_clk = 0;
time_check_pll = 0;
startT=1;
endT=length(t1);

%%  Count the pulses in filename (the file under analysis)
%%% The loop cycles through each time step.
for i=startT:endT
    temp = v1_2(i);
    %%% When the voltage is equal to or greater than the threshold
    %%% check to see if the pulse has been counted. If it has (flag=1),
    %%% then keep flag=1 and move to next time step. If it has not been
    %%% counted (flag=0), then increment the counter, store the time
    %%% step, and set flag=1.
    if(temp>=threshold)
        if(flag == 0)
            count = count + 1;
            time_check_pll(count) = t1(i);
        end
        flag = 1;
    else
        flag = 0;
    end
end

%%  Reset variables for data analysis
flag = 0;
startT=1;
endT=length(t2);
```

```
%%  Count the pulses in compFilename (the reference signal)
%%% Same procedure as previous.
for i=startT:endT
    temp = v2_1(i);
    if(temp>=threshold)
        if(flag == 0)
            count2 = count2 + 1;
            time_check_clk(count2) = t2(i);
        end
        flag = 1;
    else
        flag = 0;
    end
end

%%  Denote the number of errors in filename defined as the number of
%%% missing or additional pulses in filename as compared to the
%%% reference signal. Errors (erroneous pulses) = number of pulses in
%%% filename - number of pulses in compFilename
errors = abs(count - count2);

%%  Reformat the arrays storing the time steps where pulses were
%%% counted. If any errors exist, meaning one of the arrays will be
%%% greater than the other, remove the entries at the end of the larger
%%% array until they are equivalent.
while length(time_check_pll)~=length(time_check_clk)
    if length(time_check_pll)>length(time_check_clk),
        time_check_pll(:,length(time_check_pll))=[];
    else
        time_check_clk(:,length(time_check_clk))=[];
    end
end

%%  Calculate the time and phase error
%%% The time error is the difference between corresponding elements in
%%% the time arrays. The phase error in degrees is the time error %%%
divided by the period, multiplied by 360.
time_error=abs(time_check_pll-time_check_clk);
max_time_error = max(time_error);
max_phase_error = max_time_error/PER*360;

%%  Create a new file or open the existing file, and write the data
%%% The data will be formatted as tab delimited data with four columns
%%% representing the index, the filename, the number of errors, and %%%
the phase error. The file will be saved using the following naming %%%
scheme: pll_data_(frequency)_(LET code or charge).txt
fileString=strcat('pll_data_',freq,'_',chrg,'.txt');
fileString=char(fileString);
fid=fopen(fileString,'a+');
fprintf(fid,'%1.0f\t',filecount);
fprintf(fid,char(filename));
fprintf(fid,'\t');
fprintf(fid,'%1.0f\t',errors);
fprintf(fid,'%6.2f\n',max_phase_error);
fclose(fid);
```

```
end

%% function getPeriod(filename)
% Author: Daniel Loveless
% Last Updated: 10/19/2006
%
% Description:
% This function determines the period of the input signal
%
% Input Variables:
%       filename:   filename of signal
% Output Variables
%       per:        period of signal
%       filedata:   matrix of data points in file

function [per,filedata] = getPeriod(filename)
%  Load data into variable and set time and voltage arrays
    filedata = load(filename);
    t = filedata(:,2);
    v = filedata(:,3);

%  Initialize variables for data analysis
%%% threshold:    voltage threshold used to determine a rising pulse
%%%               edge
%%% flag:         0-pulse not counted
%%%               1-pulse counted
%%% count:        counter denoted number of pulses counted
%%% time_check_file:    array of timesteps corresponding to each rising
%%%                     pulse
%%% startT:       initial index
%%% endT:         final index

    threshold = .5;
    flag = 0;
    count = 0;
    time_check_file = 0;
    startT=1;
    endT=length(t);

%  Count pulses and determine the corresponding timestamp
    for i=startT:endT,
        temp = v(i);
        if(temp>=threshold)
            if(flag == 0)
                count = count + 1;
                time_check_file(count) = t(i);
            end
            flag = 1;
        else
            flag = 0;
        end
    end

%  Find the time difference between each timestamp
%%% time_diff_file: array of time values denoted the difference between
%%% consecutive pulses
```

```
     time_diff_file = zeros(count-1,1);
     for i=2:count,
       time_diff_file(i-1) = time_check_file(i) - time_check_file(i-1);
     end

%%  Average the resulting differences to obtain the average period
%%% The average frequency will then be 1/per
     per = mean(time_diff_file);

%%  This script can also be used to determine the jitter of the signal
%%% looking at the variation of the pulse widths away from the mean
%%% value.
%%%
%%% Ex. varPer = std(time_diff_file) gives one standard deviation away
%%% from per.

end
```

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