# A BUILT-IN SELF-TEST (BIST) TECHNIQUE FOR SINGLE-EVENT TRANSIENT TESTING IN DIGITAL CIRCUITS

By

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# CHAPTER I

# INTRODUCTION

The radiation effects community has been studying and analyzing the effects of radiation on space-based and terrestrial-based electronics for the past four to five decades. The radiation environment is populated with electrons, protons, cosmic rays and ions, which have sufficient energy to ionize the material through which they pass. A single-event effect (SEE) results from a single energetic particle that strikes a micro-electronic device causing device malfunction. Single-event phenomena can be classified into hard or soft errors depending on whether the ions cause permanent damage or temporary malfunctioning of the circuit they strike. Some common SEEs are i) single-event upset (SEU) ii) single-event transient (SET) iii) single-event latchup (SEL) and iv) single-event burnout (SEB). This thesis primarily deals with two types of single-event phenomena- SETs and SEUs that occur in digital logic micro-electronic circuits, and a novel built-in testing technique to assess their vulnerability to these SEs.

## SETs and their Significance with CMOS Scaling

Single-event transients were first identified following an in-flight anomaly in the TOPEX POSEIDON spacecraft [1]. SETs are caused by ionizing radiation passing directly through or near the p-n junction of a semiconductor device, and are defined as momentary voltage excursions at a node of an integrated circuit. Depending on the operating conditions of the micro-electronic device, the voltage spike may propagate away from the node it was generated at, and eventually appear at the output of the

circuit. At the circuit output it may appear as the same voltage transient, an amplified or attenuated version of the original transient, or as a change in the expected logical output. If the voltage spike is captured by a sequential element such as a latch in the micro-electronic circuit, an SET becomes a single–event upset (SEU), resulting in a static error leading to disruption in circuit operation. An SEU is a type of SEE and is defined as a static upset in storage cells such as latches and flip-flops.

Until recently, the radiation community has not been very concerned about SETs being a reason for flawed operation of micro-electronic circuits. In older technologies with minimum feature sizes being larger than 0.3 μm, SETs did not have a high probability of being captured [2]. As minimum dimensions of the integrated circuits (ICs) continue to decrease to yield high density and high performance circuits, their susceptibility to SETs has also increased significantly [3]-[15]. With technology scaling, SETs are becoming a larger source of soft errors in digital circuits for primarily two reasons. Firstly, it is the scaling of nodes. In the past, nodal capacitances were larger and only ions with a high Linear Energy Transfer (LET) striking the device could cause an SET. But with minimum feature sizes having reached the sub-micron level, nodal scaling has reduced nodal capacitances, allowing more SETs having sufficient pulse width and amplitude to be formed. The amount of charge differentiating logic HIGH from logic LOW has decreased [4], increasing the probability for SETs to occur. Secondly the increasing frequency of circuit operation leads to a higher probability of SET pulse capture [10],[11],[16].

In the sub-micron technologies, the major source of soft errors results from combinational logic cells as against from sequential cells. Recent research has shown

that the potential for soft errors increases dramatically because the error cross-section of combinational logic may far exceed that of traditional latch structures. There has been as much as a 5-10 times increase in the number of combinational gates in a particular design compared with static-latch cells [16]. The following references discuss in detail the effects of SETs on devices and their propagation through combinational logic [3], [17]-[22]. All these factors contribute to the capture of a substantial fraction of these transients generated in combinational logic; due to the higher operating frequencies and lower charge requirements in advanced deep sub-micron technologies [4],[16].

Additionally, upset error rates caused by SETs are a strong function of the SET pulse width, arrival time of an SET with respect to the clock edge and clock frequency [11][16]. When an SET occurs in a combinational logic node (such as an inverter or a NAND gate), it may propagate and potentially become latched in a static cell. In order to become latched and cause an error, the SET pulse must have sufficient width and amplitude and must coincide with a valid clock window for latching. This is because, for an SET to be captured by a latch, it is required that an SET arrives within the set-up and hold time requirements of the latch [3]. Slower clock frequencies in older technologies provided relatively fewer clock edges for this latching to occur. Conversely, due to GHz range scale of operation in advanced technologies, CMOS digital logic circuits exhibit higher sensitivity to SETs. Also, as device capacitances have scaled with the sub-micron technologies, these SETs are able to propagate more easily through several gates without attenuation and have a higher likelihood to be captured by latches and other sequential elements.

## Testing of circuits for SETs

The errors due to SETs are expected to dominate the overall error rate of the entire circuit [3], [10], [16]-[12], [23], as described in the previous section. For future technologies, the feature sizes of digital circuits will continue to shrink making them even more susceptible to these SEEs. Research has shown that SETs are a concern not only to space based electronics, but also to ground based systems with small feature sizes [24]. Hence, it is of paramount importance to design and manufacture circuits that have a high degree of immunity to SEEs. Amongst several other things, this will require extensive testing on part of the researchers to improve understanding of the physics involved behind the ionic interactions, to develop and check new designs for SEE and SET sensitivity. This can help assure that circuits meet a specific minimum level of SEE tolerance in order to be deployed in space or for use in terrestrial electronics.

Ideally, SET testing has to be done in the actual environment where the electronic circuits will operate. Since this is not practical for circuits intended for space applications due to extremely high costs associated and the long time requirements involved, other alternative methods of testing have to be resorted to. Widely used testing alternatives are with accelerators (heavy ion, neutron, proton) and pulsed laser techniques [25]. As much as these testing procedures mimic the space environment, there is the inconvenience of testing at a facility remote from the manufacturing or assembly plant. Also, most accelerators are not configured to provide information on the spatial and temporal dependence of SEE [20]. Accelerator testing can also cause displacement damage to the semiconductor material. Testing an IC in a heavy ion beam for short time duration with a predetermined set of random test vectors may not identify

the most vulnerable conditions or actual error rate that will be observed in the radiation environment.

Laser testing is more convenient as the laser light can be used to deposit energy at small spots for identifying areas sensitive to SEUs. The arrival time of a laser light pulse can also be synchronized to the circuit clock for measuring the time interval during which a node is receptive to an SEU. But due to device scaling, vulnerable areas become smaller than the size of the laser beam making it difficult to measure thresholds accurately as the amount of energy needed to produce an SET is very sensitive to the position of the beam. Additionally, metal fill makes it harder to test devices from the front side with laser. Backside testing with a laser is very complicated as well. It has to be kept in mind that both the accelerator and laser facilities are incidentally very expensive considering the manpower, mask sets that need to be used, beam time, fabrication costs and equipment. As the SET pulse width is a function of not only the base technology, but also circuit parameters such as nodal capacitance, device currents, and supply voltage [16], it is essential that SET characterization be performed for every IC design. But, the difficulty with such a testing approach is the overhead in terms of cost, time and testing challenges. In the past, researchers have also emulated radiation environments by injecting errors in circuits by using codes in software, but such techniques may not accurately include several circuit level parasitic effects [26]-[34]. This thesis describes new design methods that can be adopted for SET testing of digital logic circuits.

## Overview of Thesis

As the cost and time involved with these conventional testing methods are very expensive, lab-based built-in self-testing approaches that can estimate error rates due to SETs in digital circuits can be an attractive alternative [35]-[41]. In this thesis, a new built-in self-test design is presented, that allows for SET testing of any complex circuit using laboratory-based equipment without the need for expensive heavy ion or laser testing. The proposed technique electrically injects pulses similar to SETs at the chosen nodes of a circuit for estimating the overall susceptibility of the same. The methodology illustrated in this thesis can be used for a variety of measurements, including

(i) providing circuit designers with information for improving SET immunity of tested circuits

(ii) determining the reason behind failure of circuits to meet designed levels of SET tolerance

(iii) measuring relative levels of SET susceptibility for hardness assurance

(iv) understanding and studying the fundamental mechanisms responsible for SETs

The following chapters of the thesis describes how an SET pulse is modeled in hardware, the technique behind the generation and injection of SET pulses, and the simulation and experimental results that compliment this design procedure. Furthermore, this technique is applied to a couple of commonly used digital logic circuits, illustrating the steps involved in the application of this testing scheme. The injected SET pulses have randomly varying characteristics to mimic actual SET pulses, to evaluate the radiation response of the circuit with the added advantage of reduced

cost and time requirements. The advantages of the Built-in Self-Test (BIST) method of testing over other testing methods are

(i) requires no specialized external equipment or manpower and can be performed in any conventional laboratory

(ii) electrical injection of pulses do not cause any damage to the semiconductor material/circuits evaluated

(iii) may be used to inject pulses simultaneously at multiple nodes to test for multi-bit upsets

(iv) electrical injection of pulses can be controlled precisely, or can be made completely random as well, depending on the circuit and application for which the testing is done

(v) it incurs minimal cost and testing time requirements

# CHAPTER II

# SINGLE-EVENT TRANSIENT PULSE CHARACTERISTICS

As the built-in self-test procedure requires that pulses be electrically injected into the circuit under test, the pulses have to be generated in hardware. In order to generate pulses similar to SETs through circuit design, it is essential to understand how an SET is formed, and what characteristics of an SET are important in understanding and analyzing the circuit response to SETs. The following sections discusses the outcomes that result from a single-event strike, how an SET is formed and what parameters of the SET to realize in hardware.

## SET Formation

When a single-event hit occurs at a node, it results in charge generation, followed by charge collection and circuit response [42]. These three primary factors result in the formation of an SET. The ionic interaction with semiconductor materials results in charge deposition or generation depending on whether the ion strikes the drain of an nmos or pmos transistor. The amount of charge generated/deposited at the struck node depends on the properties of the particle such as the ion species, energy and angle at which it strikes the semiconductor device. It also depends on the properties of the semiconductor material such as its doping and junction depth. The charge generation/deposition is generally modeled in simulations by a current source at the struck node [42]. Device parameters such as the current drive, size of the transistors and

circuit parameters such as the capacitances at the strike node and power supply voltage determine the shape of this current pulse, used for modeling SE strikes.

## Circuit Model for SET Charge Collection in Simulations

For any circuit design used to model an SE in hardware, such charge collection has to be reproduced by circuit elements such that the overall circuit response is similar to the actual single-event. The circuit design needs to emulate the relationship between the SE-induced perturbations in circuit currents and voltages to SETs. A common circuit model for the charge collection at a junction due a single-event is a double exponential, time-dependent current pulse as shown in Fig. 1.

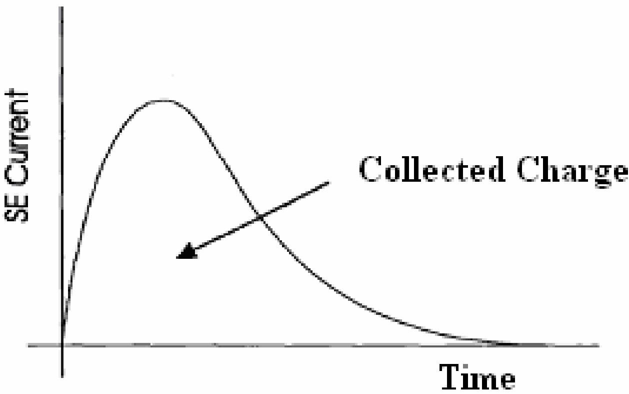


Fig. 1. Typical shape of the SE charge collection current at a junction

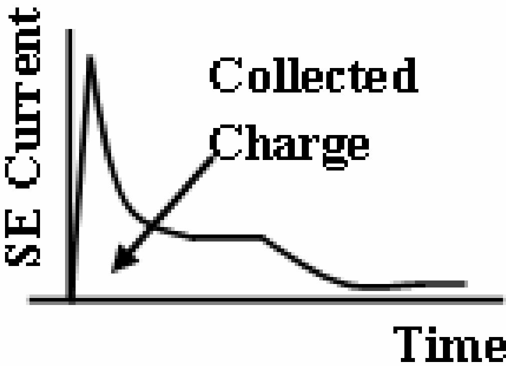


Fig. 2. Typical shape of the SE current pulse for advanced technologies

The circuit model in Fig. 1. was used for modeling in older technologies. However, for deep submicron technologies (90, 130 and 180 nm), as the devices are placed much closer to one another due to technology scaling, the redistribution of electric fields extends over several nodes. This causes a distinctive change in the shape of the current pulse from earlier observed technologies. Characterization of SETs through Technology Computer Aided Design (TCAD) simulations also indicates a distinct change in the transient current waveform from the familiar double exponential shape. The first departure from the double exponential form was shown explicitly in TCAD simulations by Dodd *et al*. [11], [43] on 180 nm bulk CMOS and SOI processes. This was also shown by Turowski *et al*. in [44] for 90nm CMOS. For these deep submicron technologies, the current pulse has a plateau shaped region, as shown in Fig. 2, which is critical in deciding the width of the SET that propagates through the circuit [45].

## SET Modeling in Hardware

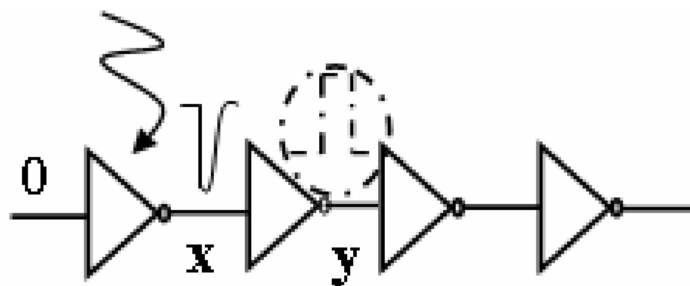


Fig. 3. Inverter string showing an n-hit at node 'x'

This thesis proposes on-chip built-in testing for SETs and involves the electrical injection of pulses. Pulses that are electrically injected can either be current pulses or

voltage pulses. Modeling current pulses and replicating their precise shapes at the strike node, in hardware using circuit design would result in significant area and power overhead making any built-in self-test (BIST) approach based on such current sources impractical.

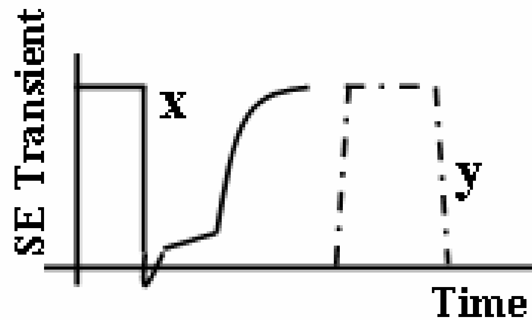


Fig. 4. Voltage transients at hit node 'x' and one node after hit node 'y'

Another approach is to inject voltage pulses at the circuit nodes, instead of current pulses. The voltage pulse at the hit node is also a complex function of multiple parameters, depending on the amount of charge collected due to the ion strike, the drive strength of the transistors and the properties of the ion that strike the device. Any voltage (or current) transient at the hit node will propagate through the logic gates connected to it [Fig. 3] and become a logic signal that switches between the supply voltage and the ground as shown in Fig. 4. Replicating the voltage pulse at the hit node 'x' will also require complex circuit designs with high overhead. On the other hand, the voltage pulse at 'y' that is one logic node away from the hit node is relatively easier to model, as it an almost square waveform going rail to rail.

The propagated transients can be easily created by building simple circuit designs with relatively less area and power requirements. The voltage transients must be

modeled and replicated in such a way that varying pulses can be injected into any node of any circuit under test, to mimic the actual SE randomness. In the next chapter, the BIST approach presented is based on injecting such voltage pulses at requisite nodes to estimate SE performance and vulnerability of a circuit.

# CHAPTER III

# BUILT-IN SELF-TEST (BIST) TECHNIQUE

BIST is distinctive from heavy ion and laser testing methods in the aspect that, it does not physically strike a node with an ion or deposit charge with a pulsed-laser, but electrically injects voltage pulses at the node of interest. It is essential to understand and recognize what parameters of SETs affect soft error rates so they can be controlled and modeled for the electrical pulse injection. Combinational logic error rates due to SETs are largely dependent upon the pulse width and arrival time of the SET pulse with respect to the clock edge [43], [44]. Hence the objective behind the BIST design method is to randomly insert SET pulses of random width and arrival instances with respect to the clock edge into the chosen nodes of the circuit under test. Circuit designs are developed to achieve random control of the pulse width, pulse arrival and pulse injection, to mimic actual SET randomness. The first parts of this chapter describe how the SET's characteristics influence its propagation through logic elements, and the remaining sections discuss pulse generation and randomization for the BIST.

## SET Control Parameters

SET amplitudes and widths in combinational logic depend on the relative magnitudes of the restoring drives and output loads of transistor devices. Large loads and large restoring drives reduce the probabilities of SETs, whereas small loads and small restoring drives increase the probabilities of SETs. The amount of charge required

to create an SET of amplitude $V_{DD}/2$ depends on the gate strength and loading capacitance at the struck node. Attributes of an SET such as its width, arrival time w.r.t the clock edge, amplitude and states of the gates it passes through, determine whether an SET will actually reach its destination and cause an error [3], [20], [22]-[23]. For an SET to be observed in a combinational logic, it must propagate to the circuit output or must be captured by a latch eventually causing an upset.

As a transient pulse propagates through a chain of logic gates, it may degrade both in width and amplitude. Simulations have shown that amplitude degradation can occur, when the inputs to a gate transition before the output of the gate has completely switched from a previous transition [46]. When this happens, the output switches in the opposite direction before it reaches the peak amplitude, $V_{DD}$ in the case of a zero to one transition, or ground in the case of a one to zero transition. Past research [47] has also shown that the rise and fall times of the SET pulse may be increased due to switching delays caused by the transitions of the gates. SET pulses of short duration may also be filtered out, if they occur farther away from the circuit output, due to the factors mentioned above.

Propagation of an SET to the output or a latch occurs when its amplitude and duration exceeds a certain minimum value for a particular technology. The width and amplitude of the transient are the result of a battle between the charge collection and charge conduction away from the strike node. For instance, consider an SET propagating through a chain of inverters connected to the input of a latch. If an ion strike occurs on the off drain of the inverter farthest from the latch, the SET will propage to the next inverter. Nonetheless it will affect the output of that inverter, only if

the amplitude of the SET is sufficient to drive the voltage on the gates of the two transistors beyond their switching levels for a time greater than half the total logic transition time.

Apart from the amplitude and duration of an SET pulse, which are key factors that decide the soft error rate, the clock frequency and arrival time of the SET pulse w.r.t the clock edge are also deciding factors affecting the soft error rate. Prior studies have shown that the occurence of SEUs in logic circuits increases with increasing clock frequency [22],[48]-[53]. There is also substantiation that the dynamic SEU rate may be dominated by errors generated in combinational logic such as NANDs and Inverters, as against sequential logic such as flip-flops [48]. Clock frequency is an important factor that must be considered for measuring dynamic SEUs in logic circuits, and its effects are different for combinational and sequential logic [3].

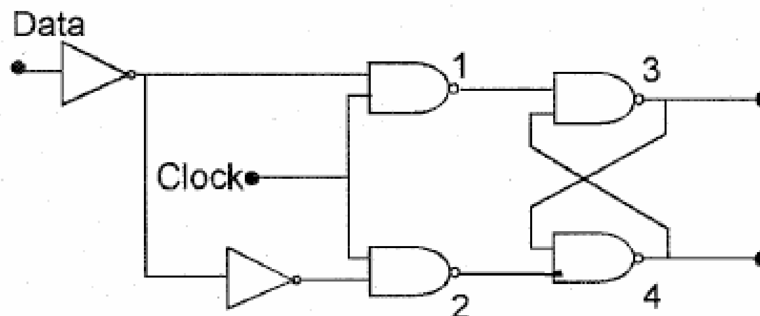


Fig. 5. D-type flip-flop containing 6 NAND gates and an input inverter [3]

For instance, consider the example of a D-latch with an inverter on the data input line shown in the Fig 5 . The inverter is a simple combinational logic element and the D-latch, a sequential element. When the clock is low, the data stored in the D-latch is unchanged and isolated from the value on the Data line. Under these conditions, nodes 3 and 4 in the D-latch are sensitive to SEU's. When the D-latch is enabled

forcing a fixed state on it, the latch is immune to SEU's [3]. Nevertheless if an ion hit at the output of the inverter just prior to the clock transitioning from high to low, has sufficient charge, the resulting voltage transient may be latched into the D-latch, causing an upset. If the ion strike occurs at a finite time prior to the clock edge, an upset may still occur, provided sufficient charge has been deposited for the voltage transient to last until the clock pulse arrives. As SEU's that originate from sequential logic (in this instance a D-latch) occur when the voltage on the clock line is low (50% of the time at all frequencies), they do not exhibit any frequency dependence, provided the setup time for the node is much less than the clock period. However, for SETs that originate in the combinational logic prior to the clock edge, inverter in this case; changing the clock frequency by a given factor will change the error rate by the same factor [3]. Based on the simple example, it can be understood that the sequential logic error rate should be largely independent of frequency, but the combinational logic error rate should be linearly dependent on frequency.

SETs must have a width greater than the critical transition time in order for them to propagate without attenuation [19]. Based on this, one can say that SETs produced by ions with larger LET have a greater probability of propagating without attenuation. But with feature sizes decreasing, SETs produced by lower LET ions will also be able to propagate. Assuming an SET has sufficient width and amplitude to propagate, it may still not reach a latch or register if it is masked by the gates through which it propagates. For a situation where the input conditions of the gates are favourable for the transient to propagate to a latch or register, it may still have no effect on the circuit owing to two additional obstructions. The first is that an SET must arrive at the latching clock edge

to be captured by a synchronous latch, and the second is that the incorrect data in the register may have no effect if the register is not accessed or if the corrupted information captured by the register is corrected before the next time the register is accessesed [3]. Transients shorter than the setup and hold time of the register will not be latched.

In a nutshell, digital logic error rates due to SETs are dependent upon the pulse width, amplitude and arrival time of an SET pulse with respect to the clock edge. SETs that do not reach rail-to-rail amplitude generally do not propagate far enough through the circuit to contribute significantly to the error rates. As a result, such perturbations can be largely ignored for error rate estimation without any loss of accuracy. . Only those voltage transients at the hit node that are large enough to cause the adjacent device to switch will propagate through the logic gates connected to it and become a logic signal that switches between the supply voltage and ground. Therefore it is sufficient to be concerned only about the maximum amplitude for a particular technology.

For a BIST technique to be efficient, it must be able to generate SET pulses of varying width and varying origination time with respect to the clock edge. The two primary parameters that one should be concerned about here are the pulse width and pulse offset with respect to the clock edge, as shown in Fig 6.

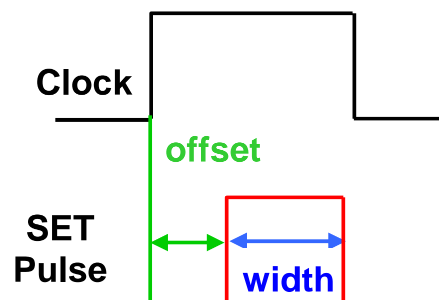


Fig. 6. Primary SET pulse parameters

## Technique to Control Pulse Width

Fig 7. demonstrates a straightforward method to control the pulse width of a generated transient using a delay chain. When the input 'in' to the X-OR is switched from low to high (or high-low), 'in' and the delayed 'in' which goes through a delay chain creates a voltage pulse at the output of the X-OR gate. The pulse width is almost equal in duration to the delay in the path since the output of the X-OR remains at logic

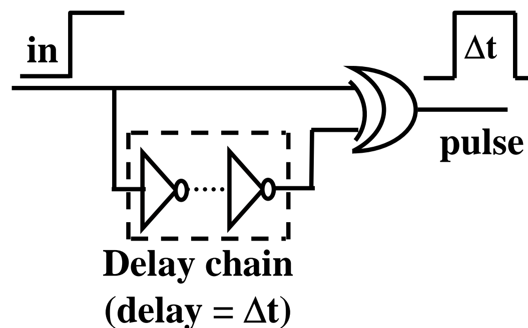


Fig. 7. Technique to create pulses of multiple widths based on delay set by the delay chain

'1' only when the inputs to it are logic '0' and '1'. By controlling this delay in the delay chain, the pulse width can be controlled. Different types of delay elements may be employed (current starved inverter buffer chains with an analog control input to starve the chain or a series of inverter buffers).

## Technique to Control Pulse Arrival

Fig. 8. shows a circuit principle used in controlling the origination time of a transient signal using a delay element and a NAND-based SR flip flop. The input 'in' propagates through a delay element to the 'S' input of the SR flip-flop, thus S goes low based on the delay set by the delay path. The output 'Q' will go high after the

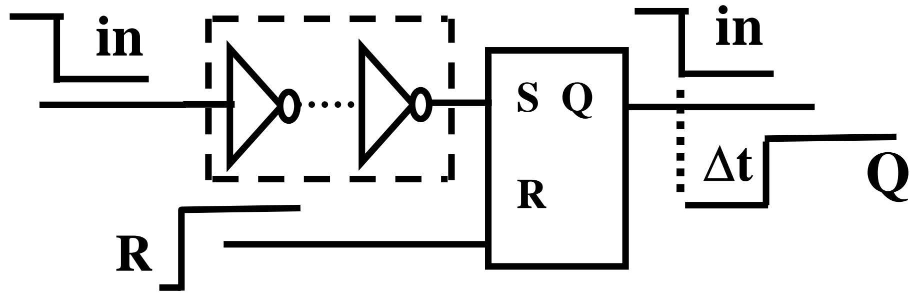


Fig. 8. Technique to control transient onset w.r.t to a synchronous input.

appropriate delay for the latch. Since the latch consists of two cross-connected NAND gates, the delay of the latch may approximately equal 4 gates. If the signals 'in' and 'R' are synchronized with the clock, the output 'Q' will be delayed from the clock edge by a time Δt. The value of Δt is the sum of the delay time in the 'in' signal and the delay of the latch as shown in Fig. 8.

## Single-event Transient Pulse-Generate Circuit

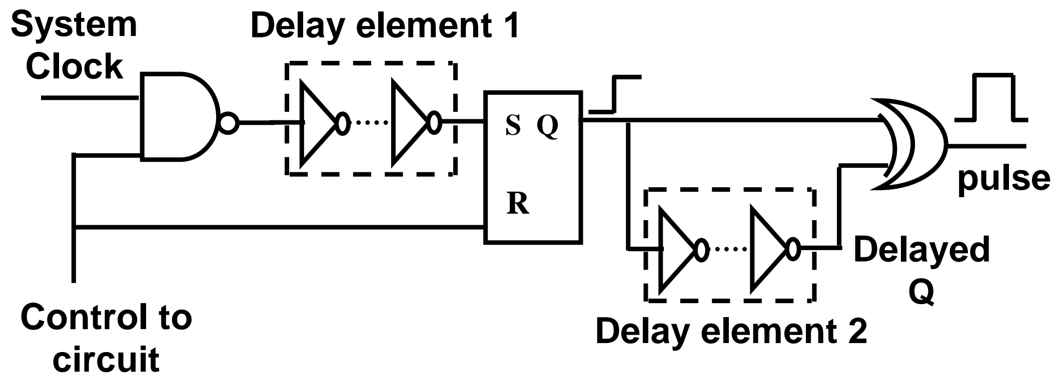


Fig. 9. Circuit to generate SETs of varying arrival times and pulse widths

The principles used in the previous two sections are put together to create a circuit that generates a transient similar to an SET as shown in Fig. 9. A NAND gate is

introduced before ‘delay element 1’ to control the generation of the voltage transient with respect to the clock edge. When the control input to the NAND gate, which is also the Reset to the NAND-based SR flip flop, is switched to logic high, the output of the SR flip flop switches high based on the time delay set by ‘delay element 1’. When Q goes high, a pulse is produced at the output of the XOR gate, whose width depends on the delay set by ‘delay element 2’. The control input can be brought low any time after the transient pulse is generated. By using varying lengths and different types of delay chains, the width and offset of the pulse with respect to the clock can be varied.

## Implementation in a Self-Test Mechanism

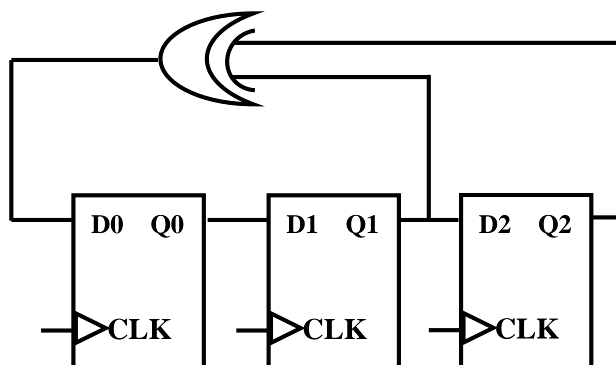


Fig. 10. A Linear Feedback Shift Register (LFSR)

Single-event strikes that occur in space are absolutely unpredictable and occur at random. The ions and other charged particles may strike any node of a circuit at any instance of circuit operation, which may or may not result in SETs. The SET pulses thus created using the Pulse-Generate circuit described in the previous section must be able to generate pulses of random widths and arrival times with respect to the clock edge to be able to operate in a self-test mechanism. Furthermore, the generated pulses have to

be randomly injected into the desired nodes of the circuit under test.

As the delay chains of the Pulse-Generate circuit shown in Fig. 9. determine the width and arrival of the generated pulse, the delay set by the delay elements need to be randomly controlled. This is achieved by the use of a Pseudo Random Number Generator [54]-[60] (PRNG) circuit that is used to randomly vary the delays set by the delay chains used in Figs. 7 and 8. There are several types of PRNGs – white noise, thermal noise from a resistor, photons, stream ciphers, linear feedback shift registers etc. A PRNG can start from an arbitrary state, and it will always produce the same sequence subsequently when initialized with that state, called the seed state. The maximum length of the sequence before the PRNG starts to repeat it is determined by the size of the seed state, measured in bits. Hence, if a PRNG's seed state contains n bits, the maximum length of the random sequence that can be produced is $2^n$. A Linear Feedback Shift Register (LFSR) is a pseudo random generator that can produce sequences of length $2^n - 1$ and is shown in Fig. 10. [61]-[65]. This LFSR uses an X-OR gate and a 3-bit shift register to produce a pseudorandom binary sequence (PRBS). By correctly choosing the points at which the feedback is taken from the 3-bit shift register, the outputs Q0Q1Q2 of the LFSR produce a PRBS of length $2^3 - 1$, a maximal-length sequence that includes all possible patterns (or vectors) of 3 bits, excluding the all-zeros pattern [66]-[67]. The advantage of the LFSR is that, it is purely a digital design made of only active components and hence occupies less area as compared to that of an analog device with passive components. Moreover, the randomness of the numbers produced can be easily varied by using a more complex LFSR [61]-[65].

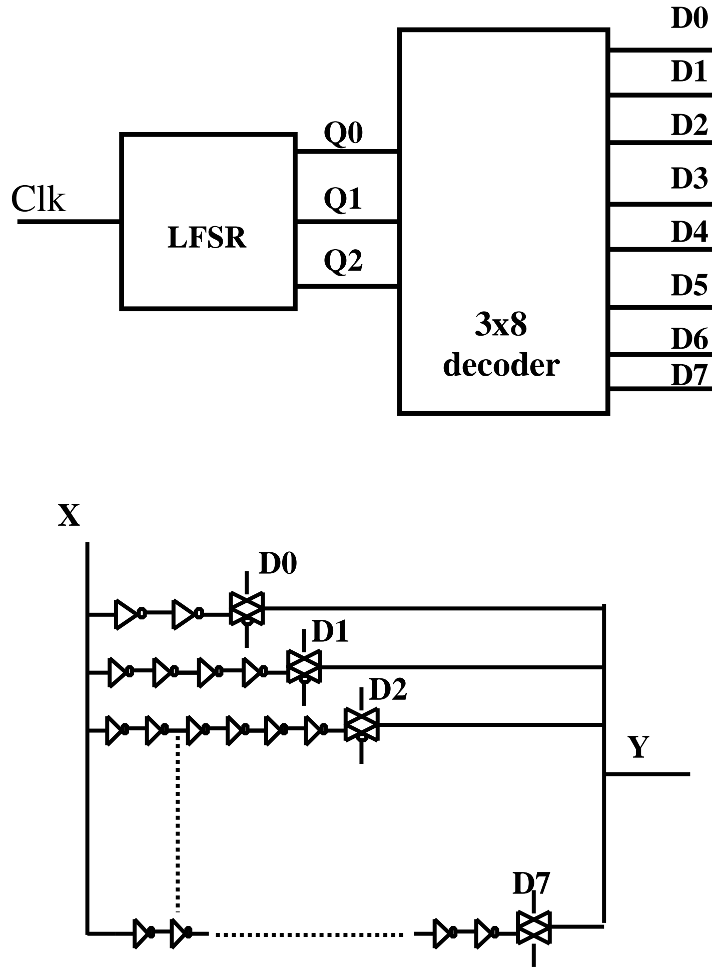


Fig. 11. LFSR with a decoder that sets the inverter delay

The number generated from the LFSR can be used to vary the delay as shown in Fig. 11. In Fig. 10, only a 3 stage LFSR is used to generate a random number that is fed into a decoder to yield 8 different pulse widths. The outputs of the LFSR (Q0Q1Q2) are connected to the inputs of a 3x8 decoder. The outputs D0-D7 of the decoder are given as control inputs to 8 Transmission Gates (TGs). Nodes X and Y in Fig. 11. correspond to the input and output of the delay element in Fig. 9. The input to each TG comes from a chain of inverter buffers of varying length. Depending on the sequence generated by the LFSR for a particular clock cycle, the delay is set for that cycle. For instance, if the

number generated by the LFSR is 001 (Q0Q1Q2), then D2 would go high, enabling the corresponding transmission gate, and the input signal at X would be delayed by the delay chain connected to the transmission gate controlled by D7, in this case being 4 inverter delays. By using such PRNGs in combination with delay elements to control both the width and arrival time of the pulse, pulses may be randomly generated with changeable arrival times and delays.

It may be noted that other forms of delay elements such as current-starved inverters, may also be used instead of inverter chains for precise control of delays. If used, they would require an analog control input to current starve the inverter chain. In such a case, the LFSR along with a basic Digital-to-Analog Converter (DAC) circuit might be used for the implementation of random pulse generation.

# CHAPTER IV

# SIMULATION/EXPERIMENTAL RESULTS

Simulation and experimental results for the Pulse-Generate circuit are presented in this section that verifies the practicality of the built-in testing design scheme.

## Simulation Results

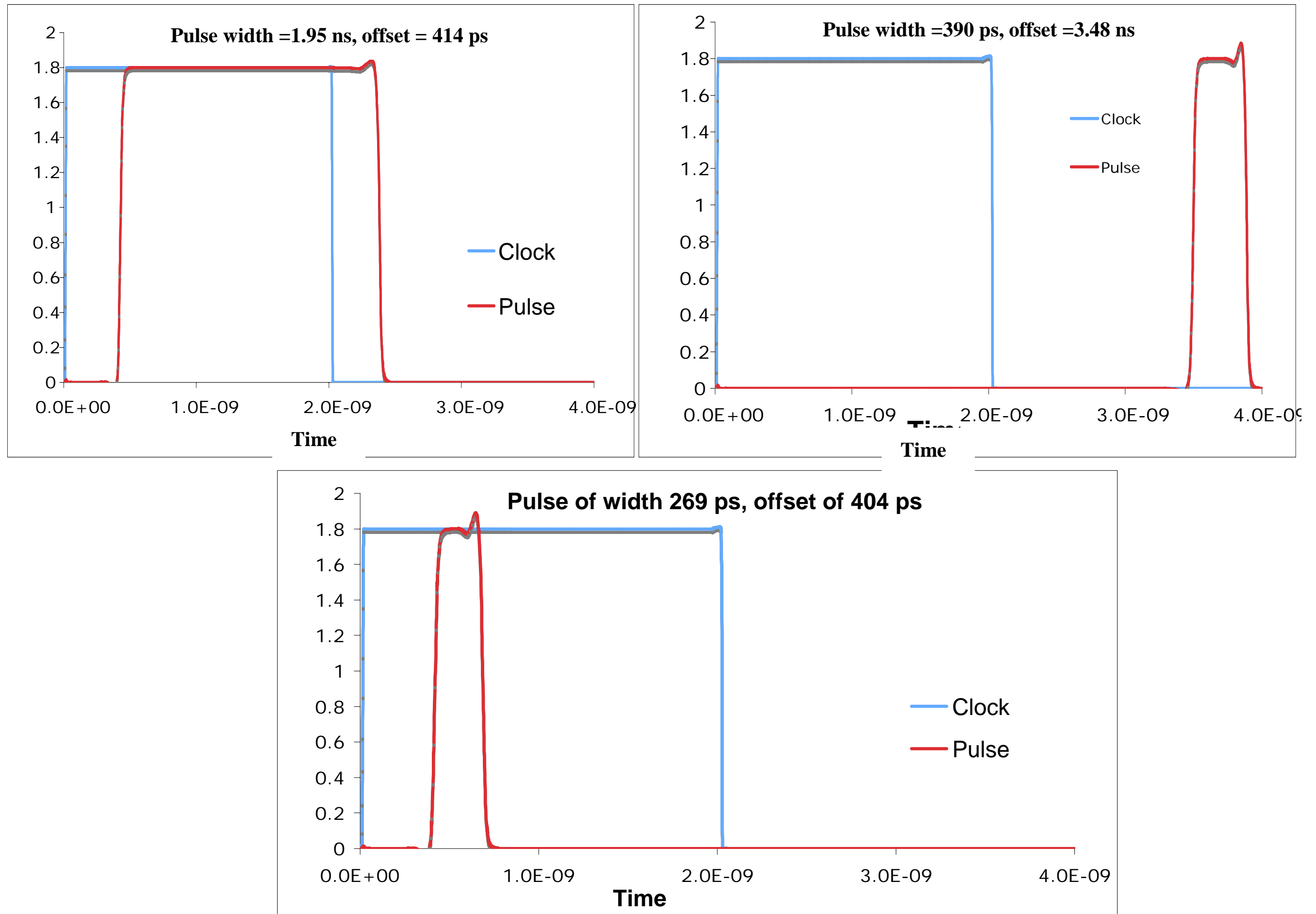


Fig 12. Sample simulations showing variation in pulse width and arrival

The Pulse-Generate cicuit described in Fig. 9. of the previous chapter was designed in 180 nm, with a series of 4 current-starved inverters to control both the arrival and width of the pulse. It was simulated on Cadence using the IBM cmos7sf process for the 180 nm tecnology node. The current-starved inverters required an analog control input to control the delay through the inverter chain, and by varying this control voltage, the width and arrival of the pulse w.r.t the clock were changed.

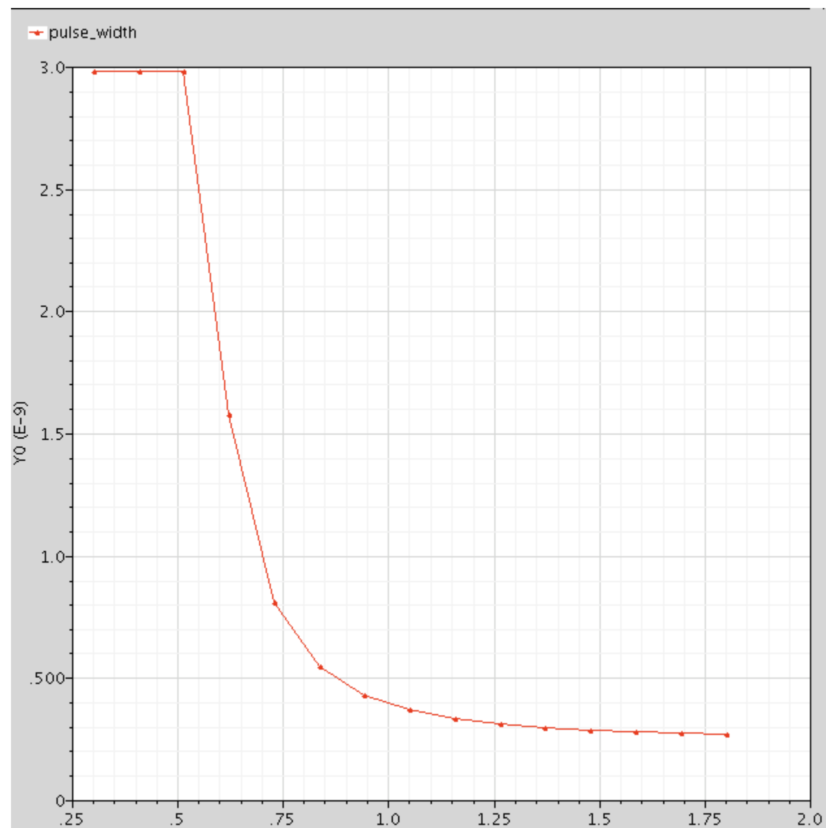


Fig. 13. Pulse width as a function of the current-starved inverter's control voltage

A few sample simulations done using the Cadence Spectre tool suite is shown in Fig. 12. The figures show sample pulses of widths varying from 270 ps to 1.95 ns, and offset w.r.t clock edge varying from 400 ps to about 3.5 ns. It should be noted that one

is able to control the pulse arrival over at least one whole clock window, and also generate pulses comparable to the width of the positive half cycle of the clock. For this set of sample simulations, a series of 4 current-starved inverters were used, but based on the range of pulse widths that need to be generated, a longer inverter chain may well be employed.

Parametric simulations performed for the Pulse-Generate circuit show that the range of pulse widths that can be obtained using a series of 4 current-starved inverters ranges from about 270 ps to about 3 ns. The pulse width is plotted as a function of the current-starved inverter's control voltage in Fig. 13.

## Experimental Results

The Pulse-Generate cicuit shown in Fig. 14. was fabricated in the 180 nm technology node through MOSIS, in collaboration with NASA. A series of 4 current-starved inverters were used as delay chains to control the pulse offset w.r.t clock edge and the pulse width. Fig. 15. shows the layout of the fabricated IC. The red oval in the layout shows the location of the Pulse-Generate circuit in the fabricated IC.

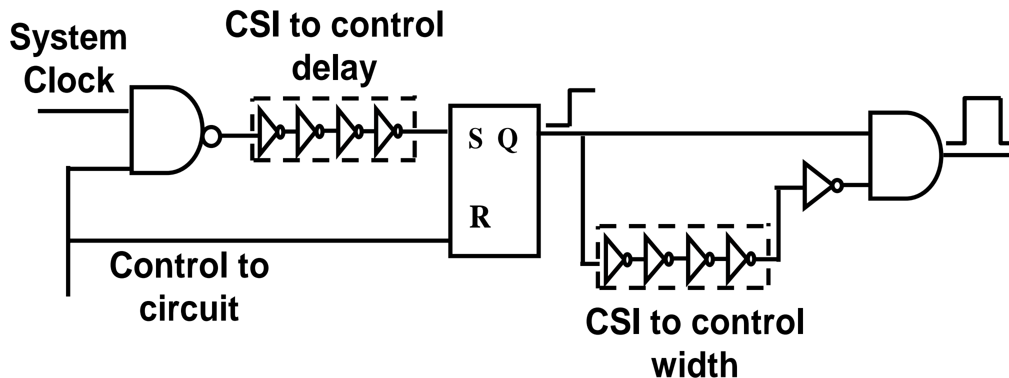


Fig. 14. Pulse-Generate circuit with a series of 4 current-starved inverter chain as delay elements

Based on simulations, the pulse widths that could be obtained in the 180 nm technology node were in the range of 300 ps to about 3 ns. Since pulses in the picoseconds range are fairly small pulses and there is a possibility that very small pulses can be killed by the output pad capacitance if it had to be measured on an oscilloscope,

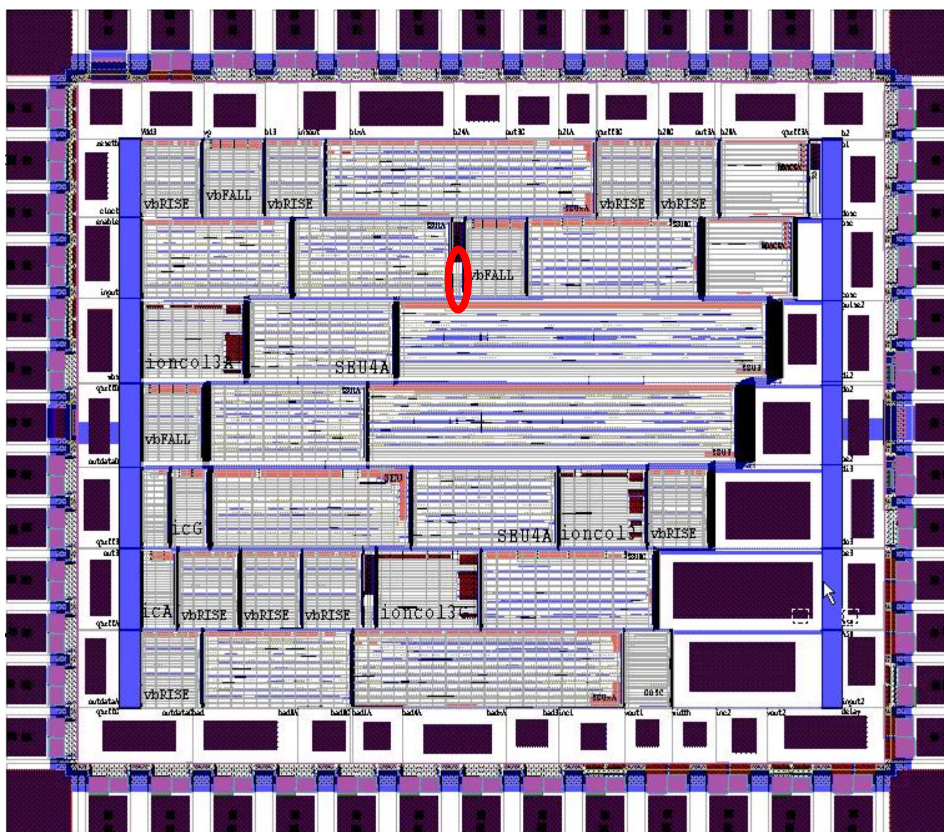


Fig. 15. Layout of fabricated IC; red oval indicates location of Pulse-Generate circuit

a pulse-capture circuit was used to measure the width of the pulses generated. An oscilloscope was also used to record the larger pulse widths off-chip. Results obtained using both techniques are presented in this section. Core supply voltage was 1.8 V.

## **On-chip Measurements**

Narasimham *et al.* designed a Pulse-Capture circuit that characterized the SET

pulsewidth in units of latch delays [68]. The Pulse-Capture circuit captures an SET pulse in a series of latches, which is then read out to determine the width of the pulse. For measuring the pulse widths generated from the Pulse-Generate circuit, the output of the same was fed into the input of the Pulse-Capture circuit. Every time a pulse was generated, it triggered the Pulse-Capture circuit which measured the pulse width in terms of inverter delays. Using FPGA programming, the pulse width was read out of the capture circuit.

The pulse width recorded with the Pulse-Capture circuit ranged from about 450 ps to over 4 ns. The range of pulse widths measured for varying control voltages of the current-starved inverters is shown in Fig. 16. The propagation delay for each measurement stage (latch) in the Pulse-Capture circuit in the 180 nm technology was 150 ps. Simulations indicated that when transients propagated through a long chain of gates, those less than about two to three times the propagation delay of a single stage

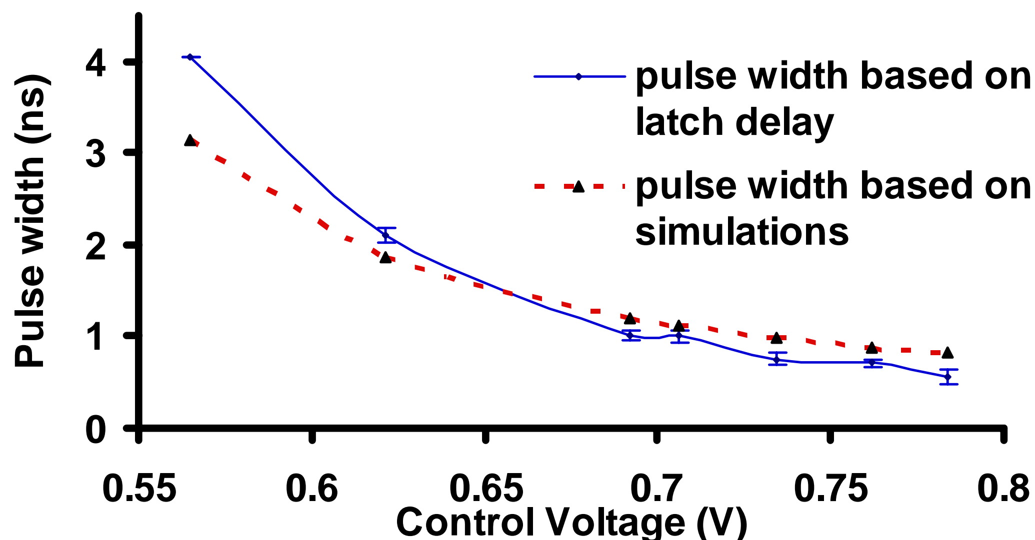


Fig. 16. Measurements taken on-chip with Pulse-Capture circuit

attenuated considerably. Those greater than this propagated without any significant attenuation. The output of the Pulse-Capture may indicate the pulse width as one, two or three stage delays wide although this may not be the actual starting width of the pulse; instead it might be the attenuated pulse width. For widths greater than about 450 ps, the measured pulse width is expected to be the actual width. It is because of this reason that pulses shorter than 450 ps could not be measured using the Pulse-Capture method, although the Pulse-Generate circuit is able to produce transients in that range. For every technology, the minimum pulse width and pulse offset that can be generated is approximately equal to two inverter delays of that technology. The Pulse-Capture circuit recorded the pulse widths in units of latch delays and the results along with the mean and standard error bars are plotted in Fig. 16.

## Off-chip Measurements

The output of the Pulse-Generate circuit was connected to an output pad and measured with an oscilloscope as well. Since such direct off-chip measurements are difficult to perform because of pulse distortion due to stray capacitances of the measurement system, including the loading and line capacitance effects, only larger pulses could be recorded with the oscilloscope.

The pulses recorded off the Tektronix 12GHz oscilloscope are shown in Figures 17 and 18. The blue waveform is that of a 25 MHz clock and the red waveform shows the pulse produced by the Pulse-Generate circuit. The ringing seen in the waveforms may be because of impedance mismatches, cables used for testing and the stray capacitances of the measurement system.

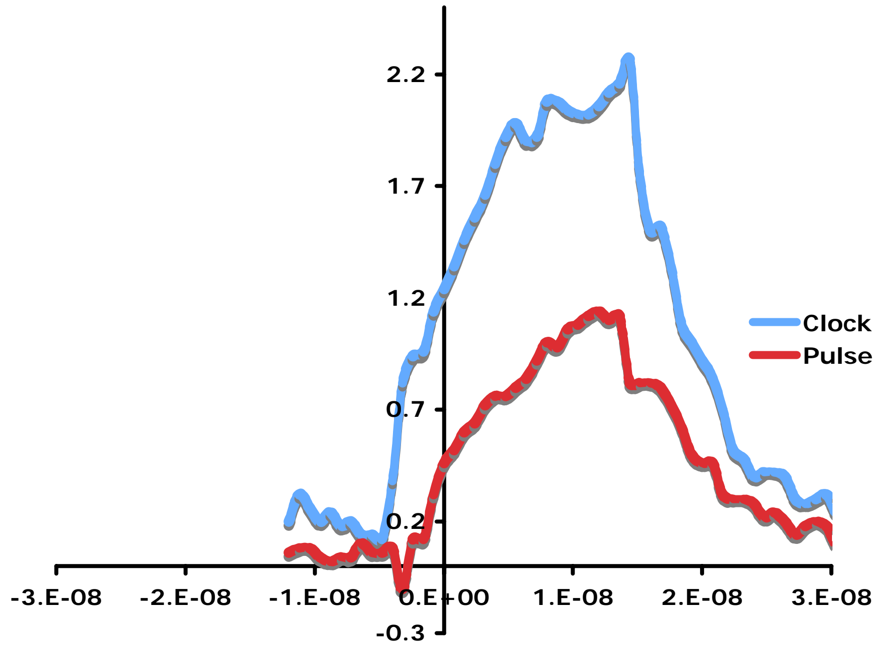


Fig. 17. Pulse arriving close to the rising edge of the clock

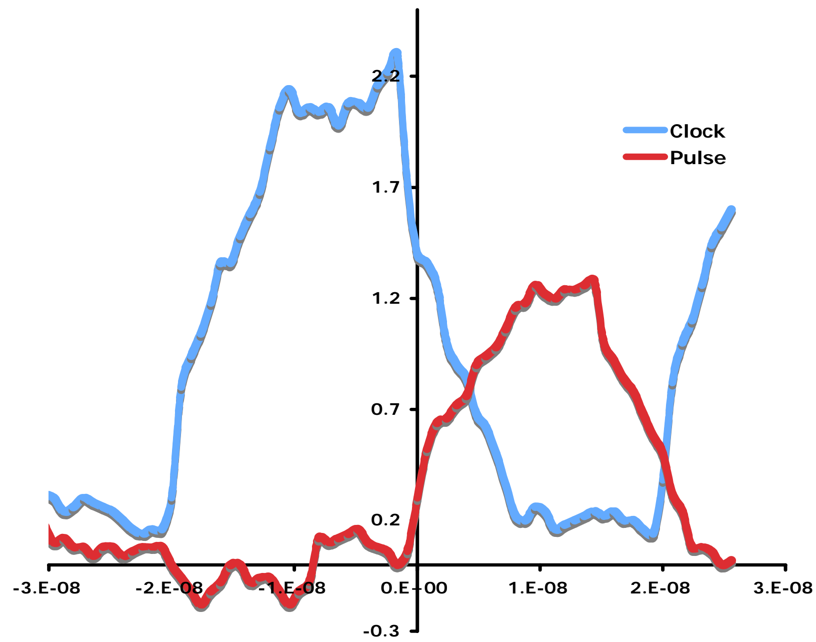


Fig. 18. Pulse arriving close to the falling edge of the clock

The pulse in Fig. 17. arrives closer to the rising edge of the clock. The pulse in Fig. 18. arrives close to the falling edge of the clock, and is primarily present in the negative half of the clock cycle. The width of the pulse in both figures is about 15 ns.

# CHAPTER V

# IMPLEMENTATION OF BIST IN DIGITAL CIRCUITS

The pulses generated using the BIST mechanism are used for the purpose of testing digital logic circuits. Digital logic circuits include both sequential and combinational elements, and the propagation of transients through these logic elements have to be comprehended in the first place, before implementing the BIST technique in digital circuits. Furthermore with decreasing feature sizes, the density of circuits are increasing tremendously and it is not feasible if each and every node of a circuit has to be tested using this method. The following sections discuss how the BIST can be implemented in digital logic circuits.

## Transients in CMOS Digital Logic Circuits

High-speed microprocessors, microcontrollers and digital signal processors contain both combinational and seqential logic elements. The output of a combinational logic circuit is purely a function of the present inputs only. Whereas in sequential logic, the output depends not only on the present inputs, but also the clock levels at prior times and the previous inputs. SETs are a concern in both combinational as well as sequential logic, and is becoming a severe problem for advanced technologies where smaller capacitances and smaller drive curernts result in lower charge requirements to cause an upset or a momentary voltage transient.

Charge collection in combinational logic differs from that in sequential logic. In

sequential logic, there is feedback in which a voltage transient generated at the drain of an off transistor feeds back to the gate of the same transistor and to the gate of its complementary transistor. When an SET reaches these two gates, they turn on the one involved in charge collection and turns off the other one, thus removing the reverse bias on the drain ensuing in the cessation of charge collection.

On the contrary, combinational logic circuits do not have any feedback mechanism associated with them. To demonstrate the difference, consider a single inverter with one nmos and one pmos transistor. The gates of the nmos and pmos are connected together, which forms the input to the inverter. The drains of the two transistors are shorted, which forms the output of the inverter. When the input is a logic low, the nmos is turned off, reverse biasing the drain of the transistor. When a single-event strike occurs at the drain of the nmos, most of the charge generated in or near the the junction by the energetic ions will be collected. During the course of this charge collection process, the bias on the drain remains essentially unchanged, except for the change in bias induced by the deposited charge itself. With an unchanging bias on the drain of the nmos, charge collection persists, unlike the case of in sequential logic, where the collected charge is removed. Thus, in combinational logic, there is an increase in charge colleciton.

With respect to SETs, there are three different ways by which combinational logic elements respond. First, they are sources of SETs when ions strike sensitive p-n junctions of the transistors. Second, under certain conditions they block the propagation of SETs that appear at their inputs, and third, they transmit and attenuate SETs.

## Identification of insertion nodes

With decreasing feature sizes and densely packed circuits, it is not feasible if transients have to be electrically injected into all nodes of a circuit using the built-in self-test scheme. For this reason, based on signal transition observability at the output, multiple nodes may be covered by a single node. These insertion nodes have to be identified and the chosen nodes need to be electrically injected with pulses. Using algorithms similar to test-vector generation for stuck at faults, a small subset of insertion nodes can be identified. Previous research [69] has also shown that more than 80% of the combinational logic soft errors in a circuit are caused by less than 50% of the nodes. The most vulnerable nodes to soft errors primarily determine the radiation response. This also allows reduction of the total number of nodes that need to be tested in a BIST approach.

The functionality of a digital logic circuit has a signficant influence in the soft error rate and sensitive area cross section. All the nodes in a digital logic circuit are not equally receptive to soft errors [69]-[72]. SETs are a cause for concern and change the computational functionality of the circuit only when captured by the storage elements in the circuit. All nodes in a circuit are vulnerable to single-events for some data input to that node, but the most critical metric in determining the sensitivity of that node is to evaluate the number of times it has an active path to the output and is capable of causing an upset [69], [73]. Propagation of the transient to the output depends on the following masking factors [74]-[76]:

(a) logical masking arises if there is no active path from the sensitive node to the output or a latch;

(b) latch-window masking occurs when the generated transient from the sensitive node propagates and reaches the latch/flip-flop at an instant other than the clock window for latching;

(c) electrical masking occurs if the generated transient attenuates as it propagates from the struck node to the output

All the above masking effects reduce the soft error rate in a combinational logic circuit. But again, with minimum feature sizes decreasing resulting in high density circuits, these masking effects could diminish significantly.

A 16-bit adder and a 4-bit multiplier are taken as examples to demonstrate how these masking effects can result in some nodes being more vulnerable than the others. In order to identify the insertion nodes, single-event simulations were performed on every node of the circuit. To assume a worst case situation, the simulated strikes were used to generate a transient of sufficient amplitude and width. Also, input conditions to the adder and multiplier decide whether the transient would propagate to the output. For example, a single-event strike which pulls an output node to ground would not have any effect on the system, if the input conditions to the circuit already pull the output node to ground.

## BIST in a 16-bit Adder

A 16-bit adder has about 300 nodes, and implementing BIST is not practical if pulses have to be introduced at all the 300 nodes, as it would result in too much area overhead. As the 16-bit adder is made up of 16 one-bit adders, SPICE simulations were performed on a single one-bit adder in the CMOS9SF 90nm IBM process to identify

sensitive nodes that are responsible for a majority of the errors. Simulations were carried out for SE strikes on every node in the 1-bit adder for the 8 different input combinations.

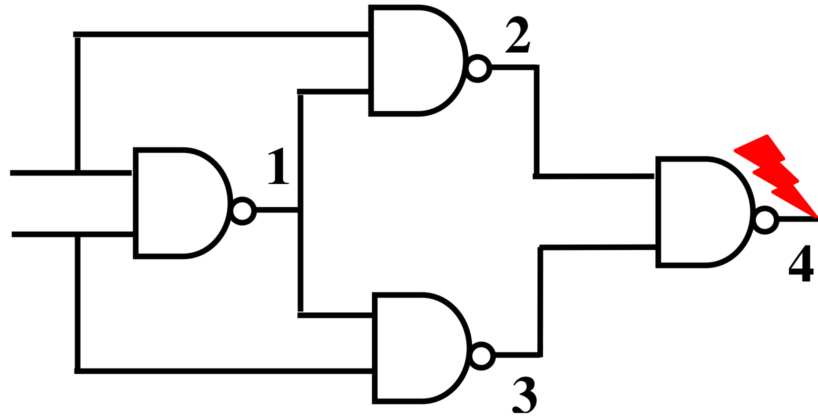


Fig. 19. Block diagram of a half-adder

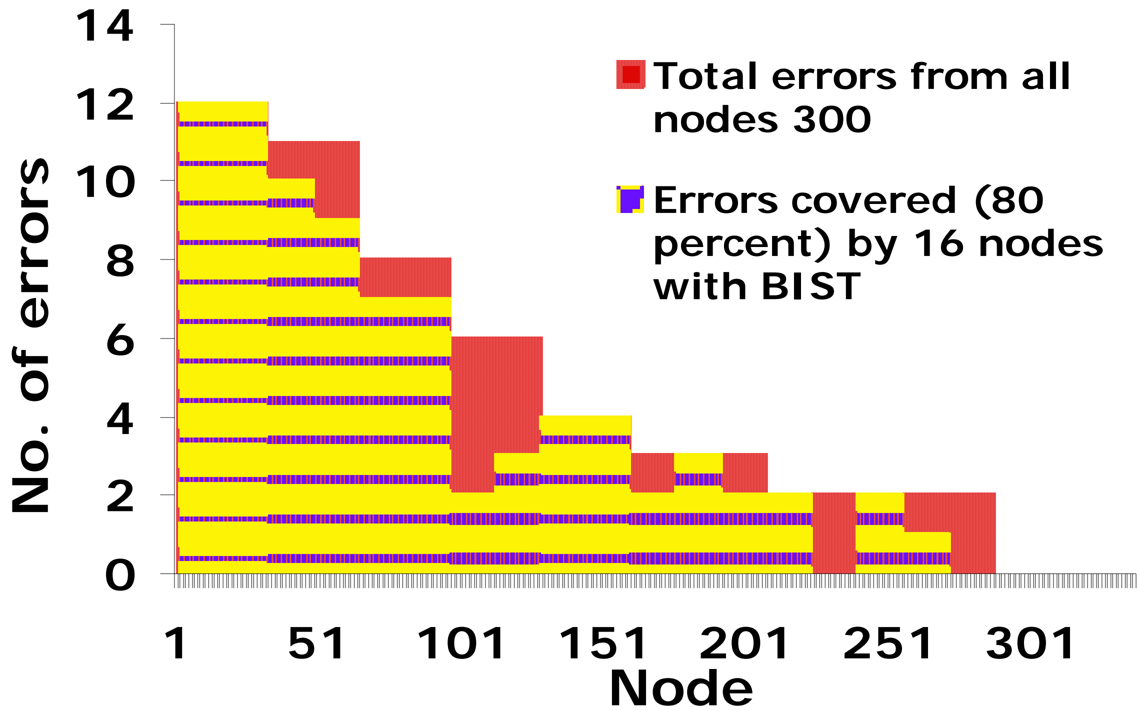


Fig. 20. Distribution of soft errors for all nodes and insertion nodes using BIST (80% coverage) in a 16-bit adder

Using equivalent inputs (an SE hit at both inputs of a NAND gate can be modeled by injecting a single pulse at its output) and logical masking (hits on multiple gates can be modeled by a single pulse injection at a logic gate present later on in the circuit path), the total number of nodes to test in any digital logic circuit can be reduced. Consider as an example, the half-adder shown in Fig. 19. which has 4 nodes. A single-event hit at each of the nodes 1,2,3 and 4 can be modeled by a single-event strike at node 4 alone. By employing such techniques and masking effects, the total number of nodes requiring pulse injection was reduced from 300 to 16.

Such analyses were performed for the one-bit adder and the coarse estimation was extended to the entire 16-bit adder. The total number of nodes requiring pulse injection was reduced from 300 to 16, and these 16 nodes were chosen in order to facilitate maximum coverage of errors. About 100 upsets were recorded for a one-bit adder, which when extended to the entire 16-bit adder accounted for 1600 errors. BIST was then used to inject error pulses into the chosen 16 nodes to give an overall estimation of the circuit's vulnerability to single-events. About 1600 upsets were recorded for the 16-bit adder and the distribution of errors is shown in Fig. 20. To account for the response of all the 300 nodes, the 16 insertion nodes were injected with pulses multiple times, and that accounted for about 80% of the total upsets, as shown in Fig. 20. The red bars in the figure account for all the 1600 errors, with the distribution shown for each node. The striped yellow and blue bars that overlap the red bars account for 80% of the errors that are accounted for by the chosen 16 nodes.

## BIST in a 4-bit Multiplier

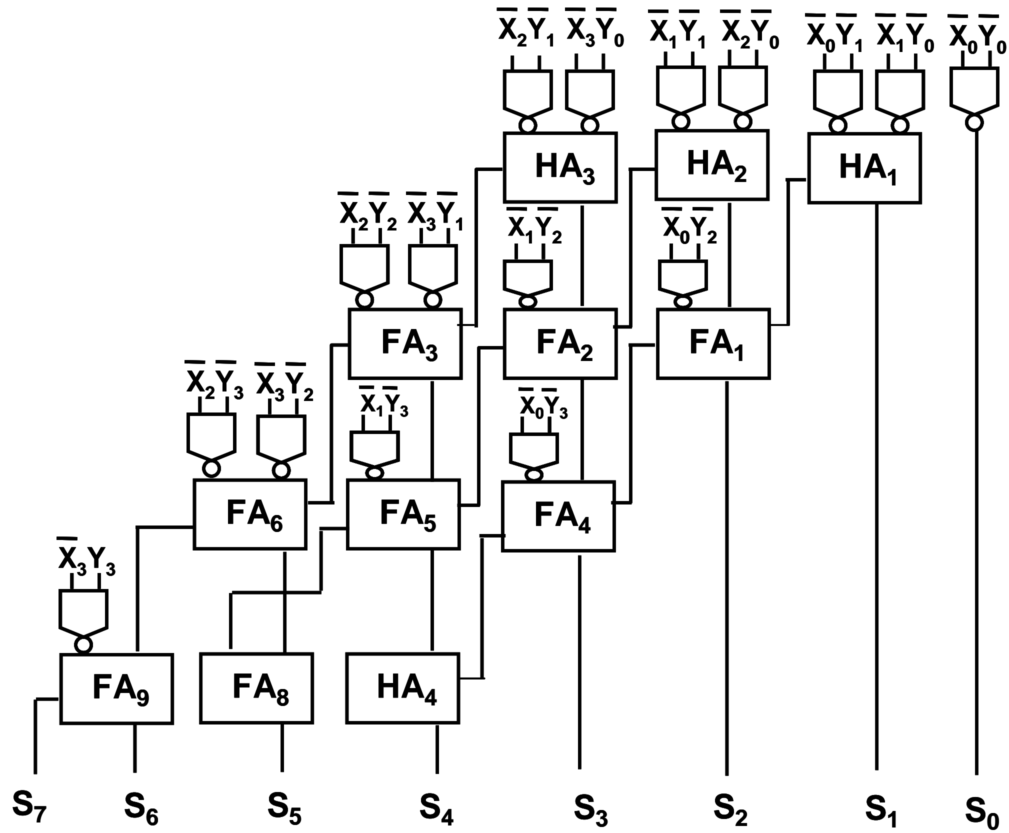


Fig 21. A 4bit-multiplier

A similar but in-depth and exhaustive anaylsis was performed on the 4-bit multiplier shown in Fig. 21. A 4-bit multiplier has about 211 nodes that are receptive to single-events, with 8 inputs and 8 outputs. In terms of total node count, it has fewer nodes than the 16-bit adder but in terms of analysis it is much more complex. A 16-bit adder is made of 16 full adders, and each full adder has exactly the same functionality. In such a case, one full adder could be analyzed in detail and the analysis was extended to the entire 16-bit adder. But the same is not possible in a 4-bit multiplier, although it also comprises of half adders and full adders. The 4-bit multiplier shown in Fig. 21.

cannot be broken down into simpler blocks that are repeated several times, requiring that the above described processes to identify insertion nodes has to be done

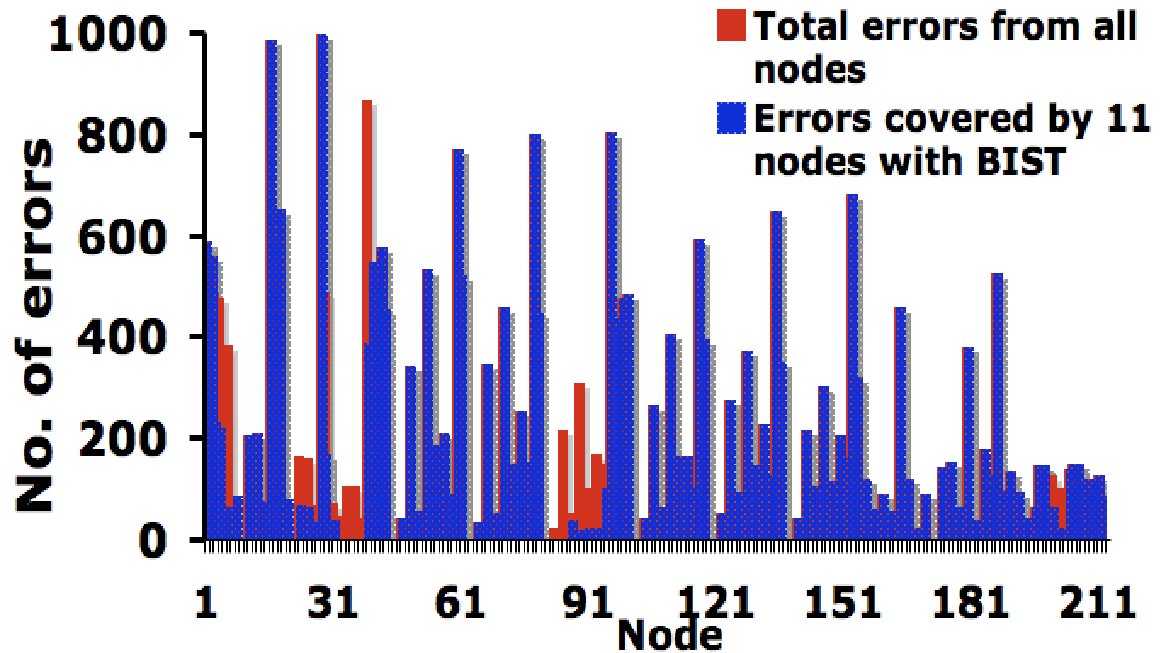


Fig. 22. Distribution of soft errors for all nodes and insertion nodes (88% coverage) using BIST in a 4-bit multiplier

considering the circuit as one whole block, making the analysis very difficult. Single-event strikes (both n-hits and p-hits) were simulated on every node of the circuit, for all the 256 input combinations, which resulted in a total of about 83,000 simulations. These simulations were performed using the Cadence Spectre tool suite in the CMOS9SF 90 nm IBM process on ACCRE (Advanced Computing Centre for Research and Education, Vanderbilt University).

The 4-bit multiplier has 8 outputs that were analyzed, and a transient on any of the multiplier outputs was considered as an error. A total of 30,707 errors were recorded for the 83,000 simulations performed. The multiplier circuit was analyzed by using equivalence of nodes, logical and electrical masking as described in the previous

sections. Using this analysis the number of insertion nodes that contributed to the majority of the errors was determined to be 11 nodes. Using the BIST to inject error pulses into these chosen nodes covered approximately 88% of the total recorded errors generated using the exhaustive approach. The distribution of soft errors for the multiplier is shown in Fig. 22. The bar chart in Fig. 22 shows all the errors recorded for the 4-bit multiplier, which are shown in red. The bars shown in blue are the errors covered by the chosen 11 nodes of the 4-bit multiplier circuit. It can be seen that most of the blue bars overlap the red bars, showing that they cover a major percentage of errors recorded from all 211 nodes. Since these chosen 11 nodes account for errors that are caused by strikes at other nodes as well, the 11 nodes have to be struck multiple times to account for the errors caused in the nodes.

Using such analyses, any digital logic circuit can be analyzed and tested for SETs using the BIST procedure. From the two illustrations here, it can be understood that the total number of nodes that require to be tested for any circuit using the BIST methodology can be reduced by a few orders of magnitude from the original node count. For circuits with an even larger number of nodes, there can be reduction in the node count by several orders of magnitude.

## Pulse Injection

The 16-bit adder and 4-bit multiplier were taken as examples to illustrate how the BIST approach could be applied to different types of digital logic circuits. In a general case of a digital design that has latches between chains of combinational logic elements, it is left to the discretion of the designer as to how the pulses have to be

injected. The pulse injection may be done at random or it can be controlled with the reset signal so it is introduced into the circuit only at specific instances of its operation. Depending on the circuit under test, the pulse may be injected into a combinational block and the generated transient may propagate to an input of a latch where it can get registered as an error, or the pulse may be directly inserted into a sequential block where it can be stored and could propagate to the rest of the circuit.

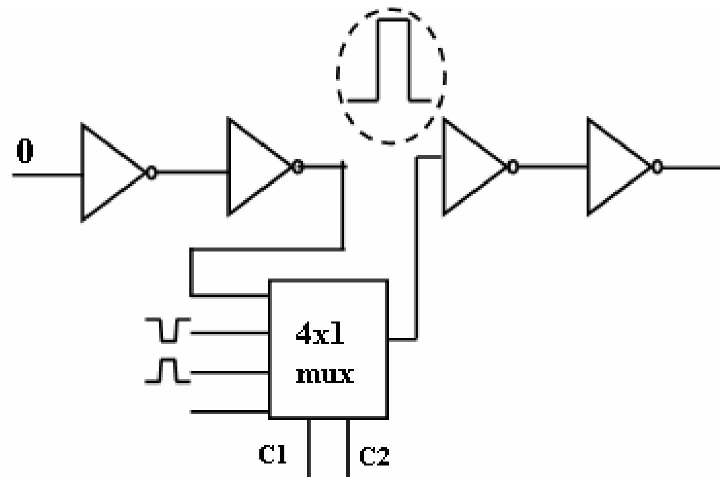


Fig. 23. Multiplexer design to inject a transient pulse into a logic node

The BIST should be able to operate under three conditions; (i) when no strike is modeled, the unchanged logic value of the node has to propagate (ii) when modeling an n-hit, a high-low-high pulse has to be injected and (iii) when modeling a p-hit, a low-high-low pulse has to be injected. The generated pulse can be injected into the requisite nodes by using a simple multiplexer design as shown for a sample inverter chain in Fig. 23. The figure shows a multiplexer with the unchanged logic value of the node, a low going, or a high going transient that can be injected into the circuit and the mode of

operation can be controlled using the control inputs C1 and C2 to the multiplexer. In the chain of inverters shown in Fig. 23, the input to the first inverter is logic low. For this input condition, only a p-hit at the drain of the second inverter will affect the circuit output, and the controls to the multiplexer should be given accordingly. The circuit response to SETs can be evaluated by injecting pulses of varying duration and origination time while the IC is operating with the desired set of input voltages. Additionally to include charge sharing, multiple SETs can be easily injected into the circuit within the same clock cycle.

# CONCLUSIONS

SETs are becoming increasingly important for advanced technologies, and it is important that each and every circuit design be tested in depth to understand the SE response of the same. This thesis describes a novel built-in design to test for SETs in digital logic circuits. Single-event strikes that occur in space or in the terrestrial environment are completely random, and one cannot predict which nodes of a circuit will be struck or what the mode of operation of the circuit would be during the time of strike. The BIST, by electrically injecting pulses of randomly varying width and arrival times with respect to the clock, mimic the actual SET unpredictability. The Pulse-Generate circuit that forms part of the BIST mechanism was simulated and fabricated in the 180 nm technology node. Simulations show that a wide range of pulse widths can be generated at varying arrival instances w.r.t the clock. Experimental data from the 180 nm technology prove that the pulses recorded ranged from 450 ps to over 4 ns. The width and offset of the pulse can be varied by using different types of delay elements.

As more circuits are being packed in less area now, the number of nodes to test also increases. If all nodes of a circuit have to be tested with the BIST technique, it would result in too much area overhead. To make the BIST design more efficient and realistic, identifying the receptive nodes and taking advantage of the masking factors reduce the total number of nodes requiring pulse injection. This is demonstrated with a 16-bit adder and a 4-bit multiplier. In the 16-bit adder, about 5% of the nodes covered 80% of the soft errors. For the 4-bit multiplier, 5% of the nodes accounted for 88% of the total soft errors.

In view of the fact that conventional methods of testing such as laser and heavy-ion are very expensive and can be time consuming, such built-in testing methods are a very attractive alternative. Based on the circuit that requires to be tested, the BIST design can be altered to suit the testing requirements. By monitoring the outputs of the circuit while operating under the BIST mechanism, the total number of errors can be recorded.

The BIST approach presented here injects SET pulses of random duration at random circuit nodes. This will help to determine the circuit-level response to SEs efficiently, though the technology related device-level effects (such as parasitic bipolar-transistor contribution to charge collection) cannot be obtained. Additionally, to relate results from BIST approach to results from heavy-ion testing, a calibration has to be carried out relating SET pulse width distribution to LET of an ion.  This calibration needs to be done for all the ions present in the environment of interest.

In a nutshell, BIST is a cost effective method of testing for SETs in any conventional laboratory that can give an overall estimate of the circuit's vulnerability to single-events.

# APPENDIX

## DATA ANALYSIS SCRIPTS

The following are some of the basic scripts that were used to automate the simulations of the 4-bit multiplier using CADENCE and the SPECTRE environment in the CMOS9SF 90 nm technology node. The multiplier had 8 inputs, with 211 nodes receptive to n and p-hits, resulting in a total of 83,000 simulation results to analyze. Scripts were written to automatically change input combinations, strike location, save results and extract errors from the multiplier outputs. The files are listed in the sequence they were run.

**File 1 – startSim.pbs**

```
#!/bin/bash

#PBS -M anitha.balasubramanian@vanderbilt.edu
#PBS -m a
#PBS -l mem=600mb
#PBS -l nodes=1:ppn=1:x86
#PBS -l walltime=25:00:00
#PBS -l cput=25:00:00
#PBS -o /home/balasua2/multiplier_nhit_transients_042208/log/pbs_output174.log
#PBS -j oe

count=1
startNum=1
HOMEPATH="/home/balasua2/multiplier_nhit_transients_042208"
tmpSring="fileCmp.tmp"
HITTYPE="n"

##########################################################################
##########
# Create Binary Input Arrays X and Y: Loop through all combinations of X and Y #
##########################################################################
##########
```

```
for X3 in 0 1; do
for X2 in 0 1; do
for X1 in 0 1; do
for X0 in 0 1; do
for Y3 in 0 1; do
for Y2 in 0 1; do
for Y1 in 0 1; do
for Y0 in 0 1; do

#for X3 in 0 0; do
#for X2 in 0 0; do
#for X1 in 0 0; do
#for X0 in 0 0; do
#for Y3 in 0 0; do
#for Y2 in 0 0; do
#for Y1 in 0 0; do
#for Y0 in 0 0; do

echo "X=$X3$X2$X1$X0 and Y=$Y3$Y2$Y1$Y0"; echo;
########################################################################
###########                    Loop through all NODES                    #
########################################################################
##########

#for ((NODE=2; NODE<204; NODE+=1))
for ((NODE=174; NODE<176; NODE+=1))
do
    #if the current value is greater than or equal to the start number
    if [ $count -ge $startNum ]
    then
        #if file exists then remove it
        #if [ -e $HOMEPATH/filesCmp.tmp ]
        #then
        #    rm $HOMEPATH/filesCmp.tmp
        #fi

        #list the filenames of the completed sims in filesCmp.tmp
        #ls $HOMEPATH/sim_data > $HOMEPATH/filesCmp.tmp
        #tmpComplete=$(wc -l $HOMEPATH/filesCmp.tmp)

        #grab number of files (mod out filename)
        #runsComplete=${tmpComplete%$HOMEPATH/filesCmp.tmp}

        #echo "Last completed run: $runsComplete"
        #echo $count
```

```
        #if current count is greater than the number already completed
#in other words: don't rerun a sim that has already been completed
        #if [ $count -gt $runsComplete ]
        #then
            tmpFile="$HOMEPATH/sim_data/nAdder-$HITTYPE"
            tmpFile2="$tmpFile$NODE-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0"
            tmpFile3="$tmpFile2.data"
            echo "running $tmpFile3"; echo;
            cat $HOMEPATH/simulate.sh | sed s/%X3%/$X3/g | sed s/%X2%/$X2/g | sed
s/%X1%/$X1/g | sed s/%X0%/$X0/g | sed s/%Y3%/$Y3/g | sed s/%Y2%/$Y2/g | sed
s/%Y1%/$Y1/g | sed s/%Y0%/$Y0/g | sed s/%NODE%/$NODE/g | bash
#sed s/%HOMEPATH%/$HOMEPATH/g | bash
        #fi
    fi
    count=$((count+1))
done
done; done; done; done; done; done; done; done
```

**File 2 – simulate.sh**

```
#!/bin/bash

# Commands go here
X3=%X3%
X2=%X2%
X1=%X1%
X0=%X0%
Y3=%Y3%
Y2=%Y2%
Y1=%Y1%
Y0=%Y0%
NODE=%NODE%
HOMEPATH=/home/balasua2/multiplier_nhit_transients_042208
#HOMEPATH=%HOMEPATH%

cd $HOMEPATH
#echo $HOMEPATH
#echo "in simulate.sh"
cat run_scripts.sh | sed s/%X3_SH%/$X3/g |sed s/%X2_SH%/$X2/g | sed
s/%X1_SH%/$X1/g | sed s/%X0_SH%/$X0/g | sed s/%Y3_SH%/$Y3/g | sed
s/%Y2_SH%/$Y2/g | sed s/%Y1_SH%/$Y1/g | sed s/%Y0_SH%/$Y0/g | sed
s/%NODE_SH%/$NODE/g > sh/$NODE-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0.sh

#sed s/%HOMEPATH_SH%/$HOMEPATH/g > sh/$NODE-X$X3$X2$X1$X0-
Y$Y3$Y2$Y1$Y0.sh
```

```
bash sh/$NODE-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0.sh
```

**File 3 – runscripts.sh**

```
#!/bin/bash
#source /usr/local/cadence/bashrc.cadence
X3=%X3_SH%
X2=%X2_SH%
X1=%X1_SH%
X0=%X0_SH%
Y3=%Y3_SH%
Y2=%Y2_SH%
Y1=%Y1_SH%
Y0=%Y0_SH%
NODE=%NODE_SH%
HOMEPATH=/home/balasua2/multiplier_nhit_transients_042208
#HOMEPATH=%HOMEPATH_SH%

if [ $Y0 -eq 1 ]
then

    Y00=1.2
else
    Y00=0
fi
if [ $Y1 -eq 1 ]
then

    Y11=1.2
else
    Y11=0
fi
if [ $Y2 -eq 1 ]
then

    Y22=1.2
else
    Y22=0
fi
if [ $Y3 -eq 1 ]
then

    Y33=1.2
else
    Y33=0
```

```
fi
if [ $X0 -eq 1 ]
then

    X00=1.2
else
    X00=0
fi
if [ $X1 -eq 1 ]
then

    X11=1.2
else
    X11=0
fi
if [ $X2 -eq 1 ]
then

    X22=1.2
else
    X22=0
fi
if [ $X3 -eq 1 ]
then

    X33=1.2
else
    X33=0
fi

cat $HOMEPATH/tmpl/nAdder.tmpl | sed s/%X3%/$X33/g | sed s/%X2%/$X22/g | sed
s/%X1%/$X11/g | sed s/%X0%/$X00/g | sed s/%Y3%/$Y33/g | sed s/%Y2%/$Y22/g |
sed s/%Y1%/$Y11/g | sed s/%Y0%/$Y00/g | sed s/%NODE%/$NODE/g >
$HOMEPATH/data/raw/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-n$NODE.scs

/usr/local/isde/cadence/IC5141/tools/bin/spectre $HOMEPATH/data/raw/nAdder-
X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-n$NODE.scs

python $HOMEPATH/scripts/fixraw_tran.py $HOMEPATH/data/raw/nAdder-
X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-n$NODE.raw >
$HOMEPATH/data/sorted/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-
n$NODE.raw.sorted

for ((i=0; i<8; i=i+1))
do
    python $HOMEPATH/scripts/getTransient.py $HOMEPATH/data/sorted/nAdder-
```

```
X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-n$NODE.raw.sorted 0 $((i+2)) 0 >>
$HOMEPATH/sim_data/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-n$NODE.data
done

rm $HOMEPATH/data/raw/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-
n$NODE.raw

#rm $HOMEPATH/data/sorted/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-
n$NODE.raw.sorted

rm $HOMEPATH/data/raw/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-
n$NODE.scs

rm -r $HOMEPATH/data/raw/nAdder-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0-
n$NODE.ahdlcmi

#rm $HOMEPATH/sh/$NODE-X$X3$X2$X1$X0-Y$Y3$Y2$Y1$Y0.sh

#rm $HOMEPATH/log/pbs_output.log
```

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