AN ENHANCED SINGLE-EVENT CHARGE CANCELLATION TECHNIQUE FOR SENSITIVE CIRCUIT NODES

By

Daniel Scott Vibbert

Thesis

Submitted to the Faculty of the

Graduate School of Vanderbilt University

In partial fulfilment of the requirements

for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

August 31, 2018

Nashville, Tennessee

Approved:

William Timothy Holman, Ph. D.

Jeffrey Scott Kauppila, Ph. D.

ACKNOWLEDGMENT

I would like to acknowledge the expertise and wisdom of my advisor, Dr. Tim Holman, whose investment of time and energy into my career has made this work possible. I would also like to thank Dr. Jeff Kauppila for his tremendous devotion to technical accuracy in the field of radiation effects and for his years of hard work that has built the foundation upon which my thesis now stands. I am also indebted to Dr. Lloyd Massengill for his masterful perspective and strong leadership that propelled me and my classmates beyond our goals and into the glory of cutting-edge academic achievement.

I must also express my sincere gratitude to the Defense Threat Reduction Agency for funding my work, and would like to thank my fellow students and professors at Vanderbilt University and the Institute of Space and Defense Electronics for their encouragement and ideas. I would also like to acknowledge my engineering faculty at the University of Evansville for inspiring me to pursue graduate studies.

Finally, I would like to thank my parents for their unwavering support and guidance, who have sacrificed so much because they believed in me.

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CHAPTER I

Introduction

As early as the 1960s, electrical engineers have sought to develop microelectronic integrated circuits that are radiation tolerant by virtue of their design, as opposed to their semiconductor process [1]. The term “radiation-hardening-by-design” (RHBD) describes these efforts and, as shown in Chapter II, represents the culmination of decades of research performed by the radiation-effects community. Designing a radiation-hardened circuit requires knowledge of the radiation environment, physical and electrical understanding of radiation effects, identification of radiation vulnerabilities, and a firm grasp on integrated circuit layout design principles.

In this thesis, a novel enhancement to a recently developed RHBD technique is proposed. The technique under investigation is called Sensitive Node Active Charge Cancellation (SNACC) and was shown in [2-4] to protect critical circuit nodes from single-event effects (SEE) in the form of single-event transients (SET). The SNACC technique exemplifies the RHBD approach by identifying a sensitive circuit node and leveraging physical charge collection mechanisms to mitigate SETs originating on that node.

To facilitate the following RHBD discussion, a prerequisite chapter containing single-event radiation effects background information will be given first. After discussing the basic physical mechanisms behind SETs and the advancement of SET models over the decades, a critical analysis of SNACC is presented. Once room for improvement with the SNACC technique has been identified, a conceptual renovation of SNACC is

presented as Enhanced SNACC (ESNACC). A suggested implementation of ESNACC in a 180 nm bulk CMOS technology is then presented, followed by simulation results that demonstrate the success of the proposed technique enhancements.

CHAPTER II

Single-Event Transients Background

To understand how RHBD techniques might be applied to microelectronic circuits, the engineer must first possess a practical understanding of how different kinds of radiation effects are induced and how they can be detrimental to electronic systems. Single-event transients (SET), the radiation effects mitigated by the SNACC hardening technique, will be introduced in this chapter, along with the pertinent physics that are required to understand how SNACC mitigates SETs. After the basic mechanisms, characteristics, and models of SETs have been established, a brief discussion on circuit-level SET error metrics are given to provide RHBD insight. Finally, an explanation of the phenomenon known as charge sharing will be given as a prerequisite to SNACC.

Single-Events Overview

Single-event effects are distinguishable from total-ionizing dose (TID) effects because of the tight locality of their related phenomena, while TID effects generally occur throughout an entire integrated circuit. Single-event effects occur when an energetic particle interacts with a circuit's semiconductor lattice. As the energetic particle travels through the semiconductor, it slows down and loses energy. As shown in the charge generation section of this chapter, most of the lost energy is absorbed by the semiconductor, which excites electrons from the valence band to the conduction band. In the following charge collection section, it is shown how the sudden burst of charge can be collected by the microelectronic circuit, and create a measurable transient or pulse that interferes with correct circuit operation.

Single-Event Charge Generation

Energetic particles from radiation are responsible for single-event charge generation in one of two ways, direct ionization or indirect ionization [5]. With direct ionization, a particle's ability to generate single-event charge depends how much energy it can deposit in the semiconductor as it passes through. A metric which describes the amount of energy a directly ionizing particle can transfer per unit length, normalized to the target material's density, is called linear energy transfer (LET) and is typically expressed in units of MeV * cm^2 / mg. For a short cross section of silicon and an incoming particle of known LET, it is possible to estimate the amount of charge per unit distance that is generated in the cross section with Equation 1.

$$\text{Generated Charge [fC / μm]} = 10.4 * \text{LET [MeV} * \text{cm}^2 \text{ / mg]} \quad (1)$$

The constant in equation 1 is a result of silicon's density (2330 mg / cm^3) and the amount of energy required to generate a single electron-hole pair, which is about 3.6 eV. Equation 1 gives charge generation with the dimensions of charge per unit length because

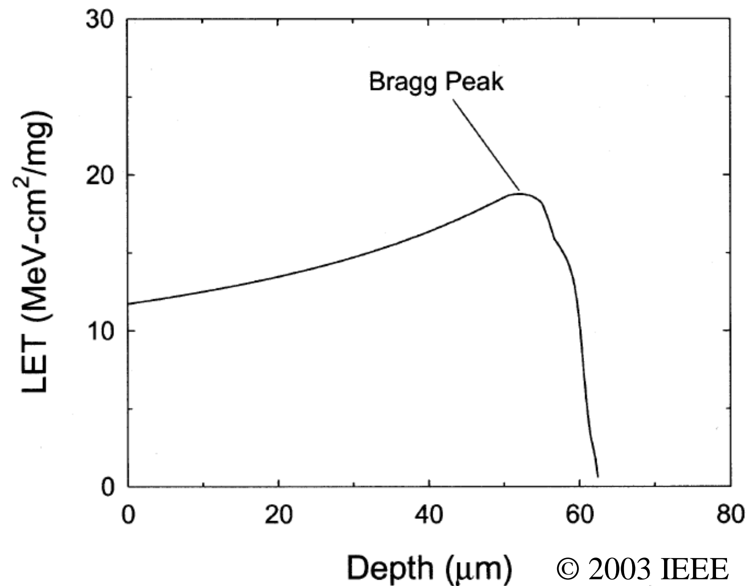

Fig. 1. Linear energy transfer (LET) versus depth curve for 210-MeV chlorine ions in silicon [5]

a particle's LET changes as it burrows deeper and deeper into the semiconductor. Fig. 1, reproduced from [5], shows the relationship between the LET of a 210-MeV chlorine ion as it travels through silicon. Because the total amount of generated charge is the integral of this plot, the prominent Bragg Peak feature is significant. The depths at which single-event charge may be found can also be estimated from the Bragg Peak. Ionization curves similar to that in Fig. 1 can be computed for a variety of heavy ions using the Stopping Range of Ions in Matter (SRIM) codes presented in [6] and available online through [7].

If a particle is unable to create significant perturbation or error in a circuit through direct ionization, it might be able to generate a large amount of charge through indirect ionization [8]. Indirect ionization occurs when the incident particle interacts with the target material to create secondary particles which are directly ionizing [5]. Light, highly energetic particles such as trapped protons [9] can collide with a target nucleus and create a variety of secondary particles ranging from gamma ray photons to nucleus fragments, all of which can generate a significant amount of charge through direct ionization [5]. In circuits containing high-Z materials such as tungsten, indirect ionization from heavy particles such as the ones comprising galactic cosmic rays [9] can contribute a significant number of SETs [10, 11].

Single-Event Charge Collection

Because single-event charge cannot cause a transient unless it is collected, it is important to understand the physics behind charge collection. Integrated circuits collect most transient charge with the electric fields of their reverse-biased PN junctions. This phenomenon was mathematically described in [12] for the case transient photocurrents

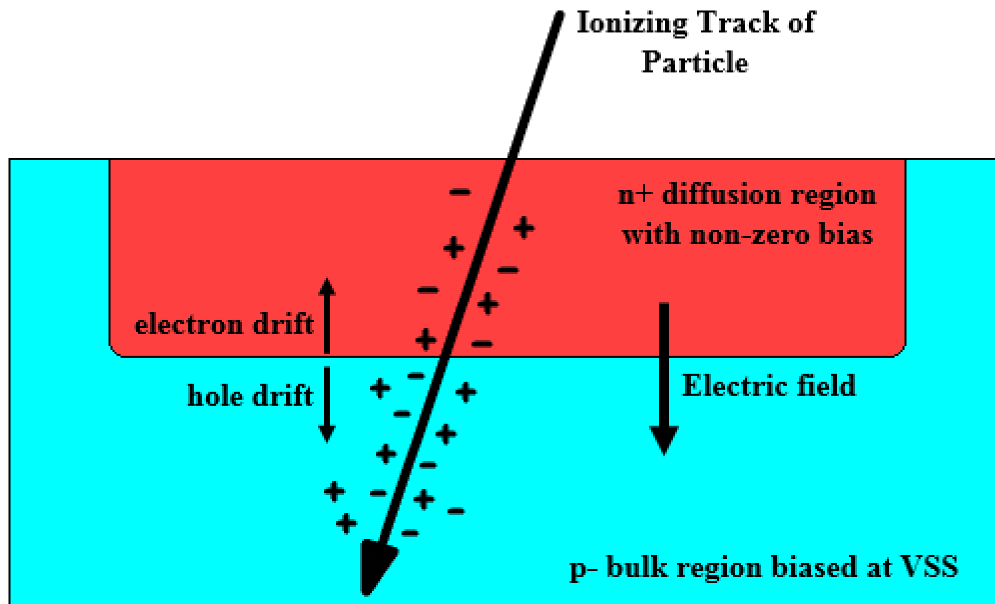

Fig. 2. Single event charge generation and collection in a cross-section of a CMOS diffusion region

resulting from photonic radiation pulses, and later reexamined in [13] for the case of ionic particles that are responsible for single-events.

In Fig. 2, a directly ionizing particle leaves a “charge cloud” of electron-hole pairs along its ionizing track. These freshly generated charges will thermally recombine if they are not collected by the electric field of a PN-junction. If the charge is near a reverse biased PN-junction as shown in the figure, the electrons and holes drift and diffuse across the junction, resulting in a transient current. Electrons are collected by the n+ diffusion and the holes are collected by the p- bulk, resulting in a current pulse that appears to be traveling out of the diffusion region towards VSS. These current pulses can last for a few nanoseconds to hundreds of nanoseconds depending on the strength of the electric field in the PN-junction’s depletion region and the geometry of the junction.

In addition to being heavily locazlied, charge collection resulting from a single-event [13] is fundamentally different from charge collection resulting from transient

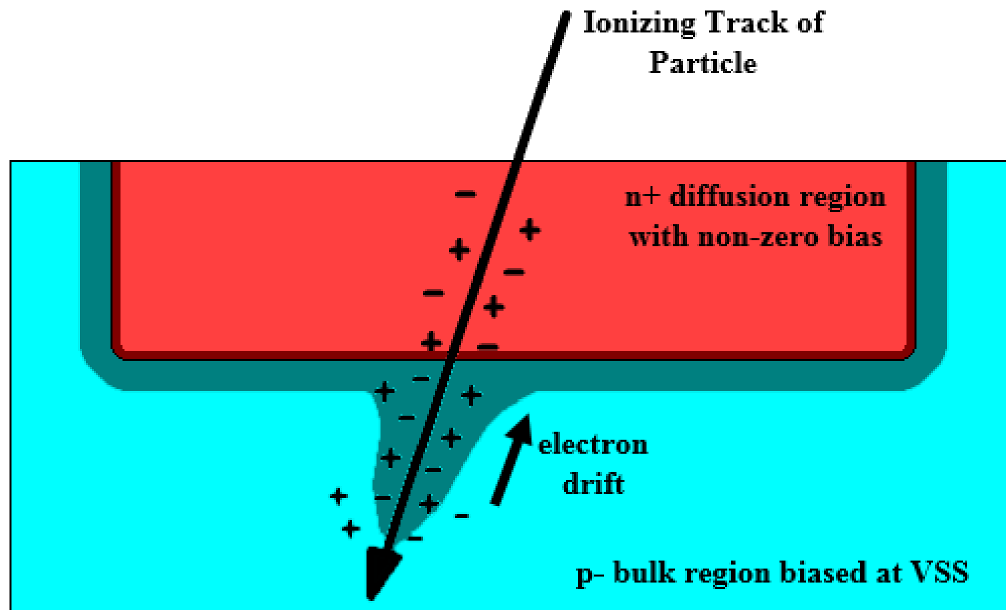

Fig. 3. The shaded equipotential region is malformed due to the single-event, which enhances electron collection

photonic radiation pulses [12]. It was shown in [14] that the electric field of the depletion region can be drastically malformed by the highly conductive ionizing track, resulting in a phenomenon known as field funneling. The funnel-shaped electric field, as depicted in Fig. 3, can collect minority carriers through drift current very efficiently [5]. Because of the important role that electric field strength can have on charge collection, it is necessary for SET models to include circuit bias conditions as well as device geometry.

In bulk CMOS circuits, virtually every source and drain region constitutes a reverse biased PN-junction with the body of every transistor. When a particle strikes these regions, the generated electrons are swept to the n+ region (higher potential), and the holes are swept to the p- region (lower potential). For NMOS devices, the resulting SET current flows from the struck source or drain into the p-type substrate. For PMOS devices, the SET current flows out of the n-well body (typically biased at VDD) to the struck source or drain. Figure 4 shows the polarity of the SET currents resulting from

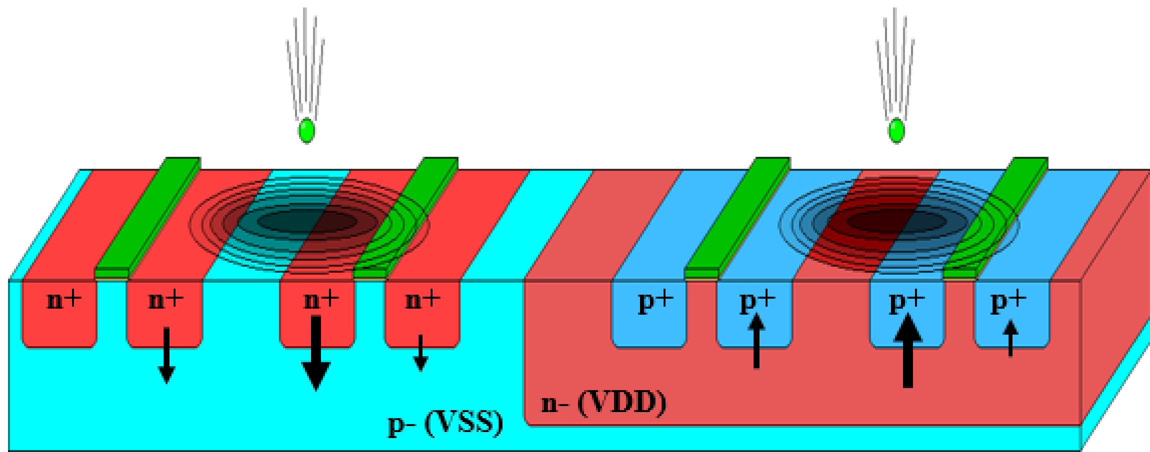

Fig. 4. Single-event transient current polarity and relative magnitude shown as arrows on PN-junctions in proximity of a particle strike

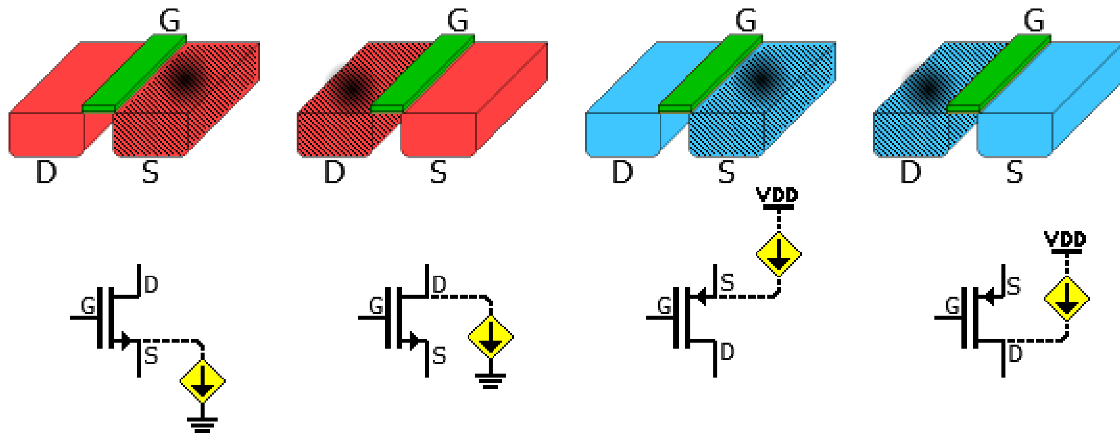

Fig. 5. Correspondence between struck MOSFET region and polarity of single-event transient shown as current source on schematic

particle strikes in proximity to either NMOS or PMOS transistors. Figure 5 tabulates the polarity of the SET currents by representing them as current sources between the terminals of a MOSFET symbol.

Single-Event Transient Models for Circuit Simulation

While an engineer's RHBD efforts are somewhat informed by the physical mechanisms that cause single-event transients, they benefit much more from convenient

and accurate simulation models that foster the innovation of novel RHBD techniques. Tremendous effort from the radiation effects community has been put forth over the past few decades [15] to understand single-event effects so that such models might be developed. Modeling SETs accurately enough to simulate analog RHBD circuits requires a plethora of parameters and experimental calibrations that include but are not limited to: circuit layout, 3D device dimensions, circuit bias, ion species, LET, and the azimuthal and roll angle of the particle strike.

In the modern semiconductor processes relevant to the RHBD techniques discussed in this thesis, it does not suffice to simply calibrate the double-exponential current source presented in [13] and attach an independent current source to a SPICE simulation to represent the total injected charge. In submicron technologies, where circuit response times are on the same time scale as SETs, circuit-level interactions such as bias-dependence become significant [16]. To account for the circuit-SET interactions, a kind of simulation called mixed-mode [17] must be used, where semiconductor physics modeling software is coupled with SPICE simulation. Unfortunately, mixed-mode simulations are computationally expensive compared to conventional SPICE simulations and they are not very portable between semiconductor technologies. The SET current's bias-dependence that necessitates mixed-mode simulations manifests itself as a current plateau [18], as shown in Fig. 6. If this plateau is ignored, as in the double-exponential current source model, then the circuit-level simulations of SETs can become extremely unrealistic.

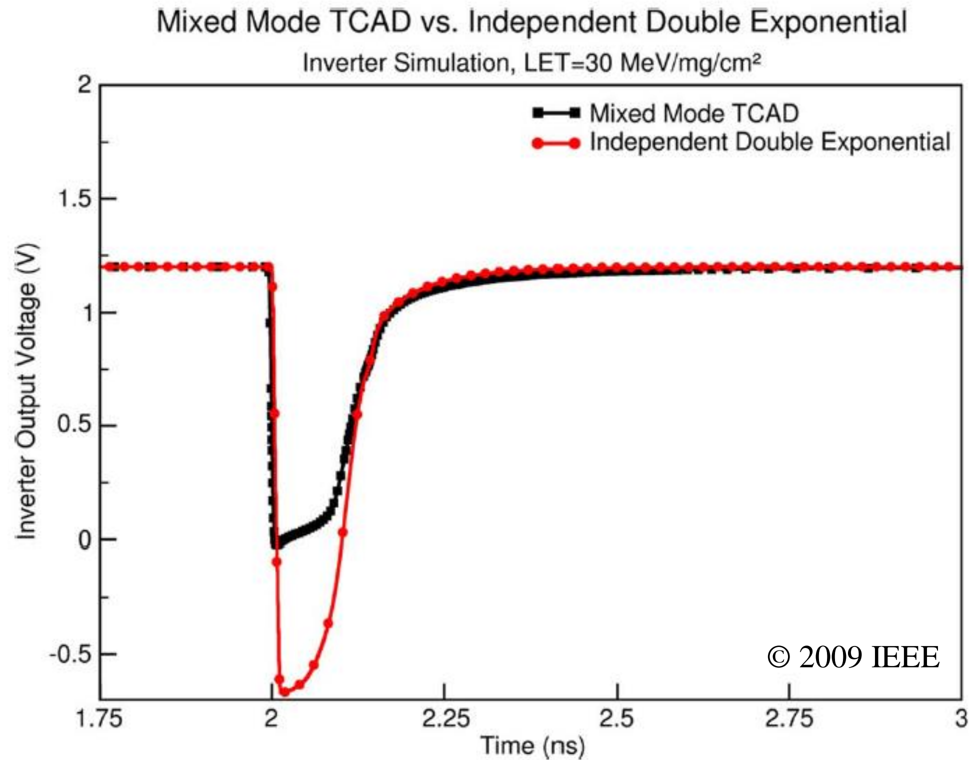

Fig. 6. Current plateau that arises from mixed-mode technology computer-aided design (TCAD) simulations [19]

In [19], it was recognized that the current plateau can also be calibrated from semiconductor physics simulation and used to reshape the double-exponential SET current pulse model. This innovation results in a calibrated SET model that grants the RHBD circuit designer simulation results that are as accurate as mixed-mode simulation but without the computational drawbacks. The simulation model developed in [19] has been integrated into the BSIM4 MOSFET model [20] and was ported to the 180 nm process development kit (PDK) used in this work. The model developed in [19], henceforth referred to as the Vanderbilt University Bias-Dependent SET Model, allows designers to rapidly simulate their RHBD techniques and evaluate their performance at an efficiency and accuracy previously unobtainable.

Single-Event Transient Error Metrics

To evaluate the success of an RHBD technique, it is necessary to define some criteria that shows the impact of SETs. In digital systems, metrics that describe the errors caused by single-event transients are simple to define. This is because every SET that manifests in a digital system either corrupts binary data or it does not. However, in analog and mixed-signal systems, quantifying the system-level impact of SET perturbations is more application-specific. When the SET's impact on a subcircuit within a larger system is being analyzed, the temporal characteristics of the transients that appear on the most important signals of that subcircuit may be described. Three useful quantities that describe the SET are depicted in Fig. 7. Maximum perturbation describes how far the signal is perturbed above or below its correct value. Full-width-half-max (FWHM) pulse width describes the duration of the SET. Integral-square-error (ISE) [21]

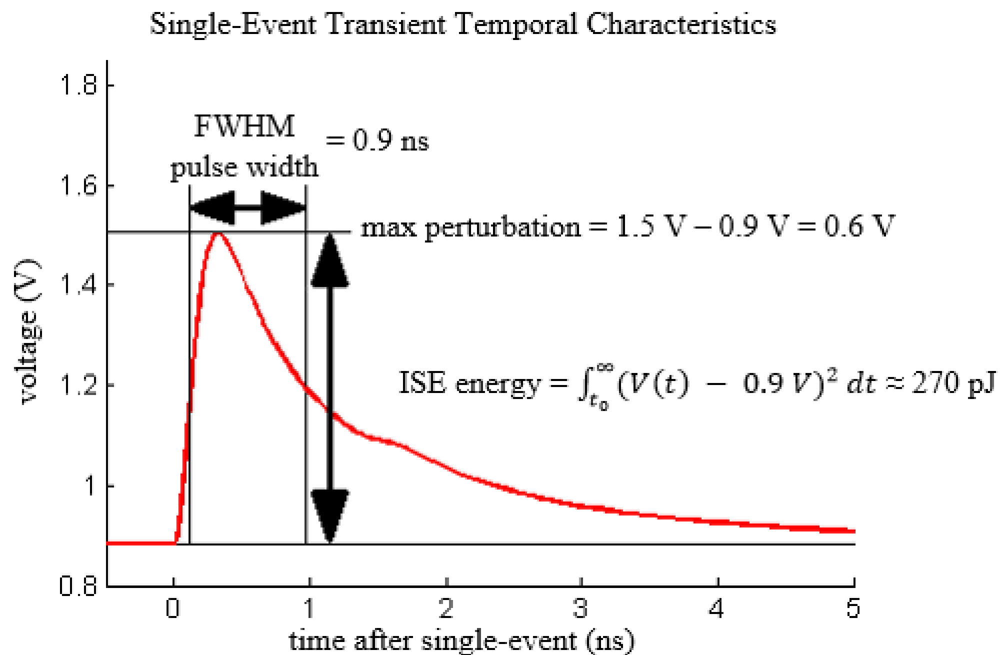

Fig. 7. Single-Event Transient with maximum perturbation, FWHM pulse width, and ISE energy shown

energy describes both the SET's duration and amplitude simultaneously, but in less detail. ISE energy can obtained by using equation 2:

$$\text{ISE Energy} = \int_{t_0}^{\infty} (V(T) - V_{ref})^2 \, dt \qquad (2)$$

ISE energy is useful for system-level analysis in analog systems because the energy of the signal can be treated as a noise contribution which propagates through other system-level elements [21]. With all three metrics, it is necessary to define a nominal quiescent or steady-state value that represents correct circuit operation.

Charge Sharing

Of the several physical mechanisms that determine the true waveforms of SET currents, the phenomenon known as charge sharing plays a central role in the RHBD techniques discussed in this paper. Charge sharing occurs when a particle strikes in the vicinity of multiple bulk devices such that each device collects a portion of the generated charge cloud, resulting in multiple SETs. Charge sharing has been shown through simulation [22] and laser testing [23] to be a concern for submicron bulk technologies due to device dimensions being scaled to the point that they are comparable to the dimensions of single-event ionizing tracks. Charge sharing as a consequence of technology scaling has been understood for some time and has conventionally been a nuisance for digital circuit designers due to it causing multiple bit errors that foil traditional, single-bit error detection and correction schemes [24]. In more recent technologies, digital circuits that are considered very radiation hardened to single-event upsets are vulnerable to multiple-bit upsets caused by charge sharing [25]. Circuit layout techniques have been developed for the sole purpose of reducing the effects of charge sharing on single-event error susceptibility [26].

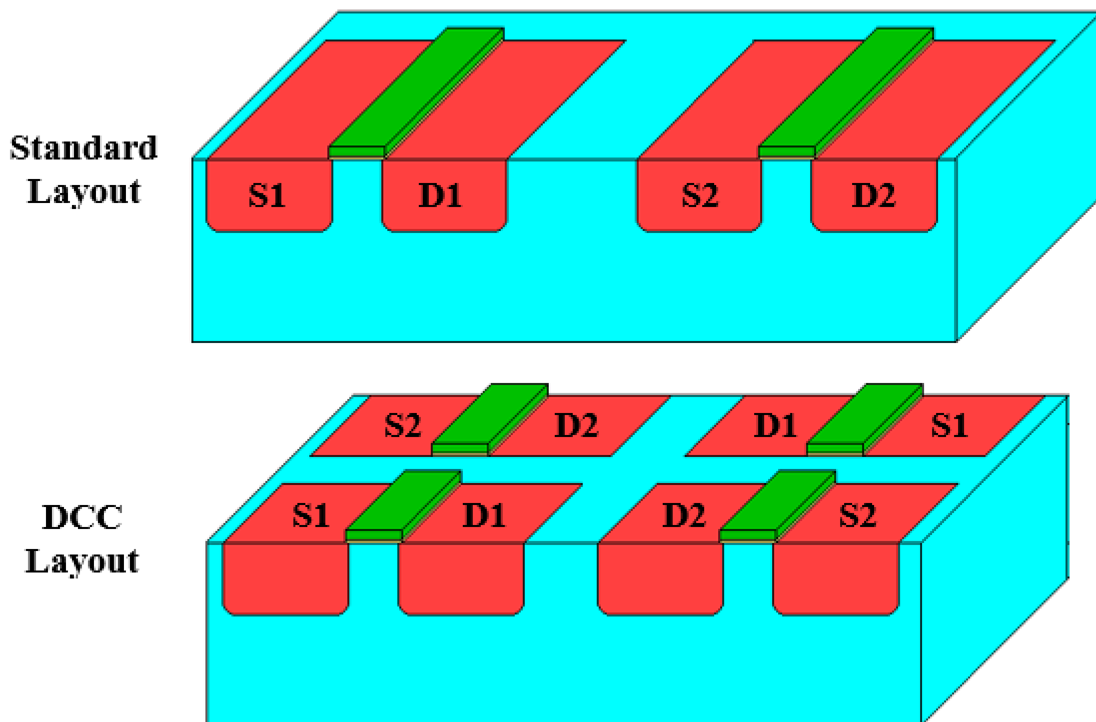

Fig. 8. Standard layout of two transistors versus DCC layout of two transistors. S1 (S2) and D1 (D2) mark the source and drain of transistor 1 (2) respectively.

An excellent example of why RHBD circuit designers should be informed physical mechanisms behind single-event transients is the ironic and surprising exploitation of charge sharing to improve SET tolerance. It was revealed in [27-29] that charge sharing could be used to turn SETs into a common mode signal that is rejected by differential circuitry. A circuit layout technique now referred to as the Differential Charge Cancellation (DCC) layout is used to deliberately enhance charge sharing between two nodes. The DCC layout technique is contrasted against a standard layout in Fig. 8.

The complication of charge sharing, either as a benefit or detriment, has conventionally required technology-computer assisted design (TCAD) and mixed-mode simulation to incorporate into RHBD designs. Fortunately, the Vanderbilt University

Bias-Dependent SET Current Model can be adapted through its calibration parameters to become layout-aware and take factors like strike location and charge sharing into account [30]. This layout-aware adjustment can be performed automatically as in [30, 2], or it can be done approximately with distance-based SET parameter look-up tables using data from sources like in [22].

CHAPTER III

Sensitive Node Active Charge Cancellation

Charge Cancellation Concept

Sensitive Node Active Charge Cancellation is employed to protect important and sensitive circuit nodes by expediting the node's recovery from single-event transients [2-4]. SNACC accomplishes this with additional circuitry which is connected to the sensitive node as shown in Fig. 9. SNACC cancels SET currents by providing its own current pulses. If an NMOS device connected to the sensitive node is struck by a single-event, the SNACC pull-up network delivers a positive current pulse. If a PMOS device connected to the sensitive node is struck, the SNACC pull-down network delivers a negative current pulse. For this scheme to be effective, the delivered current pulses must

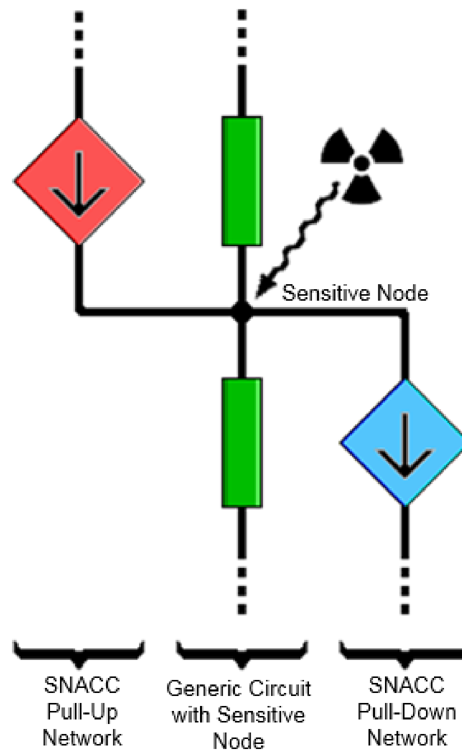

Fig. 9. SNACC concept. The sensitive node is protected by a pull-up network and a pull-down network to cancel single-event charge collected by NMOS and PMOS devices respectively

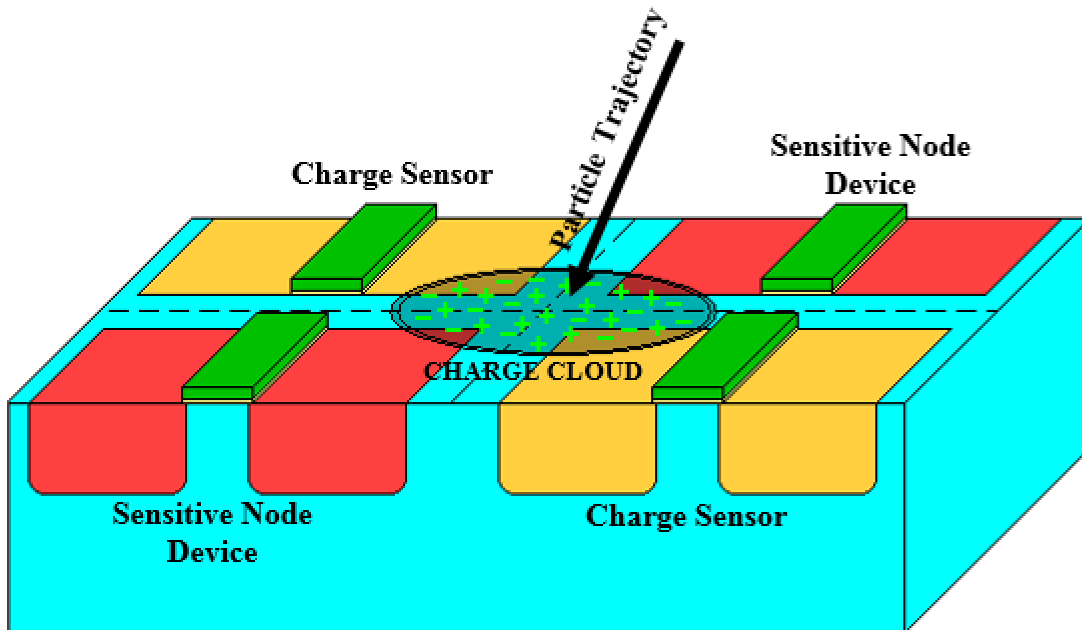

Fig. 10. Charge sensing performed with the DCC layout technique. Charge collected by the sensitive node device contributes to ISET1 while collection towards the charge sensors contributes to ISET2

carry a total amount of charge similar to that collected by the struck device. The current pulses must also be delivered at approximately the same time as the SET.

SNACC Charge Sensing

To produce current pulses that accurately cancel SETs, SNACC uses specially located charge sensors. These charge sensors consist of NMOS or PMOS transistors that are patterned with the sensitive node devices in the DCC layout [27-29], as shown in Fig. 10. The DCC layout is used to ensure that with each SET that hits the sensitive node, a second SET occurs on an alternate signal path. From here onwards, the SET current that manifests on the sensitive node will be referred to as I_{SET1} and the SET current that manifests on the SNACC signal path will be referred to as I_{SET2}. With both I_{SET1} and I_{SET2}

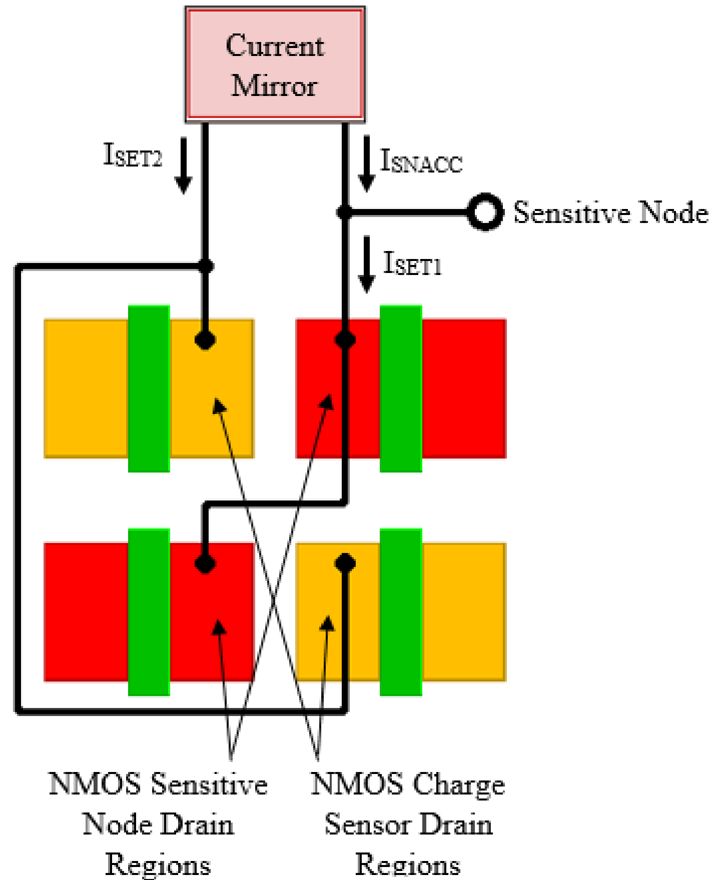

Fig. 11. SNACC charge sharing and SET mirroring concept

created at the occurrence of a single-event, it is possible to mirror or fold the current I_{SET2} back onto the sensitive node as I_{SNACC}. This concept is shown in Fig. 11. If the current waveform I_{SNACC} closely matches I_{SET1}, the SET on the sensitive node will be mitigated very effectively. The SNACC concept can be summarily understood as canceling an SET on a sensitive node with another SET.

Unfortunately, I_{SNACC} cannot perfectly match I_{SET1}, due to the inevitable imbalance of charge collection between the sensitive node transistor and the charge sensor. Additionally, there is a small propagation delay through the current mirror which guarantees I_{SNACC} will always lag behind I_{SET1} by a few picoseconds. However, as technologies scale to the point that transistor dimensions become small compared to

ionizing track charge clouds, the charge distribution between I_{SET1} and I_{SET2} will become more even and the propagation delay through the current mirror will shorten. This indicates that SNACC's charge sensing scheme will become more effective as bulk CMOS circuits continue to scale.

Implementation of SNACC on a Sensitive Bias Circuit

Fig. 12 shows a simple bias circuit consisting of the cascoded transistors M1-4. The voltage V_{BIAS} is referenced by many other subcircuits within a folded cascode op amp first introduced in [31]. Ionizing particles landing near transistors M1-4 will likely cause transients that propagate throughout the entire analog system. Because of the

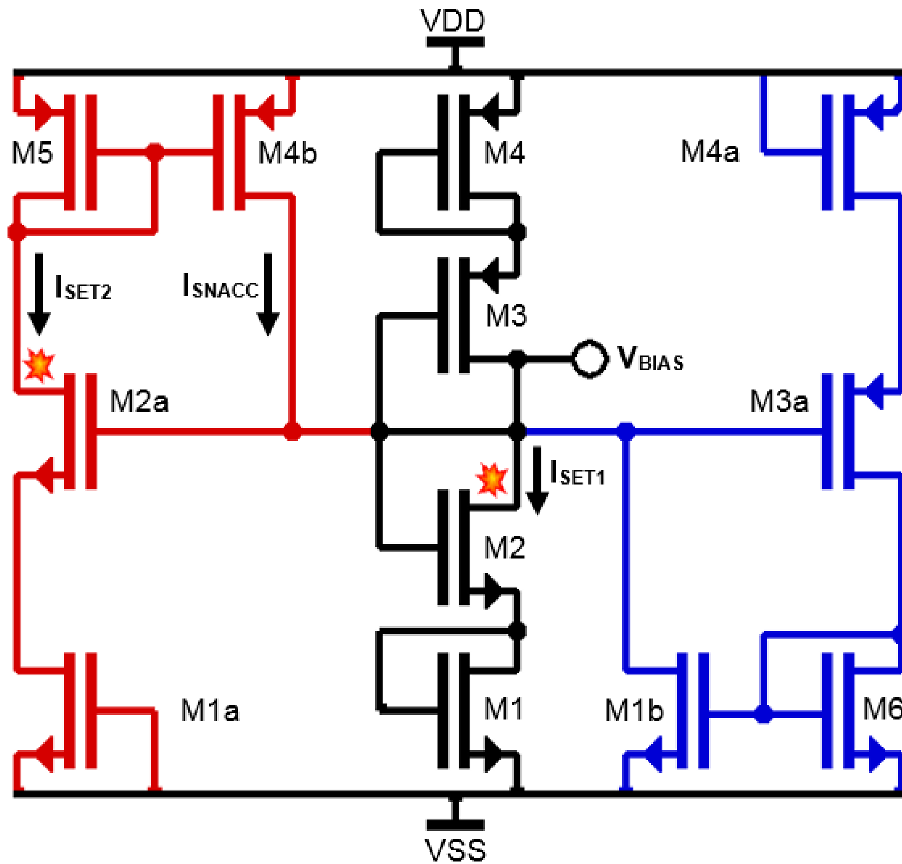

Fig. 12. Bias Circuit M1–4 protected by the SNACC pull-up network (red) and pull-down network (blue).

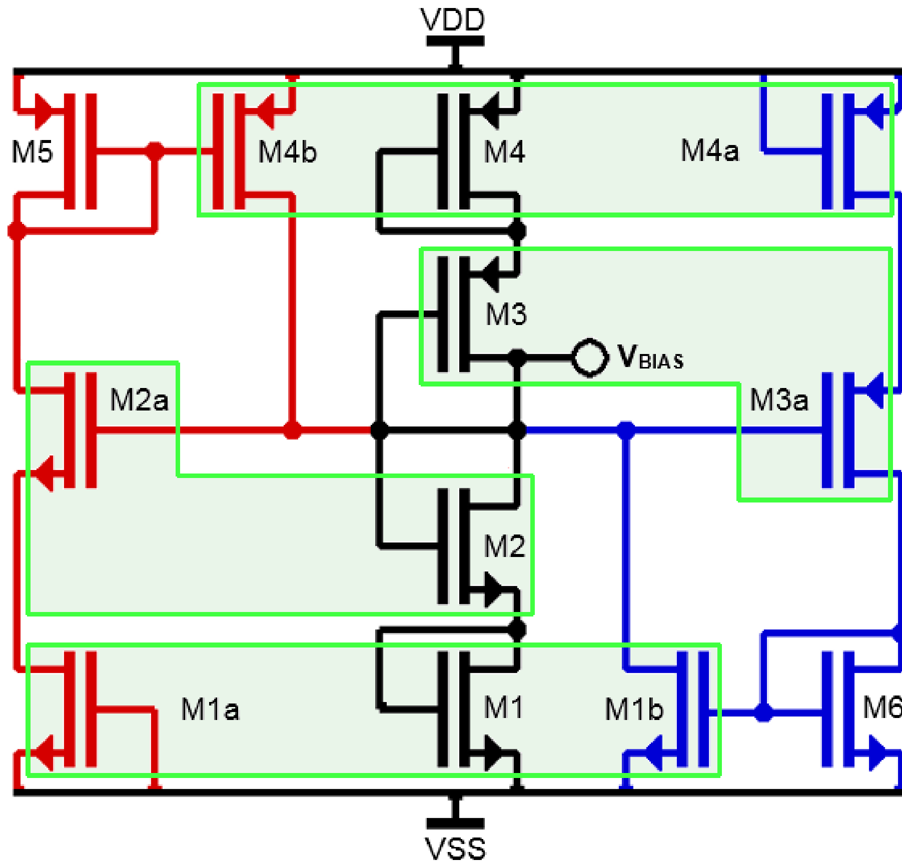

Fig. 13. Bias circuit protected by SNACC. Devices that share charge are grouped in green regions.

system-wide errors that may occur if V_{BIAS} is perturbed, the node connecting the drains of M2 and M3 can be recognized as a sensitive node, justifying the additional circuitry required to apply SNACC to it.

The SNACC transistors M1a, M2a, M4b, and M5 form the “pull-up network” which detects and compensates for particle strikes on n-channel devices connected to the sensitive node. In a symmetrical fashion, M1b, M4a, M3a, and M6 form the “pull-down network” which protects p-channel devices connected to the sensitive node. In the pull-up network, the charge sensing device M1a collects charge from particle strikes near M1 and M1b, while M2a detects particle strikes near M2. If M2 is struck for example, the SET

currents I_{SET1} and I_{SET2} will manifest simultaneously as shown in the figure. The current mirror made of M5 and M4b will reflect I_{SET2} onto the sensitive node as I_{SNACC} to cancel I_{SET1}. A similar scenario with the pull-down network will occur if M3 and M3a collect charge from a particle strike. The variant of SNACC shown in Fig. 12, named Multi-SNACC (M-SNACC) by the author of [2], not only compensates for single-event transients on the sensitive node carrying V_{BIAS}, but also for SETs on the drains of M1 and M4, whose voltages are also sensitive in the same way as V_{BIAS}, but to a lesser degree.

The charge sharing arrangement in Fig. 13 summarizes the layout of the schematic in Fig 12. Devices share charge to ensure that all conceivable SETs which could threaten the sensitive node voltage will be compensated. The only diffusion regions that don't require compensation are the drains of M5 and M6, because SETs originating in these regions cannot propagate to the sensitive node.

SNACC SET Mitigation Performance

The author of [2] simulated the circuit of Fig. 12 within a folded cascode op amp [31] in a voltage follower configuration. The simulations were performed with a 180 nm bulk CMOS process design kit in conjunction with the layout-aware single-event simulation techniques developed in [30]. For the op amp hardened with M-SNACC, it was shown that the ISE energy of SETs that propagate to the op amp's output from its bias circuit were reduced by approximately a factor of 5 versus the unhardened op amp [2]. The interested reader may inspect the simulation methodology section of [2] for more details on how this simulation was performed.

Cost of M-SNACC Implementation

Compared to brute force hardening, SNACC has relatively low chip area penalty, and virtually no power penalty. The biggest drawback with SNACC hardening is the resulting increase in sensitive area. In the case of the Multi-SNACC implementation shown in Fig. 12, every transistor except M5 and M6 contributes to sensitive area. While most ionizing particles will create smaller voltage perturbations on the SNACC-hardened circuit than on the unhardened bias circuit, the hardened circuit is approximately 2.5X more likely to be struck by a particle in the first place. Depending on the application of the bias circuit, or any SNACC-hardened circuit, this increase in sensitive area might reduce the radiation hardness that SNACC can afford the circuit designer.

CHAPTER IV

Conceptual Overview of Enhanced SNACC

Improving the Sensitive Area Penalty of SNACC

To reduce SNACC's sensitive area penalty identified in the previous chapter, a pragmatic modification to the SNACC concept is necessary. To understand what changes are necessary, consider the SNACC concept again in Fig. 14, with the charge sensors in the DCC layout explicitly shown. When the current I_{SET1} is approximately equal to I_{SET2}, excellent SET mitigation occurs. However, when I_{SET2} is much larger than I_{SET1}, the SNACC circuitry overcompensates I_{SET1} at best, and at worst introduces an SET to the

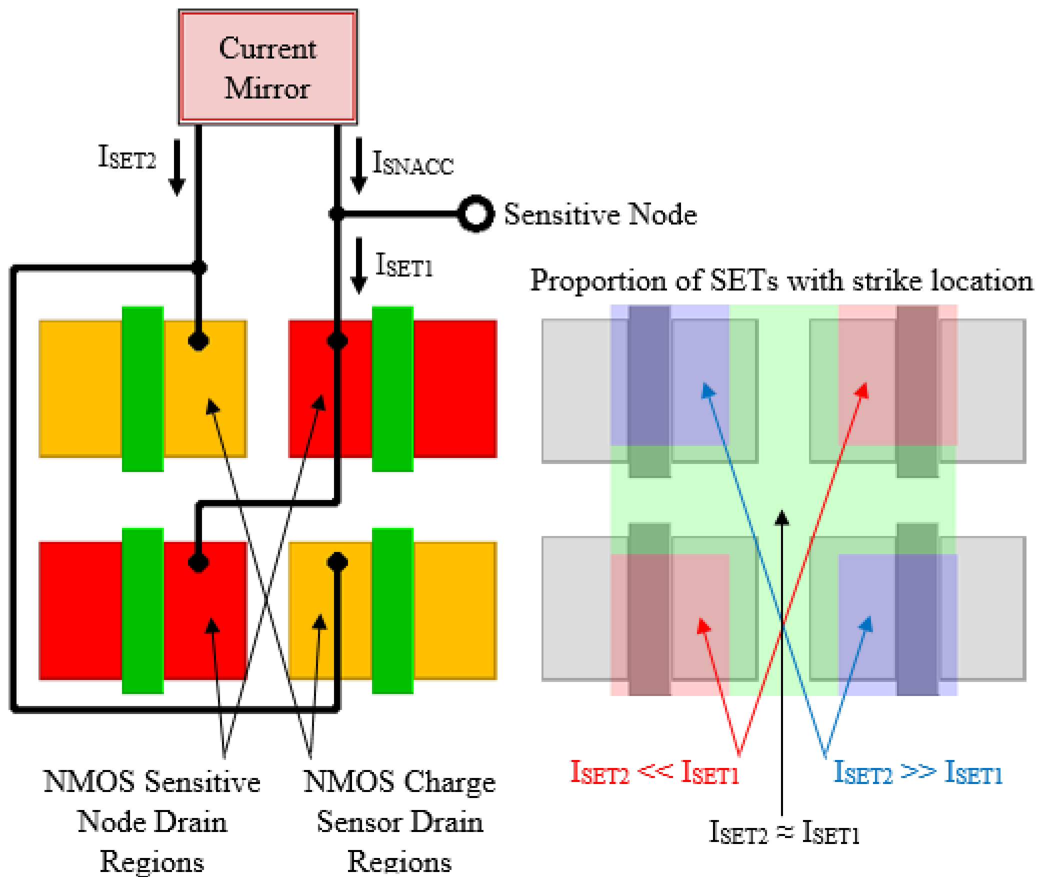

Fig. 14. Sensitive area contribution from SNACC charge sensors due to I_{SNACC} overcompensating I_{SET1}

sensitive node when there would not have been one in an unhardened circuit. The proportion of I_{SET2} to I_{SET1} depends on the location of the particle strike, as shown in the right side of Fig. 14. From this perspective, it becomes apparent that if there were a way of preventing the SNACC circuitry from overcompensating, all of the sensitive area contributed by the charge sensors would vanish.

Rather than attempting to match I_{SNACC} with I_{SET1}, suppose the designer deliberately imbalanced I_{SNACC} to provide the fastest charge cancellation possible, while relying on the charge sensors to initiate compensation and voltage feedback to halt compensation. This is the foundation of the Enhanced SNACC (ESNACC) concept which will be elaborated upon in this chapter. After discussing the overall structure and ideal operation of ESNACC, each ESNACC subcircuit will be shown in greater detail in chapter V, followed by simulations performed with the Vanderbilt University Bias-Dependent SET Model in chapter VI.

Enhanced SNACC Structure

The schematic shown in Fig. 15 organizes the ESNACC pull-up network (red) and pull-down network (blue) into four logical groups: the voltage feedback control, the current driver, the charge sensor array, and the gating transistor (M5 or M6). The voltage feedback control circuit monitors the sensitive node voltage, and turns on the gating transistor only if V_{BIAS} strays from its nominal value by a fixed threshold. If any active regions in the charge sensing array collect enough charge, the corresponding current driver will activate and rapidly pull V_{BIAS} back towards its correct value. After V_{BIAS} is within a few millivolts of recovering, the control circuit begins turning off the gating transistor to prevent overcompensation.

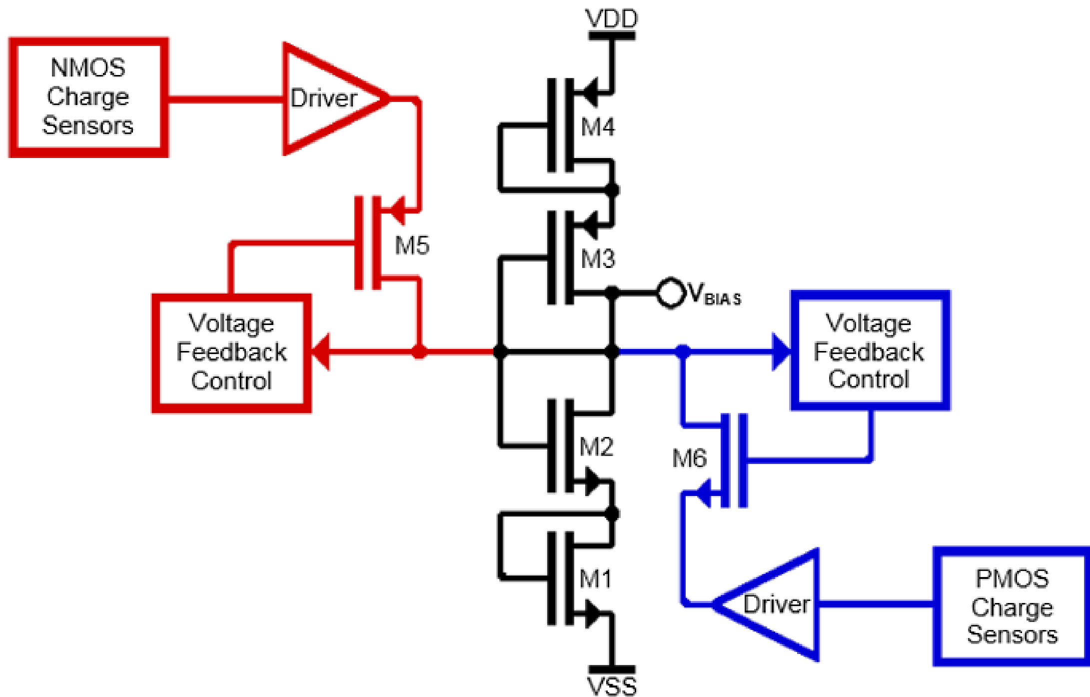

Fig. 15. Enhanced SNACC block diagram applied to bias circuit consisting of transistors M1-4

Ideal Single-Event Transient Response of ESNACC

Fig. 16 shows the bias circuit's ideal response to a direct hit on the drain of M2, with and without ESNACC. At point A, the voltage feedback control circuit detects the perturbation and turns on M5 to deliver the compensation current I_{ESNACC}. At point B, the current driver begins to eliminate the collected charge, marked by the steep voltage slope. At point C, the voltage feedback control circuit switches modes and turns off M5. By point D, the compensation current has completely shut off, and the sensitive node voltage has settled.

Advantages of ESNACC Technique

Before considering quantitative results, ESNACC already has a number of conceptual advantages over SNACC. First, ESNACC only contributes two transistors to

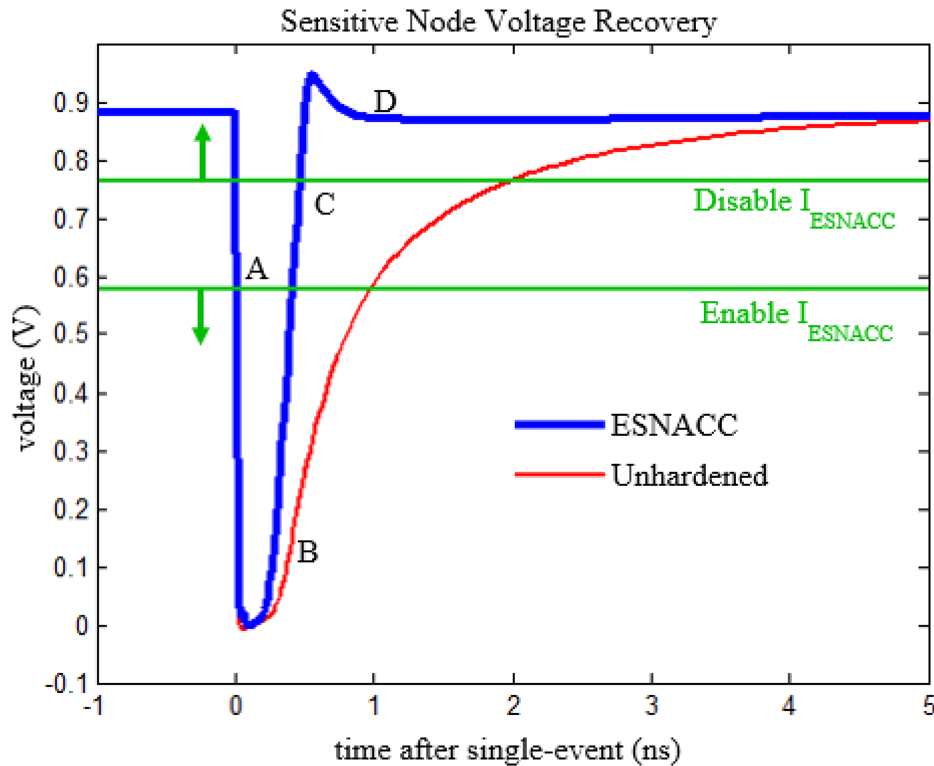

Fig. 16. Ideal sensitive node response to particle strike on the drain of M2.

the sensitive area of the bias circuit. With appropriate layout, any SET which perturbs the control circuit will not propagate to the sensitive node, and any SET originating in the current driver will by logically masked by the gating transistor. The only way for either the pull-up or pull-down network to affect the sensitive node is for a charge sensor to collect charge while the sensitive node is in need of charge cancellation.

A second advantage is that the compensation current is not a function of the charge collected by the charge sensors. Once a small amount of charge has been collected by the charge sensors, the current driver turns on and provides as much current as the gating transistor can deliver. Since it is not necessary to balance I_{SET2} and I_{ESNACC}, there is no need to match ESNACC devices with the sensitive circuit devices, the DCC layout

technique is no longer required, allowing ESNACC to be integrated into any design more conveniently than the original SNACC.

CHAPTER V

ESNACC Subcircuits

In the following section, each component in ESNACC's pull-up network will be exhibited in greater detail. The pull-down network's operation is symmetrical to that of the pull-up network and is omitted for brevity.

NMOS Charge Sensor Array

An array of charge sensing devices are implemented as several transistors that are biased in cutoff, as shown in Fig. 17. These devices are placed in close proximity to M1, M2, and M6, such that they share charge generated from single events. The drains of these devices carry the signal V_{SENSE}, which activates the current driver once it has fallen below a switching level. At steady state, the weak pull-up transistor returns V_{SENSE} to one threshold voltage below VDD. Lowering the steady-state value of V_{SENSE} by stacking

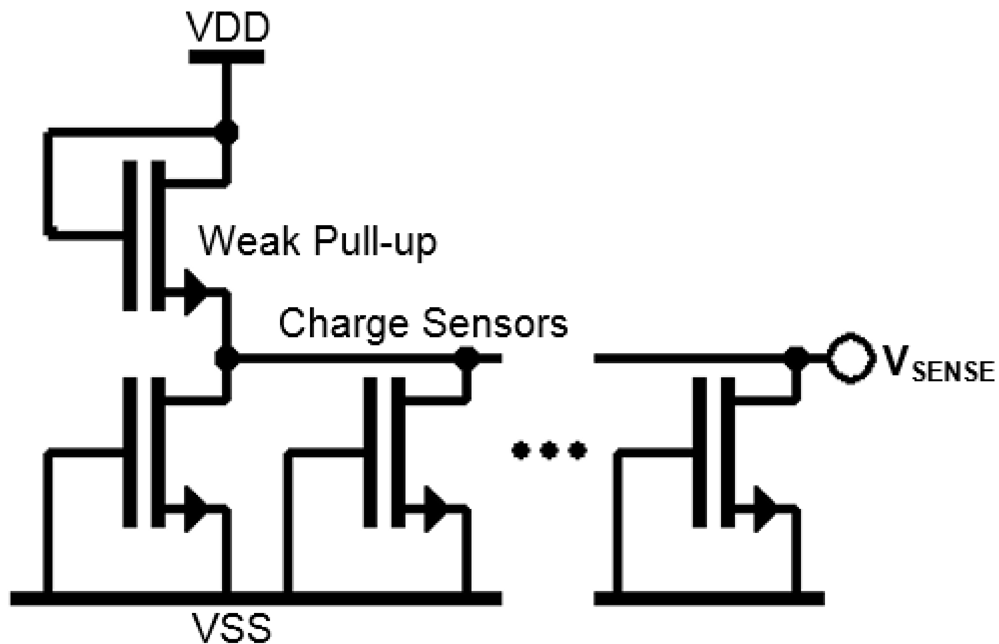

Fig. 17. NMOS Charge Sensor Array Topology

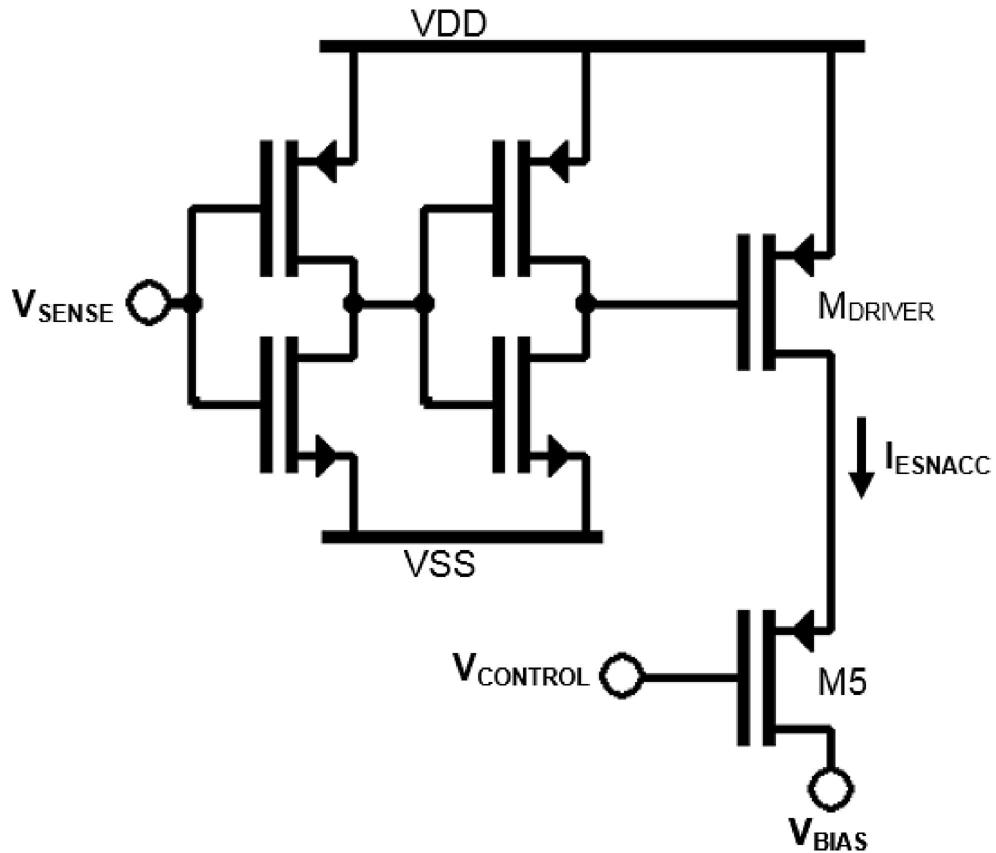

Fig. 18. Current driver topology with gating transistor M5

multiple pull-up transistors will reduce the amount of charge necessary to upset the V_{SENSE} node, but can also reduce charge sensor's ability to attract charge from nearby single-events.

Current Driver and Gating Transistor

The current driver and gating transistor M5 are shown together in Fig. 18. Unlike the current mirror used in SNACC, which folds the transient current originating on its charge sensing devices, this current driver consistently delivers the saturation current of M_{DRIVER}, as soon as the V_{SENSE} node upsets. The speed of ESNACC's compensation can be adjusted through the aspect ratio of the gating transistor and M_{DRIVER}.

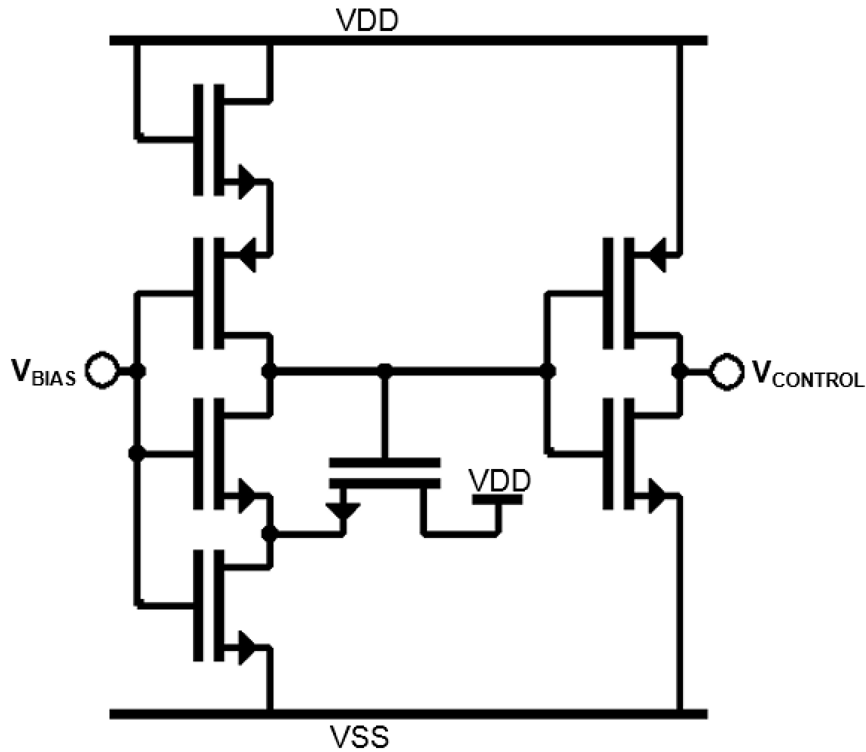

Fig. 19. Current driver topology with gating transistor M5

Voltage Feedback Control

The voltage feedback controller is the most difficult ESNACC subcircuit to design, as it controls the gating transistor which prevents the current driver from overcompensating the sensitive node. Different feedback controller designs and switching thresholds are necessary, depending on the nominal quiescent voltage and expected signal swing of the sensitive node. In the case of ESNACC being applied to this particular bias circuit, a “half Schmitt trigger” may be used, as shown in Fig. 19. This topology is based off of the 6-transistor Schmitt trigger developed in [32], but with only one abrupt switching point instead of two.

CHAPTER VI

ESNACC Simulation Results

To demonstrate the efficacy of the Enhanced SNACC technique, single-event transient simulations of the bias circuit protected by ESNACC were performed. By viewing the transient response of the bias circuit's output to particle strikes at various locations near its charge sensors, it is possible to see if the concept presented in chapter IV was implemented successfully.

Simulation Setup

The simulations were performed using Cadence Spectre in a 180 nm bulk CMOS process development kit. The Vanderbilt University Bias-Dependent SET Model developed in [19] was used, while using one-dimensional charge collection parameters from [18] to take strike location into account at various distances between the sensitive drain of M2 and the nearest charge sensor. Single-event model parameters for a direct-incidence particle strike with LET of 30 MeV * cm^2 / mg were used.

Simulation Results

Single-event transient simulations of particles with a linear energy transfer (LET) of 30 MeV • cm2 / mg, direct incidence, and various distances from the ESNACC-protected drain of M2 are shown in Figure 20. In all cases, it is possible to see the moment when the current driver activates, marked by a sudden increase in the recovery slope. Once the voltages are within a few millivolts of the nominal value of V_{BIAS}, the

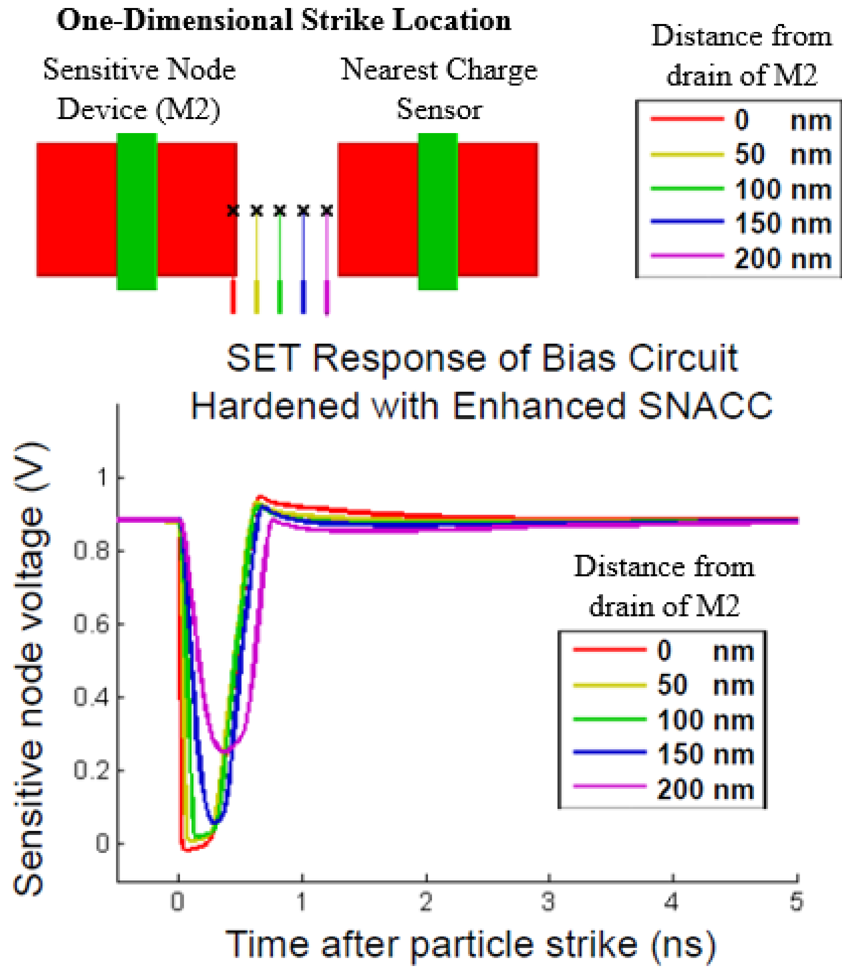

Fig. 20. Single-event transient simulations of ESNACC-hardened bias circuit at various strike locations between M2 and M2a

voltage feedback controller turns off the gating transistor, the compensation current stops, and any remaining charge from the single-event is gradually eliminated by the inherent current drive of the bias circuit.

The transient responses shown in Fig. 21 were simulated in an identical situation to those in Fig. 20, but with the ESNACC pull-up network disconnected from the bias circuit. By comparing the responses between the two figures, it is readily seen that ESNACC greatly reduces the pulse width of the SETs seen on the bias circuit output. In

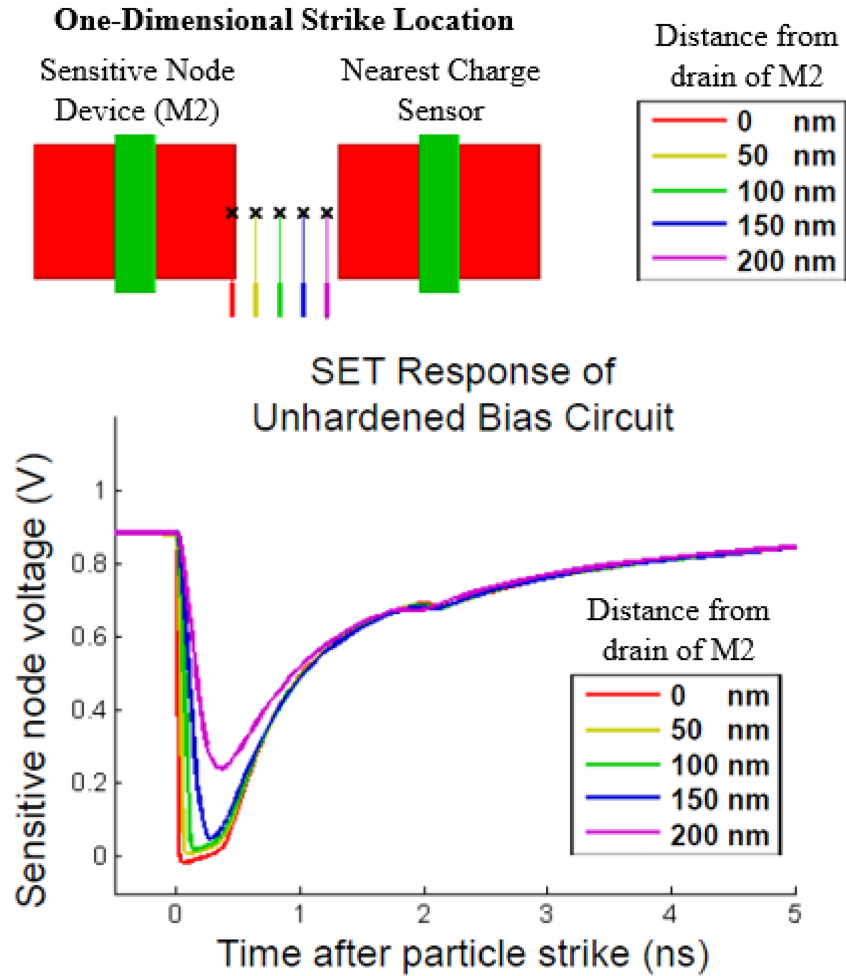

Fig. 21. Single-event transient simulations of unhardened bias circuit at various strike locations between M2 and M2a

Fig. 22, a plot of the ISE energies for the two circuits at all tested strike locations is shown. At the output of the bias circuit, the ISE energy is reduced approximately by a factor of 2. Because errors in the sensitive node voltage are amplified by the time they propagate to the output of the op amp, this simple reduction can be quite significant.

Interpreting Simulation Results as Proof of ESNACC Concept

It can be seen from the plots in Fig. 20 and 21 that the SETs become weaker as the particle strike distances from M2 increases. Direct strikes to the charge sensor

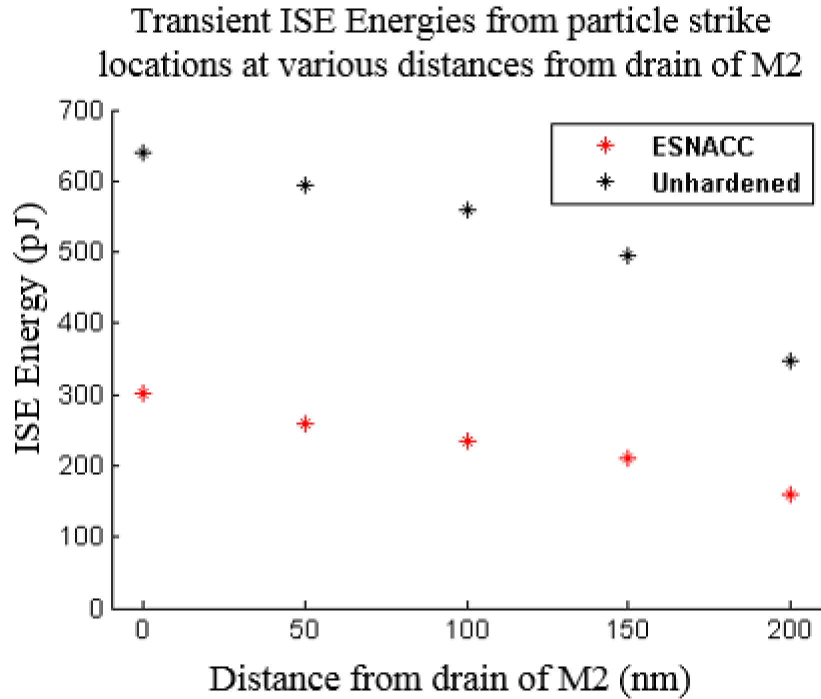

Fig. 22. Integral-square-error energies resulting from particle strikes on both the unhardened bias circuit and the ESNACC-hardened bias circuit

produce a negligible transient due to their relatively large distance from M2. This is an improvement over the SNACC implementation, in which a direct strike to M2a where would produce an inverted SET as severe as a direct strike to M2. It can be concluded that the ESNACC charge sensors do not contribute sensitive area like the ones in the original SNACC do.

CHAPTER VII

Conclusion and Future Work

Great insight gained through decades of work by the radiation effects community has been used to develop radiation hardening schemes such as SNACC. In this thesis, the steps that lead to SNACC's prerequisite radiation models and mechanisms have been retraced and used to explain SNACC's operation. Beyond this, critical analysis has been combined with RHBD insight to identify the cause of SNACC's sensitive area drawback and formulate a solution. It was recognized that SNACC's charge sensors perturb the protected sensitive node if they are struck directly by single-events. Enhanced SNACC, the RHBD technique proposed in this work, uses analog and mixed-signal circuits to implement a voltage feedback system that masks SETs originating in the hardening circuitry. This new scheme ensures that the area contributed by the charge sensors and any other ESNACC circuitry is not sensitive. For a small area and power penalty and some model-assisted design effort, sensitive nodes can be protected with ESNACC in the same fashion as SNACC but without any significant increases in sensitive area.

In the near future, ESNACC will be modified for implementation in more advanced technology nodes to capitalize upon its inherent dependence on charge sharing and transistor switching speed. To this end, further refinement of the voltage feedback controller design used in ESNACC will be performed with a focus on portability and process invariance. As research in such advanced technology nodes gathers interest, opportunities to fabricate ESNACC test circuits will arise. Once proven with physical

data, ESNACC will soon join the global RHBD community's growing repertoire of techniques.

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