Capacitance-frequency Estimates of Border-trap Densities in Multi-fin MOS Capacitors

By

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ABSTRACT

This thesis focuses on radiation effects of multi-fin MOS capacitors with high-K dielectrics built in Ge and InGaAs FinFET technologies. Capacitance-frequency (*C-f*) measurements are applied to provide lower-bound estimates of border-trap densities in these devices before and after X-ray irradiation. The method is illustrated for SiO_2-based planar MOS capacitors, and compared with high-frequency capacitance-voltage (*C-V*) measurements. Lower border-trap densities are found before and after irradiation for multi-fin capacitors built in a strained Ge *p*MOS FinFET technology than for similar devices built using an early-developmental stage InGaAs MOS technology. These results show the utility of *C-f* measurements in characterizing defect densities in MOS capacitors, particularly when large border-trap densities exist.

CHAPTER I

INTRODUCTION

Transistors and capacitors are commonly used to evaluate the basic mechanisms of radiation effects on MOS structures [1]-[3]. For FinFETs and other highly-scaled multi-gate technologies, characterization to date has focused primarily on the properties of transistor test structures [4]-[11]. Modern FinFET technologies increasingly incorporate alternative channel materials to Si, with the most maturity in development for SiGe and Ge for *p*MOS applications [8],[10]-[12]; these typically include high-K gate stacks [10]-[14]. High-K gate dielectrics often show higher defect densities than thermal SiO_2 gate dielectrics of comparable thickness [3],[15],[16]. Capacitive methods are commonly applied to evaluate charge trapping effects in high-K dielectrics; these are especially useful when attempting to distinguish effects of interface and border traps in advanced dielectrics [17]-[20].

In this chapter, several key words related to the research are introduced, including an overall introduction of radiation effects especially for total ionizing dose (TID) effects, background information about why high-K dielectrics have a great potential in the development of semiconductor electronic devices, and advantages of using Ge/III-V channels and FinFET structures as substitute for planar Si MOS. Finally, an overview is given to conclude the highlight of methods and results in this thesis.

1. Radiation Effects Overview

1.1 Background

The huge development of semiconductor technology has a tremendous influence on applications of microelectronic industry [21]. Therefore, high-tech products consisting of microelectronic chips are broadly applied in lots of fields in our daily life such as medical devices, aviation and spacecraft. Besides, this group pushes the national defense industry especially in nuclear power plant control systems and subspace missile systems. However, the appearance of ionizing radiation that results from cosmic environment, nuclear weapons and reactors, or isotopes in chip packaging materials affects the original stable function of semiconductor electronic devices and circuits [22].

Thus, study of the radiation effects is highly required for the improvement of related microelectronic applications [23]. Motivated by this, this research was focused on the study of radiation effects.

1.2 Total Ionizing Dose Effects

Various types of radiation in space, such as electrons and protons, result in total ionizing dose, displacement damage and single event effects to microelectronic components. Among these three different radiation effects, total ionizing dose induces significant charge buildup in oxides and insulators, which determines the long-term reliability of MOS devices in space [3].

Therefore, this thesis focuses on the total ionizing dose (TID) effects. The mechanism of total ionizing dose is shown in Fig. 1.1 below.

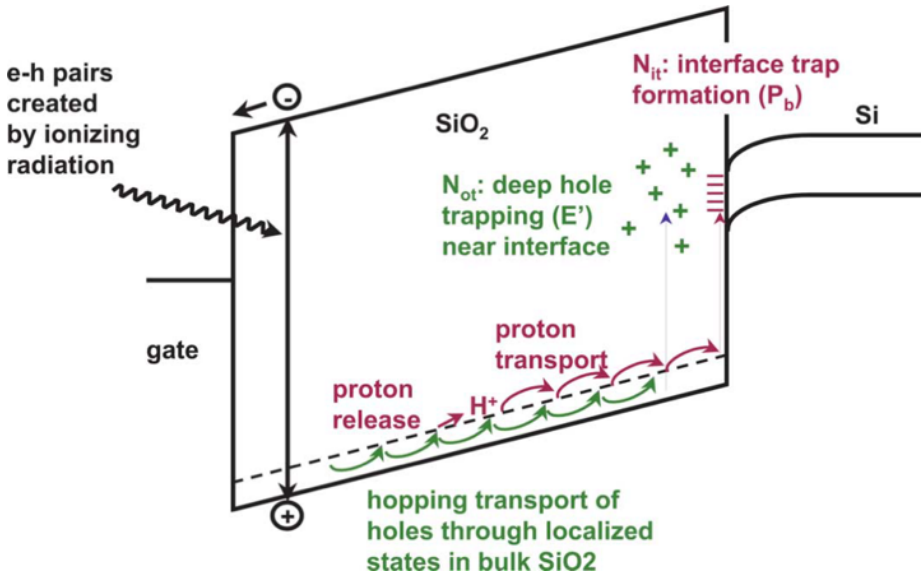


Fig. 1.1. Schematic diagram illustrating physical processes for radiation-induced charge generation in MOS capacitor [3].

The main processes for radiation-induced charge generation can be explained based on the band diagram above. Under the influence of ionizing radiation, electron-hole pairs are first generated in the oxide. Then immediately, most of electrons will rapidly drift to the gate due to high mobility. Holes, on the other hand, move slower than electrons, so they are trapped in micro-structural defects and pre-existing traps. Before electrons leave the oxide, some of them will recombine with holes [3].

For those electron-hole pairs who escape initial recombination, holes will further transport toward the Si/SiO_2 interface by hopping through localized states in the oxide [24]. This process

typically takes less than a second, but may also take place over many decades [25]. As approaching to the Si/SiO_2 interface, some of the holes are trapped, forming a positive oxide-trap charge. Meanwhile, hydrogen ions (protons) are released and drift to the interface, forming an interface-trap charge. Between oxide- and interface-traps, the near-interfacial oxide traps that communicate with the Si are called "border traps". It is difficult to draw a firm distinction between border traps and oxide traps. One useful rule is that for defect sites within about 3 nm of the Si/SiO_2, or the gate/SiO_2, interface can be considered as border traps [26]. Switching times between ~ 10^{-6} s and ~ 10^{-3} s are defined as fast traps and slow traps are those switching times greater than ~ 10^{-3} s [19].

For total ionizing dose effects on MOS devices, the threshold-voltage shift ΔV_{th} caused by radiation is mainly investigated. The voltage shift resultes from both oxide-trap charge ΔV_{ot} and interface-trap charge ΔV_{it}. As introduced above, oxide-trap charge is a positive charge, which causes negative threshold-voltage shift in both n- and p-channel MOS transistors. Interface traps are positive in p-channel MOSFETs causing negative threshold-voltage shift, and negative in n-channel MOSFETs causing positive threshold-voltage shift. Therefore, oxide-trap charge and interface-trap charge compensate with each other for n-channel MOSFETs and add together for p-channel MOSFETs.

2. Device Characteristics

The state-of-the-art devices we investigated in this thesis included several research interests: high-K gate dielectrics, Ge and III-V channel material, and FinFET structure. Technology innovations are needed in transistor scaling to extend Moore's law. Several transformative changes have been implemented and explored since 2005 to maintain the scaling, as shown in Fig. 1.2 [27].

In 2007, high-K gate stacks were investigated to reduce gate leakage and improve gate performance. Channel material such as Ge and III-V were explored as a substitute for Si in 2011 due to their high carrier mobility. At the same time, a dramatic change was invented in the design of modern processors. Several different 3d structures work as a substitute for the original planar structure. The most significant 3d structure is FinFET (also known as Fin Field Effect Transistor), and it has the advantages of reduced short-channel effects, reduced leakage current, improved gate control and better device performance compared with planar devices [11].

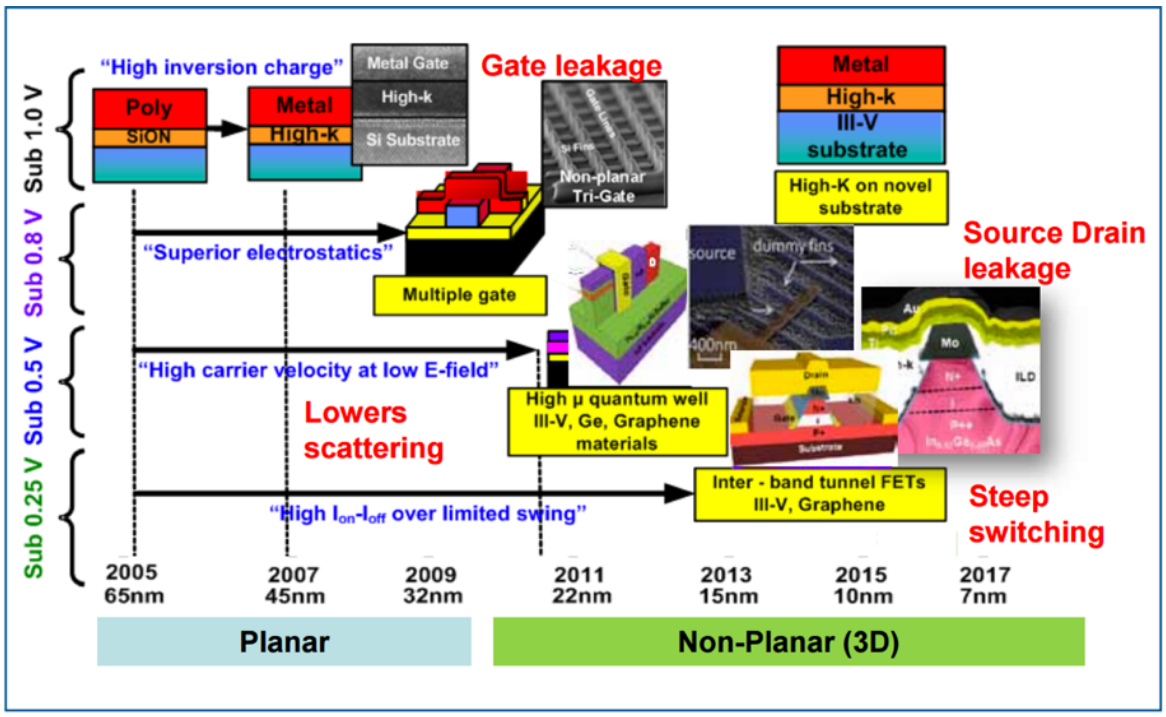


Fig. 1.2. Trends in state-of-the-art high performance (HP) CMOS transistor innovation. Transformative changes in materials (high-k dielectric, Ge, III-V channel) and the transistor architecture (3D, Tunnel FET) being implemented and explored to maintain historical rate of performance, density and power scaling [27].

2.1 High-K Dielectrics

Due to the increasing demand of portable electronics, the electronic devices tend to become smaller in size [29]. Traditionally, SiO_2 was applied as a gate oxide, which has dominated microelectronic industry for decades. As capacitance is inversely proportional to thickness, to increase the gate capacitance and to improve the device performance, the thickness of SiO_2 needs be decreased.

However, when the thickness of SiO_2 goes under 1.4 nm, the electron tunneling effects and high leakage current would cause the decrease of device reliability [30]. Under this circumstance, high-k dielectrics become a potential substitute due to its higher dielectric constant in an acceptable thickness. As capacitance is proportional to dielectric constant, the increase of gate capacitance can be achieved by increasing the dielectric constant. Therefore, the drawback of reducing thickness will be avoided when using high-k dielectrics. In most cases, the thickness of high-k dielectrics is bigger than SiO_2 ones, which reduces leakage current and improves the gate dielectric reliability [31], [32]. Due to these reasons, high-k material has a great potential in the development of semiconductor electronic devices [33].

2.2 Ge and III-V Channel

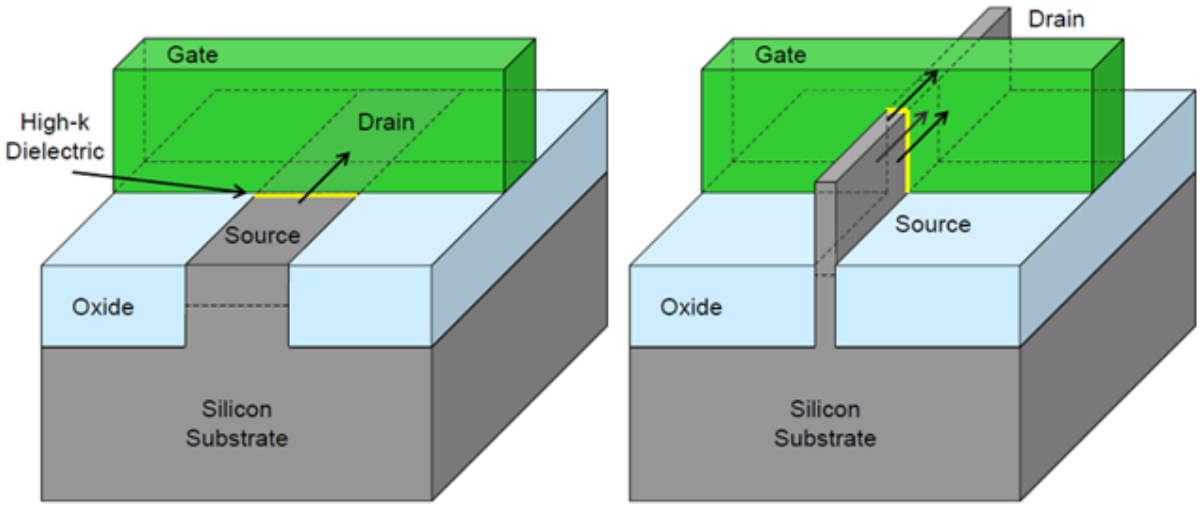
With the implementation of high-k dielectrics at the beginning of the millennium, the effect of reduced carrier mobility caused a problem [34]. Therefore, the use of Si as preferred channel material was put into question, which made high-mobility channel like Ge or III-V with intrinsically higher carrier mobility as a potential substitution [7].

The electron mobility in III-V materials, especially for InGaAs which is investigated in this thesis, is about 10 times higher than the electron mobility of Si. That is because InGaAs has a lower effective mass of electrons compared with Si. A similarly conclusion was found in Ge material whose hole mobility is significantly higher than Si [28].

2.3 FinFET Structure

On the other hand, to reduce the leakage current and approach better performance, the traditional MOSFET (metal–oxide–semiconductor field-effect transistor) was replaced by a 3d structure FinFET (Fin Field Effect Transistor) [5].

Fig. 1.3 shows a simplified depiction of a planar FET and a FinFET. In the traditional 2-d planar structure, a single gate controls the source-drain channel. Due to the leak of gate control, leakage currents are large for a planar FET. The FinFET, on contrary, forms conducting channels on three sides of vertical fin structure, providing a "fully depleted" operation. Therefore, this 3-d structure reduces leakage current and short-channel effect, and results in much better electrostatic gate control of channel and thus better electrical characteristics [5], [11].



Traditional Planar 3D FinFET

Fig. 1.3. Planar and Tri-Gate FinFETs, courtesy of Intel.

Based on FinFET structure, the Ge FinFETs we investigated in this thesis have the advantages of higher hole mobility, reduced short-channel effects, reduced bias-temperature instabilities and compatibility with conventional Si integration processes, which makes it play an important role in the development of future technology [11].

3. Overview of Thesis

Chapter II describes capacitance-voltage (*C-V*) and capacitance-frequency (*C-f*) techniques that have been used to evaluate the effects of border traps in a variety of materials [19], [20], [35], [36] and illustrate the method for MOS capacitors with relatively thick SiO_2 gate dielectrics. The experiment details are also shown in this chapter.

Chapter III illustrates the method applied to multi-fin capacitors built in a state-of-the-art strained Ge *p*MOS FinFET technology with a Si capping layer and SiO_2/HfO_2 gate dielectrics [11]-[14]. Voltage shifts due to radiation-induced oxide- and interface-trap change in multi-fin capacitors are found to be similar to voltage shifts in FinFET transistors built in the same technology [14].

C-f measurements enable estimates of pre-irradiation border-trap densities of ~ $1.3\times10^{11}/cm^2$, which are larger than densities ($< 1\times10^{11}/cm^2$) of radiation-induced trapped charge at doses up to 1.0 Mrad(SiO_2). Hence, these Ge *p*MOS devices are affected more strongly by defects introduced during device fabrication than by irradiation.

The same method was applied in Chapter IV to assist in the characterization of capacitors built in an early development stage InGaAs FinFET technology with Al_2O_3/HfO_2 dielectric layers, which is of interest for future *n*FET applications [28], [37]-[40]. Much larger border-trap densities are observed in these devices than in Ge *p*MOS devices. This most likely occurs due to the different stage of process maturity and higher defectivity of the Al_2O_3/InGaAs interfaces in these devices, as compared with the Ge/Si capping layer/SiO_2 interfaces in the Ge *p*MOS devices.

Smaller radiation-induced defect densities are estimated for capacitors than transistors in this InGaAs technology, indicating that improved transistor response is likely with future technology optimization. These results illustrate the value of using multi-fin capacitor test structures to assist in evaluation of the radiation response of FinFET technologies, and highlight the low defect densities in present-generation Ge *p*MOS FinFETs, compared with III-V FinFETs.

Chapter V provides the summary and conclusions of this work.

CHAPTER II

METHODOLOGY

In this chapter, we describe capacitance-voltage (*C-V*) and capacitance-frequency (*C-f*) techniques, and illustrate the method for MOS capacitors with relatively thick SiO_2 gate dielectrics. The experiment details are also shown in this chapter.

1. Mechanism of *C-V* Measurement

Capacitance–voltage (*C-V*) measurement is an important technique for characterizing semiconductor materials and devices. The change of oxide-trap charge and interface-trap charge can be observed directly from the *C-V* curves, which is more obvious to analyze radiation effects. Furthermore, radiation effects in transistor can be affected by the isolation oxide in-between, which makes it hard to tell the actual radiation effect [4]. Even though shallow trench isolation (STI) technique have been applied to some devices to avoid isolation oxide [42], *C-V* measurement still plays a significant role in investigating more comprehensive and accurate radiation effect.

During *C-V* measurement, the silicon substrate is connected to ground and voltage is applied to the gate, which forms a parallel-plate capacitor. A direct current (DC) bias and an alternating

current (AC) small-signal voltage are simultaneously applied to gate. The AC small-signal is used to measure the value of capacitance at the various DC gate biases, and different *C-V* curves are formed depending on the frequency of the AC signal [43]. Ideal low-frequency and high-frequency *C-V* curves are shown in Fig. 2.1.

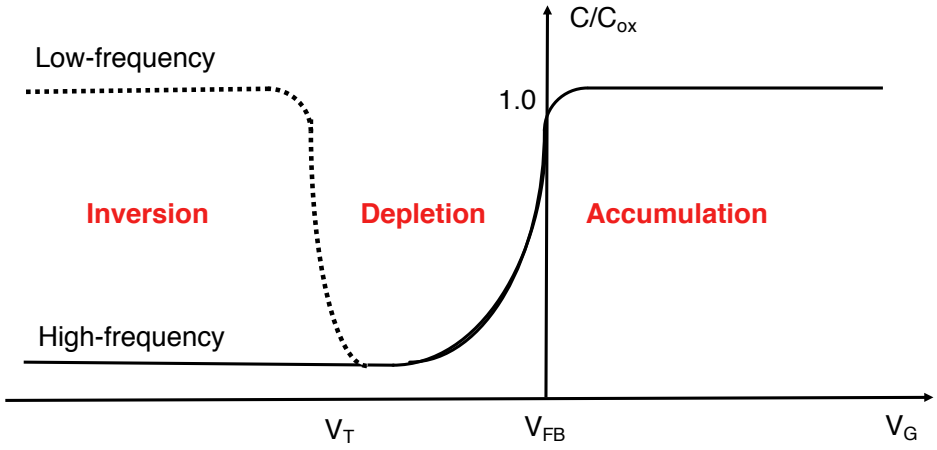


Fig. 2.1. *C-V* curves in low- and high-frequency of a MOS capacitor on a n-type substrate [43].

When a voltage is applied to the gate, the voltage partially dropped across the oxide and partially across the semiconductor. Therefore, the capacitance of MOS device is the oxide capacitance C_{ox} in series with semiconductor capacitance C_s. As the gate voltage changes, the variation of semiconductor surface potential and space-charge region distribution results in three different situations: accumulation, depletion and inversion. These three situations corresponding to three different regions in *C-V* curves is shown in Fig. 2.1 above.

In accumulation region, the surface is heavily accumulated by majority carriers. Thus, the capacitance of the majority carrier is very high, approaching a short circuit [20]. In this way, the

capacitors in semiconductor are all shorted, which makes the overall capacitance equal to the oxide capacitance in Eq. (1). Because the oxide thickness and oxide dielectric constant remain unchanged, the capacitance in accumulation region stays the same (see accumulation region in Fig. 2.1).

$$C = C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}} \tag{1}$$

When it comes to depletion region, the majority carrier density in the surface decreases as the value of surface potential increases, so the surface is depleted. As the value of gate bias increases, the depletion width x_d increases [20]. Because the overall capacitance is the oxide capacitance in series with capacitance in depletion region in Eq. (2), the total capacitance value is reduced. As the semiconductor capacitance is inversely proportional to the depletion width in Eq. (3), the total capacitance is decreasing as the depletion layer increases (see depletion region in Fig. 2.1).

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_S}} \tag{2}$$

$$C_S = \frac{\varepsilon_s}{x_d} \tag{3}$$

With the value of gate voltage growing, the majority carrier density in the surface will decrease to a point where minority carrier density overtakes. In this case, the depletion thickness becomes maximum. If the inversion charge is able to follow the frequency of the applied ac

voltage, inversion layer will be generated at the surface, which makes the capacitance the same as accumulation region (see low-frequency curve in inversion region in Fig. 2.1) [20].

However, if the frequency of applied small AC signal is high, thermal generation cannot create minority carriers fast enough to support a variation of charge in the inversion layer [43]. Therefore, the overall capacitance for high-frequency is C_{ox} in series with C_s in Eq. (2), where x_d reaches the maximal depletion thickness. No matter how gate voltage changes, the *C-V* curves in this case stays minimum (see high-frequency curve in Fig. 2.1).

The *C-V* measurement mechanism can be applied in both *p*-type and *n*-type MOSFET. P-type MOSFET (*p*MOS) has *p*-channel and n-substrate, so the majority carrier is electron and minority carries is hole. The *C-V* curves are shown in Fig. 2.1 above. As for *n*MOS, it's a *n*-channel and *p*-substrate MOSFET with hole as the majority carrier. Its *C-V* curves have accumulation region in negative bias, and depletion and inversion region in positive voltage, which is shown in Fig. 2.2 below.

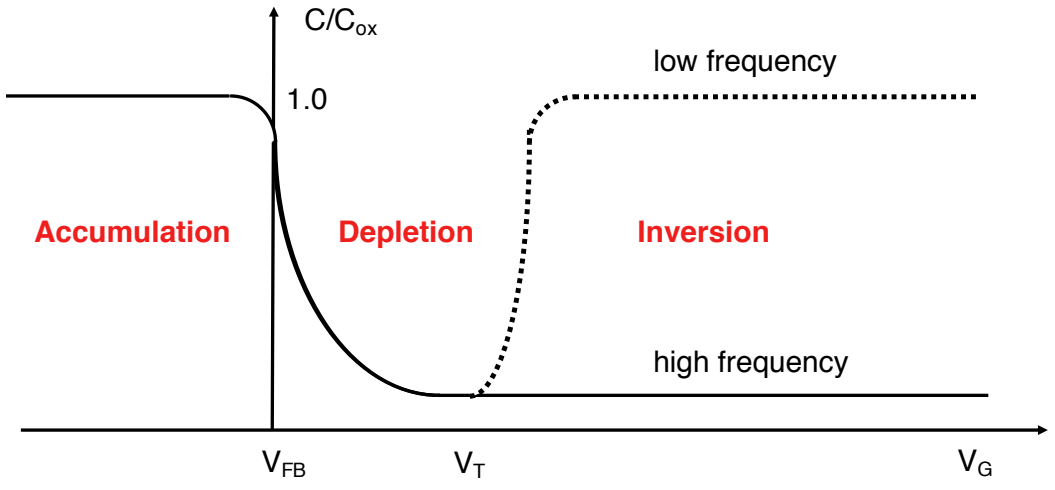


Fig. 2.2. *C-V* curves in low- and high-frequency of a MOS capacitor on a *p*-type substrate [43].

2. Experiment Setup

TID experiments were performed at room temperature using a 10-keV ARACOR X-ray source at a dose rate of 30.3 krad(SiO_2)/min. To be consistent with previous work, 3 V gate bias was applied to the Si MOS capacitors during irradiation, and Ge MOS and InGaAs multi-fin capacitors were biased in the range of ± 1 V. An Agilent 4284A LCR meter supplied DC bias and AC small-signal voltage simultaneously, and perform *C-V* and *C-f* characterization before and after exposure.

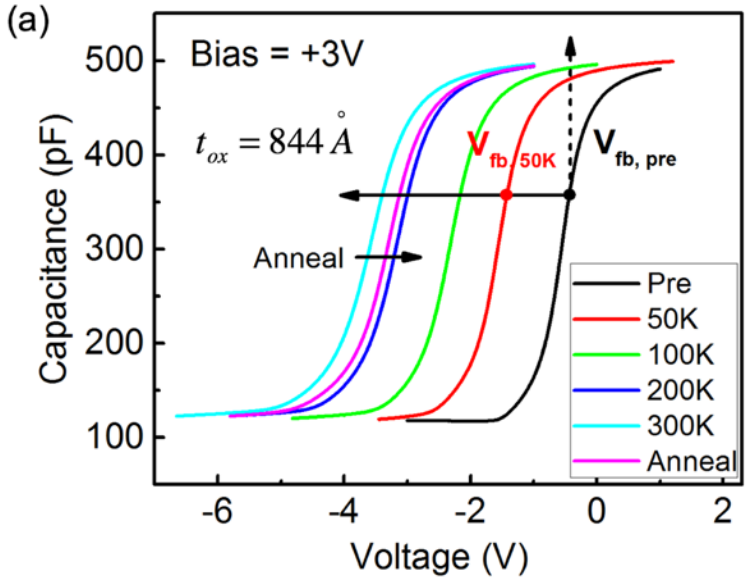
An Agilent 4284A LCR meter (Fig. 2.3) is used to obtain the value of capacitance. During testing, the LCR meter is controlled by computer program with GPIB connection. The low signals in LCR meter is connected with the substrate, and high signals are contacted with the gate of the device. The level of ac small-signal is 30 mV.

Fig. 2.3. Agilent 4284A LCR meter.

3. *C-f* Measurement on Si MOS Capacitors

The Si MOS capacitors in this work include an Al gate and SiO_2 oxide. Two devices from lot E4403A fabricated at Sandia National Laboratories (see [44] for details), with oxide thicknesses of 334Å (W4) and 844Å (W6) are analyzed to motivate and illustrate the *C-f* method for a technology with well-known trapping properties. W6 received an 1100 °C anneal to increase the O vacancy density in its SiO_2 dielectric layer [44].

Fig. 2.4 shows high-frequency *C-V* curves for (a) W6 and (b) W4. Doping densities (*n*-type) are ~ $(1.3 \pm 0.1)\times10^{15}$ cm^{-3} for these capacitors, based on standard $1/C^2$ vs. voltage analysis [20]. *C-V* curves shift negatively with dose, consistent with hole trapping. Larger shifts are found for W6 because this device has a greater oxide thickness and received a high temperature anneal in N_2 that introduced additional oxide traps, as compared with W4 [15],[44]. Flatband voltage shifts (V_{fb}) are shown in Fig. 2.5 for these devices. Net trapped charge densities at V_{fb} at 300 krad(SiO_2) are estimated to be 7.8×10^{11} cm^{-2} for W6 and 1.4×10^{11} cm^{-2} for W4. These estimates include contributions of oxide, interface, and border traps [1],[44].



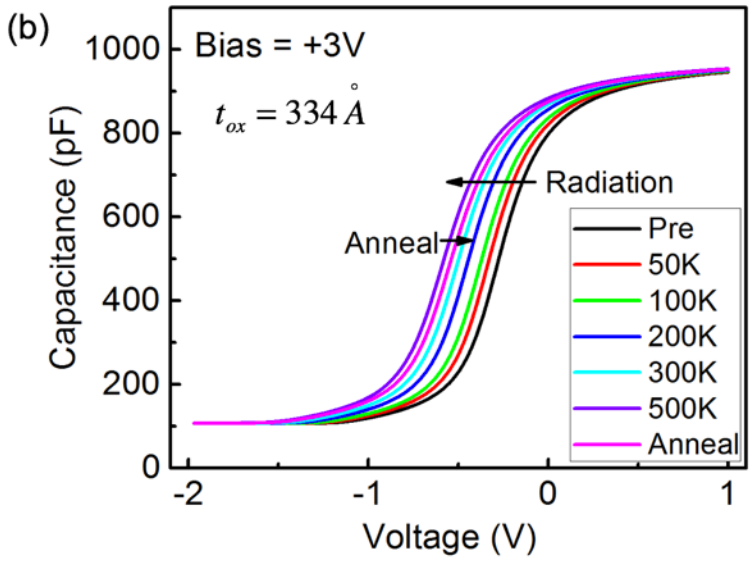


Fig. 2.4. High-frequency (800 kHz) *C-V* curves as a function of dose and room temperature annealing for (a) W6 (t_{ox} = 844 Å; *C-V* ramp rate = 278 mV/s), and (b) W4 (t_{ox} = 344 Å; *C-V* ramp rate = 56 mV/s), irradiated with 10-keV X-rays at V_G = +3 V. Arrows at flatband in (a) show schematically that net hole trapping causes the capacitance at flatband to increase with dose at constant voltage and shift the *C-V* curve to the left at constant capacitance.

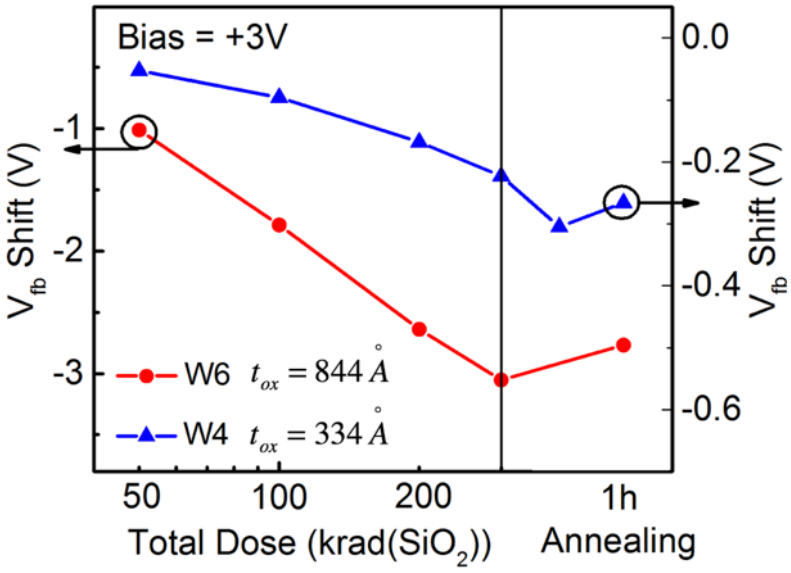


Fig. 2.5. V_{fb} shifts as functions of dose for gate biases V_G = +3 V and room temperature annealing for the devices and measurements of Fig. 2.4. The left-hand scale is for W6, and the right-hand scale is for W4.

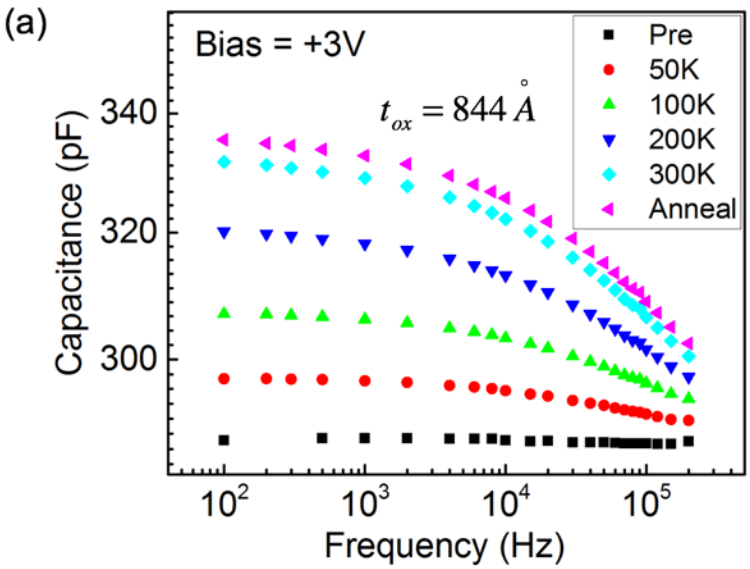
Using the midgap technique of Winokur et al. [1], the net radiation-induced oxide-trap charge density, projected to the Si/SiO_2 interface, can be estimated from high-frequency *C-V* curves via [1]:

$$\Delta N_{ot} = (C_{ox}\Delta V_{mg})/q. \quad (4)$$

Here q is the electronic charge, C_{ox} is the capacitance per unit area, and V_{mg} is the midgap voltage. The combined radiation-induced interface- and border-trap charge density at flatband ΔN_t can be estimated via [1],[45]:

$$\Delta N_t = [(\Delta V_{fb} - \Delta V_{mg})\, C_{ox}]/q. \quad (5)$$

Fig. 2.6. shows the results of *C-f* measurements at fixed DC voltage, V_{fb}, measured initially at high frequency, and then held constant for subsequent measurements at lower frequencies before irradiation, and for each step-stress dose.



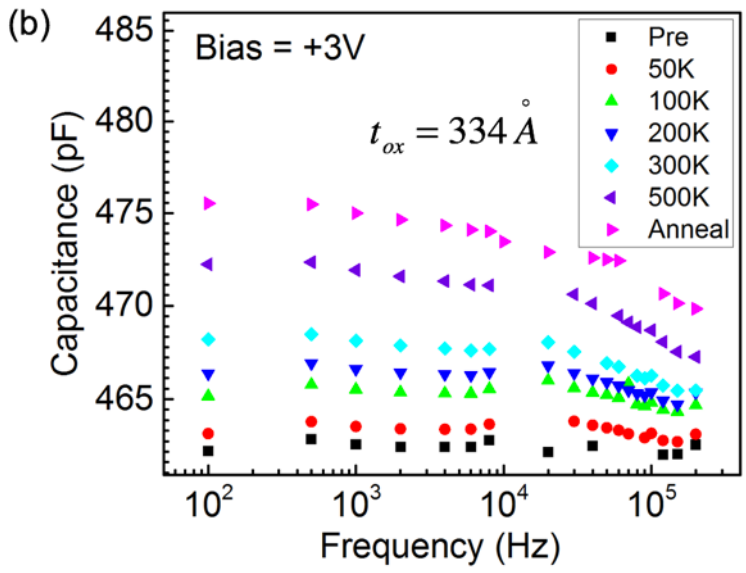


Fig. 2.6. *C* vs. *f* plots as functions of dose and room temperature annealing at flatband for (a) W6, and (b) W4, irradiated and annealed at room temperature with V_G = +3 V.

In the limit of small variations around V_{fb}, additional hole trapping causes the capacitance to increase when the voltage is held constant in the same way that it causes curves to shift to the left when capacitance is held constant (Fig. 2.4 a). In contrast, an increment of negative charge will cause the capacitance at fixed voltage to *decrease* in the same way that it shifts the curve to the right at fixed capacitance, as confirmed below. Flatband potential is selected for these measurements so that varying carrier response times with frequency do not interfere with trap density estimates, as is typically the case at or near inversion [20], and because interface traps are typically charge neutral at midgap [1],[46],[47].

In Fig. 2.6, *C(f)* is relatively constant before irradiation, but increases with decreasing frequency. This increase in capacitance with decreasing frequency occurs because of (1) an increase in border-trap density with increasing dose, and (2) the increasing sensitivity of

electrical measurements to border traps with decreasing frequency [17]-[20],[45]. The increase in border-trap charge density with decreasing frequency has been exploited in previous combinations of *I-V*, charge pumping, and low-frequency noise measurements to provide quantitative estimates of effective border-trap charge densities [17],[19],[48]-[49]. But until now, this simple technique has not been adapted to estimate border-trap densities in irradiated MOS capacitors via *C(f)* measurements.

When there is a measurable difference between values of *C(f)* at high and low frequencies, an estimate of the effective border-trap density $N_{bt,C\text{-}f}$ before and after irradiation can be obtained before irradiation and at each dose level via a simple expression that is analogous to Eq. (4), but modified for application at fixed voltage and varying capacitance:

$$N_{bt,C\text{-}f} = [(V_{fb} - V_{mg})\, \Delta C_f]/q \ . \tag{6}$$

This expression assumes that, like interface traps, border traps are approximately charge neutral at midgap. It also corrects for effects of trapped oxide charge on surface potential in the same way as in Eq. (4) [1],[45]. ΔC_f is the difference in capacitance observed at low and high frequencies, here 1 kHz and 200 kHz.

We designate the effective trap density in Eq. (6) as $N_{bt,C\text{-}f}$ because the time scales on which *C-f* measurements are performed are different than those on which *C-V* measurements are performed. To put the two methods on a common time scale for these devices, a correction factor must be applied.

4. Correction Factor

For Si MOS capacitors with relatively thick SiO_2 oxides, it is relatively straightforward to correct for time-scale differences between *C-f* and high-frequency *C-V* measurements. The dominant border trap in SiO_2 is typically an O vacancy [2],[3],[15],[19],[46],[51]-[53]. Charge exchange between the Si channel border traps occurs via tunneling and/or thermal activation [2],[3],[15],[16],[54]-[56]. Each of these processes is approximately linear with logarithmic time [2],[54]-[56].

For border traps distributed uniformly in space and energy, a typical simplifying assumption often made tacitly or explicitly in similar analyses [1],[2],[16], roughly equal amounts of charge are exchanged between the Si channel and border traps within each accessible time decade. For the *C-f* measurements, the upper and lower limits on the observable time scales for charge exchange with border traps are determined by the maximum and minimum measuring frequencies f_H and f_L (Fig. 2.6).

For high-frequency *C-V* measurements, the time scale is set by the measurement frequency f_{CV} and the respective ramp rate ρ (Fig. 2.4). The latter helps to determine the time $\tau = (V_{fb} - V_{mg})/\rho$ during which charge is able to be exchanged with border traps during *C-V* measurements, under the above assumptions.

Quantifying this comparison, effective border-trap densities sensed via *C-f* and *C-V* measurements, $N_{bt,C\text{-}f}$ and N_{bt}, are related via the following expression:

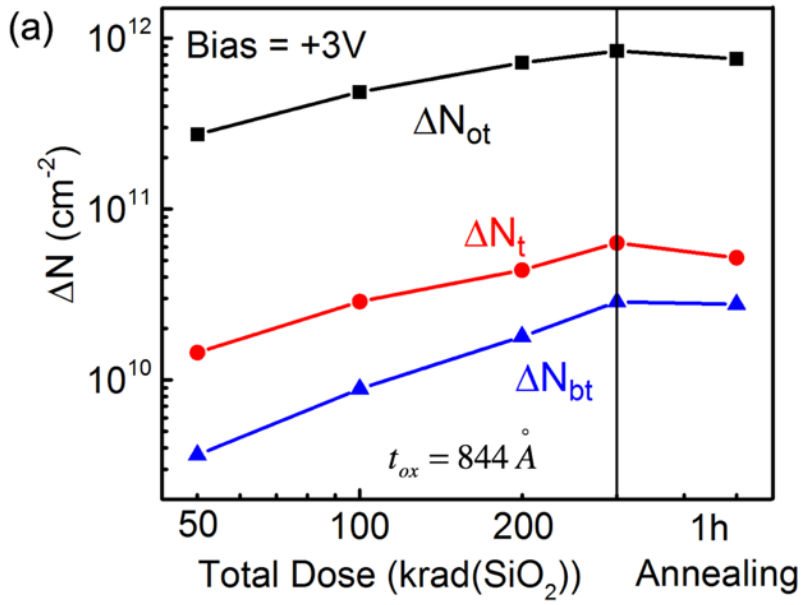
$$N_{bt} / \log_{10} (f_{CV}\ \tau) \approx N_{bt,C\text{-}f} / \log_{10} (f_H/f_L) \quad (7)$$

Rearranging terms, we write this as:

$$N_{bt} \approx N_{bt,C\text{-}f}\ [\log_{10} (f_{CV}\ \tau) - \log_{10} (f_H/f_L)] \quad (8)$$

Figs. 2.7 (a) and (b) show estimates of ΔN_{ot}, ΔN_t, and ΔN_{bt} for W6 and W4 using Eqs. (4)-(8). Oxide-trap charge clearly dominates the radiation response of these devices [44]. Before irradiation, estimated border-trap densities are below the threshold of detection, ~ 2-3×10^8 cm^{-2}, for these devices and measurement conditions.

These are lower bound estimates of fast border-trap densities [19], since *C-f* measurements cover only ~ 3 decades of response.



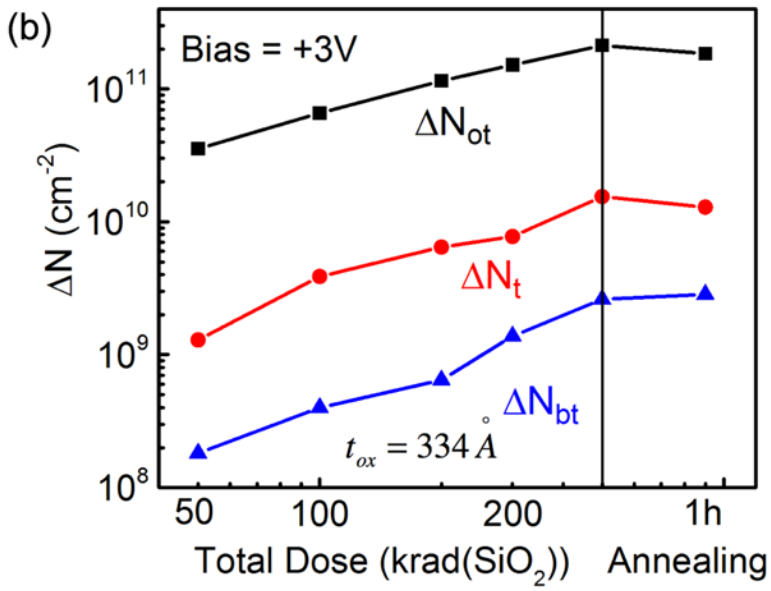


Fig. 2.7. Radiation-induced charge densities as functions of dose and room temperature annealing at flatband for (a) W6, and (b) W4, irradiated and annealed at room temperature with V_G = +3 V. The pre-irradiation, effective border-trap density is less than 2-3×10^8 cm^{-2} in each device, which is approximately our threshold for detectability via *C-f* measurements.

However, Fig. 2.7 shows that up to 50% of the stretchout in the high-frequency *C-V* curves of Fig. 2.4 can result from border traps, with higher percentages observed at higher doses and for the thicker oxide (W6) that received the high-temperature anneal in N_2 to enhance its O vacancy density. Inferred densities of border traps and ratios to interface-trap charge densities in Fig. 2.7 are comparable to previous work on Si MOS transistors with similar oxides using *I-V*, charge pumping, and/or 1/*f* noise measurements [17],[45],[48], reinforcing the utility of this approach.

Finally, we note that, for oxides other than SiO_2, and/or alternative channel devices, correction factors either may not be needed, and/or may differ significantly from those in Eqs. (4) and (5) [3],[15],[35]. That is because ultrathin dielectric layers with multi-gate interfaces are under much stronger gate control than planar MOS capacitors with thick oxides [4],[5],[8], and because charge trapping and annealing is often quite different for SiO_2 and high-K gate dielectrics. Hence we limit the use of Eqs. (7) and (8) to estimates of border-trap densities in relatively thick SiO_2 oxides (Fig. 5). Eqs. (4)-(6) are applied to the remainder of the devices tested, without attempts at adjustment.

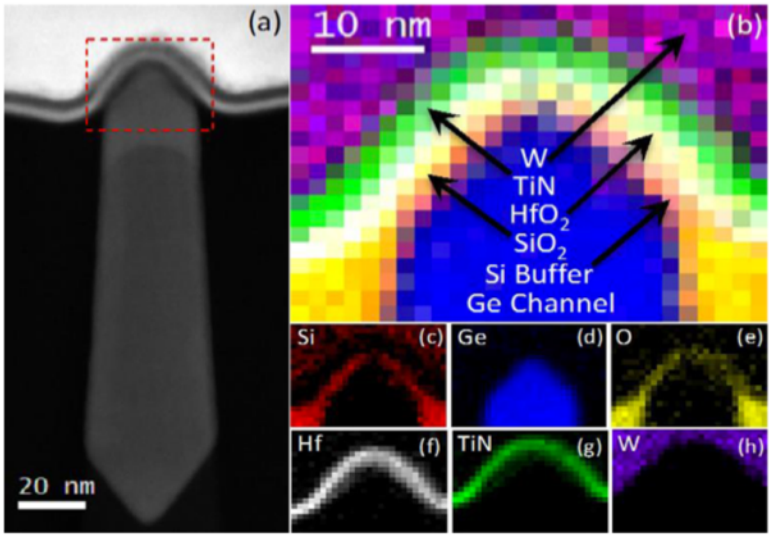
CHAPTER III

GE MUTI-FIN CAPACITORS

This chapter introduces the method applied to multi-fin capacitors built in a state-of-the-art strained Ge *p*MOS FinFET technology with a Si capping layer and SiO_2/HfO_2 gate dielectrics. The device information is illustrated first, and *C-V* and *C-f* results for these devices are shown later. The radiation-induced trap charge densities are estimated and provided in this chapter.

1. Device Information

Ge *p*MOS FinFETs capacitors were fabricated at imec on 300 mm bulk Si (100) wafers. Details of the structures and processing are provided in [11]-[14]. A STEM image and chemical composition map of this device are shown in Figs. 3.1(a)-(h). Above the thin SiO_2 interfacial layer, a ~1.5 nm HfO_2 layer and TiN metal gate were deposited to form the gate stack. The effective oxide thickness (EOT) is ~1.9 nm [11]-[14]. Capacitors vary in Ge fin width from 46 nm to 75 nm, and have a fin length of 12.5 μm. Fig. 3.1(i) shows the layout grid of the multi-fin capacitor test structure used for this work.



(i)

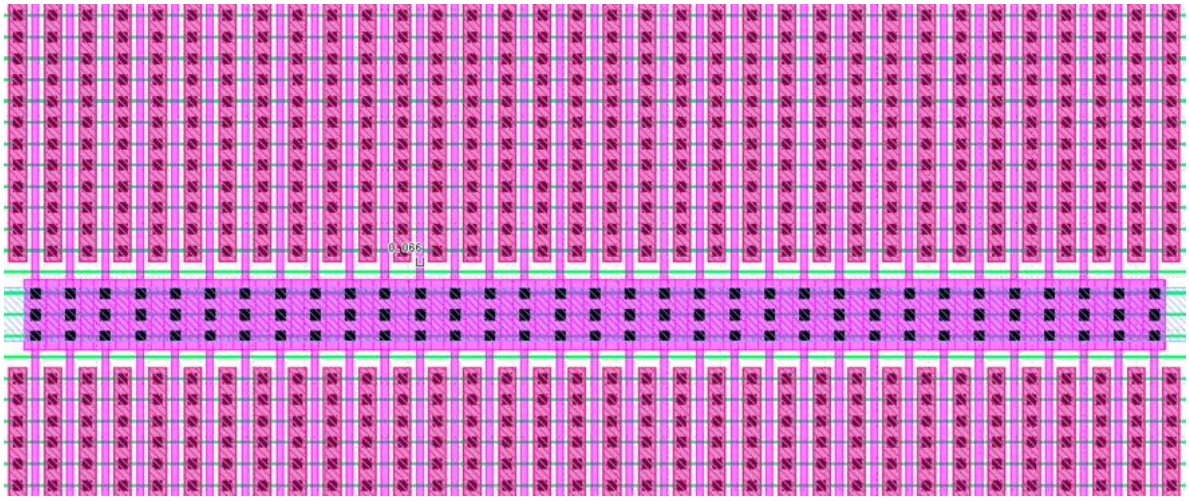


Fig. 3.1. (a) STEM image of bulk Ge FinFETs. (b) Chemical composition map of structure layers from EELS. (c)-(h) Individual maps of elements/compounds in the device (after [14]). (i) Layout of capacitor test structure. 2 fins were connected in parallel for the Ge FinFET capacitors that were measured. The total area of each capacitor includes multiple surfaces of multiple fins.

The device map of the capacitors is shown in Fig. 3.2. In each block (CAP), there are 8 devices with different area. Fin length is decreasing from the first row to the last. Fin width for the first and third rows is increasing from the first element to the tenth, and is decreasing for second and fourth rows.

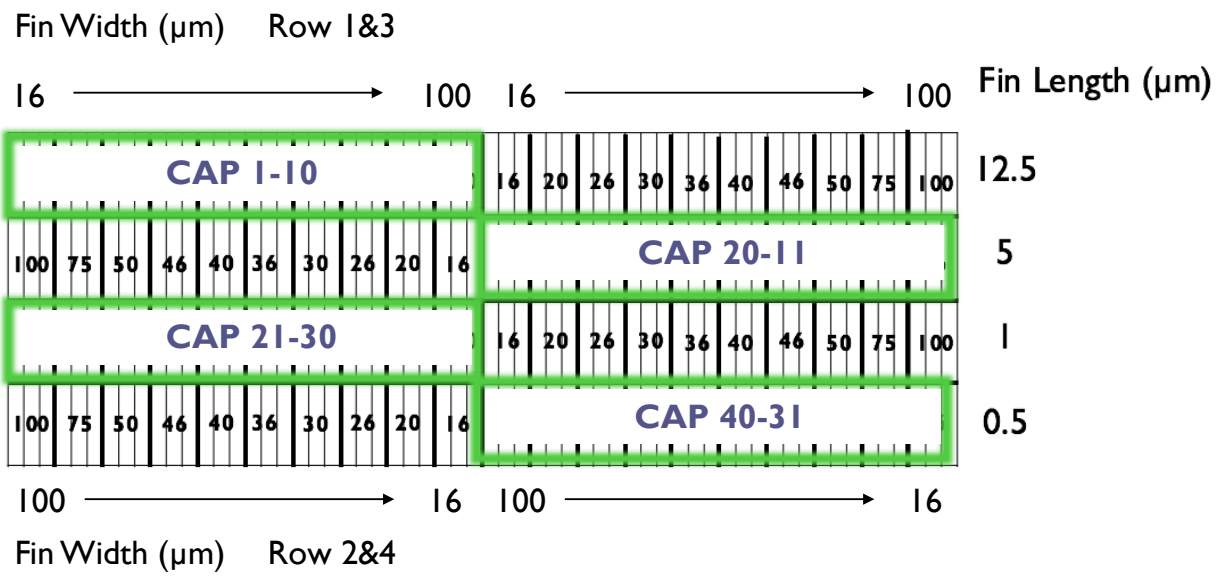


Fig. 3.2. Layout of Ge pMOS capacitor FinFET with fin length from 0.5 μm to 12.5 μm and fin width from 16 nm to 100nm.

2. *C-V* and *C-f* Measurements

Fig. 3.3(a) shows high-frequency (1 MHz) *C-V* curves for Ge two-fin capacitors irradiated with +1 V bias for a device with fin length of 12.5 μm and fin width of 75 nm. The effective (*n*-type) doping density for these structures is ~ 6×10^{16} cm^{-3}, based on standard $1/C^2$ vs. voltage analysis [20]. The *C-V* curves shift positively with irradiation, consistent with net negative charge trapping in the HfO_2 [13],[14]. Arrows at flatband in Fig. 3.3 (a) show schematically that net negative charge trapping causes the capacitance at flatband to decrease with dose at constant voltage and shift the C-V curve to the right at constant capacitance. Flatband voltage shifts (V_{fb}) are shown in Fig. 3.3(b) for devices with different fin widths, irradiated with +1 V or 0 V bias. Larger shifts are found at +1 V bias than 0 V bias during irradiation, with no significant effects

of geometry observed, consistent with trends for FinFETs in [14]. Ge multi-fin capacitors were also irradiated at -1 V, with voltage shifts of (0 ± 2) mV at 1 Mrad(SiO_2).

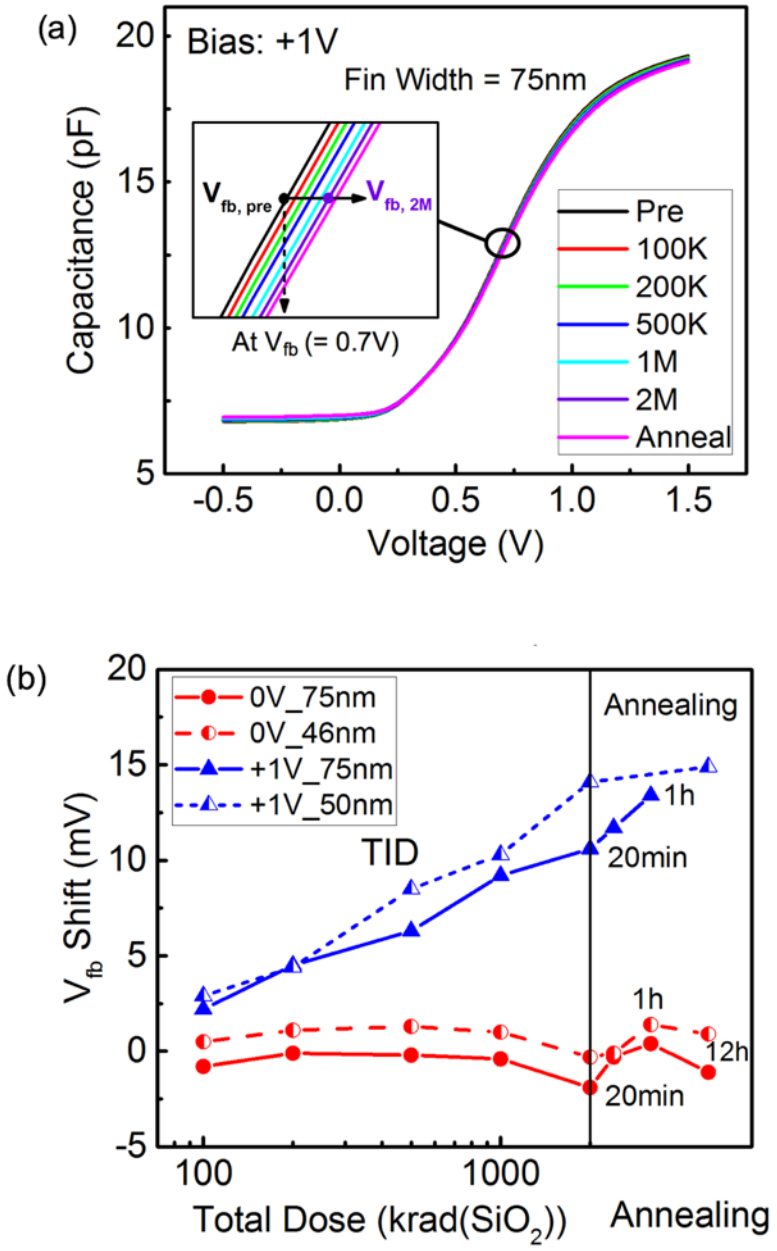
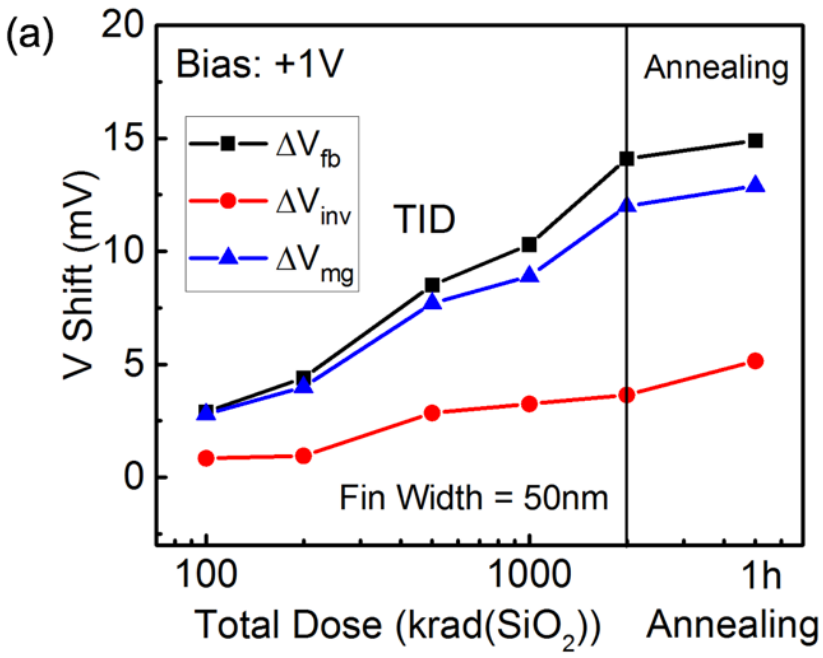


Fig. 3.3. (a) High-frequency C-V curves as functions of dose and room temperature annealing for a two-fin capacitor with fin length of 12.5 μm and fin width of 75 nm at gate bias V_G = +1V, and (b) V_{fb} shifts as functions of dose for gate biases V_G = 0 V and +1 V, and room temperature annealing up to 12 h for devices with fin length of 12.5 μm, and fin widths of 75 nm, 50 nm, and 46 nm, as noted.

Fig. 3.4(a) shows flatband, midgap, and inversion voltage shifts for a device with 50-nm fin width irradiated at +1 V. The similarity of the midgap and flatband shifts suggests that oxide-trap charge is more significant than interface-trap charge in these devices [1],[13],[14].

Results for *p*MOS transistors built in the same FinFET technology are shown for comparison in Fig. 3.4(b). Similarly small shifts are observed for capacitors and transistors, and results under similar bias conditions typically differ by less than 10-20 mV for the two kinds of structures. Hence, for these Ge *p*MOS devices, capacitors and transistors show similar radiation responses.



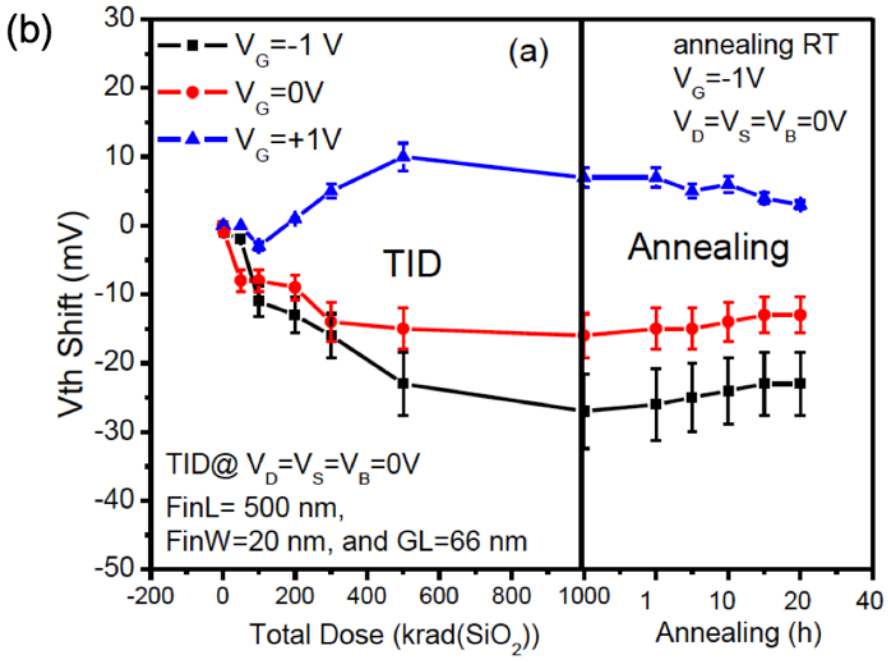


Fig. 3.4. (a) V_{th}, V_{fb}, and V_{mg} shifts as functions of dose and room-temperature annealing for the device showing the worst-case shifts in Fig. 3.3(b), and (b) V_{th} shift as functions of dose and room-temperature annealing for transistors from the same wafer (from [14]).

C-f curves for a two-fin Ge *p*MOS capacitor are shown in Fig. 3.5(a); the dose and frequency response are quantified in Fig. 3.5(b). The capacitance increases with decreasing frequency even before the devices were irradiated, consistent with a significant border-trap density (~ 1.3×10^{11}/cm^2) in these devices before irradiation.

These devices show net negative charge trapping during irradiation; consequently, the capacitance at flatband decreases with dose in Fig. 3.5 during the *C-f* measurements, as shown schematically in Fig. 3.3(a).

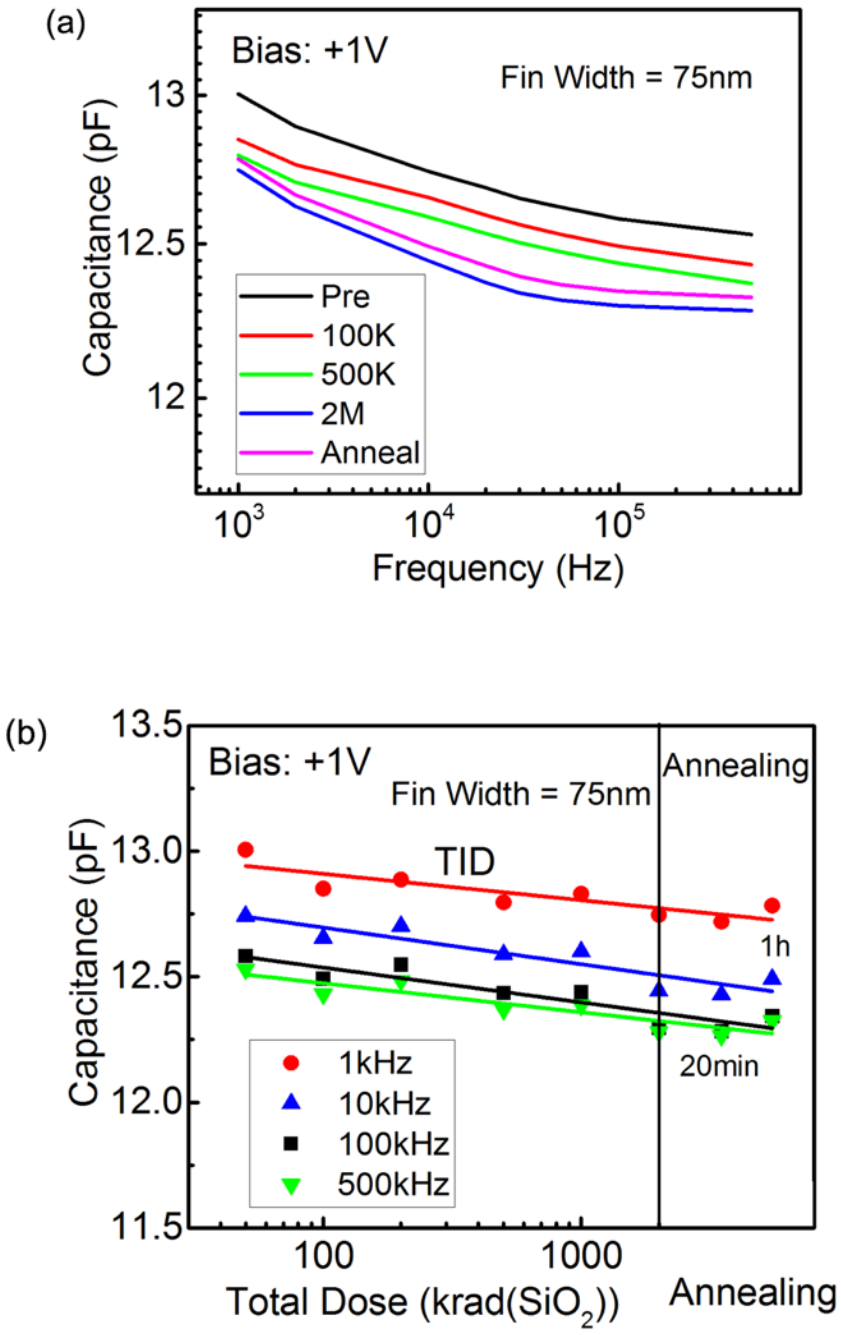


Fig. 3.5. (a) C vs. f plots, and (b) capacitance at flatband as functions of dose and room temperature annealing, for two-fin capacitors with fin length of 12.5 μm and fin width of 75 nm, irradiated and annealed at room temperature with V_G = +1 V.

3. Estimating Trapped Charge Densities

Oxide, interface, and border-trap charge densities for the device of Fig. 3.5 are estimated via Eqs. (4)-(6), without the corrections of Eqs. (7) and (8), and shown in Fig. 3.6. Radiation-induced trapped charge densities are modest in these devices; $\Delta N_t \approx 10^{11}/\text{cm}^2$, and ΔN_{ot} and ΔN_{bt} are each ~ $1.5\times10^{10}/\text{cm}^2$ at a dose of 1 Mrad(SiO_2).

Hence, negatively charged interface traps are the dominant radiation-induced defect in these devices, but their density is less than the pre-irradiation density of border traps. We conclude that the properties of these devices are influenced more strongly by defects introduced during device fabrication than ones created during ionizing radiation exposure.

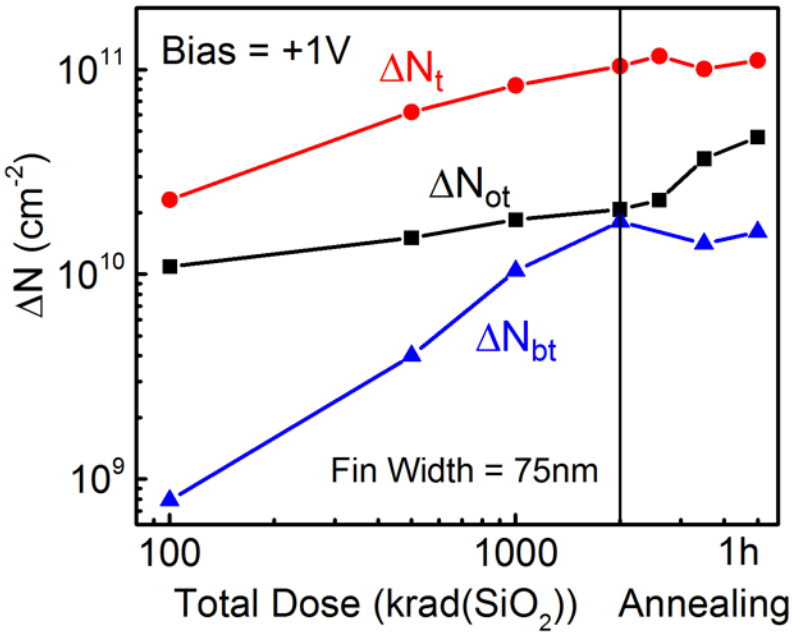


Fig. 3.6. Radiation induced charge density as functions of dose and room temperature annealing at flatband for the devices of Fig. 3.5. The pre-irradiation border-trap density is 1.3×10^{11} cm^{-2} for this device.

CHAPTER IV

InGaAs MUTI-FIN CAPACITORS

This chapter introduces the method applied to capacitors and transistors built in an early development stage InGaAs FinFET technology with Al_2O_3/HfO_2 dielectric layers. The device information is illustrated first, and *C-f* results and radiation-induced trap charge estimations for these devices are shown later.

1. Device Information

InGaAs *n*MOS FinFETs were also fabricated at imec in an early development stage technology. These devices have n-type substrate and are operated in accumulation mode [39],[40]. A STEM image and schematic diagram of this device is shown in Fig. 4.1 [40].

Above the 2 nm Al_2O_3 layer, a 2 nm HfO_2 layer and TiN metal gate were deposited to form the gate stack. The EOT for this stack is ~1.5 nm, as measured from planar structures. The capacitors vary in InGaAs fin width from 20 nm to 26 nm, and have a fin length of 5 μm. The transistors shown in this work have fin width of 26 nm and fin length of 5 μm.

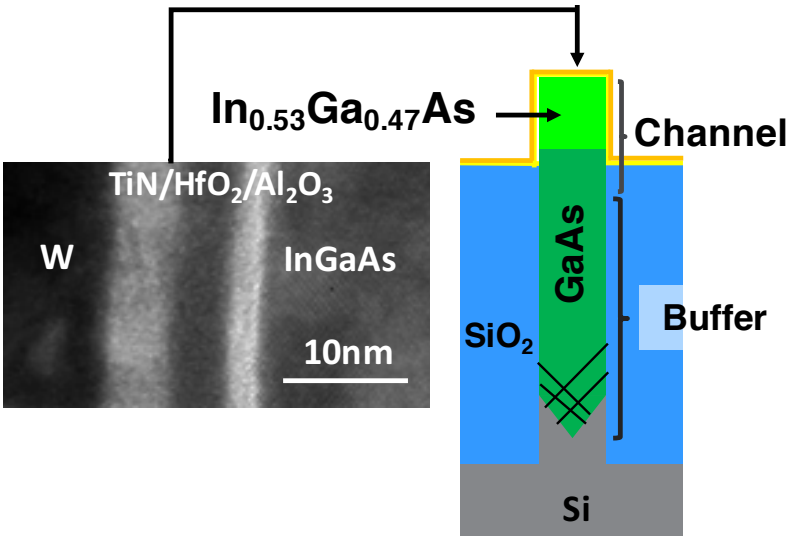


Fig. 4.1. STEM image of bulk InGaAs FinFETs (after [40]). The test structure layout for these devices is similar to that in Fig. 3.1 (i). The gates of multi-fin capacitors are common with FinFET test structures. The bottom contact is connected the channel (body) through the substrate for Ge MOS capacitors, and to the channel (body) directly from a top contact for the InGaAs MOS capacitors.

The layout grid of the multi-fin capacitor test structure is the same as Fig. 3.1 (i) shown in Chapter III. For the InGaAs FinFET capacitors, 50 fins were connected in parallel. The total area of each capacitor includes multiple surfaces of multiple fins.

The device map of the capacitors is the same as Fig. 3.2 shown in Chapter III. In each block (CAP), there are 9 devices with different area. The device map for transistors is shown in Fig. 4.2. Fin length is decreasing from the first row to the last. Fin width for the first and third rows is increasing from the first element to the tenth, and is decreasing for second and fourth rows. In each block (FE), there are 8 devices with different gate length.

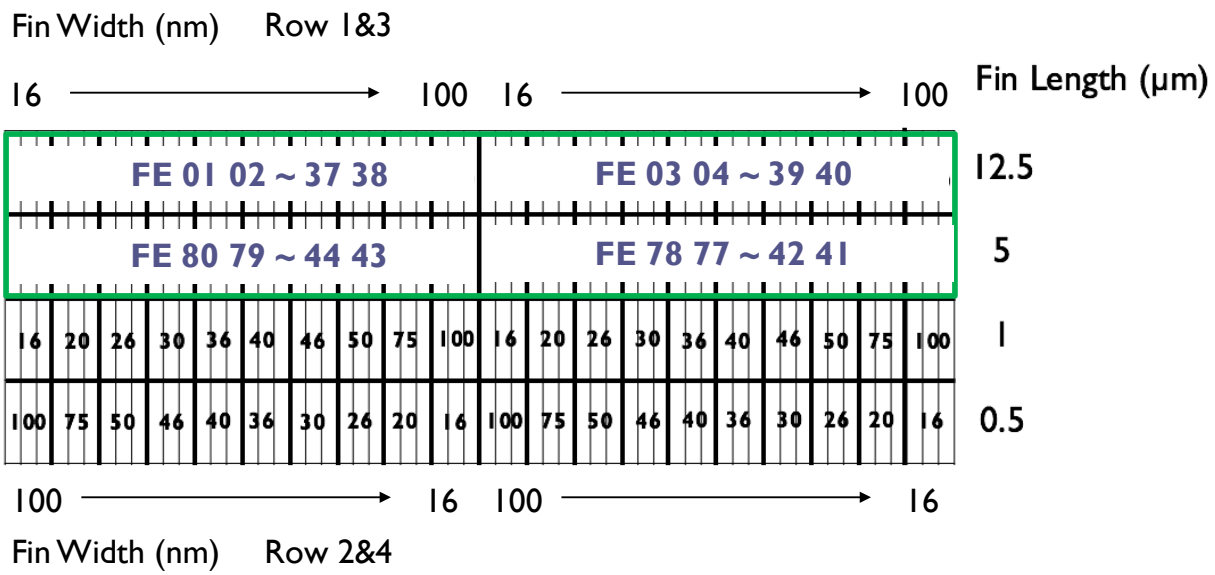


Fig. 4.2. Layout of InGaAs transistor FinFET with fin length from 0.5 μm to 12.5μm and fin width from 16 nm to 100nm.

2. Total Ionizing Dose Effects on InGaAs Capacitors

Fig. 4.3 shows (a) high-frequency (1 MHz) *C-V* curves and (b) *C-f* curves from 100 Hz to 1 MHz for 50-fin InGaAs capacitors irradiated with +1 V bias. These devices have a fin length of 5 μm and fin width of 20 nm. The effective (*n*-type) doping density of these structures is ~ 4×10^{18} cm^{-3}, based on standard $1/C^2$ vs. voltage analysis [20].

Net hole trapping is observed in these devices in Fig. 4.3 (a); the apparent increase in capacitance below inversion in Fig. 4.3(a) is due to gate leakage. Arrows at flatband in Fig 4.3(a) show schematically that net hole trapping causes the capacitance at flatband to increase with dose at constant voltage and shift the *C-V* curve to the left at constant capacitance.

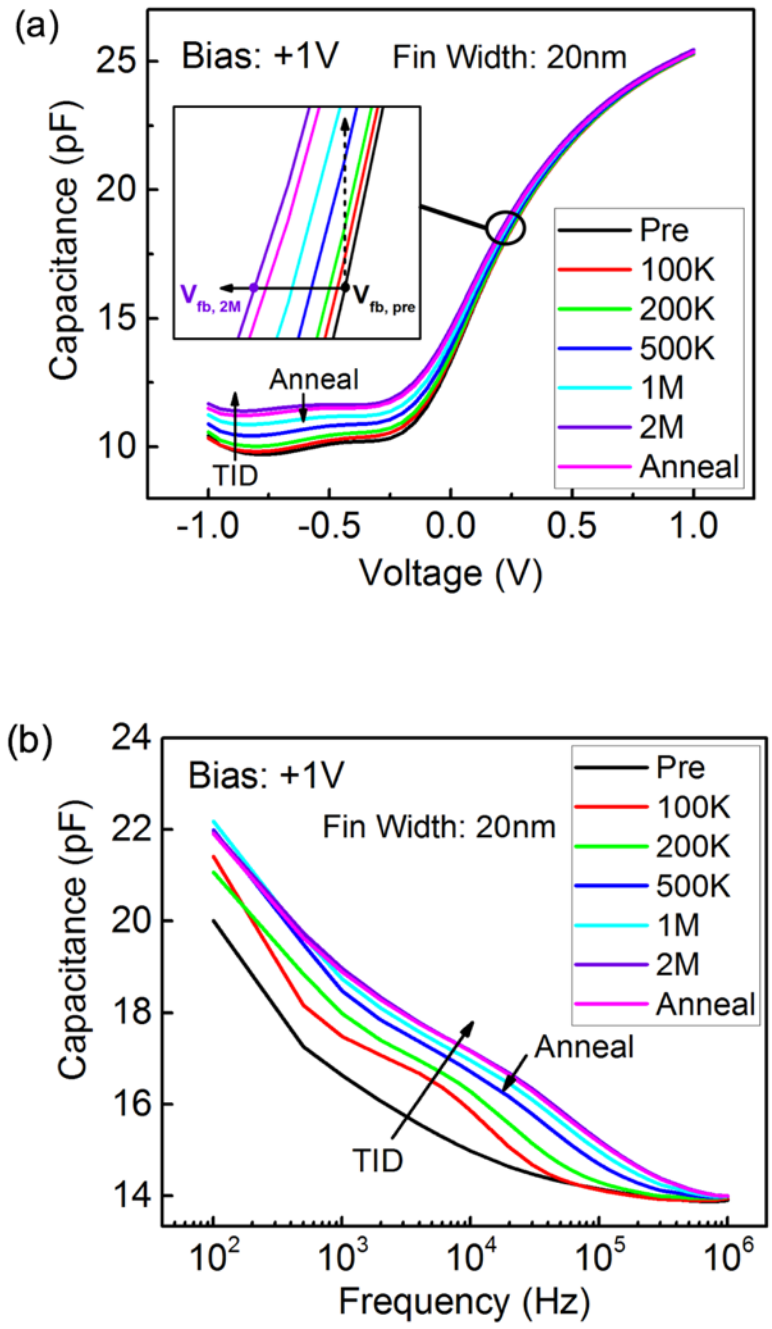


Fig. 4.3. (a) High-frequency (1 MHz) *C-V* curves, and (b) *C-f* curves as functions of dose and room temperature annealing for a 50-fin capacitor with fin length of 5 μm, fin width of 20 nm, at gate bias V_G = +1 V.

Fig. 4.4 shows flatband, midgap, and inversion voltage shifts for a device with 20-nm fin width irradiated at +1 V.

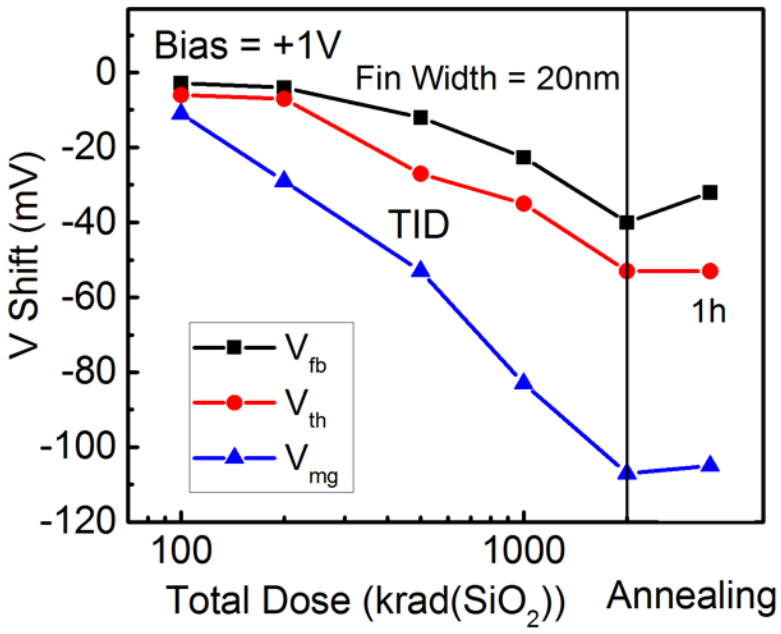


Fig. 4.4 V_{th}, V_{fb} and V_{mg} shifts as functions of dose and room temperature annealing for a device with fin length of 5 μm, fin width of 20 nm at gate bias V_G = +1V.

The capacitance increases with decreasing frequency and increasing dose in Fig. 4.3(b). The pre-irradiation border-trap density, estimated from Eq. (6), is ~ 1.7×10^{11}/cm^2.

The dose and frequency response are quantified in Fig. 4.5. The capacitance increases with decreasing frequency even before the devices were irradiated, consistent with a significant border-trap density (~ 1.3×10^{11}/cm^2) in these devices before irradiation.

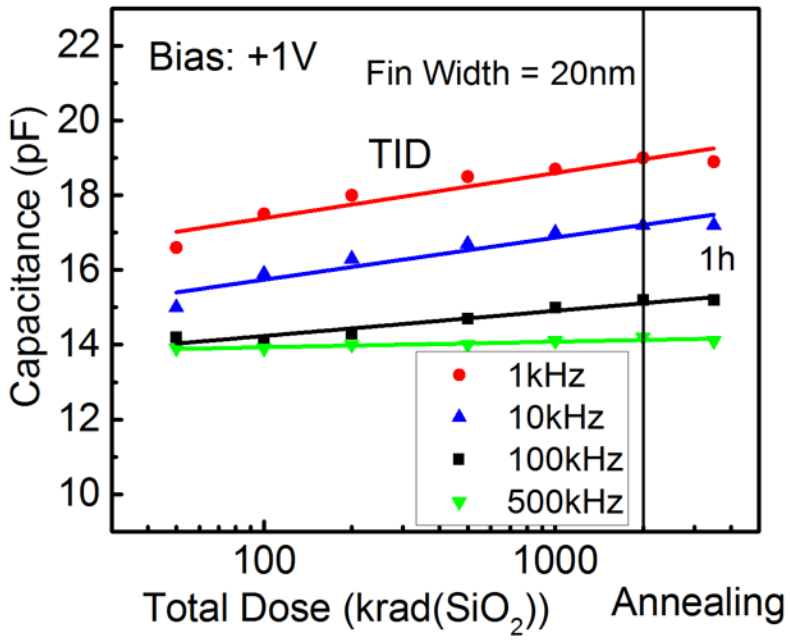


Fig. 4.5 Capacitance as functions of dose and room temperature annealing up to an hour at flatband, for devices with fin length of 5 μm and fin width of 20 nm, irradiated and anneal at room temperature with $V_G = +1$ V.

The radiation-induced trapped-charge densities for the devices of Fig. 4.3 are shown in Fig. 4.6, again using Eqs. (4)-(6) without the corrections of Eqs. (7) and (8). There is a large shift due to radiation-induced oxide-trap charge, consistent with significant hole trapping in these Al_2O_3/HfO_2 gate stacks [57].

The increase in border-trap density in these devices at 2 Mrad(SiO_2) is similar to the as-processed density of border traps. The large density of border traps in as-processed and irradiated InGaAs devices is consistent with much previous work [35],[37]-[40],[58]-[60].

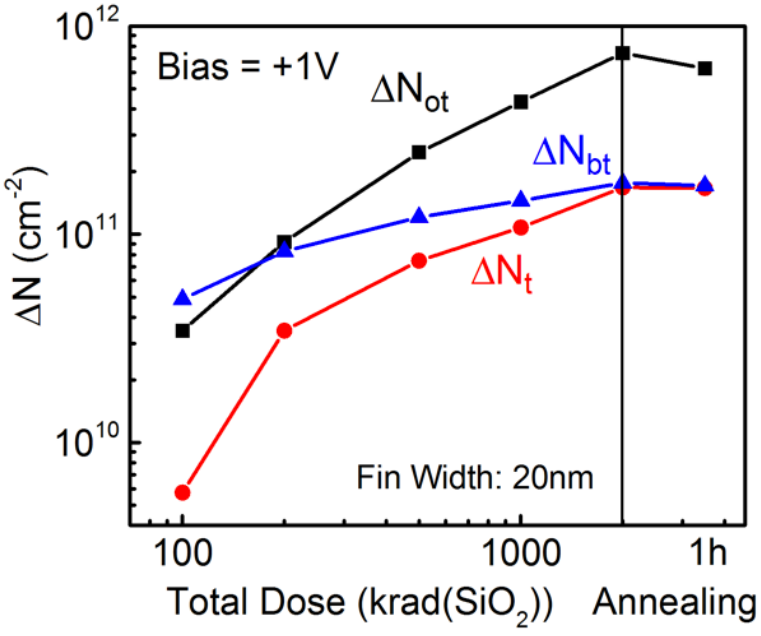


Fig. 4.6. Radiation induced charge densities as functions of dose for the devices and irradiation conditions of Fig. 4.3. The pre-irradiation border trap density is 1.7×10^{11} cm^{-2} for this device.

Figs. 4.7 - 4.9 show results for similar devices irradiated with -1 V gate bias. Again, a large initial border-trap density and significant radiation-induced shifts are observed, with hole trapping dominating the radiation induced shifts, and border traps comprising a significant fraction of the stretchout in the *C-V* measurements.

In Figs. 4.3(b) and 4.7(b), a hump is shown in the *C-f* characteristics at frequencies of ~ 10^3-10^5 Hz. This hump can be due either to interface traps or fast border traps. But the dominant change in the *C-f* curves occurs at lower frequencies, and likely is due to border traps [35],[58],[59].

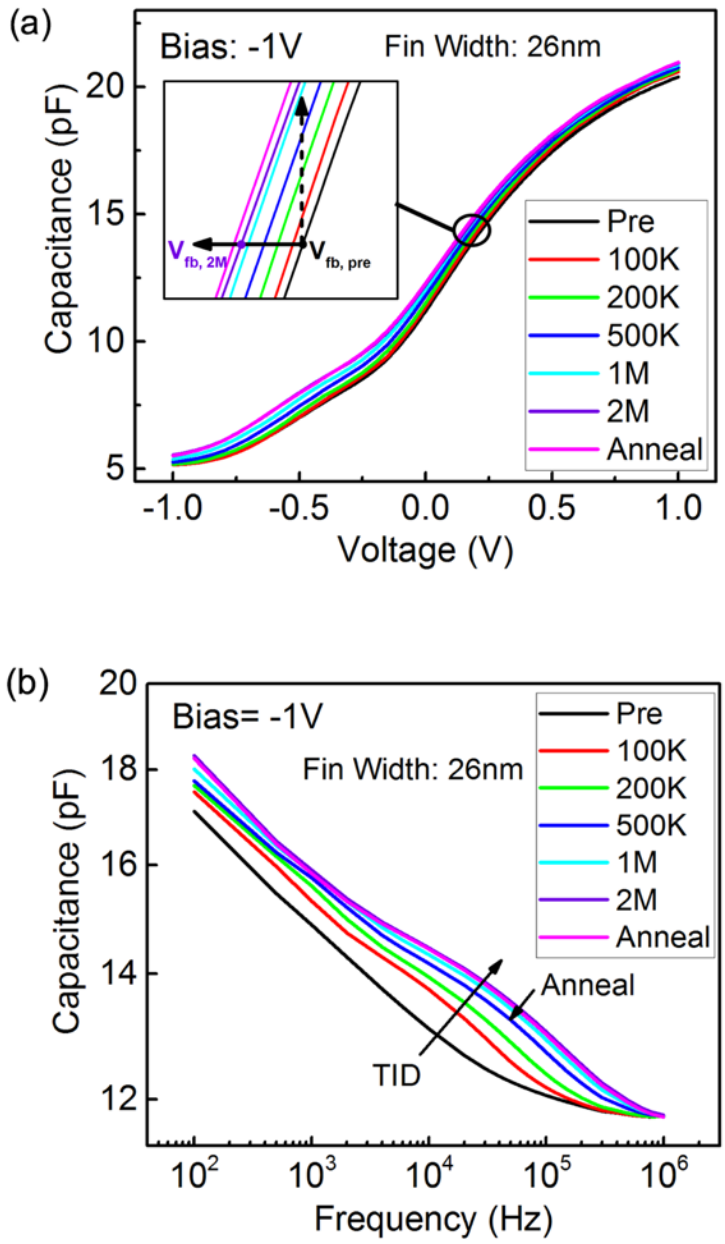


Fig. 4.7. (a) High-frequency (1 MHz) *C-V* curves, and (b) *C-f* curves as functions of dose and room temperature annealing for a 50-fin capacitor with fin length of 5 μm, fin width of 26 nm, at gate bias V_G = -1 V.

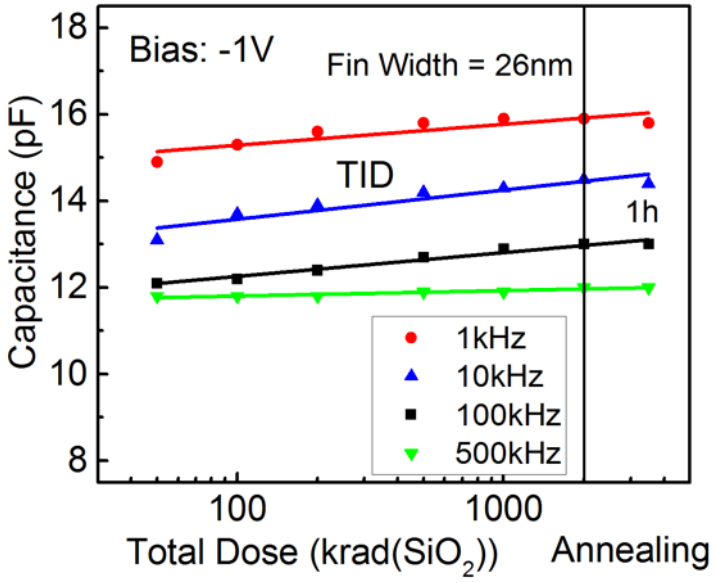


Fig. 4.8 Capacitance as functions of dose and room temperature annealing up to an hour at flatband, for devices with fin length of 5 μm and fin width of 26 nm, irradiated and anneal at room temperature with V_G = -1 V.

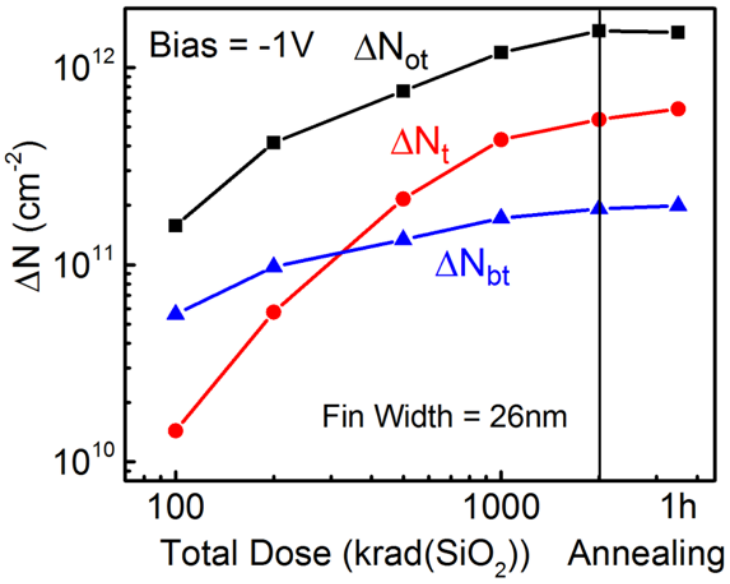


Fig. 4.9. Radiation induced charge densities as functions of dose for the devices and irradiation conditions of Fig. 4.7. The pre-irradiation border trap density is 3.9×10^{11} cm^{-2} for this device.

Figs. 4.10 - 4.13 show results for similar devices irradiated with 0 V gate bias. Similar results were found. A large initial border-trap density and significant radiation-induced shifts are observed. From *C-V* curves, hole trapping dominating the radiation induced shifts, and border traps comprising a significant fraction of the stretchout in the *C-V* measurements.

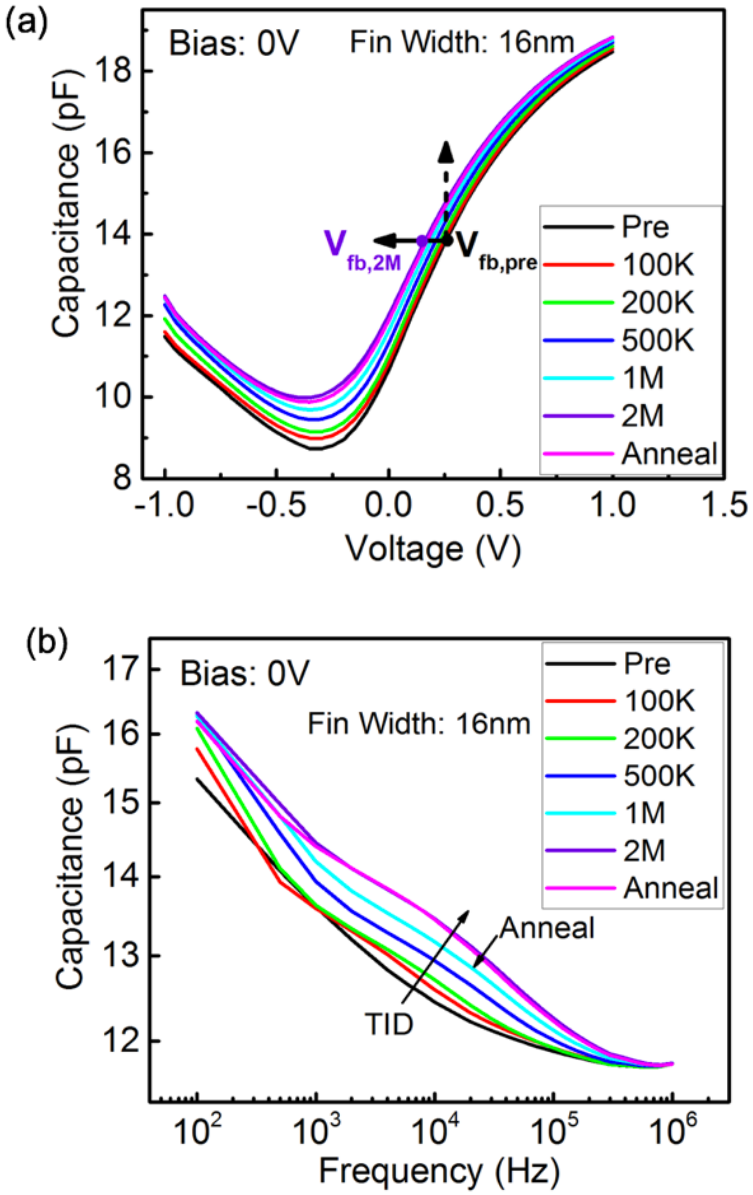


Fig. 4.10. (a) High-frequency (1 MHz) *C-V* curves, and (b) *C-f* curves as functions of dose and room temperature annealing for a 50-fin capacitor with fin length of 5 μm, fin width of 16 nm, at gate bias V_G = 0 V.

Fig. 4.11(a) shows flatband, midgap, and inversion voltage shifts for a device with 16-nm fin width irradiated at 0 V. Same as Ge *p*MOS capacitor, the similarity of the midgap and flatband shifts suggests that oxide-trap charge is more significant than interface-trap charge in these devices.

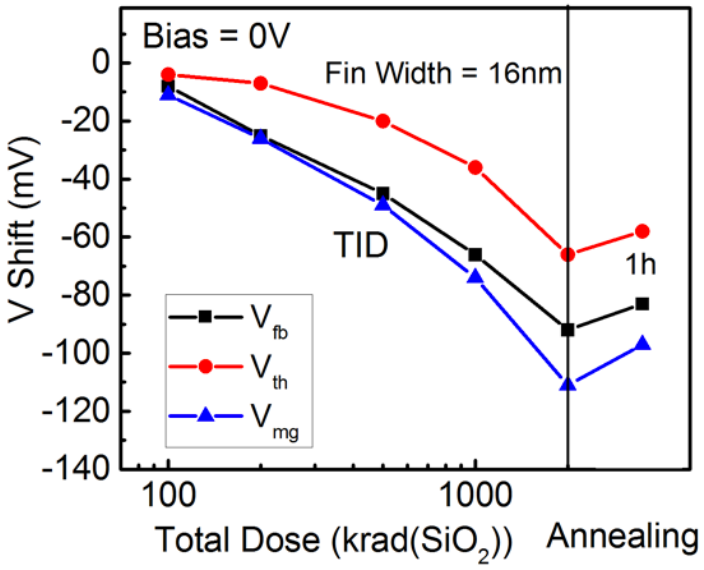


Fig. 4.11 V_{th}, V_{fb} and V_{mg} shifts as functions of dose and room temperature annealing for a device with fin length of 5 μm, fin width of 16 nm at gate bias V_G = 0 V.

The dose and frequency response are quantified in Fig. 4.12. The capacitance increases with decreasing frequency even before the devices were irradiated, consistent with a significant border-trap density (2.36×10^{11} cm^{-2}) in these devices before irradiation.

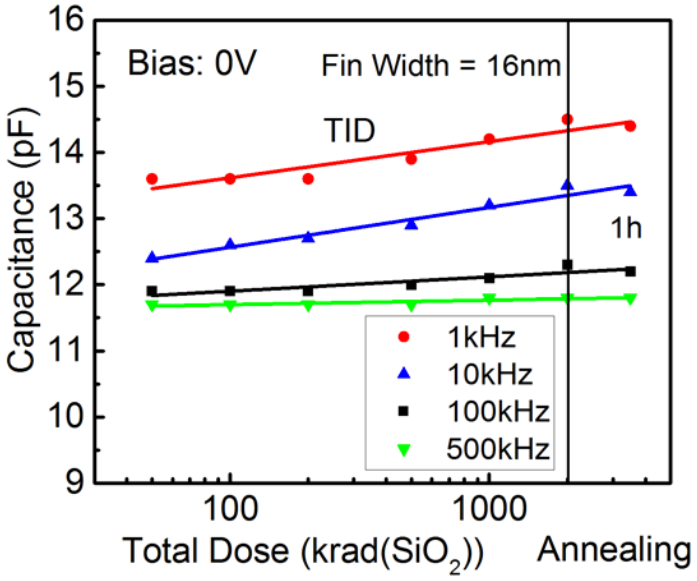


Fig. 4.12 Capacitance as functions of dose and room temperature annealing up to an hour at flatband, for devices with fin length of 5 μm and fin width of 16 nm, irradiated and anneal at room temperature with $V_G = 0$ V.

The radiation-induced trapped-charge densities for the devices of Fig. 4.10 are shown in Fig. 4.13, using Eqs. (4)-(6) without the corrections of Eqs. (7) and (8).

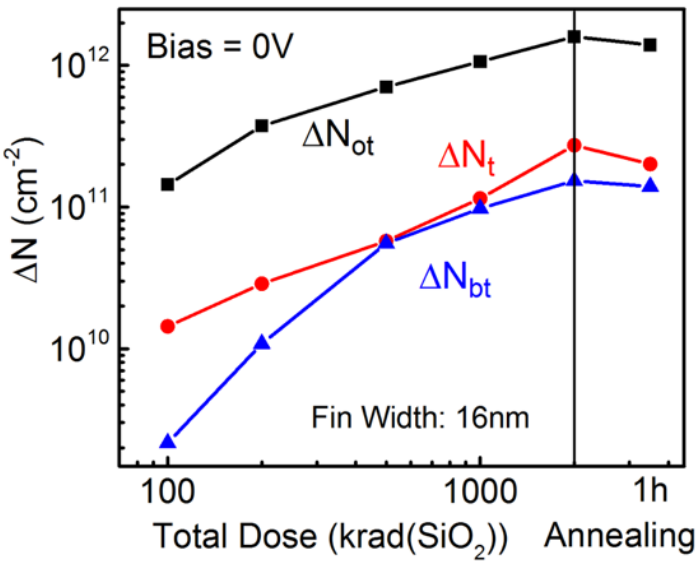


Fig. 4.13. Radiation induced charge densities as functions of dose for the devices and irradiation conditions of Fig. 4.10. The pre-irradiation border trap density is 2.36×10^{11} cm^{-2} for this device.

3. Total Ionizing Dose Effects on InGaAs Transistors

Fig. 4.14 shows initial results of irradiations of FinFET transistors on the same set of test chips as the multi-fin capacitors under (a) +1 V bias and (b) -1 V bias. Again, large radiation-induced charge trapping is observed for both positive and negative-bias irradiation. The negative shifts in the curves are evidence of significant hole trapping, and based on the above *C-f* results of Figs. 4.3-4.13, it is very likely that the large stretchout in these curves is due to a combination of interface and border traps.

The radiation-induced shifts in the transistors of Fig. 4.14 are much larger than the shifts in the capacitors in Figs. 4.3-4.13, perhaps as a result of a potentially thicker insulator near the base of the fin [6], and/or charge trapping in the STI layer of the transistors that is in proximity to the device channel [61].

Improved dielectric quality has been observed with further gate stack optimization [39],[40], reinforcing the potential of utility of InGaAs FinFETs for use in future highly-scaled MOS devices as replacements for Si *n*MOS devices. This complements the use of Ge FinFETs as replacements for Si *p*MOS devices.

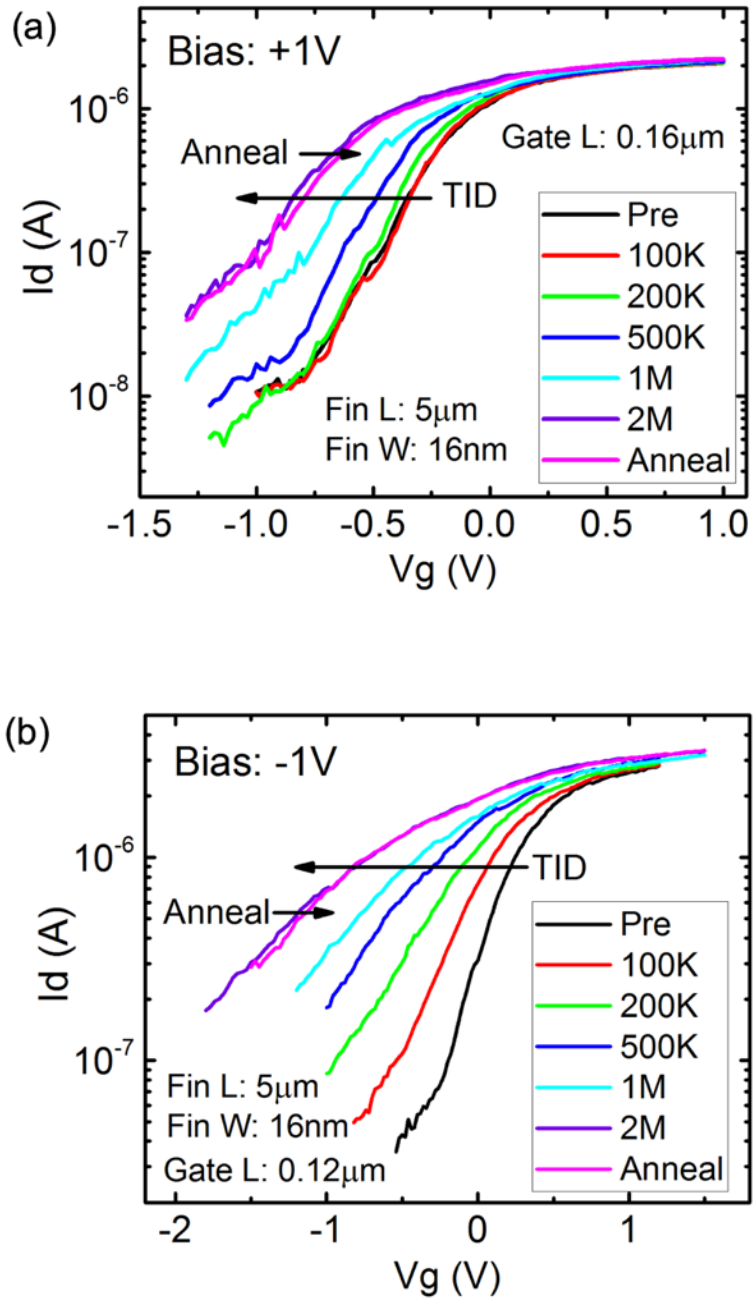


Fig. 4.14. *I-V* curves as functions of dose and room temperature annealing for transistors from the same InGaAs FinFET wafer as the capacitors of Figs. 10-13, irradiated with gate biases of (a) V_G = +1 V and (b) V_G = -1V.

CHAPTER V

CONCLUSIONS

In this thesis, simple methods have been applied and developed to combine *C-V* and *C-f* measurements to estimate radiation-induced oxide, interface, and border trap densities in MOS capacitors. The change in capacitance with frequency enables estimates of border-trap densities before and after irradiation using assumptions and analyses that are similar to ones validated in detailed studies on MOS transistors.

Then, *C-V* and *C-f* measurements have been applied to estimate radiation-induced trapped-charge densities in multi-fin Ge and InGaAs capacitors with high-K gate dielectrics. Trapped charge densities are below $2\times10^{11}/cm^2$ at doses up to 1.0 Mrad(SiO_2) for the Ge *p*MOS multi-fin devices; capacitor results are consistent with transistor results. From *C-f* measurements, we infer that as-processed border-trap charge densities in these devices are ~ $10^{11}/cm^2$.

Higher border-trap densities are found in as-processed, development-stage InGaAs capacitors. For these devices, charge trapping in transistors was greater than that observed in capacitors. These results further support the potential use of Ge *p*MOS devices in electronics for space systems, and provide useful insight for the future development of InGaAs-based FinFETs.

In summary, the radiation response of Ge *p*MOS FinFETs and InGaAs MOS FinFETs has been evaluated in detail. Capacitance-frequency (*C-f*) measurements are used to provide lower-bound estimates of border-trap densities on these devices. These results show the utility of *C-f* measurements in characterizing defect densities in MOS capacitors, particularly when large border-trap densities exist.

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