$1/f$ NOISE AND AGING EFFECTS ON MOS TRANSISTORS

By

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To my loving grandmother, Maria Danciu, an excellent electrical engineer for 40 years, a constant inspiration and role model

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CHAPTER I

INTRODUCTION

1/*f* noise of electronic devices has been a topic of interest for many decades since its discovery in vacuum tubes in 1925 [1], [2]. Experimental research and theoretical work have been the driving forces to help understand the nature and practical implications of 1/*f* noise [3], [4].

Understanding device response in different environments is extremely important for defense and space applications where technology is advancing very rapidly. It is well known that ionizing radiation exposure can greatly degrade the operation of MOS transistors [5], [6]. The main effects of ionizing radiation are reflected in threshold voltage changes, due to interface as well as oxide-induced charge. The industry focus is shifting more and more to concentrate on hardness assurance and reliability testing, in an attempt to increase performance and minimize system failure. Testing setups that involve mimicking space environments by exposing the MOS transistor to ionizing radiation are irreversibly destructive and extremely costly. In this context, being able to find non-destructive tests to evaluate MOS device response becomes a very important task [7]. In recent years, device degradation due to radiation-induced oxide charge has been correlated to device 1/*f* noise. There is evidence that defects responsible for 1/*f* noise are also responsible for radiation induced hole trapping in the oxide [7]-[12]. The defects are in the form of oxygen vacancies introduced at processing time. A phenomenon of particular interest to this work is device aging. It is very common for MOS transistors to

remain in operation for extended periods of time, when part of expensive equipment that cannot be replaced often. Understanding the expected behavior years down the road is extremely important and challenging at the same time.

Batyrev et al. [13] found the main aging agent to be water molecules for devices stored in non-hermetic environments. Rodgers et al. [14] showed that the device threshold voltage rebound during post-irradiation anneal increased compared with similar measurements in 1988, due to an increase in interface traps after irradiation and room temperature anneal. The post-irradiation threshold voltage shift due to interface traps of aged devices has been analyzed extensively with the devices being subjected to different processes prior to irradiation like baking at high temperatures and elevated temperature-humidity tests. Also responsible for threshold voltage shifts is oxide-trapped charge after irradiation, and the mechanisms responsible for it with aging have not been as well characterized.

This work focuses on trying to understand the changes, with aging, in the oxide microstructure leading to $1/f$ noise, and oxide trap buildup during irradiation by examining the data obtained for four wafers, and comparing and contrasting the results. Two of these four wafers underwent a high-temperature anneal in N_2 during processing, which is known to increase the density of oxygen vacancies and therefore the low-frequency noise, and makes them radiation soft. The other two wafers were not annealed in N_2, have an initial low defect density and are considered radiation hard. The nMOS $1/f$ noise after the 18 years of non-hermetic storage is analyzed versus temperature before and after baking, a procedure that is expected to reduce the amount of moisture that entered the oxide during the aging process. The temperature analysis uses the model

proposed by Dutta and Horn [15], which attributes the 1/*f* noise of nMOS transistors to a thermally activated process with a distribution of activation energies. We also analyze the gate voltage and drain voltage dependence of 1/*f* noise and compare it with results obtained in 1989 [10]. The results are consistent with the number fluctuation model of 1/*f* noise. Chapter II gives an overview of 1/*f* noise with a focus on the different models used to describe the noise and an explanation of what is currently known about the aging process. Chapter III describes the noise apparatus and the different parameters and procedures used during the noise measurements. Chapter IV discusses the results obtained experimentally in this study, and provides a comparison with similar results obtained for the same wafers in 1989. Chapter V is a conclusion for the work presented in chapter IV.

CHAPTER II

BACKGROUND

This chapter contains background information on low frequency noise in semiconductors and metals and describes a few models used to describe and explain the $1/f$ noise. In addition, we are also presenting the effects of aging observed so far on MOS devices.

Background on noise

Spontaneous fluctuations or noise are common phenomena for a large variety of systems. The random thermal motion of electrons in a resistor, leading to a random output signal, also known as Johnson-Nyquist noise, is a phenomenon that is well understood. The mean-square voltage fluctuation $< V^2 >$ across a resistor demonstrated experimentally by Johnson [1] and then interpreted by Nyquist [2] to be equal to:

$$< V^2 > = 4kRTB \qquad (1)$$

where k is the Boltzmann constant, R is the resistance, T is the absolute temperature and B is the bandwidth. This formula does not apply for really high frequencies, i.e. if kT is not $\gg hf$. Of particular interest to this work is the electrical noise observed in metals and semiconductor devices. Johnson-Nyquist noise, being a function of the random thermal motion of the electrons in a solid, is observed across a sample when $I_{dc} = 0$, $V_{dc} = 0$ across the sample. Under steady state conditions (I_{dc} = constant) the instantaneous voltage drop

across the sample fluctuates around its average value $<V> = V_{dc}$, and has been shown to increase above the value from Eq. (1). This noise is of two types: 1) shot noise which is due to the discrete number of charge carriers and which is dominant at low currents, and 2) $1/f$ or flicker noise which is of particular interest for this work.

The mechanisms of $1/f$ noise have been an interesting and controversial matter for over 60 years. In 1957 McWhorter proposed a model that described the $1/f$ noise of semiconductors as carrier-number fluctuations due to electrons tunneling in and out of surface states, leading to generation-recombination processes [16]. This model treats $1/f$ noise as a surface effect, with surface states being defined as electronic states with wave functions having maximum amplitudes at or near the surface. The surface states can be fast, meaning that they interact directly or via tunneling with the bulk silicon, and are located very closely to the interface (within 2.5 nm), and slow which require a very long time to interact with the underlying silicon. Two assumptions are made in the McWhorter model: 1) the traps have uniform spatial distribution through the oxide layer, and 2) the probability of an electron penetrating through the oxide decreases exponentially with the distance from the interface. The trapping time constant, τ, is then defined as:

$$\tau = \tau_0 exp(\beta x) \quad (2)$$

where τ_0 is a time constant for a trap at the interface, β is the attenuation coefficient of the electron wavefunction in the oxide, and x is the distance from the interface. For Si-SiO_2, $\beta = 10^8$ cm^{-1} [17]. The traps contributing to the $1/f$ noise are those around the Fermi level, since the states more than a few kT above the Fermi level are filled, and those more than a few kT below the Fermi level are empty. Trapping and detrapping events associated with these states affect the number of charge carriers in the channel, hence the

number-fluctuation nature of this model. Experimental data obtained in Sah et al. [18], Fu et al. [19], and Abowitz et al. [20], etc., are consistent with the surface nature of 1/*f* noise.

In 1969, Hooge introduced another model that attributed 1/*f* noise to carrier mobility fluctuations [21]-[24]. Working on gold films, he found that the noise is proportional to the sample resistance and therefore inversely proportional to the sample thickness, which indicates that 1/*f* noise is a property of the bulk material. To unify the noise model in metals with that of semiconductors, Hooge defined the fluctuations in conductance for a homogenous sample as a function of frequency as:

$$\frac{S_G}{G^2} = \frac{\gamma}{N}\frac{1}{f} \tag{3}$$

where γ is an approximate constant with an average $\gamma = 2\text{x}10^{-3}$ and N is the number of charge carriers in the sample. In the Hooge model, the mobility is affected by scattering due both to impurities and lattice, so the observed mobility, μ, can be expressed as:

$$\frac{1}{\mu} = \frac{1}{\mu_{imp}} + \frac{1}{\mu_{latt}} \tag{4}$$

Hooge and Vandamme (1978) found experimentally that if 1/*f* noise is also affected by impurity scattering phenomena. If the lattice scattering affects the noise, and the impurity scattering does not, based on eq (3), eq (4) can be generalized as:

$$\frac{S_G}{G^2} = \frac{\gamma}{N}\frac{1}{f}\left(\frac{\mu}{\mu_{latt}}\right)^2 \tag{5}$$

In this model S_G is related to S_I via:

$$\frac{S_G}{G^2} = \frac{S_I}{I^2} \tag{6}$$

and

$$N = C_{ox}(V_g - V_{th})WL/q \quad (7)$$

for the linear mode of operation where C_{ox} is the gate oxide capacitance, V_g is the gate voltage, V_{th} is the threshold voltage, W and L are the width and length of the channel, and q is the elementary charge. The drain current spectral density S_{Id} as a function of frequency can be expressed as:

$$S_{I_d} = \frac{I^2 q\gamma}{C_{ox}(V_g - V_{th})WLf} \quad (8)$$

Modern density-functional theory (DFT) calculations and modeling provide insight into defect microstructure and support the theory that $1/f$ noise is caused by the capture and emission of electrons at oxygen vacancy traps located at or near the semiconductor-oxide interface. In 1981 Dutta and Horn described the $1/f$ noise in metals as the sum of activated random processes [15], each of which, for a characteristic time τ, has a Debye-Lorentzian spectrum:

$$S(\omega) \tilde{=} \frac{\tau}{\omega^2\tau^2 + 1} \quad (9)$$

If the process is thermally activated then:

$$\tau = \tau_0 exp(E/kT) \quad (10)$$

This process was shown to lead to activation energies

$$D(E) \tilde{=} \frac{\omega}{kT} S(\omega, T) \quad (11)$$

for $D(E)$ varying slowly over any range $\sim kT$. Defining the frequency exponent α locally as:

$$\alpha = -\frac{\partial lnS_{vd}}{\partial ln\omega} \quad (12)$$

the frequency and temperature dependence of α becomes:

$$\alpha(\omega, T) = 1 - \frac{1}{ln(\omega\tau_0)}(\frac{\partial lnS(\omega, T)}{\partial lnT} - 1) \tag{13}$$

In 2002 Xiong [25] has found that eq (13) is valid for lot G1916A, wafer 33 nMOS transistors fabricated at Sandia National Laboratory in 1984, devices that are particular interest for our work.

In 1990 Hung et al. [26] proposed a unified 1/*f* noise model that includes the effects of correlated mobility and number fluctuations. Flicker noise is attributed to charge fluctuations in the oxide traps, with mobility fluctuations attributed to Coulombic scattering. The resulting mobility fluctuations are not the same as those envisioned in the Hooge model, and the effects of changes in carrier number as a result of trapping and detrapping events tend to have a more significant effect on the measured noise than do the changes in carrier mobility, depending on whether a scattering center is charged or uncharged.

1/*f* noise relies entirely on whether traps with specific energies and locations are available in the SiO_2 so they can exchange charge with the Si. It has been demonstrated that these traps are oxygen vacancies that lead to three types of configurations in amorphous SiO_2 [27], [28]. In 1987 Rudra and Fowler [29] showed that in the neutral state the two silicon atoms left with dangling bonds due to the absence of an oxygen atom bond together forming a dimer defect. This type of center is now known as an E'_δ. Work by Lu et al., in 2002 [30] has showed that 90% of the oxygen vacancy sites form E'_δ dimer configurations shown in Figure 1 (a), with 5% forming the 4-fold puckered

configurations $E'_{\gamma 4}$ of Figure 1 (b) and 5% forming the 5-fold puckered configurations $E'_{\gamma 4}$ of Figure 1 (c). Puckered configurations $E'_{\gamma 4}$ happen when one of the Si atoms relaxes past the plane of its three oxygens and bonds with a nearby oxygen and forms a dipole upon hole capture. $E'_{\gamma 5}$ is very similar to $E'_{\gamma 4}$ in the sense that the oxygen relaxes back past the plane of its oxygens but the Si atom bonds with another oxygen and another Si and does not form a dipole upon hole capture. Bond angles and atomic spacing determine whether a Si is spatially located close enough to form the $E'_{\gamma 5}$ configuration.

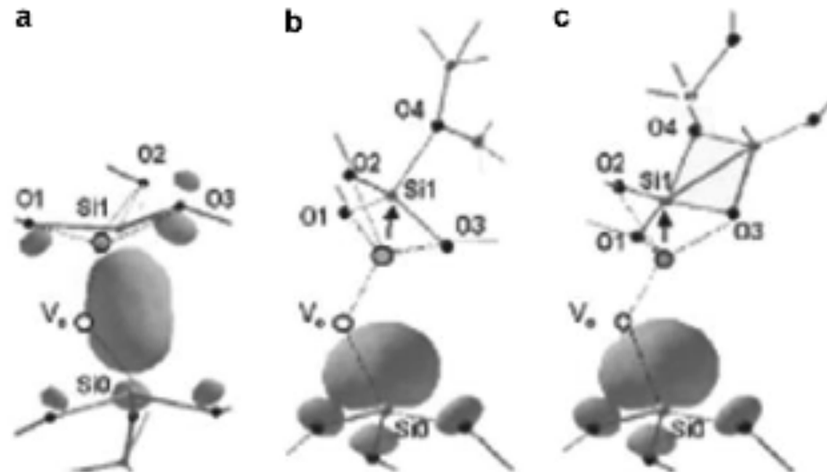

Figure 1: Schematic diagrams of the atomic positions and electronic densities of (a) ''dimer,'' (b) ''four- fold puckered,'' and (c) ''fivefold puckered'' oxygen vacancies. After [30].

In an irradiated nMOS transistor one of the potential sources for 1/*f* noise is the charge exchange with $E'_{\gamma 4}$ centers. Another potential source is the conversion of $E'_{\gamma 4}$ centers to $E'_{\gamma 5}$ centers due to thermal energy that makes the atoms stretch and rotate. Another possibility is that 1/*f* noise is caused by electron capture and emission from a stretched dimer. Since a dimer with equilibrium spacing (bond length 0.25-0.30 nm) does

not have any available states for an electron, the entity responsible for this process would have to be a dimer with a stretched Si-Si bond (bond length 0.35-0.40 nm) where midgap states start to open up with increased bond length [31]. After the electron is captured the Si-Si bond length decreases leading to an energy increase and electron re-emission.

Background on aging

Aging is extremely important for devices that must remain in operation for decades. In non-hermetic environments, exposure to moisture and hydrogenous species over long periods of time contributes to the aging effects observed in MOS transistors.

Work by Batyrev et al. [13], [32] and Bakos et al. [33], [34] has shown that water molecules interact with the SiO_2 via two mechanisms. First, if water molecules are present, via diffusion, in the vicinity of an oxygen vacancy center, they are attracted to the vacancy. Upon the reaction, the oxygen molecule fills in the oxygen vacancy, and the H_2 left over remains as an interstitial molecule in the oxide. The second mechanism involves “dangling oxygens”, oxygens sharing a bond with a silicon and having a dangling bond. One hydrogen atom in water passivates this dangling bond, leading to a silanol, while the remaining silanol attaches to a neighbor silicon as a fifth bond. The hydrogen can then be released as a proton during the hole transport that occurs during irradiation. The H+ then migrates to the interface under positive bias where it reacts with Si-H bonds to form interface trapped charge [35].

In 2005 Rodgers et al. [14] observed an elevated threshold voltage rebound during post-irradiation anneal. This phenomenon is explained by an interface trap buildup during

non-hermetic storage. Baking these parts before irradiation, a process that is expected to reduce the reduce the amount of moisture, also reduced the threshold voltage shifts. This clearly indicates that water absorption during non-hermetic storage for long periods of time can lead to changes in transistor response observed with aging.

CHAPTER III

EXPERIMENTAL DETAILS AND MEASUREMENT TECHNIQUES

Devices

For the experiments performed, n-channel MOS devices 3 μm long and 16 μm wide were used. The transistors were fabricated in the same lot (G1916A) at Sandia National Labs using the 4/3 μm "old baseline processing" technique. The transistors came from four different wafers: W10, W22, W33 and W44, with multiple chips from each wafer being analyzed. The choice of devices is consistent with the devices used by Scofield et al. in 1989 [10]. The substrate doping for all NMOS devices used was 2.7 x 10^{15} cm^{-3}. The transistors from different wafers vary in oxide thickness (32 nm for W10 and W22, 48 nm for W33 and 60 nm for W44), and oxidation and annealing conditions. The devices from wafers 10 and 33 underwent a 30 minute anneal at 1100 ºC in a relatively inert ambient (N_2), process known to introduce high oxygen vacancies and strained Si-Si bonds in the oxide and make the oxide radiation "soft". All chips used in these experiments were set in ceramic 24 pin ceramic dip packages and were stored for 18 years before being analyzed.

Measurements

Threshold voltage measurements

The threshold voltage measurements were performed with a HP 4156A parameter analyzer computer controlled via an IEEE-488 general purpose instrument bus (GPIB) interface. The gate was swept from subthreshold to inversion while a constant 100 mV voltage was applied to the drain. A plot of the measured drain current I_d versus the measured gate voltage V_g was generated, and the threshold voltage was extracted from the linear region - the x-axis intercept right when the device begins conducting. A typical I-V curve is presented in figure 2 below.

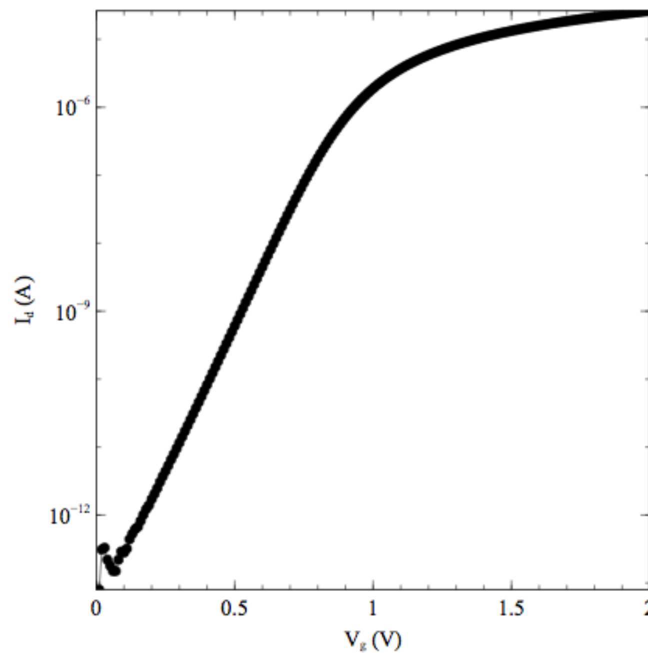

Figure 2: Typical nMOS drain current versus gate voltage for a wafer 33 transistor. The threshold voltage for this device, $V_{th} = 1$ *V.*

Noise measurements

Excess noise measurements were performed on a few devices from each of the four wafers under constant bias conditions. The experimental setup is presented in the figure 3 below.

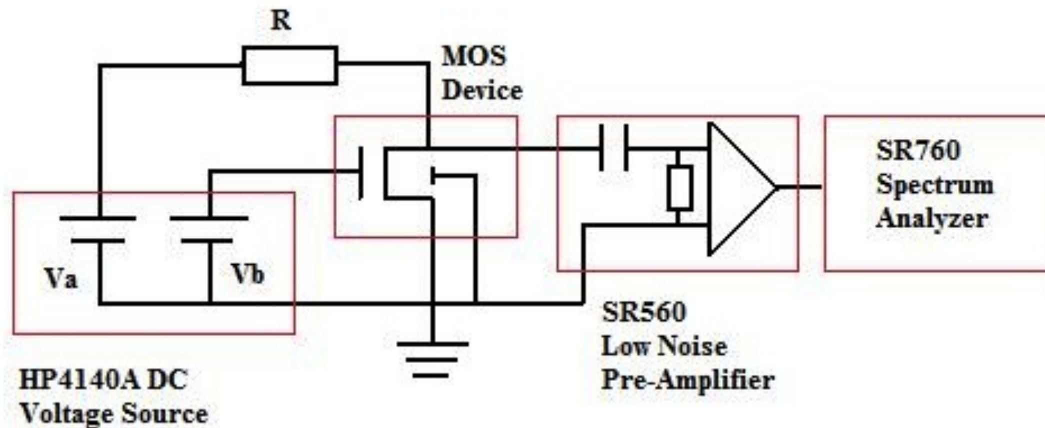

Figure 3: Schematic diagram of the noise measurement circuit

The devices were operated in their linear regimes with the source and the substrate grounded. The drain was connected to a HP4140A dc voltage source via a ballast resistor (R = 20 kΩ) which insured a constant drain current of 100 mV. A dc voltage, also supplied by the HP4140A dc voltage source was applied to the gate. The gate voltage was set such that V_g-V_{th} = 1 V for the majority of the experiments. Data were also collected for a variable V_g (e.g., with V_g increased in 0.2 V increments ranging from V_{th} + 0.5 V to V_{th} + 2.5 V). The fluctuations in the drain voltage were passed through a Stanford Research (SR) model 560 low-noise preamplifier operated in low-noise mode battery mode and allowed frequency ranges of [0.3 Hz – 1 kHz]. The pre-amplification

gain was set to 100 and was numerically accounted for in the results. The pre-amplifier output was connected to a SR760 FFT spectrum analyzer. The drain voltage noise spectra were measured for frequencies in the [0, 780 Hz] range, and 2000 consecutive measurements were taken and averaged via the root mean square (RMS) method, resulting in data with good precision. Figure 4 below shows an example of a noise curve at different sampling rates.

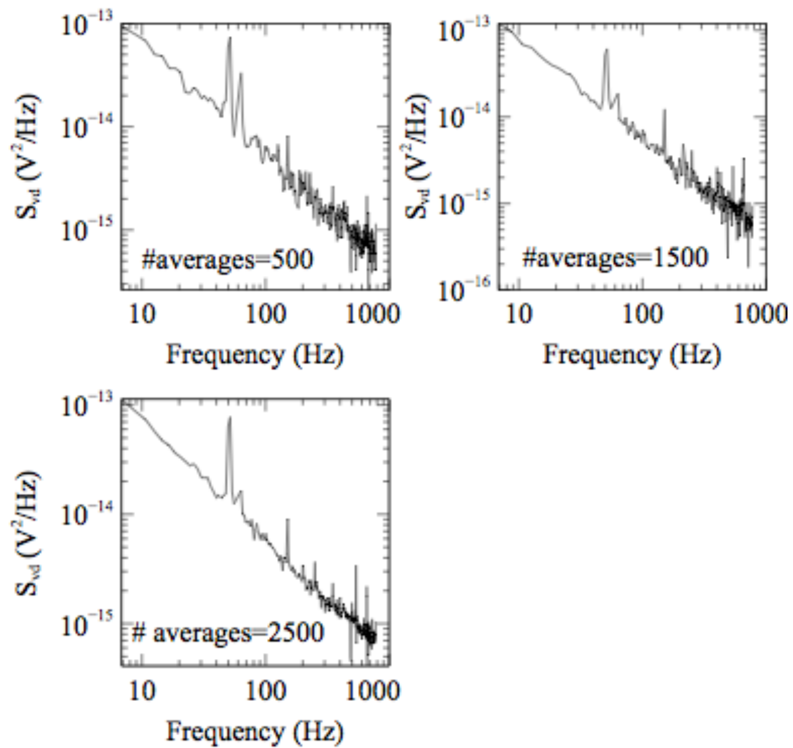

Figure 4: Noise power spectral density for nMOS transistors measured at different sampling rates.

The curve obtained with the most averages (2500) is much more precise and much less “noisier” then the curve obtained with the least averages (500). Finding just the right

sampling rate is very important for obtaining accurate noise data, while leveraging the increase in measurement time incurred due to an increasing sampling rate.

The nMOS transistor under test was enclosed in a metal testing box. The voltage source, pre-amplifier and spectrum analyzer were controlled by a personal computer via a GPIB card. For each device two sets of measurements were performed. First, a background noise measurement was done with the transistor biased at 0 V. The zero-bias noise is always present and is due to three causes: 1) Johnson-Nyquist noise, the random thermal motion of the carriers in the channel, which is the dominant type at high frequencies, 2) pre-amplifier noise that could not be corrected otherwise (operating the pre-amp on battery and the low-noise setting) which is dominant at low frequencies, and 3) pickup from power lines, observed at 60 Hz and harmonics, which is ignored in the analysis. In a second measurement the foreground noise was measured with the non-zero bias specified above. The background noise was then subtracted from the foreground noise, leading to the excess noise spectrum $S_{vd}(f)$. Figure 5 below shows an example of a noise curve with the background and foreground noise represented on the same graph. The decreasing slope of the background noise is due to the preamplifier noise, which, as mentioned above, is greater at low frequencies.

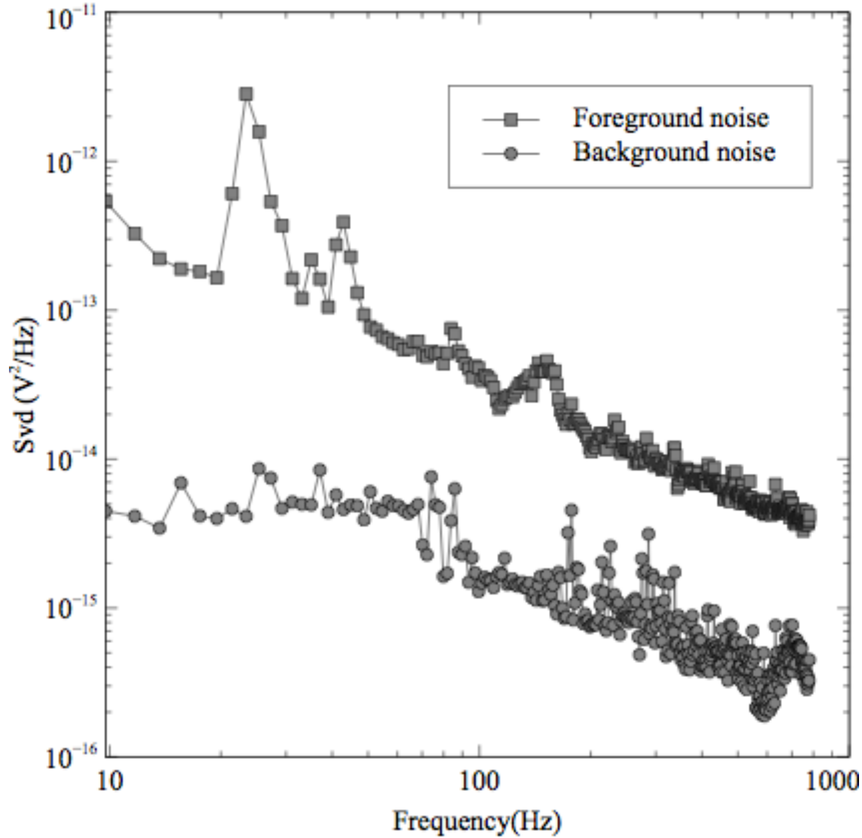

Figure 5: Noise power spectral density for an n-channel transistor with both the background and foreground noise represented.

Temperature dependent noise measurements

A set of noise measurements was performed at temperatures in the [85 K, 300 K] range. The same setup described previously was used except that the nMOS device being tested was introduced in a cryostat. The temperature was adjusted by using a computer connected to a temperature controller. Liquid nitrogen was used for cooling the cryostat chamber to cryogenic temperatures.

Baking treatments

Several devices from wafer 10 were subjected to preirradiation elevated temperature stress (PETS) to reduce the amount of moisture accumulated during the aging process. The chips were baked in a DELTA 9039 temperature chamber, with all the pins grounded for ~16 hours (overnight) at 200 ºC.

CHAPTER IV

AGING EFFECTS ON MOS LOW FREQUENCY NOISE

This section contains experimental noise data on n-channel devices from lot G1916A wafers 10, 22, 33 and 44 and describes the aging effects on the 1/*f* noise response and MOS characteristics.

1/*f* noise measurements and moisture exposure

Variation with drain voltage

The output drain voltage noise, S_{vd} is a measure of the trap distribution is space and energy along the channel. The drain voltage noise, S_{vd} varies proportional with V_d^2 and is due to fluctuations in the channel resistance. Figures 6 and 7 below compare the drain voltage noise of a device from wafer 10 in 2007 with that of a device from the wafer 10 measured in 1989 [10]. The measurements were done under the same conditions: room temperature and V_g fixed at 4 V. The noise in 1989 is more than twice that of the same type of device in 2007.

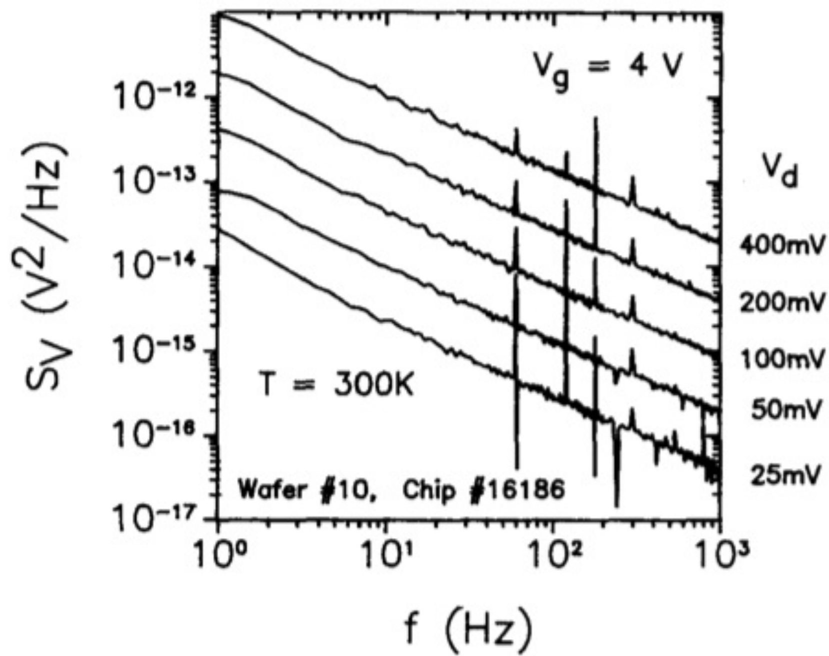

Figure 6: Noise power spectral density for a wafer #10 n-channel transistor at a fixed V_g=4 V and several values of V_d measured in 1989. After [10].

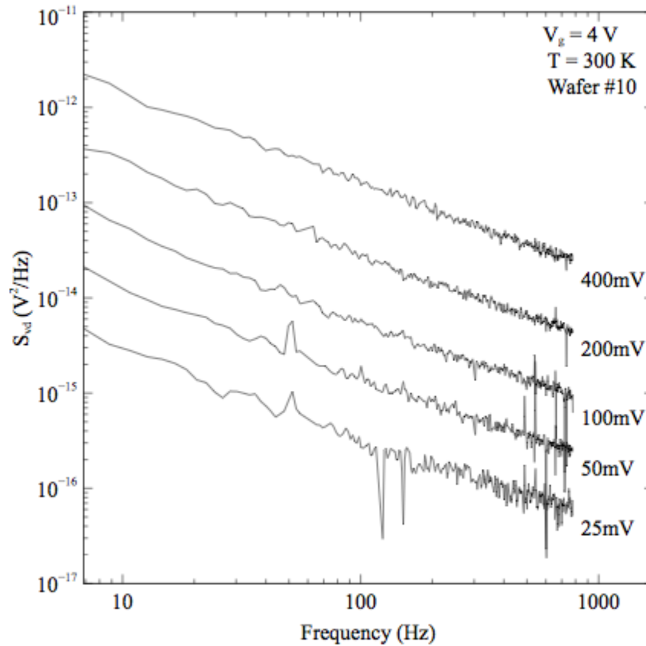

Figure 7: Noise power spectral density for a wafer #10 n-channel transistor at a fixed V_g=4 V for several values of V_d measured in 2007.

Variation with processing

Noise experiments were performed at room temperature for the nMOS devices from Sandia lot G1916A wafers 10 (4 parts), 22 (2 parts), 33 (3 parts) and 44 (3 parts). For simplicity, the gate voltage was kept at V_{th} + 1 V and the drain voltage was kept constant at 100 mV. The results presented below are for the 3 x 16 μm nMOS transistors in the four wafers, for consistency with previously reported data on these parts. The 3 micron nMOS transistor was chosen out of the 3 nMOS transistors on the part because is located in the middle of the package, so less variation is expected due to packaging and handling. The resulting drain voltage noise spectra, S_{vd}, as a function of frequency for the four wafers are presented in Figures 8-11 below, along with a comparison to the noise levels as measured in 1989 [10].

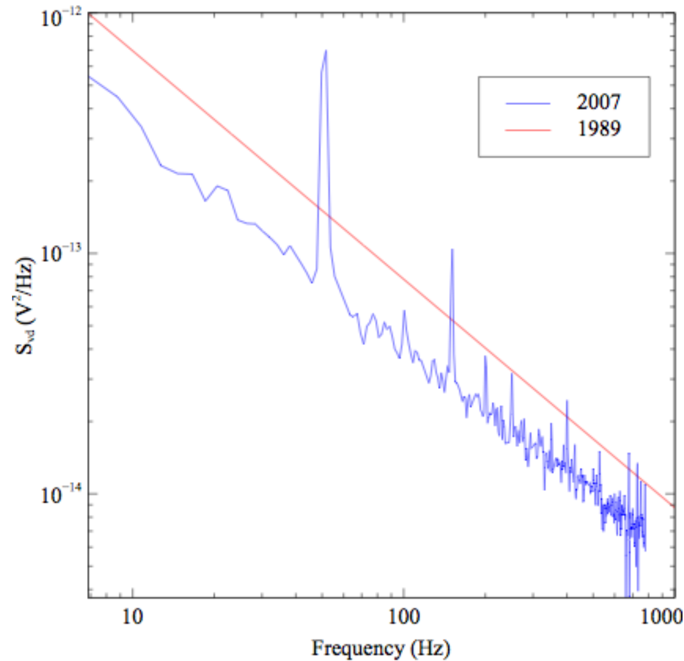

Figure 8: Noise power spectral density for a wafer #10 n-channel transistor. The straight red line represents the measured noise in 1989.

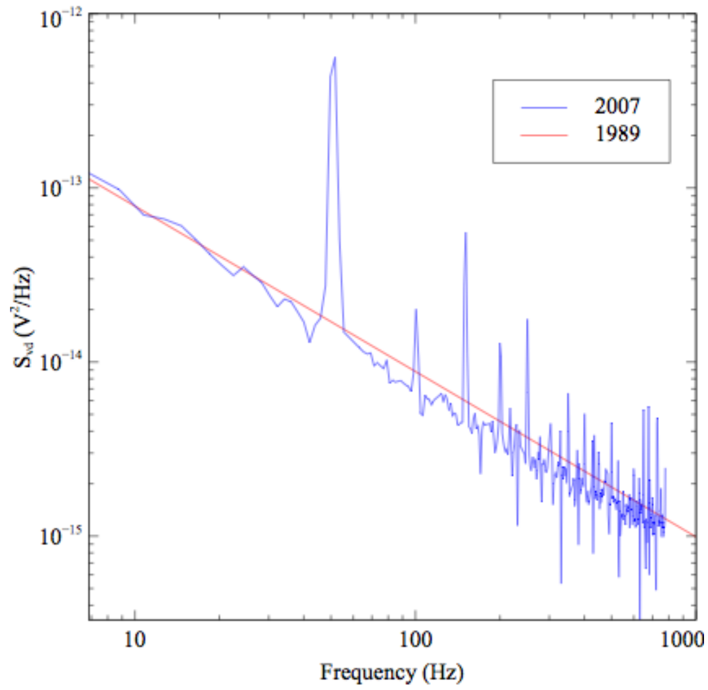

Figure 9: Noise power spectral density for a wafer #22 n-channel transistor. The straight red line represents the measured noise in 1989.

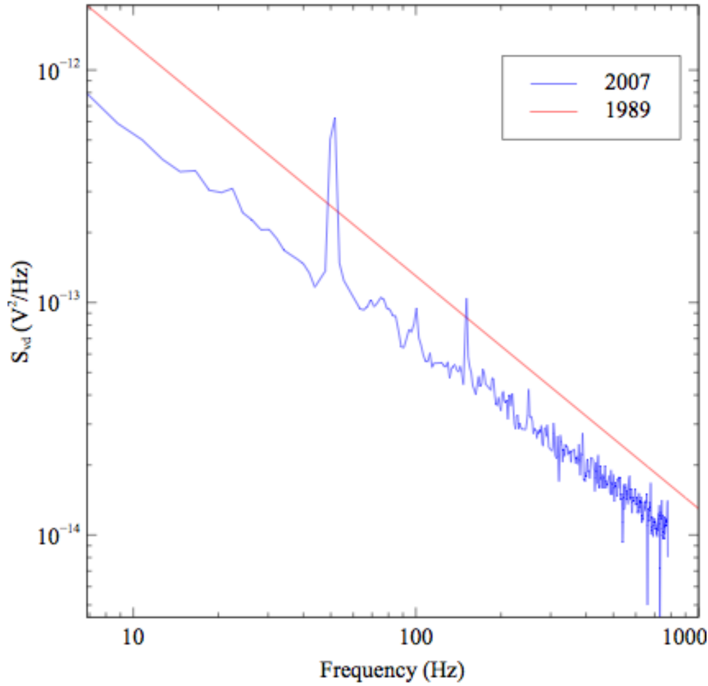

Figure 10: Noise power spectral density for a wafer #33 n-channel transistor. The straight red line represents the measured noise in 1989.

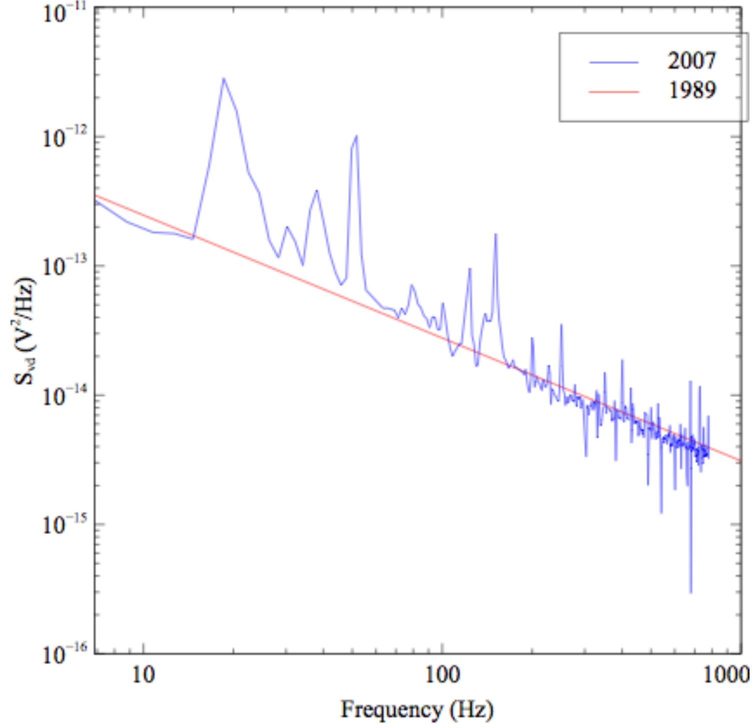

Figure 11: Noise power spectral density for a wafer #44 n-channel transistor. The straight red line represents the measured noise in 1989.

The noise levels vary greatly across these transistor types. To understand changes in device microstructure with aging, it is important to compare the 1/*f* noise of these devices to results obtained via similar analysis in 1989 [10]. To help compare the devices tested under different voltage conditions, we use the normalized noise magnitude, *K,* defined *as:*

$$K = S_{vd} \frac{f^{\alpha}(V_g - V_{th})^2}{V_d^2} \quad (14)$$

where S_{vd} is the voltage noise power density, V_g is the gate voltage, V_{th} is the threshold voltage and V_d is the drain voltage; alpha, the frequency exponent is close to unity 0.85≤ alpha ≤ 1.02, indicative of relatively constant defect densities as a function of energy. To get a better sense of the change in device response over time, we compared our data to

the normalized noise magnitudes measured in 1989 [10]. The resulting average K values in 10^{-10} V^2 for the four wafer types are presented in Figure 12 below and were 2.8±0.1 V^2 for wafer 10, 0.42±0.06 V^2 for wafer 22, and 4±1 V^2 for wafer 33 and 1.8±1 V^2 for wafer 44.

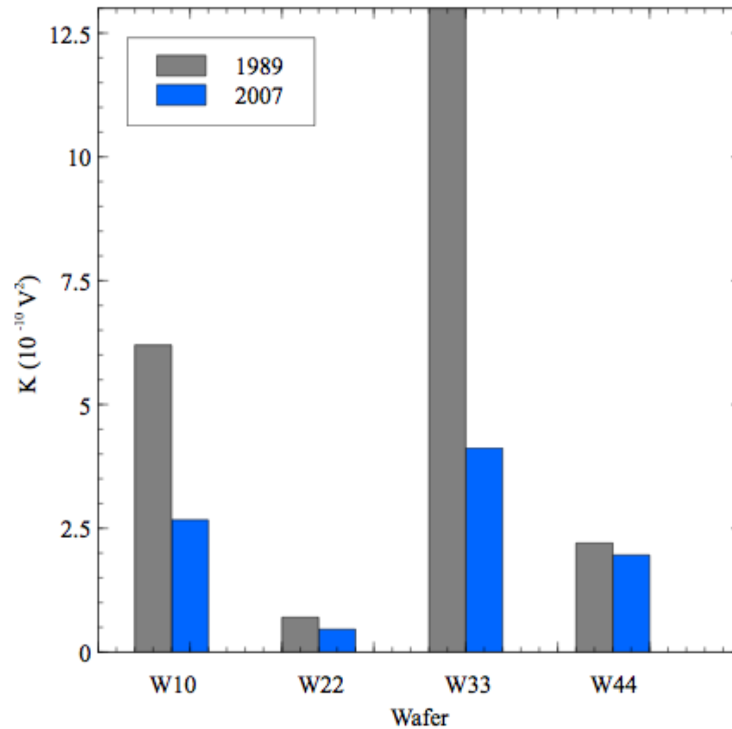

Figure 12: Comparative plot of the normalized noise level, K, in 1989 and 2007 for four wafer types.

Both wafers annealed in N_2 (10 & 33) show a decrease of more than 50% in their noise levels compared to 1989. Also important to note is the fact that the noise levels for the transistors annealed in N_2 were significantly higher than those not being annealed in N_2. The high temperature anneal in N_2 is known to increase the O_2 vacancies near the Si-SiO_2 interface region which have been known to be responsible for $1/f$ noise [36]. The

number fluctuation model can be used to give a rough estimate of the number of border traps responsible for the noise. This model assumes that trapping and detrapping events are the leading cause for noise, and carrier mobility fluctuations due to changes in trap occupancy have a negligible effect. A uniform trap energy and location distribution near the Si-SiO_2 interface is another assumption for this model. Even though this model provides a somewhat oversimplified explanation of the noise, it is consistent with a broad range of experimental data, especially for nMOS transistors. If the noise is due to charge moving in and out of border traps, the effective density of border traps N_{bt} that are responsible for the noise can be defined as [11], [16], [37]-[39]:

$$N_{bt} \tilde{=} LW(\epsilon_{ox})^2 ln(\tau_1/\tau_0)(qkT)^{-1}(t_{ox})^{-2}K \qquad (15)$$

where L is the gate length, W is the gate width, ε_{ox} is the oxide dielectric constant, τ_1/τ_2 are the “cutoff” times for the fluctuation process, q is the elementary charge, k is the Boltzmann constant, T is the temperature, t_{ox} is the oxide thickness, and K is the normalized noise magnitude.

For the devices that received the N_2 anneal, N_{bt} ~1.5 x 10^{11} (2007) and N_{bt} ~ 6.5 x 10^{11} (1989) for wafer 10, N_{bt} ~ 1.5 x 10^{11} (2007) and N_{bt} ~ 4.5 x 10^{11} (1989) for wafer 33. The border trap density is consistent between the two wafers and most importantly the decrease of border trap density with aging is also consistent between the two wafers. In the case of the wafers that were not annealed in N_2, N_{bt} ~ 1.6 x 10^{10} (1989) and N_{bt} ~ 1 x 10^{10} (2007) for wafer 22, and N_{bt} ~ 1.5 x 10^{10} (1989) and N_{bt} ~ 1 x 10^{10} (2007) for wafer 44. These results clearly indicate that, for the devices that had high trap

densities to begin with, this was dramatically reduced with aging, whereas the devices that had small trap densities initially experienced a small reduction in their trap densities.

One potential explanation for these changes can be found through density functional theory calculations. An equilibrium dimer has Si-Si bond lengths of 0.25-0.3 nm, but in the vicinity of the interface it is possible to find stretched Si-Si dimers with bonds lengths of 0.35-0.4 nm [31]. These defects are energetically prone to capturing an electron from the underlying Si under the right bias conditions. This is schematically shown in Figure 13 below.

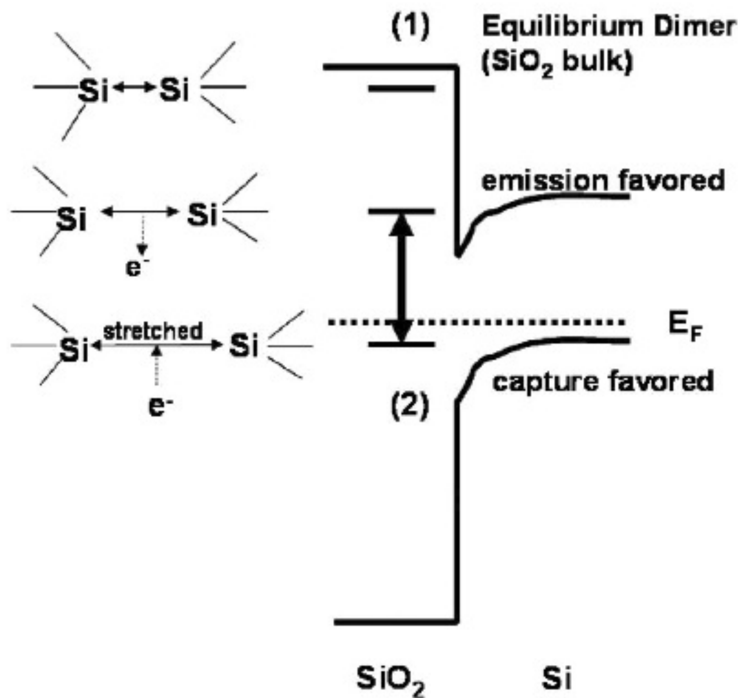

Figure 13: Schematic diagram of the energy levels of dimer O vacancies in bulk SiO_2 with equilibrium Si–Si bond spacing of 0.25–0.30 nm (1) and near-interface dimer defects with stretched Si–Si bond spacing of 0.35–0.40 nm (2). After [40].

Once an electron is captured the energy of the complex increases, the bond length decreases, and the electron is reemitted. This is a very plausible explanation for the $1/f$ noise observed in these devices. For all devices, with aging, the number of defect sites with stretched Si-Si bonds has been reduced, leading to more of the defects reaching energies more than a few kT above the device Fermi levels and therefore no longer contributing to the $1/f$ noise for the respective devices.

To understand some of the other processes and defect microstructures, it is important to also look at the threshold voltage changes with aging. The results are presented in Figure 14 below.

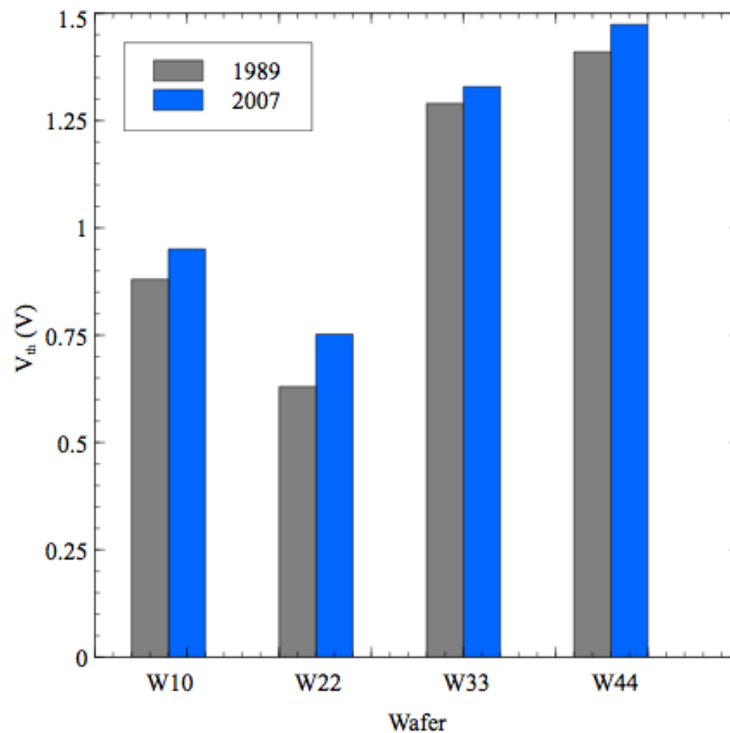

Figure 14: Comparative plot of the threshold voltage in 1989 and 2007 for the four wafer types.

A comparable increase in threshold voltage is present for all wafers. The discrepancies between the 1/*f* noise and the V_{th} results are easily explained by the fact that either that similar increases do not occur as a result of similar reactions of hydrogen in the near-interfacial SiO_2, or perhaps more likely, that the increase in effective border-trap density due to the interactions of hydrogenous species in these devices is approximately offset by the relaxation of strained Si–Si bonds in the near-interfacial SiO_2 for wafers 22 and 44 (no postoxidation anneal), or contributes much less significantly to the change in noise than the Si–Si strained bond relaxation for wafers 10 and 33 (with a post-oxidation anneal). The increase in the threshold voltage is consistent with previous studies [14], [40]-[42]. It is energetically favorable for hydrogenous species like water to enter amorphous SiO_2 and form two silanol groups, with substantial energy barriers of 1.2 - 1.5 eV. This process takes a long time at room temperature, which is the case for this aging study.

Variation with PETS

Unbiased bakes have been found to help determine whether the species responsible for trap passivation with aging can be removed, thereby restoring the device initial response. In 1994 Shaneyfelt et al. [43] analyzed the radiation response of burned-in MOS devices and found that, within experimental error, the oxide-trapped charge is not affected by pre-irradiation elevated temperature stress. In 2002, the aging experiments performed by Karmarkar et al. [44] on poly-Si-gate capacitors found similar results: no significant differences were observed between the charge trapping after

irradiation for the baked devices compared to the devices that did not undergo unbiased bakes prior to irradiation. Our work confirms this hypothesis. The results are presented in Fig. 15-16 below.

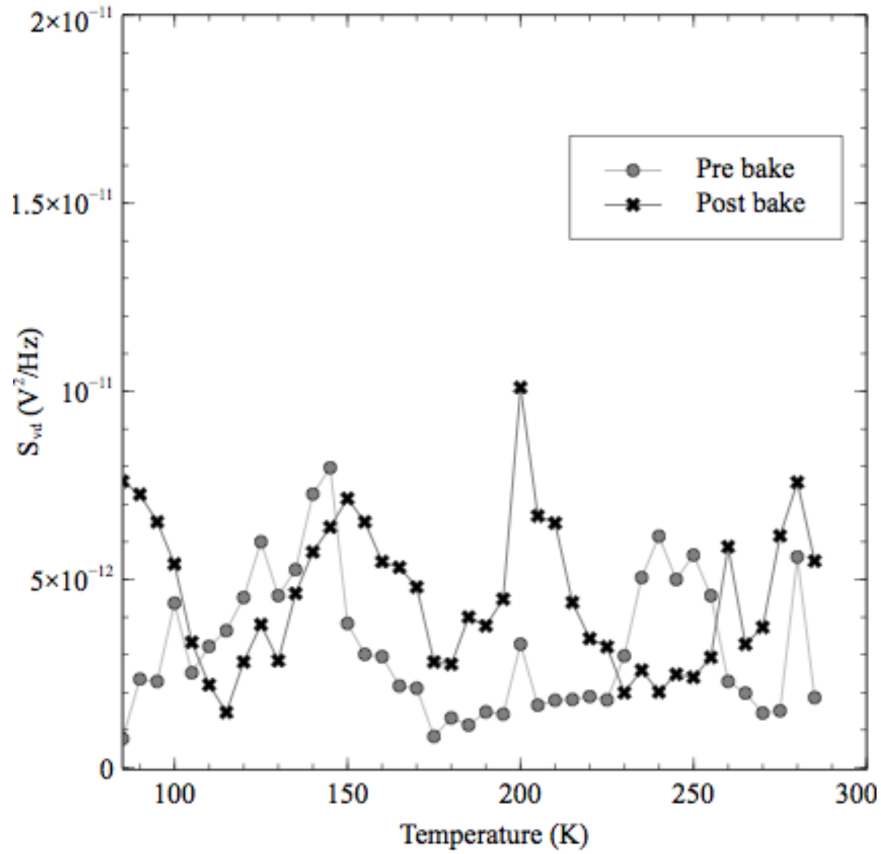

Figure 15: Noise magnitude at 1 Hz versus temperature for a wafer #10, 3x16 μm^2 n-channel transistor before and after a 200 ºC, 16 hour unbiased bake.

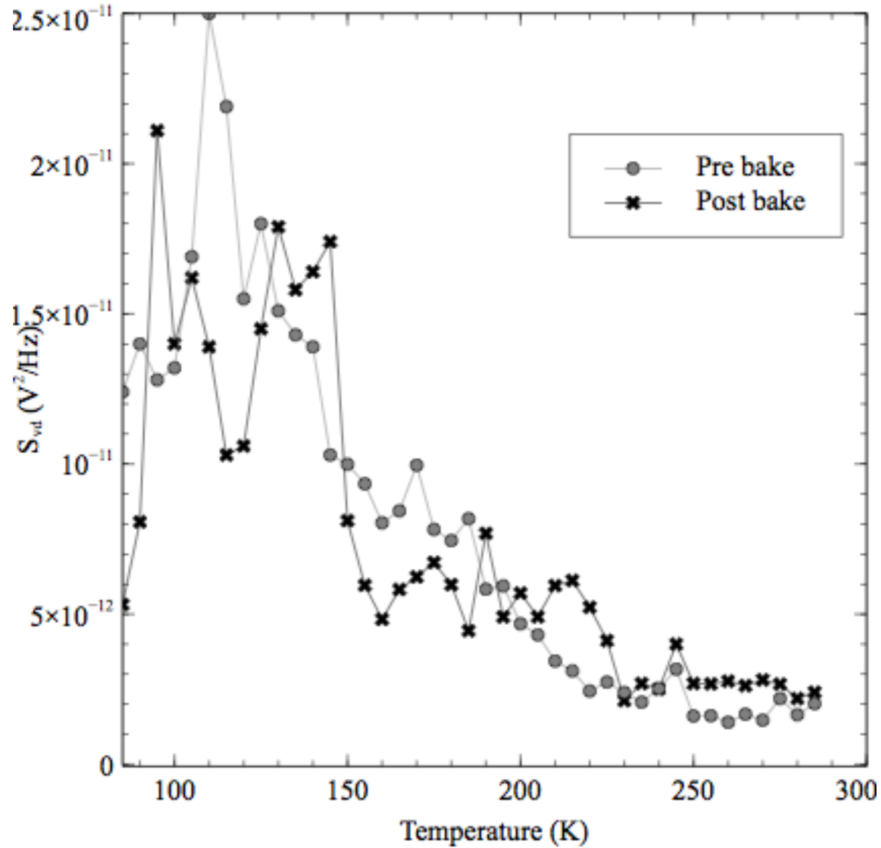

Figure 16: Noise magnitude at 1 Hz versus temperature for a wafer #10, 4x16 μm^2 n-channel transistor before and after a 200 ºC, 16 hour unbiased bake.

The noise levels after the unbiased bake are similar to the ones before the bake. The shape of the noise-temperature curves after PETS are however different, which translates to changes in defect densities and energy after the high temperature stress [45]. The very large peaks at low temperatures are not present in the 3 micron device. These peaks appear to be related to a defect that is present in the 4 micron device, but not in the 3 micron device, thus illustrating device-to-device variation in defect densities and energies. The noise due to this defect changes somewhat with baking, but not in a systematic fashion. The gate pin for this package is at the end of the package (pin 13 of a 24 pin dip), as compared to pin 17 for the 3 micron transistor (in the middle of the

package), so it is possible that this difference could have occurred at some point in packaging or handling over the years. More interestingly for our aging study, in both Figures 15 and 16, there appears to be a noise peak near 200 K (~ 0.6 eV) in each device that changes the same way (increases with baking). Interestingly, the noise levels are similar at room temperature, which would suggest comparable defect densities. At very low temperatures, however, the noise in the 4 micron device greatly exceeds that of the 3 micron device. The notion that devices with similar noise levels at room temperatures can experience significant differences at low temperatures is particularly important for devices operating in cryogenic environments. Xiong et al. [25] have hypothesized that at low temperatures it is possible for both border and interface traps to be responsible for the noise. The lower temperatures slow down the charge carrier movement in and out of interface traps.

The frequency dependence of the noise (α) corresponding to the noise spectral densities is presented in Figures 17 and 18 below.

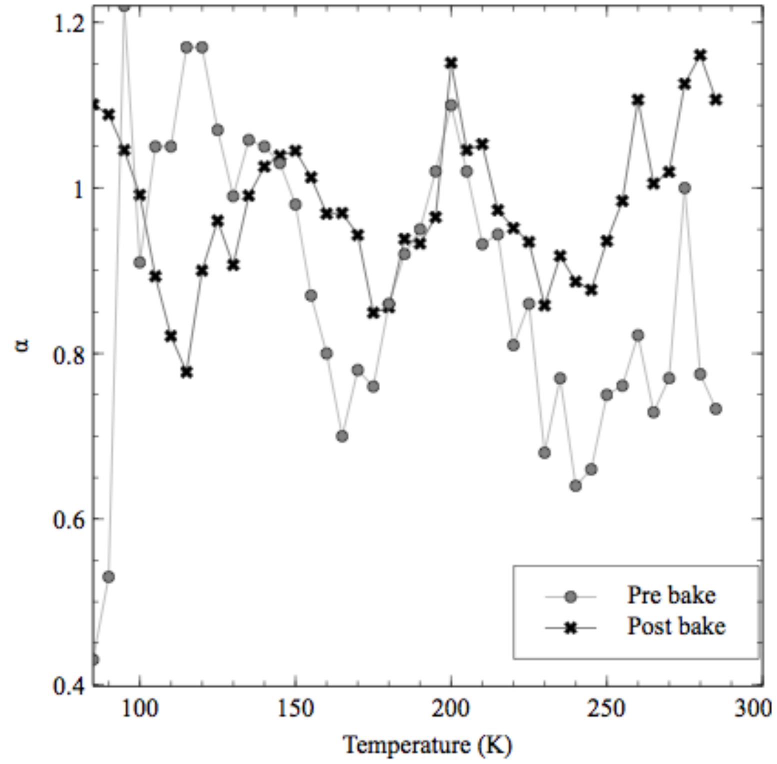

Figure 17: Frequency exponent α versus temperature for a wafer #10, 3x16 μm² n-channel transistor before and after a 200 ºC, 16 hour unbiased bake.

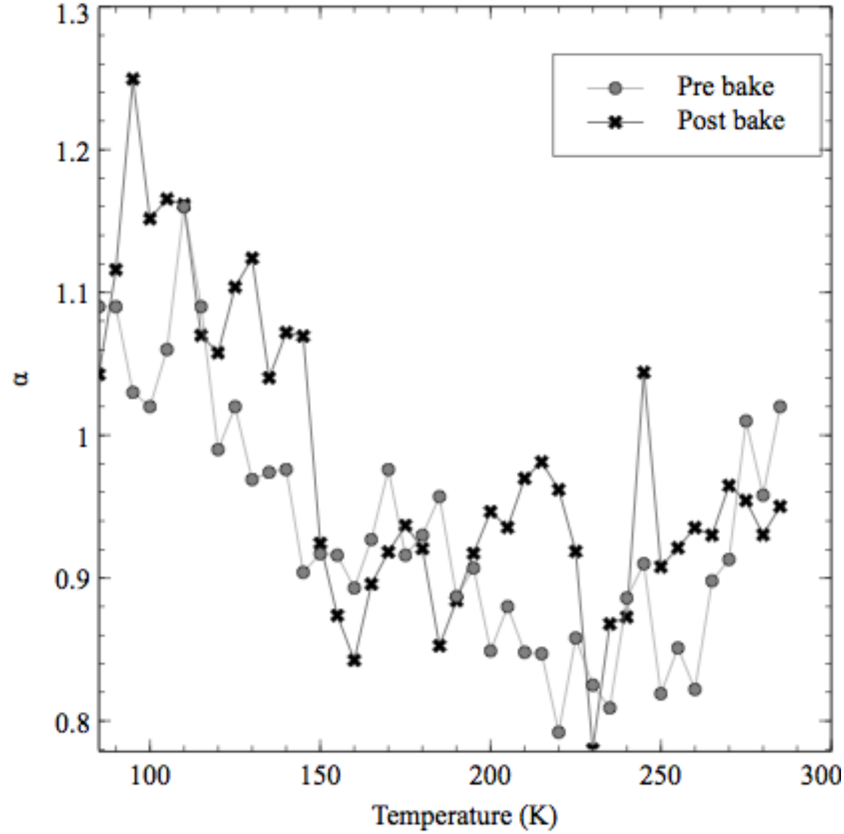

Figure 18: Frequency exponent α versus temperature for a wafer #10, 4x16 μm² n-channel transistor before and after a 200 ºC, 16 hour unbiased bake.

There is a direct correlation between the local peaks observed in the α curves and the increasing slope of the S_{vd} curves. For example, the peaks at 200 K for the 3 and 4 micron transistors correlate with the steep slope of the S_{vd} of the respective devices. The post bake slope increased observed in the 3 micron device at around 150 K translates to a peak in the α for the same device. To further this discussion, and see if the noise can be accurately predicted by the Dutta-Horn model, we used (13) to compute $\alpha(T)$ from the noise data shown in Figure 16. The resulting curves are presented in Figures 19-20 below.

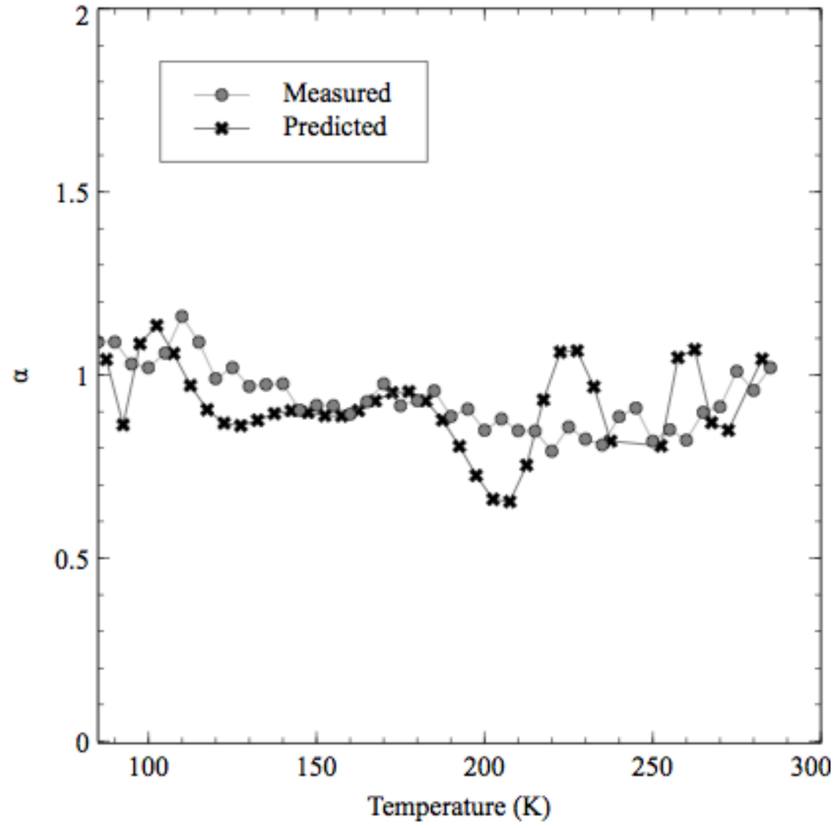

Figure 19: Frequency exponent α versus temperature measured and predicted for a wafer #10, 4x16 μm² n-channel transistor before a 200 ºC, 16 hour unbiased bake.

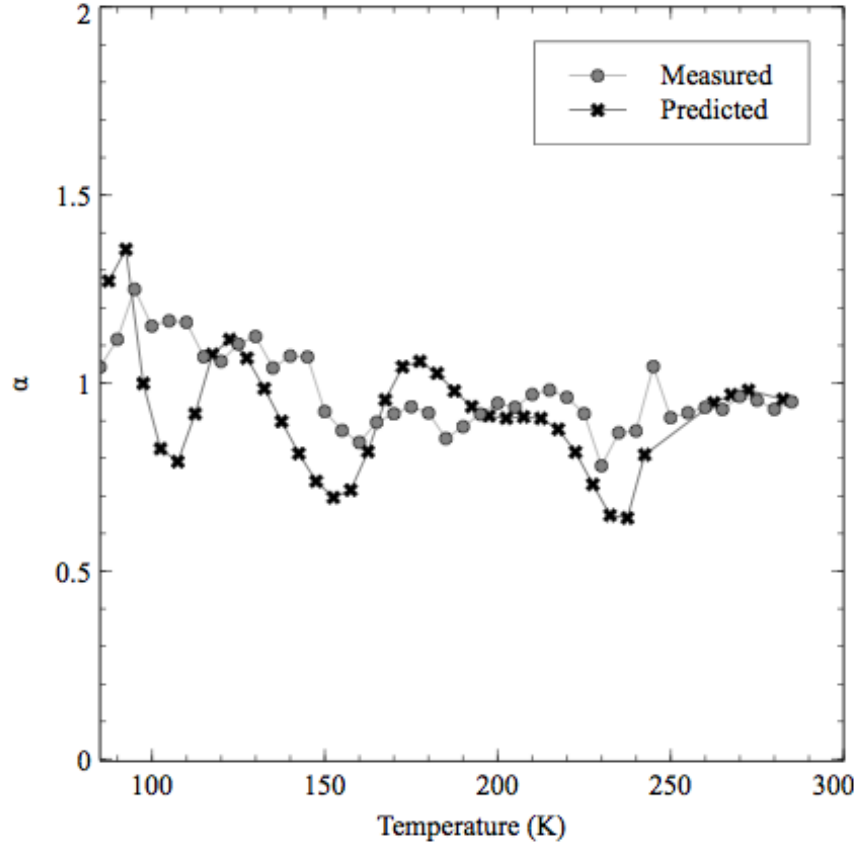

Figure 20: Frequency exponent α versus temperature measured and predicted for a wafer #10, 4x16 μm² n-channel transistor after a 200 ºC, 16 hour unbiased bake.

The predicted $\alpha(T)$ curves describe the measured α fairly well in terms of both shape and overall level. These results are typical of Dutta-Horn thermally activated processes and would not have been observed if the $1/f$ noise of these devices was due only to simple tunneling mechanisms.

Changes in defect energy distributions as those seen in these devices are indicative of changes in the atomic structure like bond length and atomic location. Changing from one defect type to another usually requires higher energies than atomic interactions within the same defect. The results presented above in Figures 15-18 strongly

suggest that aging and unbiased baking contribute to changes in defect energy distributions consistent with relaxations in strained bonds in the near-interfacial layer.

Variation with gate voltage

In MOS transistors, the gate potential determines the Fermi level of the device and therefore the traps contributing to noise and the hole density in the channel. Scofield et al., [46] have shown that important insights can be found by varying the gate voltage and temperature. They attributed the difference in gate voltage dependencies, for nMOS $S_{vd} \sim (V_g - V_{th})^{-2}$ whereas for pMOS $S_{vd} \sim (V_g - V_{th})^{-1}$ to the trap density remaining constant for nMOS and varying for pMOS with a variable V_g. For nMOS this is due to the energy of the electron traps contributing to the noise for nMOS transistors operating in strong inversion being close to the conduction band. In 2010 Francis et al. [47] found different gate voltages dependences of S_{vd} with moisture exposure and total dose radiation. $S_{vd} \sim (V_g - V_{th})^{-1.7}$ for nMOS devices from wafer #10 exposed to aging prior to irradiation. For the wafer #10 nMOS transistors exposed to moisture $S_{vd} \sim (V_g - V_{th})^{-1.5}$.

Figure 23 below investigates the excess drain voltage noise dependence on gate voltage with aging for wafer 10. Our data are consistent with $S_{vd} \sim (V_g - V_{th})^{-1.7}$, which shows a departure from uniformity ($S_{vd} \sim (V_g - V_{th})^{-2}$) with aging. Just like in 1989, the noise was greater around threshold and decreases with increasing gate voltage. The slope of the 2007 plot varies from that of the 1989 plot which showed a $S_{vd} \sim (V_g - V_{th})^{-2}$ dependence, which is due to a more significant dependence of the trap density on energy than was described previously. This observation has significant ramifications, because if

the distribution of trap energies is not constant, as suggested by this variation from uniformity, then the noise would have a different dependence on frequency ($\alpha \neq 1$), and temperature.

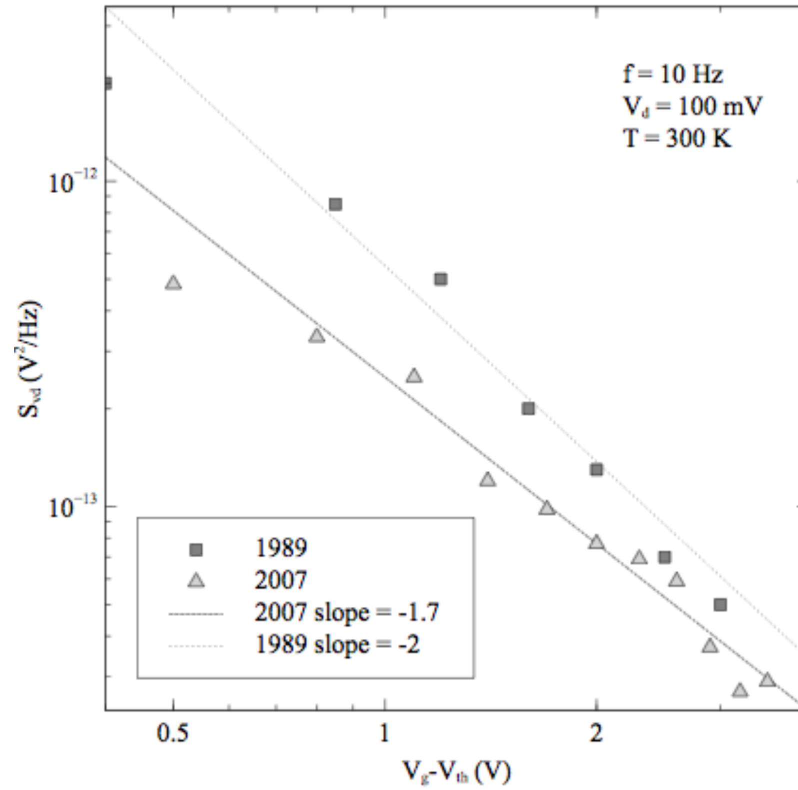

Figure 21: Comparative plot of the noise power spectral density for a wafer #10 n-channel transistor versus V_g-V_{th} at a fixed frequency (10 Hz).

CHAPTER V

CONCLUSIONS

Aging in non-hermetic environments changes the behavior of devices that must remain in operation for long periods of time. Devices fabricated through different techniques have different responses to aging, which we have demonstrated by performing noise measurements on devices annealed in N_2 and comparing the results to those obtained from devices that did not receive such a treatment. The $1/f$ noise levels for the wafers annealed in N_2 were initially much higher, indicative of higher defect densities in the near interfacial layer, and we have shown that after an 18 year aging process the noise levels have been greatly reduced potentially due to a relation of highly strained Si-Si bonds in the vicinity of the interface. Aging decreases the number of traps that are more than a few kT above the device Fermi level and therefore able to contribute to $1/f$ noise. While such changes are plausible, we would expect other materials with different defect densities, energies and governing dynamics to potentially respond differently to the aging process.

We have also compared the threshold voltage levels amongst the four wafers with aging and found very slight changes. Even through the threshold voltage changes observed with aging were small, which would be the main concern for every day applications, understanding the $1/f$ noise gives a lot of insight into the device response to ionizing radiation.

To see if the aging effects can be reversed, we performed unbiased bakes on wafer #10 devices. Since moisture and hydrogenous species are the main aging agent, we investigated if eliminating the water can restore the transistor initial response. Just like in the Karmarkar et al. study [44] we have chosen devices with soft oxides, which at fabrication time had higher defect densities but experienced dramatic $1/f$ noise reduction which aging. We observed similar noise level after aging in the baked and unbaked devices, but the changes in the temperature dependence curves are indicative of changes in defect distributions and energies, consistent with changes in bond length and atomic position.

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