# ON-CHIP CHARACTERIZATION OF TRANSIENT PHOTOCURRENT AND TOTAL IONIZING DOSE-INDUCED LEAKAGE CURRENT

By

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## TABLE OF CONTENTS

**Page**

## LIST OF FIGURES

**Page**

# CHAPTER 1

## Introduction

The characterization of radiation effects has contributed significantly to ensuring the safety and reliability of microelectronic systems. In radiation environments, unhardened components are at risk of problematic radiation effects, such as digital upsets from heavy ions, device degradation from total-ionizing-dose (TID), or even device-wide failure from transient ionizing radiation. Knowledge of these radiation effects can guide radiation hardening by design (RHBD) techniques, where designers can employ prophylactic measures to prevent failure mechanisms and increase device lifetime. Any practical path is taken to find the radiation response of a technology, whether it is through empirical calculation, device simulation, or measurement. Of these, measurement is the preferred technique, as there is little speculation of a radiation response with collected data. Motivated by RHBD, the primary purpose of this work is to measure device-level transient photocurrent induced by transient ionizing radiation in sub-50 nm silicon-on-insulator (SOI) technologies. In the past, the transient photocurrent response of a technology was characterized through current transformer probe measurements of large photocurrent collection nodes [1, 2]. Recently, this technique has been ineffective in sub-50 nm SOI technologies due to technology scaling of transistor channel thickness. For example, the channel thickness is less than 10 nm in fully-depleted SOI (FD-SOI) [3, 4, 5], which is orders of magnitude smaller in comparison to larger bulk technologies. Such small collection volumes lead to proportionally small transient photocurrent amplitudes, resulting in uncharacterizable off-chip responses due to an insufficient signal-to-noise ratio (SNR). The product of this research has created a solution to this problem by performing measurement on-chip through a variety of specialized mixed-signal circuits. Together,

these circuits form a system named the Vanderbilt Photocurrent Measurement Circuit (PMC) [6, 7]. The PMC is designed as on-chip photocurrent measurement solution; that is, the PMC does not rely on the capabilities of a particular technology. Each measurement technique is technology-agnostic and can be optimized for the transient photocurrent response of a specific technology without impacting other parts of the design. Furthermore, all outputs of the PMC are entirely digital, enabling straightforward communication with off-chip components. The PMC has been laid-out, verified in simulation, and fabricated in GlobalFoundries 22FDX (a 22nm FD-SOI technology) [4, 5]. The PMC is designed to operate in a transient ionizing radiation environment and has capability of quantifying both primary photocurrent with nanosecond-scale precision and post-irradiation secondary photocurrent with microsecond-scale precision. This work will explain in detail where both primary and secondary photocurrent are generated and how the PMC enables accurate measurement on-chip. To support this claim, simulations performed in 22FDX using Cadence Virtuoso [8] are presented. Since transient photocurrent is accompanied by significant charge deposition, the PMC is also capable of characterizing total-ionizing-dose (TID)-induced leakage in the photocurrent targets. A test characterization vehicle (TCV) has been created for the 22FDX die, and preliminary TID-induced leakage measurements from this TCV are presented.

# CHAPTER 2

# Background

## 2.1. Primary and Secondary Photocurrent Generation

Several effects contribute to the transient photocurrent response of a technology, which can be separated into two categories: primary photocurrent and secondary photocurrent [2, 10]. Primary photocurrent is the most impactful of the two and is caused by electron-hole pair generation in the active silicon of a transistor [9, 10]. Unlike other forms of radiation-induced perturbations like the single-event transient (SET), which are local to the site of a heavy ion strike, transient photocurrent is a global effect [9, 10]. Transistors under the effects of ionizing radiation will generate primary photocurrent with an amplitude that is roughly proportional to the intensity of the ionizing radiation [10]. In addition, the amplitude of primary photocurrent is roughly proportional to the collection volume of active silicon in the transistor, depicted in Fig. 2.1(a). The

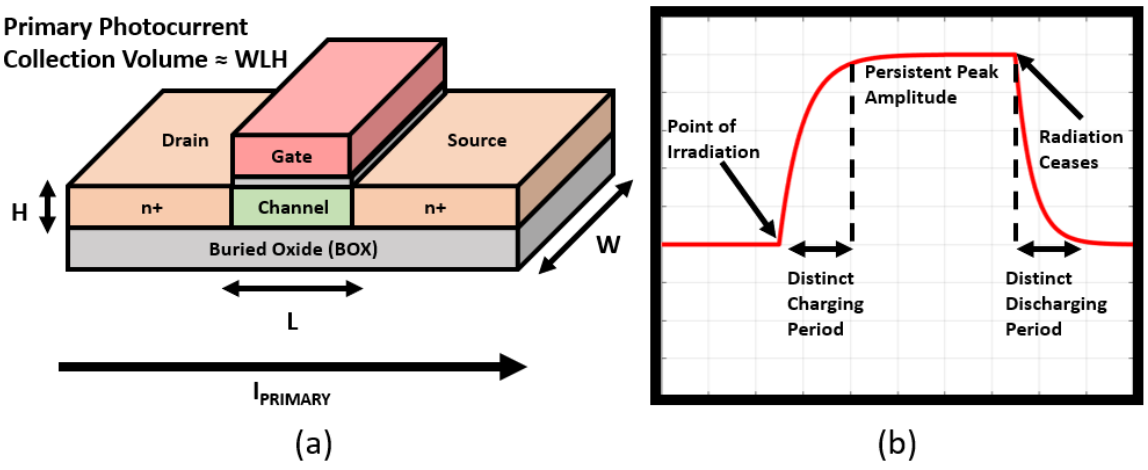


**Figure 2.1 – (a) illustration of a 22FDX transistor with the approximate photocurrent collection volume and (b) illustration of a classical primary photocurrent transient with clear rising and falling characteristics.**

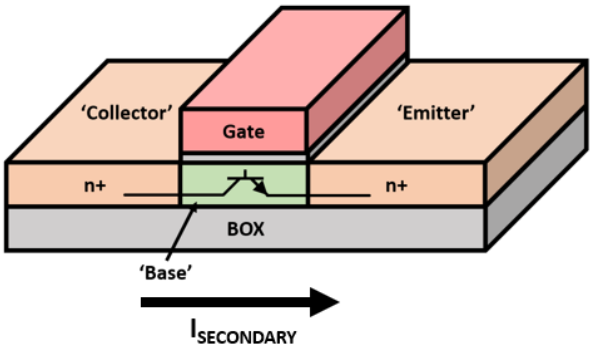


**Figure 2.2 – illustration of a N-P-N BJT structure within the 22FDX N-P-N transistor. The NMOS drain is equivalent to a BJT collector, the NMOS source is equivalent to a BJT emitter, and the NMOS channel is equivalent to a BJT base. Primary photocurrent generation in the channel can supply base current, activating the parasitic BJT. Secondary photocurrent is in the same direction as primary photocurrent.**

classical primary photocurrent response observed in [9] and [10] is akin to a double exponential or error function shape, shown in Fig. 2.1(b). The peak amplitude in the primary photocurrent response has a duration proportional transient ionizing irradiation, which is often on the order of tens of nanoseconds.

Secondary photocurrent is not caused by direct ionization of the active silicon, rather the primary photocurrent can drive parasitic effects within the transistor. One such effect is the activation of the parasitic bipolar-junction-transistor (BJT). In SOI, the N-P-N structure of an NMOS device is identical to that of a N-P-N BJT, shown in Fig. 2.2, but base current is not present under normal conditions and the BJT is therefore never active. However, primary photocurrent can provide the base current, activating the parasitic BJT [11]. This parasitic BJT induces extra current draw from the device during duration of primary photocurrent generation, and in some cases where parasitic base current remains after irradiation, the parasitic BJT can remain activated after

irradiation ceases [10]. The lifetime of the post-irradiation parasitic BJT is technology dependent and could last for several microseconds.

While these effects have been observed in older technologies, the effects of photocurrent generation in newer technologies such as sub-50 nm SOI have not been fully determined through experimentation due to SNR challenges of direct measurements. Characterization of transient photocurrent in these newer technologies could reveal unknown tendencies which are critical for radiation-hardening-by-design (RHBD) techniques.

## 2.2. Predicting Photocurrent Response using TCAD Simulation

To estimate a device-level transient photocurrent response and to guide design parameters, technology computer-aided design (TCAD) simulations were performed in a sub-50 nm FD-SOI technology using the Synopsys Sentaurus TCAD Suite [12]. Instead of irradiating a single target or an inverter, the circuit in Fig. 2.3(a) was chosen for simulation due to its similarity to the target arrays that exist in the PMC. The transient photocurrent response in Fig. 2.3(b) (in red) is mirrored by the PMOS (p-type MOS) pair at the top of Fig. 2.3(a), producing the replicated current (in blue). This response is similar to the response from [9] and [10].

From the perspective of circuit degradation and radiation tolerance, the response in Fig. 2.3(b) is unlikely to induce failure. The peak transient photocurrent amplitude is approximately 5 times that of pre-irradiation leakage, which is not significant enough to cause errors in circuits such as digital logic. However, in terms of measurement, low circuit impact generally indicates a difficult response to characterize. The on-chip measurement circuit must be capable of determining the fast rise time, low amplitude, and continued current from the activated parasitic BJT. The on-chip measurement techniques created to capture these separate characteristics are discussed in Section 6.2.

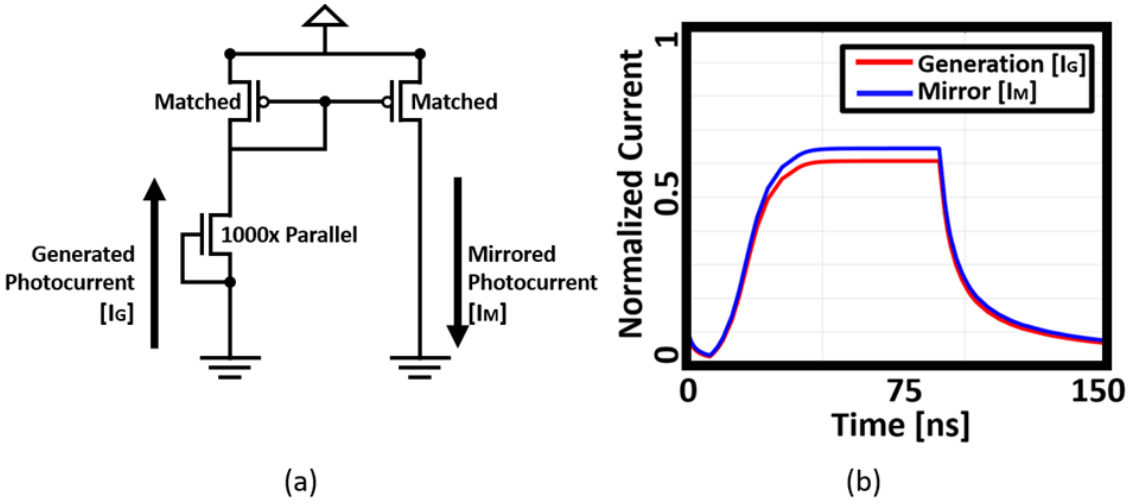


**Figure 2.3 – (a) circuit schematic of a 1000x-parallel photocurrent target that produces transient photocurrent ($I_G$) and is mirrored by a matched PMOS pair ($I_M$) (b) TCAD photocurrent simulation of the circuit in (a). The generated transient photocurrent at the target (in red) is closely followed by the current mirror output (in blue).**

## 2.3. Photocurrent-Induced Failure Mechanisms

Like all forms of radiation, transient photocurrent can degrade circuit performance and, in some instances, induce failure. Though the response from Fig. 2.2(b) is not impactful enough to induce single-device failure, the inability for power rails to handle the sudden increase in current across many components can induce chip-wide failure. Known as rail-span collapse [9], supply rails will undergo significant rail-droop (supply voltage drops below desired levels) if on-chip generated photocurrent exceeds maximum current draw at any location in the circuit. This effect is often seen in dense structures such as static random-access memory (SRAM) [9], where photocurrent collection volumes are very high. The density of the photocurrent targets in the on-chip measurement circuit are designed to be similar to that of SRAM cells in order to maximize the measurability of generated photocurrents. Because of this design decision, rail-droop effects in the photocurrent target are inevitable and must be accounted for. Techniques to mitigate rail-

span collapse are addressed in Section 4. It is also possible that single-transistor photocurrent amplitudes can reach levels that are close to transistor drive current, which is likely to induce failure in several circuits due to transient photocurrent conflicting with on-state current. Whether or not this is possible in 22FDX technology remains to be seen, but this potential failure mechanism can be accounted for with an amplitude-controllable radiation source. These techniques are discussed in sections 3.1 and 3.3, respectively.

# CHAPTER 3

## On-Chip Photocurrent Measurement

### 3.1. Signal Recovery Requirements

The photocurrent pulse in Fig. 2.2(b) is challenging to quantize on-chip. Assuming TCAD simulations match the transient photocurrent response of 22FDX, the PMC must be capable of quantizing signals with an implied rate of 1 giga-sample per second (twice that of the highest frequency component in the transient photocurrent response) to meet Nyquist's' sampling criterion. Transient photocurrent amplitude can range from a fraction of leakage to magnitudes comparable to drive strength, and the length of the photocurrent transients can vary greatly, especially with activation of the parasitic BJT. In combination, the PMC must be capable of quantizing signals which are fast, slow, high-amplitude, and low-amplitude, all while surviving the effects of chip-wide photocurrent generation.

The design philosophy in this work is to maximize the chance to characterize transient photocurrent by creating a wide range of acceptable photocurrent waveforms. Further, the linear accelerator radiation source which the PMC is designed to be irradiated with has the capability to increase or decrease photocurrent generation levels by varying the distance from the PMC to the radiation source. Maximal photocurrent generation is achieved at zero distance to the source, and the amplitude will fall off at a rate proportional to the distance squared as the PMC is moved away from the source [10]. With this capability, there should be no case where photocurrent generation is too great for the circuit, with the only true unmeasurable case being a lack of transient photocurrent seen at zero distance to the radiation source. It will be shown in Section 3.3 that this case is highly unlikely with the PMC design.

## 3.2. High-Level Design

In order to meet the strict signal recovery requirements, several on-chip current capture techniques were developed to measure transient photocurrent with both precision and accuracy. Each of these techniques is technology-agnostic; any technology with mixed-signal design capabilities and access to common components like operational amplifiers and current mirrors will be able to implement the PMC design. This design methodology was specifically chosen to expedite implementation of the PMC in several technologies without the challenges that may come with a more technology-restricted design. The high-level design is shown in Fig. 3.1, and the subsequent sections in this work will delve into the details of each significant functional block.

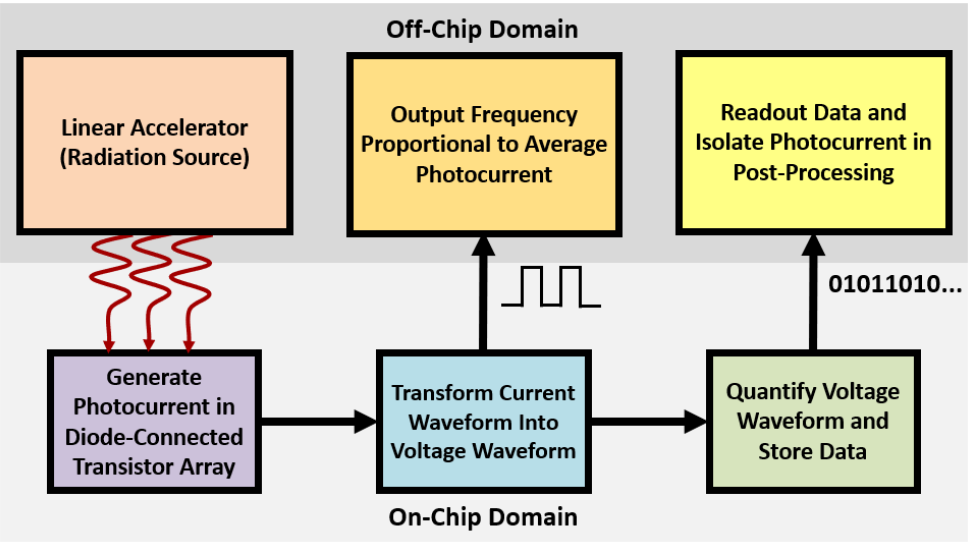


**Figure 3.1 – Illustration of the high-level design of the photocurrent measurement circuit. A linear accelerator radiation source induces photocurrent generation in a large array of off-state transistors. This current is then mirrored to a circuit which converts the current into a periodic voltage waveform. The period of this waveform is buffered off-chip for a rough estimate of photocurrent amplitude. Additionally, this voltage waveform is quantized and stored on-chip for later readout of the quantized samples.**

### 3.3. Amplitude-Controllable Target Arrays and Photocurrent Isolation

Since transient photocurrent is generated globally, all transistors behave as photocurrent targets. Transient photocurrent from potentially large devices such as buffers is undesirable and will ultimately contribute to error in measurements. In this design, transient photocurrent desired to be measured is isolated from the rest of the circuit through parallel amplification. This design philosophy assumes that if target photocurrent is amplified to thousands of times that of a single transistor, then photocurrent in the measurement circuitry will be insignificant and contribute minimally to error. Additionally, the photocurrent target arrays are scalable. Off-chip digital inputs enable the switching of transmission gates that connect to each array in the photocurrent target; this is equivalent to digitally-controlled scaling of generated photocurrent. This ability is a necessity in the PMC, since the amplitude of transient photocurrent generated in the 22FDX technology node is unknown and could vary across several orders of magnitude. The high-level circuit design of this configuration is depicted in Fig. 3.2(a), and the configurations for off-state NMOS and PMOS targets are depicted in Fig.3.2(b) and (c).

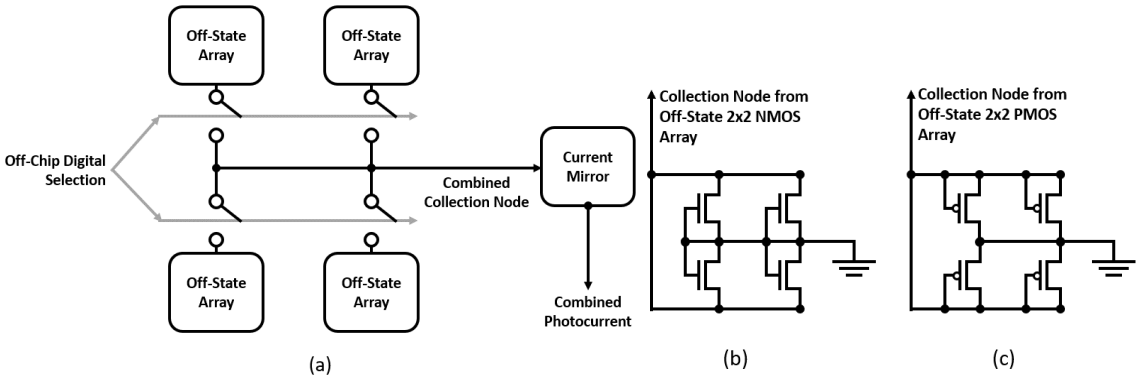


**Figure 3.2 – (a) illustration of the amplitude-controllable photocurrent target. Each off-state array can be enabled or disabled with off-chip digital inputs (b) circuit schematic of a 2x2 off-state NMOS target (c) circuit schematic of a 2x2 off-state PMOS target.**

It is up to circuit designers to choose how many transistors are necessary in each target and how many target arrays are required to encompass the full range of potential transient photocurrent amplitudes. There are significant design tradeoffs when choosing these values. For example, each additional target array attaches an additional current mirror (a photocurrent target itself) to the combined collection node, contributing to error. Further, the more transistors incorporated in single target array, the more robust the current mirror must be to be capable of following the transient photocurrent waveform. Ultimately there is no way to design a perfectly optimized target due to the transient photocurrent response being unknown, so it is best to be conscious of the design tradeoffs and choose sizes that will be capable of characterizing the most likely range of transient photocurrent responses. For this work, these design tradeoffs were identified using transient photocurrent waveforms generated from TCAD simulations similar to that of Fig. 2.1 (b). These transient photocurrent waveforms were then imported into Cadence Virtuoso to simulate realistic photocurrent generation events in the target arrays.

## 3.4. Integrator

### 3.4.1) Current-to-Voltage Techniques

A common approach to measure current in off-chip applications is to simply leverage Ohm's law and capture the voltage across a resistor. However, on-chip, silicon-based resistor values vary significantly [13], the current-to-voltage characteristics may not be linear, and to measure micro-ohm level transient photocurrent, the resistors would need to be on a megaohm scale. For these reasons, using resistors to measure transient photocurrent on-chip is intractable. Instead, capacitors were chosen as the component which transforms current into voltage. Metal capacitors do not suffer from high variance like resistors and automatically span the full voltage range in the on-chip environment as they charge. Further, ideal metal capacitors are virtually

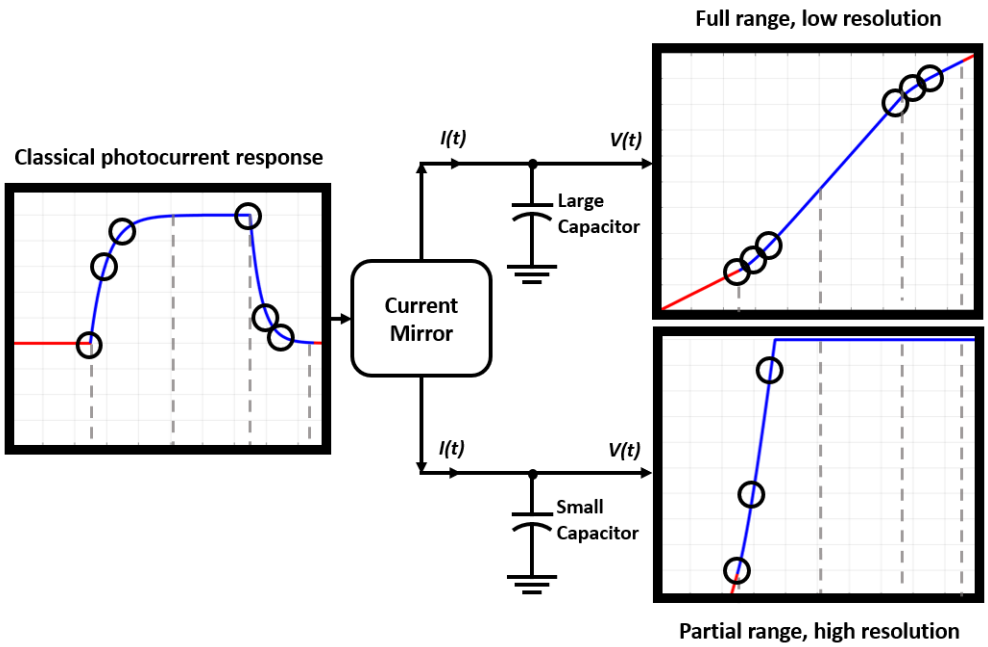


**Figure 3.3 – Illustration of the tradeoffs from using a large capacitor and a small capacitor as an integrator. In the large capacitor case, the full voltage range is utilized, but the low resolution obfuscates transient information. In the small capacitor case, the capacitor reaches charge capacity very quickly but has a high resolution. In all three plots, the circles correspond to the same point in time, and the gray dotted lines represent the rising and falling edges of the photocurrent transient.**

immune to the effects of transient photocurrent. Finally, metal capacitors behave linearly when integrating current, which is critical for signal recovery. Foreseeable downsides to using a capacitor include limited charge capacity on the capacitor and low resolution of the photocurrent integral, shown in Fig. 3.3. However, both of these downsides are completely avoided through the technique presented in the next section.

### 3.4.2) Periodic Integration

Since capacitors can only hold a finite amount of charge, the only way to continuously integrate current is to quickly discharge the capacitor once it is full. However, the amount of time

lost in a discharge can result the loss of information contained in the transient photocurrent integral. To resolve this, multiple capacitors are implemented such that, when one capacitor is full, another capacitor is switched onto a shared node. At the same time, the full capacitor switches off the shared node and is discharged separately. This technique produces a periodic voltage signal closely resembling a sawtooth wave, shown in Fig. 3.4. In addition to resolving charge capacity, indefinitely cycling capacitors enable the use of very small capacitors, which increases voltage resolution. In this context, voltage resolution is defined as the total number of volts associated with the average current over a period of time. In terms of leakage current and photocurrent, the voltage resolution is defined by the following equation:

$$\emptyset_R = \frac{(\tilde{I}_{PHOTO}+\tilde{I}_{LEAK})(T_{RAD})}{C} \qquad (1)$$

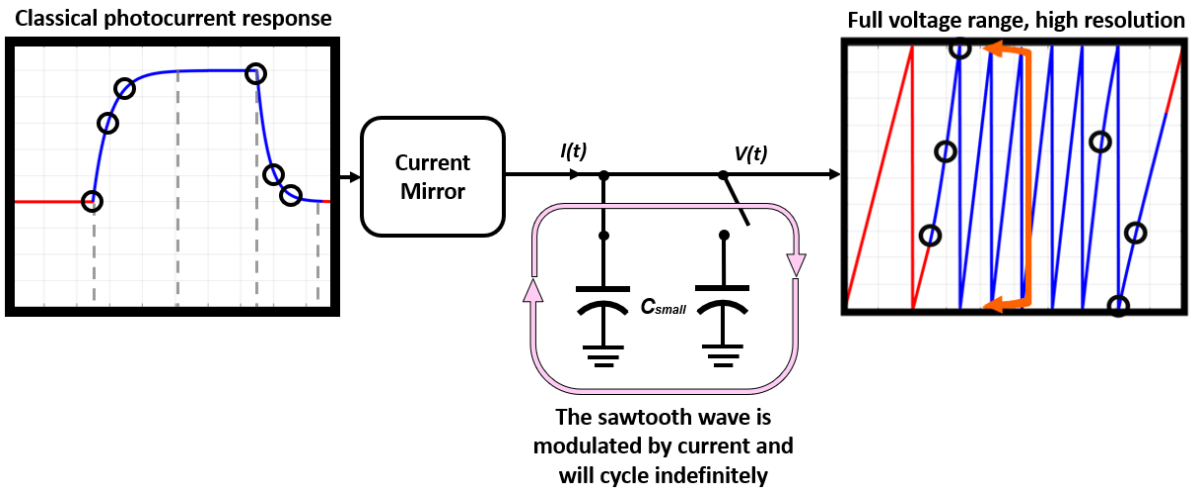


**Figure 3.4 – Illustration of the high-level circuit design of the integrator. Transient photocurrent is mirrored into a pair of small capacitors which cycle between each other when fully charged. An external discharge transistor (not shown) pulls the voltage to ground after each cycle, creating a periodic voltage waveform that resembles a sawtooth wave. This setup allows for a full voltage range with high resolution.**

Where $\emptyset_R$ is the voltage resolution, $C$ is the capacitance of a single capacitor in the integrator, $\tilde{I}_{PHOTO}$ is the average photocurrent generated during the irradiation period, $\tilde{I}_{LEAK}$ is the average leakage current in a steady environment, and $T_{RAD}$ is the period of the irradiation. A high voltage resolution indicates a signal which can more easily be observed with quantized samples. That is, an analog-to-digital converter (ADC) will be able to accurately capture signals that are stretched out over several volts as opposed to signals that are compressed due to a small voltage resolution. Ideally, the voltage resolution will be reasonably high while balancing capacitance such that the frequency of the integrator is not too large for the on-chip digital switching mechanisms. A balance of these design tradeoffs will ultimately be decided by the expected amplitude of transient photocurrent generated in the targets.

3.4.3) Improved Periodic Integration

The simple two-capacitor design was improved with two additional capacitors, shown in Fig. 3.5. This change was made for several reasons, the first of which was to ensure that an empty capacitor will always be available in the case that the charging capacitor cycles too quickly.

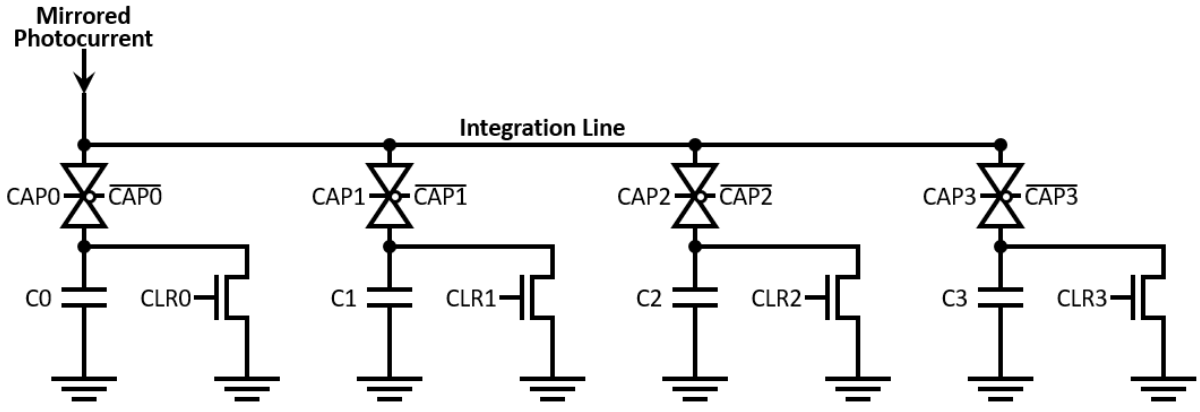


**Figure 3.5 – Detailed circuit design of the integrator. Transmission gates control which capacitor is connected to the central integration line, and NMOS transistors discharge each capacitor when disconnected.**

Second, the two additional capacitors are switched onto the integration line to assist with the nodal discharge at the peak of every sawtooth wave, significantly speeding up the discharge time. Lastly, increasing the number of capacitors to four enables common centroid techniques in layout to decrease variance across the four capacitors [15, 16]. This common centroid technique is detailed in Section 4.

3.4.4) DC and Secondary Photocurrent Measurement

The original purpose of the integrator was to improve voltage resolution and allow for continuous measurement of primary photocurrent. However, it was quickly discovered that the frequency of the sawtooth wave is directly proportional to both $\tilde{I}_{PHOTO}$ and $\tilde{I}_{LEAK}$ and can be measured to calculate the average on-chip current. The frequency of the sawtooth wave is detected by a simple D-Flip Flop (DFF) clock divider and is buffered off-chip such that it can be monitored in real time by oscilloscopes. Access to this frequency is sufficient for characterizing both high-amplitude and low-amplitude DC signals through the following equation:

$$\tilde{I} = CV_{MAX}f_{SAW} \quad (2)$$

Where $\tilde{I}$ is the average current entering the integrator, $C$ is the capacitance of the integrator, $V_{MAX}$ is the maximum voltage of the sawtooth wave, and $f_{SAW}$ is the observed frequency. Though this average current can be used to estimate the amplitude of primary photocurrent, it is much more valuable as a tool for calculating slow-speed currents entering the integrator. In the context of transient photocurrent measurement, post-irradiation secondary photocurrent could meet this criteria with potential effects observable for several microseconds.

Additionally, DC signals such as leakage current are directly proportional to the observed frequency, which doubles the PMC as a leakage measurement circuit. This capability is not

particularly important for transient photocurrent measurements, but this leakage measurement capability can be used to characterize total-ionizing-dose (TID)-induced leakage in the photocurrent targets. Other PMC applications such as this are discussed in Section 7.

## 3.5. Analog Voltage Sampler

### 3.5.1) Sampling Technique

The analog voltage sampler is a necessary component in the PMC due to a high likelihood that photocurrent generation will render ADCs unreliable during irradiation [1, 2, 14]. In order to circumvent this likely issue, voltages from the integrator are stored on clock-shielded metal capacitors until irradiation ceases. Afterwards, the analog voltages are read out sequentially, effectively recreating the input signal. Though this technique is straightforward, in order to sample voltages at gigahertz-level frequencies, the overhead is quite costly. Each metal capacitor must be small (femtofarad-scale) in order to charge at a nanosecond timescale, requiring a high-performance buffer to accompany each sample cell to overcome parasitic capacitances at the ADC input. Since a transient photocurrent event could last hundreds of nanoseconds, hundreds of high-speed buffers are required to capture the full photocurrent transient. In the fully laid-out 22FDX implementation of the PMC, the sampler takes up approximately 50% of the PMC area and is the biggest power-consumer in the circuit.

The sampler can be scaled to any number of "sample cells" using the design in Fig. 3.6. As an example, if the sampling rate of the sampler is 2 GHz and 50 ns of information is desired to be captured, 100 sample cells are required.

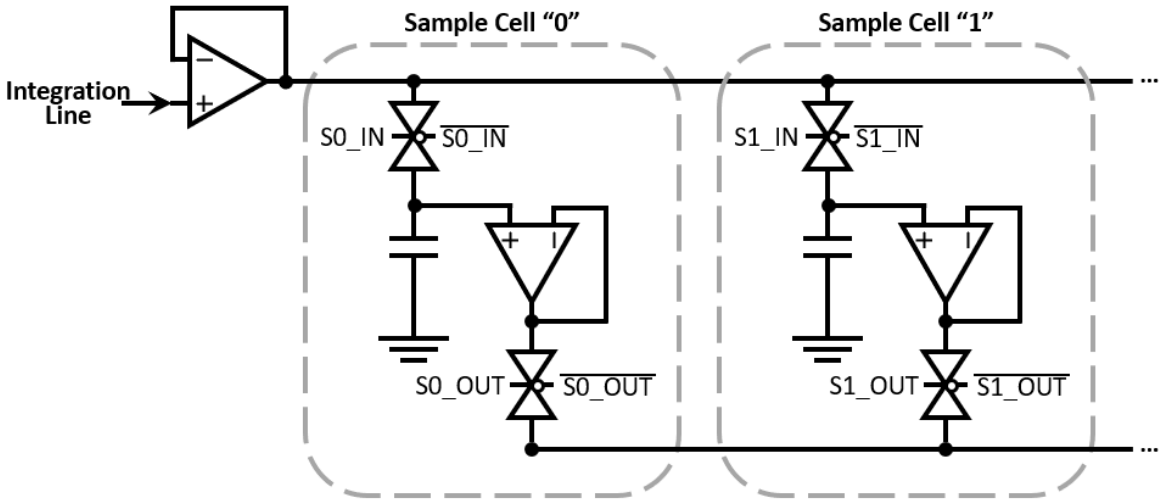


**Figure 3.6 – Detailed circuit design of the analog voltage sampler. The voltage on the integration line is buffered to a shared input node, where input transmission gates connect that voltage to a sample capacitor. The transmission gates will sequentially cycle until all sample cells have a stored voltage. At this point, the output transmission gates sequentially cycle, recreating the integration line voltage on the output. The transmission gates are controlled by two shift registers - one for the inputs and one for the outputs (not shown).**

3.5.2) Sample Degradation and Hold Time

The sample cells include femtofarad-level capacitors, and the voltages held on them will quickly degrade due to leakage current from the transmission gate and buffer. From simulations in 22FDX, the estimated hold time before one bit of information is lost on the capacitor is on the order of microseconds. Note that for this technology, one bit of information corresponds to 25 mV, since the rail voltage is 800 mV, and the ADC has a resolution of 32-levels. From this information, it is implied that from the first sample taken, all data needs to be read out within a microsecond. Otherwise, sampled voltages will degrade significantly.

Sample and readout frequencies may not be identical, so the following equation can be used to guide design choices for the sampler:

$$N_{sc}\left(\frac{1}{f_S}+\frac{1}{f_R}\right)<\tau_D \qquad (3)$$

where $N_{sc}$ is the total number of sample cells, $f_S$ is the sampling frequency, $f_R$ is the readout frequency, and $\tau_D$ is the time it takes to lose one level of resolution of a sample cell to leakage. For example, if the sampling frequency is 2 GHz, the readout frequency is 500 MHz, and number of sample cells is 256, the time required to both read in and out all information before degradation of the stored voltages would be 640 nanoseconds.

3.5.3) ADC, Voltage Reference, and Shift Register Memory

Proper implementation of the ADC is critical to ensure data recovery and will be briefly discussed. To maximize resolution, a sub-1 volt, 32-level flash ADC was chosen. Since quantization of sampler voltages occurs post-irradiation, the ADC does not need to be radiation-hardened, but the ADC voltage reference does need to be radiation-hardened. Voltage references in general require a long period to stabilize, and if perturbed by transient photocurrent, the voltage levels could become temporarily destabilized. To harden the voltage reference, switched capacitors were implemented in place of resistors, since metal capacitors behave linearly in the presence of photocurrent generation. A standard resistor ladder voltage reference is shown in Fig. 3.7(a), and the hardened switched capacitor variant is shown in Fig. 3.7(b). The variant in Fig. 3.7(b) switches capacitors at 250 MHz and creates stable output voltages within a few microseconds. Several switched-capacitor configurations were tested in simulation, and in this configuration, only the bilinear switched capacitor of Fig. 3.7(b) is functional. It was determined that the voltage reference requires symmetry and a closed loop to power or ground at all times. Otherwise, nonlinearity was introduced.

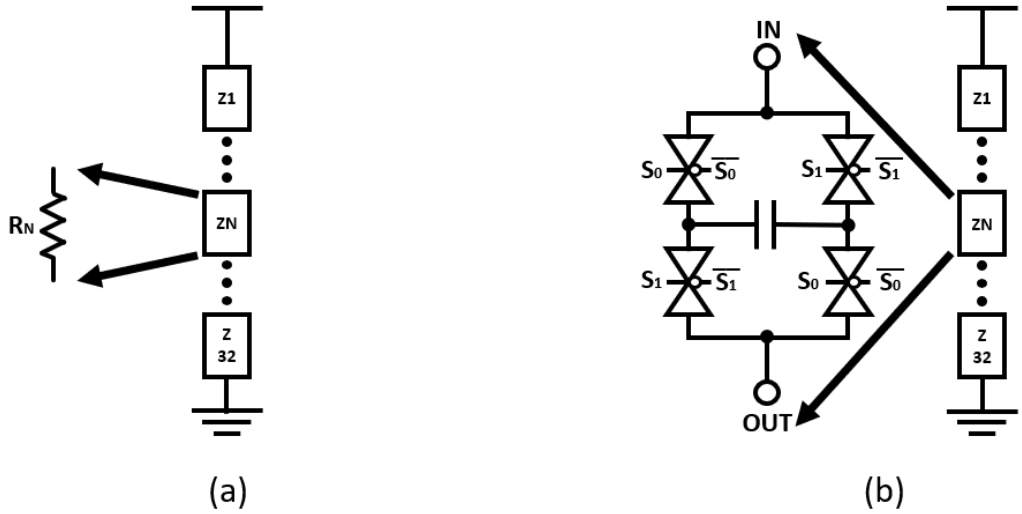


**Figure 3.7 (a) – circuit schematic of a traditional 32-level voltage reference ladder (b) circuit schematic of the switched capacitor 32-level voltage reference ladder. Instead of resistors, a metal switched capacitor is implemented. This switched capacitor is controlled by two opposing signals S0 and S1 which alternate the flow of current through the center capacitor. At high enough frequencies, this configuration mimics the function of a resistor. Additionally, circuitry such as low-pass filters and hold capacitors are present but not shown.**

Due to the timing restrictions imposed by leakage in equation (3), the ADC must operate at a frequency higher than that which can be driven off-chip in real time. For this reason, the digital ADC data is stored in a shift register memory on-chip. Once all sample cells are converted by the ADC and stored into this memory, an external clock controls a readout of the shift register memory.

### 3.6. Detailed High-Level Design

All major components in the PMC have been discussed, and a more complete high-level design that utilizes the circuits from Section 3.3-3.5 is shown in Fig. 3.8.

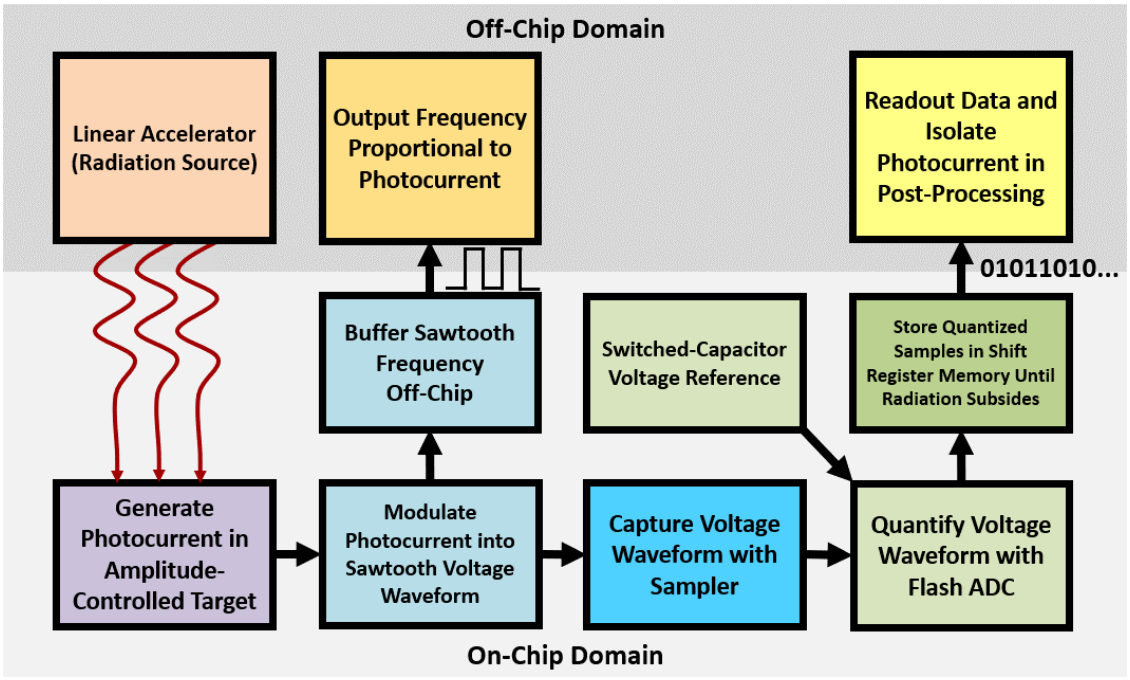


**Figure 3.8 – Complete high-level PMC design. Transient photocurrent is generated in an amplitude-controlled target and is mirrored to the integrator, which integrates the current into a sawtooth wave. The frequency of this sawtooth wave is detected and buffered off-chip for an amplitude estimate of photocurrent. This waveform is also buffered to the voltage sampler, which samples the voltage on metal capacitors and sends them to a flash ADC, which uses reference voltages from a radiation-hardened switched capacitor voltage reference. Finally, the ADC outputs are stored in shift register memory and can be read out at any time for off-chip recovery of the photocurrent voltage integral.**

# CHAPTER 4

# 22FDX Implementation and Layout

## 4.1. Technology Overview

The technology utilized in this work is GlobalFoundaries 22FDX, a 22nm fully-depleted SOI technology [4, 5]. Though transient photocurrent amplitudes are likely to be low as discussed in Section 2, the efficiency of this technology offers many benefits in the PMC implemetation. The most important of these benefits is the high transsitor drive-strength offered with little required layout space. For example, the current mirrors and buffers in this iteration of the PMC are primarily first-order designs that would only be viable with high drive-strength transistors. This advtange is significant in regard to photocurrent measurement, since these first-order designs utilize transistors with a low combined transient photocurrent collection volume, minimizing the impact of the surrounding circuitry on the intended photocurrent targets. Other impacts related to the circuits in the PMC will be discussed in the next section, where the layout of each circuit is detailed.

## 4.2. Layouts

4.2.1) PMC-Level View

The layout of the 22FDX implementation of the PMC is shown in Fig. 4.1. The labels **I-VII** represent the necessary on-chip components part of the PMC design in Fig. 3.8. To prevent rail-span collapse detailed in Section 2.3, several nanofarads of decoupling capacitance surround the active components, which appear as red rectangles in Fig. 4.1. The two biggest portions of the circuit are the sampler **(IV)** and the target arrays **(I)**, with the sampler comprising over 60% of the active components and the target arrays comprising approximately 15% of the same area. The

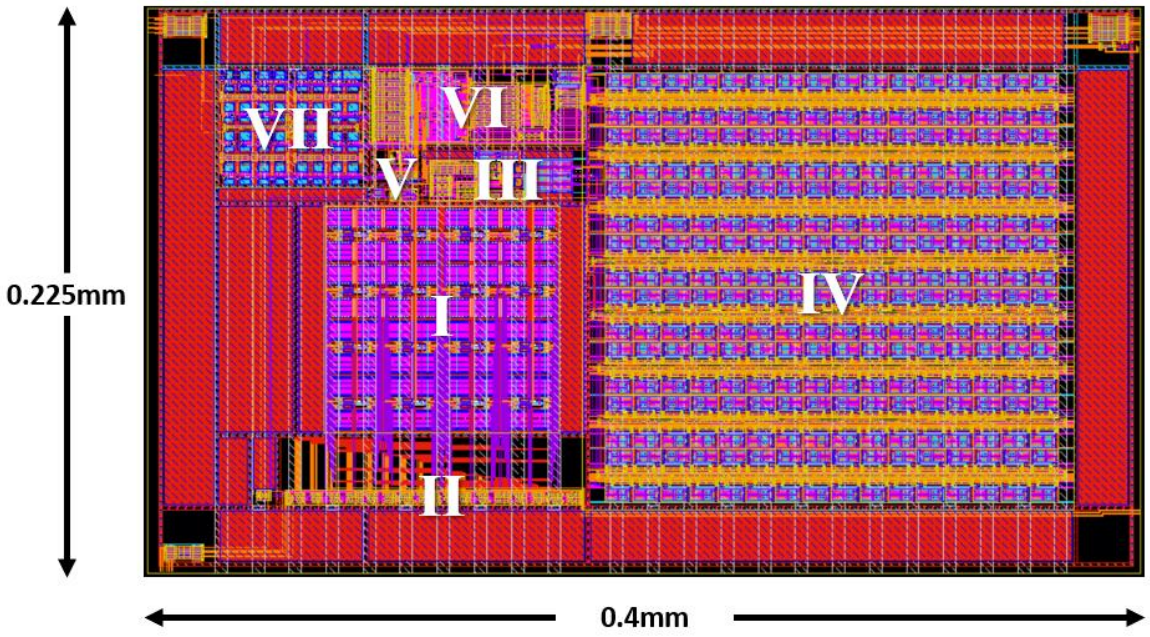


**Figure 4.1 – Layout view of the 22FDX implementation of the PMC. There are eight major components in the design, labelled I-VII. Unlabeled components include power rails, decoupling capacitors, and global I/O. The labelled components are (I) Target arrays (II) Target array digital select logic (III) Integrator (IV) Sampler (V) Built-in self-test (VI) ADC (VII) Switched capacitor voltage reference.**

dimensions of the chip which this PMC is implemented in are 3mm x 2mm; the entire PMC takes up approximately 1.5% of this available space.

4.2.2) Target Arrays

The layout view of one target array with 80 nm/20 nm minimum-sized transistors is shown in Fig. 4.2(a). This array is the smallest denomination of transistors which can be selected by the PMC, which represents approximately 312 μm² of active silicon. The drains of each transistor connect to a central metal line, which leads to a current mirror. The back-gate P-well contacts **(II)** are grounded in this target variant, but other variants implement off-chip biasing capability.

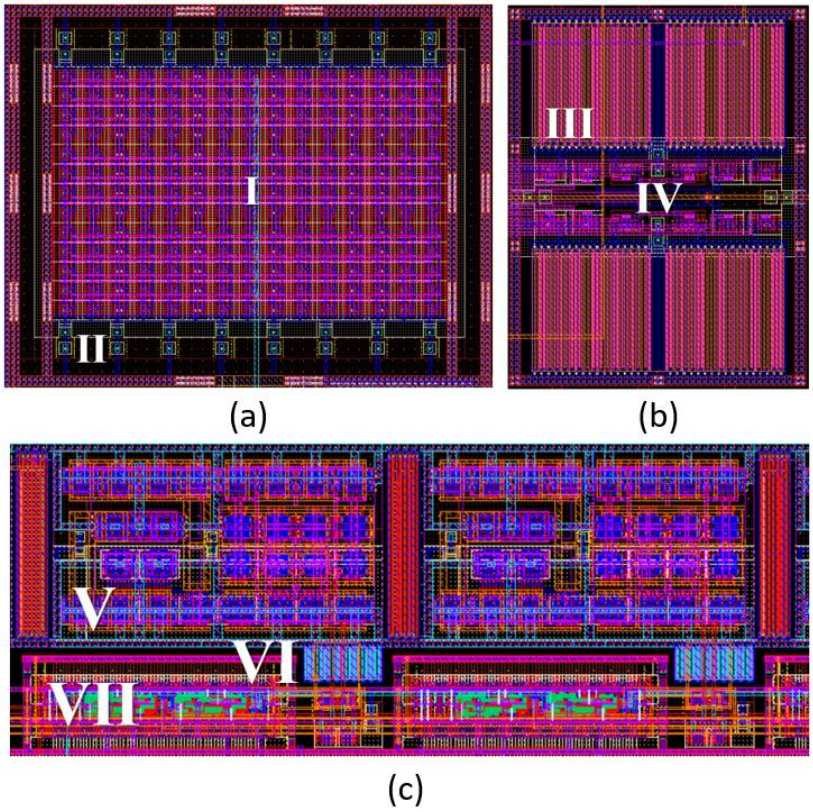


**Figure 4.2 – Close-up of several layouts in the PMC (a) – target array with 80 nm/20 nm minimum-sized transistors. (I) Drain-connected parallel transistors (II) Back-gate voltage contacts (b) Layout view of the integrator. The four metal capacitors (III) from the design in Fig. 3.5 are placed in common-centroid. The electrical pathing and switches (IV) are placed in-between the capacitors and are controlled by external digital logic (c) Layout view of two sample cells within the sampler. (V) Buffer (VI) Shielded sample capacitor (VII) D-flip flop logic which controls the buffer and sample capacitor electrical pathing.**

4.2.3) Integrator

The layout-view of the integrator is shown in Fig. 4.2(b). This integrator utilizes four 20 fF metal capacitors **(III)**, and to reduce variance in the integrator, the capacitors are placed in common centroid about the transmission gates between them **(IV)** [15, 16]. Digital logic circuits for these switches are located elsewhere to minimize switching noise and clock feedthrough.

4.2.4) Sample Cell

Two sample cells within the sampler are detailed in Fig. 4.2(c). Each sample cell is composed of a dedicated buffer **(V)**, a shielded metal capacitor to protect against clock-feedthrough degradation **(VI)** [15, 16], and the D-flip flop logic that controls the electrical pathing of both the sample capacitor and the buffer attached to the capacitor **(VII)**. The sampler is far too large to route digital logic from external circuits, so the digital logic is incorporated into the analog design. The digital logic in each sample cell is part of a D-flip flop chain that controls the analog components and propagates throughout the sampler.

## 4.3. Technology Characterization Vehicle

A technology characterization vehicle (TCV) test board, shown in Fig. 4.3, has been created to house the 22FDX die and communicate with the four on-chip PMCs. This TCV board was used to collect the data from Section 7 in this paper. Several features are available using external I/O, including: ring-oscillator frequency tuning and halving, one-half and one-eighth integrator frequency measurement, 5-bit ADC communication, 32-levels target selection, 4-level self-test selection and back-biasing capability.

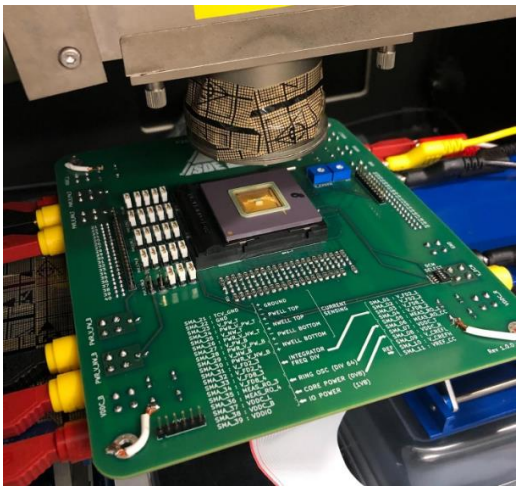

**Figure 4.3 – 22FDX technology characterization vehicle test board.**

# CHAPTER 5

# Simulation Results

## 5.1. Simulation Overview

The simulations in this chapter demonstrate the viability of the primary and secondary photocurrent measurement circuit in 22FDX technology. For this work, only simulations from novel components such as the integrator and sampler will be shown. All other components, including buffers, current mirrors, voltage reference, and ADC, were simulated and verified with post-layout, parasitic-extracted netlists during reliability testing. In addition, all major components were tested and verified at process corners and with device mismatch. All simulations were performed in Cadence Virtuoso [8].

To fully test the capability of the PMC, a “worst-case” primary photocurrent transient was chosen; that is, primary photocurrent transients with more identifiable amplitude and transient characteristics are expected during radiation testing. This worst-case transient has a 15 ns rise time and a 15 ns fall time with an amplitude on the same order as device leakage. Photocurrent generation will be active for 50 ns. To show the wide-range of acceptable transient photocurrent amplitudes, transient photocurrent amplitude is tested at 0.2-, 1-, and 5-times that of device leakage.

## 5.2. Integrator Simulation

In simulation, the integrator was tested using low-level components available and represents the most accurate available model of how a real-world circuit would behave. The only ideal component in the simulation is the transient photocurrent source. In this simulation, a device-wide reset occurs at 25 ns and transient photocurrent is generated at 250 ns. The full simulation lasts 500 ns. The results from a 0.2-, 1-, and 5-times leakage photocurrent amplitude simulation are shown in Fig. 5.1(a-i), where (a-c) are the photocurrent transients, (d-f) are the sawtooth waves generated by the photocurrent transients, and (g-i) are the frequency detector outputs that are visible off-chip.

The simulations indicate that the integrator can detect primary photocurrent at a wide-range of magnitudes. Not only is the primary photocurrent integrated into a voltage waveform that can be detected by an ADC, but the frequency detector output clearly shows an increase in sawtooth frequency. In the case of the 100 nA photocurrent transient, which is comparable to the magnitude of secondary photocurrent, the sawtooth wave visually appears unaffected, and it would be challenging for an ADC to detect the waveform. However, the frequency output captures the amplitude of the waveform and can be detected with an oscilloscope off-chip. Both the 500 nA and 2500 nA currents are detectable by an ADC and the off-chip frequency.

Though transient photocurrent can be detected at a wide range of amplitudes, high-amplitude transient photocurrent can introduce non-ideality due to switching speed limitations of the on-chip comparators. In Fig. 5.1(e), the sawtooth integral's peak voltage increased 15 mV above 600 mV (the desired peak voltage). This will contribute minimally to error, but the 100mV voltage increase above the desired peak voltage in Fig. 5.1(f) will contribute significantly to error. This non-ideal behavior from the on-chip comparators is caused by a combination of switching

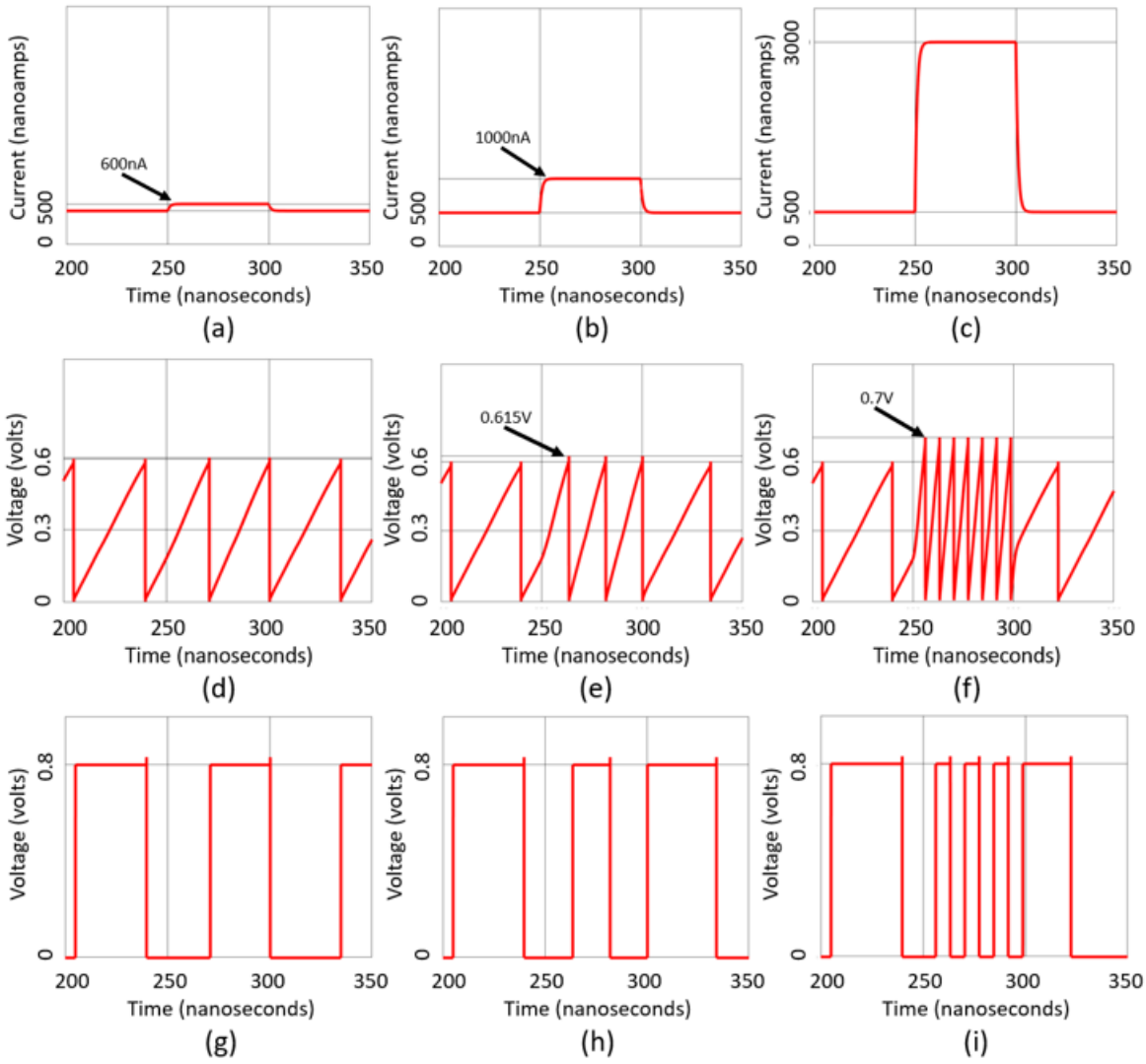


**Figure 5.1 – Simulation of the integrator (a-c) Ideal photocurrent input at 500 nA background leakage with (a) 100 nA peak amplitude (b) 500 nA peak amplitude and (c) 2500 nA peak amplitude (d-f) integrator voltage response to photocurrent input (g-i) buffered sawtooth frequency visible off-chip.**

speed in the comparators and propagation time of the reset signal through digital logic. This effect only appears at very high transient photocurrent amplitude. For reference, the 22FDX implementation of the PMC is designed to operate ideally at no more than 1000 nA input current during photocurrent generation. Using the amplitude-controllable targets, this level can be

achieved; the only instance where the PMC will operate out of the ideal range is when a single target generates photocurrent above 1000 nA, which is an unlikely scenario.

### 5.3. Sampler Simulation

Like the integrator, the sampler is constructed from the lowest-level available components in simulation and represents the most accurate available model of the real-world circuit. However, there are two ideal inputs: the voltage waveform from the integrator and the clock signals. The input photocurrent transient will have an amplitude 1-times that of leakage, and the clocks are assumed to be generated from an ideal ring oscillator with 2 GHz- and 1 GHz-capable outputs. The sampler utilizes a clock tree to equally distribute this signal to each sample cell, so clock propagation and feedthrough behavior is captured by the simulation.

The sample clock frequency is set to 2 GHz and the sampler is 256-samples long, so the sampler collects data for 128 ns. At this point, data from the sampler is read out at 500 MHz, which lasts for 512 ns. Once this data is read out to the ADC, photocurrent capture is finished, and the recreated voltage waveform is stored in shift register memory. Note that, because of the clock tree and complexity in the buffers, simulation times for the sampler can take upwards of twelve hours in Cadence Virtuoso. In early testing, it is recommended to use ideal buffers and clocks to save time in simulation. Fig. 5.2(a) is the input photocurrent transient, Fig. 5.2(b) is the integral of that input, and Fig. 5.2(c) is the recreated voltage at the sampler's output. Note that sampler readout starts at 128 ns in the simulation and lasts for 512 ns.

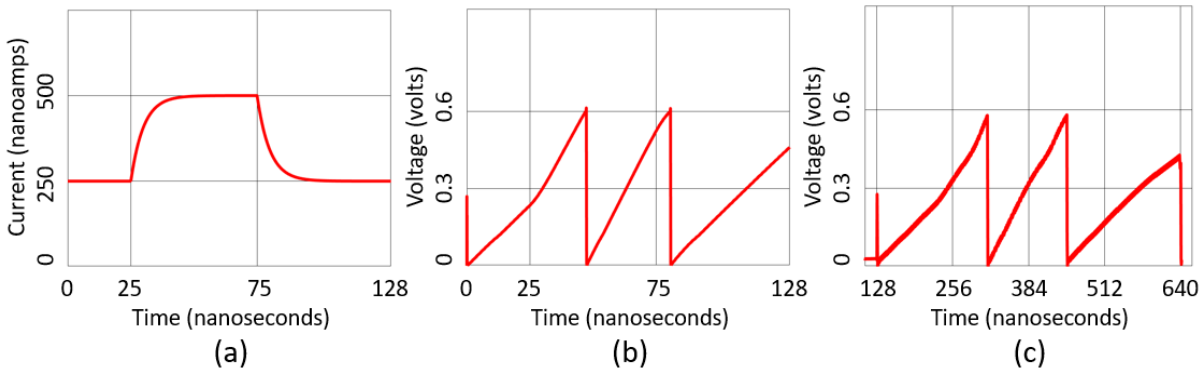


**Figure 5.2 – Simulation of the sampler (a) Input photocurrent transient (b) integrator voltage response (c) sampler recreation of (b). The sampler is capturing data for the first 128-nanoseconds and shifts data out afterwards for 512-nanoseconds.**

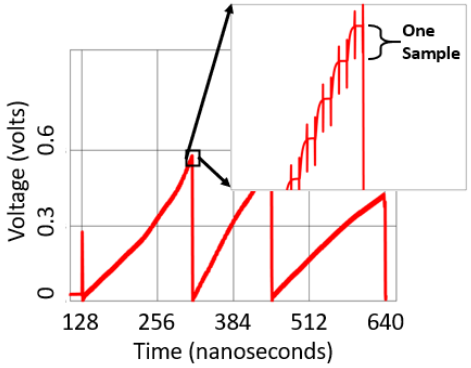


**Figure 5.3 – Detail of sampler waveform recreation. The voltage increase represented by "One Sample" is from the sampler buffering a stored value to the ADC.**

This simulation indicates that the voltage waveform from the integrator can be safely stored by the sampler and quantized afterwards by an ADC. Detail of the recreated signal can be seen in Fig. 5.3, where each sample during readout raises the output voltage to the stored analog value in the sample cell. Though some degradation of the signal is present, most notably a loss of resolution near rail voltage due to leakage within the sample cell, the shape of the signal is intact. Most importantly, the rising and falling portion of the signal are still intact and can be interpolated in

post-processing to recover transient characteristics. Further analysis and post-processing of this signal is performed in Section 6.2.

# CHAPTER 6

## Self-Test and Data Processing

### 6.1. Built-In Self-Test

The bult-in self-test (BIST) for the PMC exists to both verify that the circuit is operational and to solve for internal electrical circuit parameters. In specific, the BIST solves for the internal integrator capacitance from equations (1-2) and is necessary to determine the absolute magnitude of both transient photocurrent and leakage. The BIST is capable of disabling the photocurrent targets arrays and replacing the input integrator current with a known current that is mirrored off-chip. The following equation is used to determine the internal integrator capacitance:

$$C = \frac{I}{V_{MAX} f_{SAW}} \qquad (4)$$

Where $C$ is the internal integrator capacitance, $I$ is the observed current, $V_{MAX}$ is the maximum frequency of the sawtooth wave that is set off-chip, and $f_{SAW}$ is the observed frequency.

### 6.2. Data Reconstruction

6.2.1) Amplitude Estimate

The frequency output of the PMC can be used as a rough amplitude estimate of the photocurrent transient. This technique does not recover any high-frequency transient information, but the amplitude of secondary photocurrent such as the parasitic BJT will be captured. The simplest way to calculate this estimate is to take the running frequency of the PMC and substitute it for $f_{SAW}$ in equation (4). In some cases, this amplitude estimate is sufficient for RHBD techniques and will inform designers if the transient photocurrent will cause errors within a particular design.

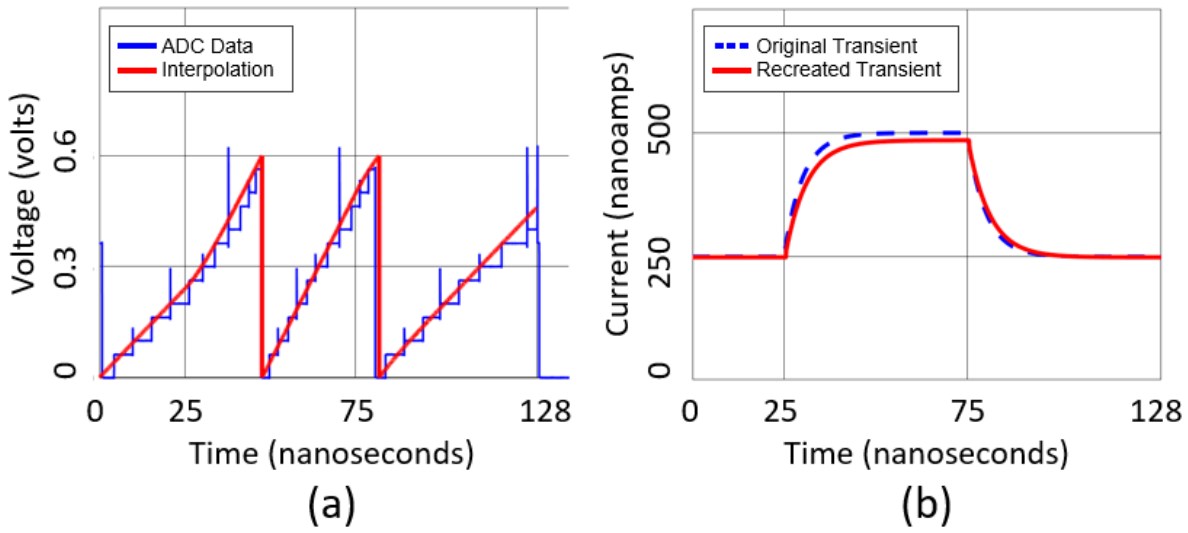


**Figure 6.1 – (a) ADC interpretation of the sampler output of Fig. 5.2(c) with interpolation of data. (b). Derivative of interpolated data compared to the original photocurrent transient of Fig. 5.2(a).**

6.2.2) Transient Data

Reconstruction of transient data requires interpolation and differentiation of the sampler's quantized output. The accuracy of this process is determined by the voltage resolution of the signal from equation (1) and by the quality of the data captured by the sampler as discussed in Section 5.3. Interpolating ADC data from Fig. 5.2(c) results in the red curve of Fig. 6.1(a), which assumes linear behavior during the period where reset error occurs. Differentiating this signal results in Fig. 6.2(b), which matches closely to the original photocurrent transient. The recreated rising and falling characteristics are close to the original transient's characteristics, and the amplitude matches closely as well. Due to the sample degradation described in 5.3, the slope of the sawtooth wave was decreased, which results in a decreased peak photocurrent amplitude (500 nA original peak amplitude versus 480 nA recreated peak amplitude). Such small error is acceptable, especially since the primary purpose of the sampling-stage of the PMC is to capture transient characteristics of primary photocurrent, which are still intact.

# CHAPTER 7

# Other Applications

## 7.1. TID-Induced Leakage Measurement

### 7.1.1) TID Overview

Total-ionizing-dose (TID) is a measure of the total dose accumulated within a device, which manifests itself in transistors as trapped charge [1, 17, 18]. This trapped charge accumulates in the oxide which alters the performance of the device [1, 17, 18]. In traditional bulk CMOS devices, this trapped charge accumulates primarily at the gate oxide volume, but in SOI technologies, the buried oxide (BOX) also accumulates traps [17, 19, 20]. NMOS and PMOS SOI transistors accumulating charge can be seen in Fig. 7.1(a) and (b). This trapped charge is primarily positive, inducing negative threshold-voltage shifts in NMOS devices (closer to an ON state) and negative threshold-voltage shifts in PMOS devices (closer to an OFF state) [17]. Additionally,

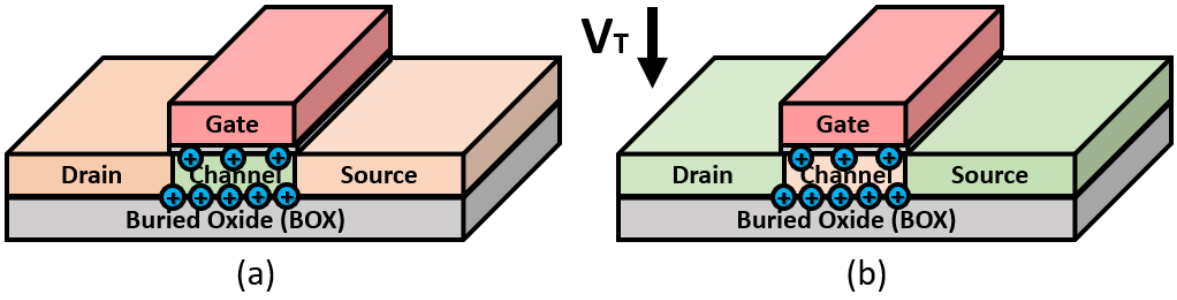


**Figure 7.1 – (a) illustration of an NMOS SOI transistor accumulating positive trapped charge (b) illustration of a PMOS SOI transistor accumulating positive trapped charge. Addition of the BOX allows positive trapped charge to accumulate below the transistor. Positive trapped charge decreases the threshold voltage of each device.**

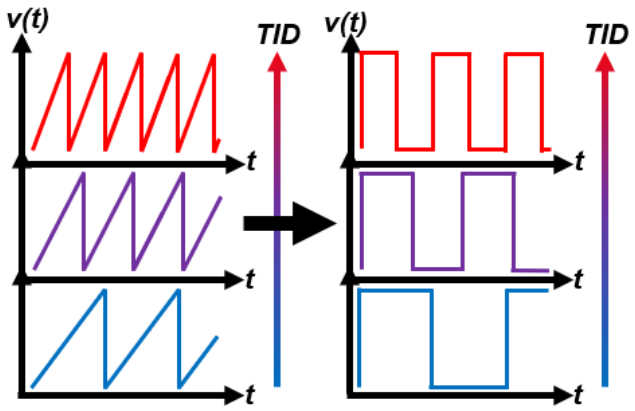


**Figure 7.2 – Illustration of the output frequency of the PMC increasing with TID.**

these threshold voltage shifts impact the leakage current of the device, inducing higher leakage current in NMOS devices and lower leakage current in PMOS devices.

7.1.2) Leakage Current and Current Measurement using the PMC

Characterizing TID-induced leakage current is built into the PMC's functionality, since transient ionizing radiation accrues dose. Leakage current is equivalent to $\tilde{I}$ from equation (2) and is equivalent to the average DC current in the absence of transient photocurrent. For NMOS targets, leakage current increases with TID and appears as an increase in integrator frequency, an example of which is shown in Fig. 7.2. This frequency increase is sufficient for characterizing increase in leakage current. Additionally, absolute values of leakage current can be determined by following the BIST procedure from section 6.1.

Though all photocurrent targets in the PMC are off-state, limiting the number of biasing choices for TID-included leakage characterization, the integrator is adaptable to targets which are not off-state. In an alternative configuration, the gate and source could be controlled externally, a configuration that could potentially allow the integrator to monitor TID-induced effects on drive current in addition to leakage current. In all cases, however, the drain of the device must be

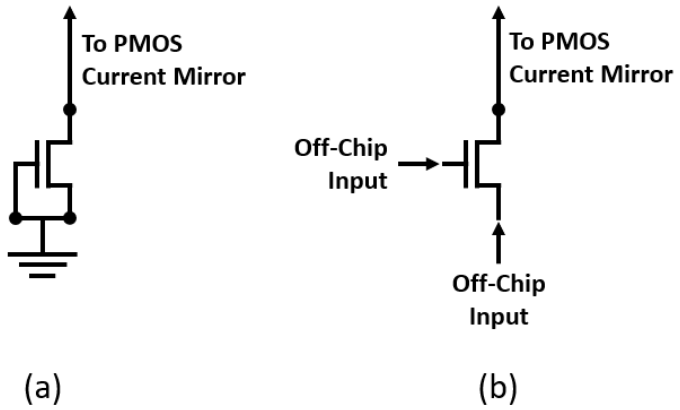


**Figure 7.3 – (a) circuit schematic of off-state targets available in the 22FDX PMC (b) circuit schematic of theoretical target configuration which enables off-chip control of the gate and source voltages**

connected to a current mirror, so this technique is limited to control over the gate and source only. Both the off-state and the controllable target configurations are shown in Fig. 7.3(a) and (b).

## 7.2. In-Situ Dosimetry and Radiation Testing

Monitoring an increase in leakage current induced by TID is a form of dosimetry. In regard to the PMC, an increase in leakage current is directly proportional to the increase in frequency, which was shown in Fig. 7.2. Provided that prior tests have been performed to relate the increase in frequency to known levels of dose, the PMC can be repurposed as an on-chip dosimeter.

To test this capability, two 22FDX die containing the PMC were setup as TID-monitors and were irradiated in the Vanderbilt ARACOR [21] up to 100 krad($SiO_2$) with measurement stops at 10, 30, 50, and 100($SiO_2$). One of these die was irradiated while all PMC targets were enabled, and the other was irradiated with all disabled. In addition, two 22FDX die containing layout-identical targets with direct measurement capability were irradiated at the same levels. As discussed in the previous section, the bias conditions for targets in the PMC are limited, and the drain voltage is unknown. To best replicate the PMC target bias conditions, the direct measurement

target's gate and source were grounded, and the drain voltage was set to 550 mV. This value was determined to be the average drain voltage of the PMC target through simulations in Cadence Virtuoso [8], where the range of drain voltages were 600mV at low leakage currents and 500 mV at high leakage currents. The PMC is also capable of grounding all nodes of the targets, so an additional set of die was irradiated in an all-grounded configuration.

### 7.3. Test Results and Discussion

The results of these tests are shown in Fig. 7.4(a-d). Frequency measurements are plotted as leakage current increase normalized to pre-irradiation measurements. Direct measurement data is plotted in blue circles, and the current-modulated frequency measurements are plotted in red squares. Error bars for direct measurement data are small enough that they are contained with the plot symbols. The bars for PMC-calculated data represent the range of leakage current jitter observed when measuring $f_{SAW}$.

The data from Fig. 7.4(a-d) indicates that on-chip measurement using the PMC is reliable until TID-induced degradation of measurement circuitry occurs after 30 krad($SiO_2$). In specific, the on-chip current mirrors are the first point of significant degradation; it was observed past 50 krad($SiO_2$) that the integrator frequency would no longer increase with all parallel arrays in the PMC enabled, indicating that the maximum current capacity of the current mirrors had been reached. This result is expected since the current mirrors in the PMC are designed to follow high-speed photocurrent transients and are not designed for TID hardness or high-current amplitudes. If a current mirror were employed having been designed for the purpose of surviving high levels of TID, the on-chip measurement technique would likely remain viable far past 50 krad($SiO_2$) for this technology.

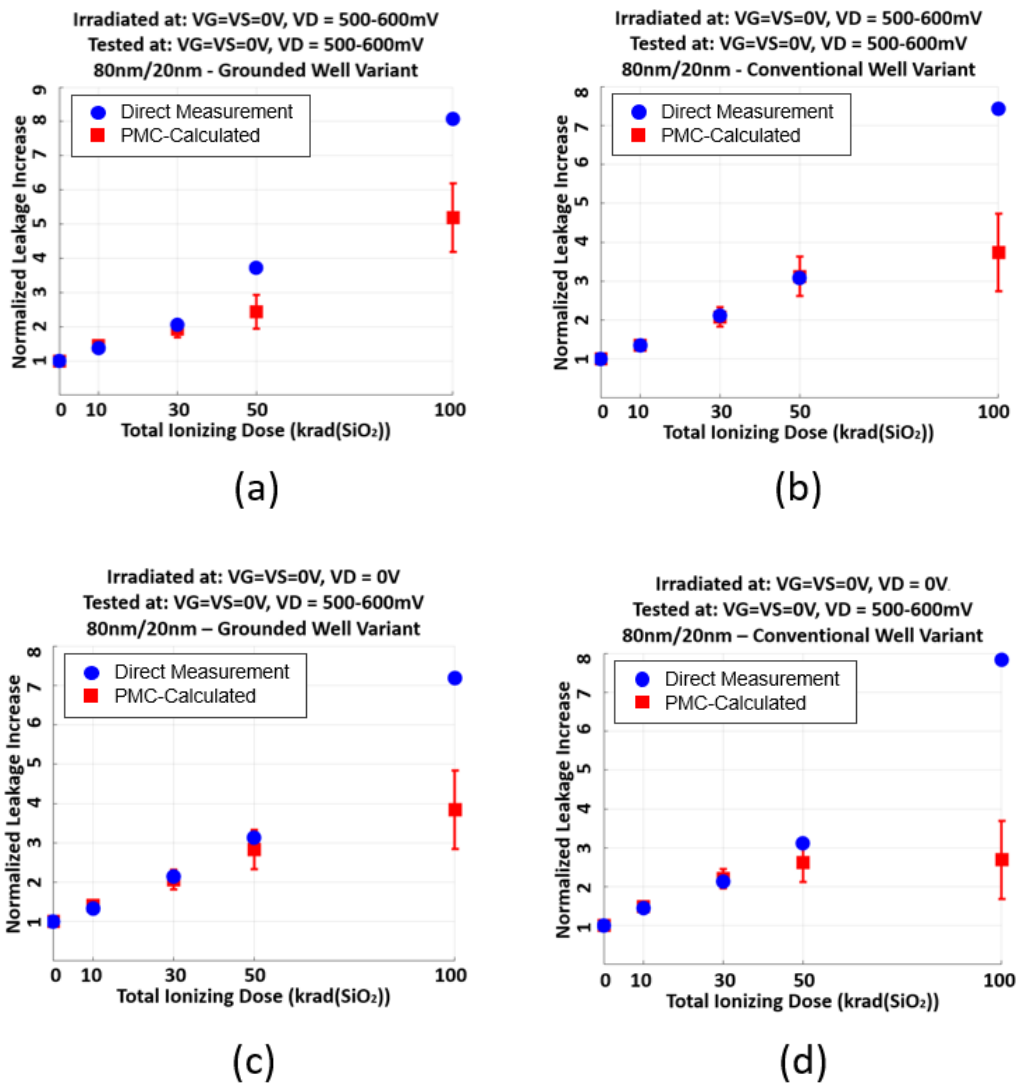


**Figure 7.4 – TID-induced leakage data from 22FDX minimum-sized devices up to 100 krad($SiO_2$). (a) High drain voltage irradiation of grounded well variant (b) High drain voltage irradiation of conventional well variant (c) Low drain voltage irradiation of grounded well variant (d) Low drain voltage irradiation of conventional well variant.**

## 7.4. Self-Compensating Back-Bias Techniques

In 22FDX technology, several well-biasing options are available. The 22FDX implementation from this work used a conventional well configuration, detailed in Fig. 7.5. The n-wells have applied back-gate bias capability of 0 to +2 V, and the p-wells from 0 to -2 V [4, 5]. These wells were implemented in the PMC for testing the effects of back-gate biasing on photocurrent generation, but the back-gate biasing capability can also be leveraged to shift the threshold voltage of both NMOS and PMOS devices. As discussed in 7.1, TID-induced degradation is primarily caused by trapped positive charge. This trapped charge can be compensated by decreasing the p-well voltage under the NMOS device in the conventional well variant. Since the targets in the 22FDX version of the PMC are NMOS, this compensation technique can be tested. However, techniques in Watkins et al. of [22] have shown that in a hybrid-well configuration, where both the NMOS and PMOS devices share a p-well, the effects of TID-induced degradation can be reversed for both NMOS and PMOS devices.

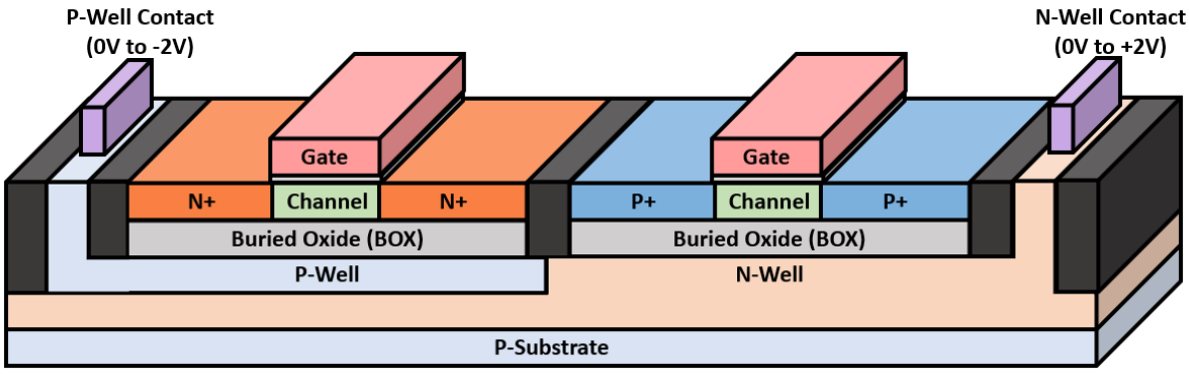


**Figure 7.5 – Illustration of a conventional well configuration for an NMOS and PMOS in the 22FDX technology. The p-well contact can be adjusted from 0V to -2V, and the n-well contact can be adjusted from 0V to +2V. The p-well's negative voltage capability can offset the threshold voltage shift induced by positive trapped charge. However, the n-well's positive voltage capability cannot mitigate the effects of positive trapped charge.**

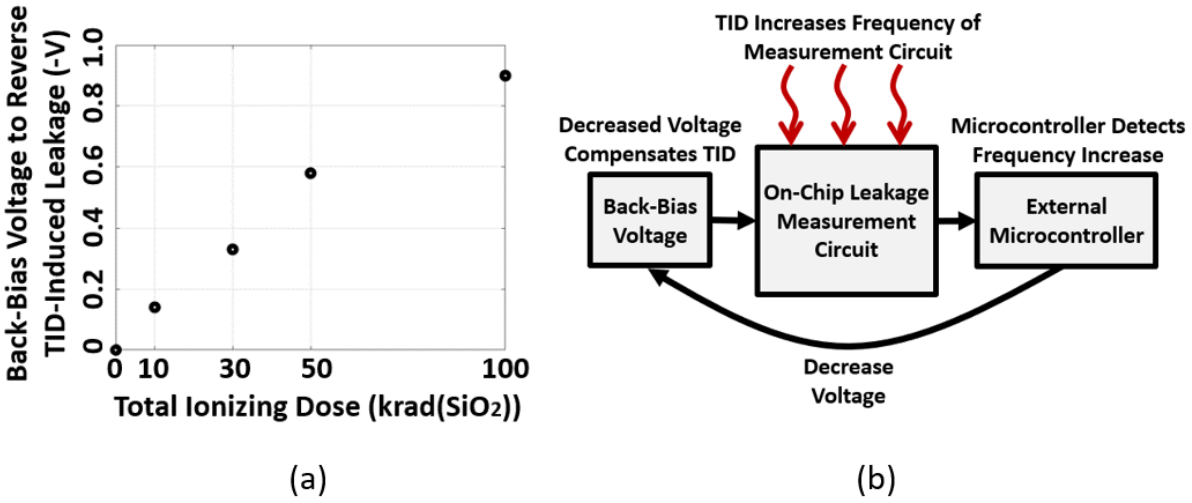


**Figure 7.6 – (a) p-well voltage required to reverse TID-induced leakage to pre-radiation levels (b) illustration of proposed feedback loop using the on-chip leakage sense capability of the PMC. An external microcontroller detects the frequency increase from the PMC and reduces the p-well voltage until the leakage returns to pre-irradiation levels.**

The current-modulated frequency enables feedback paths to control this p-well voltage. The leakage current measurement circuit does not have capabilities to measure gate voltage, but the TID-induced leakage current delta can be reversed with back-gate biasing. Though reversal of TID-induced leakage current is different than reversal of TID-induced threshold-voltage shifts, a device which has returned to pre-irradiation leakage should also experience threshold-voltage shifts that closely return to pre-radiation levels. After each irradiation step in the experiment of 7.3, the p-well back-gate bias was adjusted until perceived leakage returned to its original, pre-irradiation levels. The results of this additional test are shown in Fig. 7.6 (a). In technologies with back-gate biasing capabilities, combining the on-chip leakage measurement circuit, back-bias control, and a capable microcontroller can result in a self-TID-correctional circuit. The concept design for such a circuit is shown in Fig. 7.6 (b).

## 7.5. Background Leakage

The PMC uses transmission gates and current mirrors to isolate transient photocurrent. However, these components are also quasi-targets themselves such that they contribute leakage current to the same measurement nodes. This undesirable leakage current introduces error in measurement, and, if leakage from the targets is comparable to background leakage, distinguishing between the two can be challenging, if not impossible. Fortunately, this on-chip background leakage can be quantified by sweeping the number of active target subgroups. Fig. 7.7(a) is data taken from a ground-biased irradiated device up to 50 krad($SiO_2$). When plotting total calculated leakage current over the number of active targets, the impact of the background leakage is revealed. In this case, the background leakage is predominantly negative and approximately constant, causing the apparent current per transistor to appear reduced when fewer targets are enabled. This leakage offset increases with TID, requiring independent quantification of the offset for each irradiation step. In post-processing, this leakage current offset can be included, removing the effects of background leakage, as shown in Fig. 7.7(b).

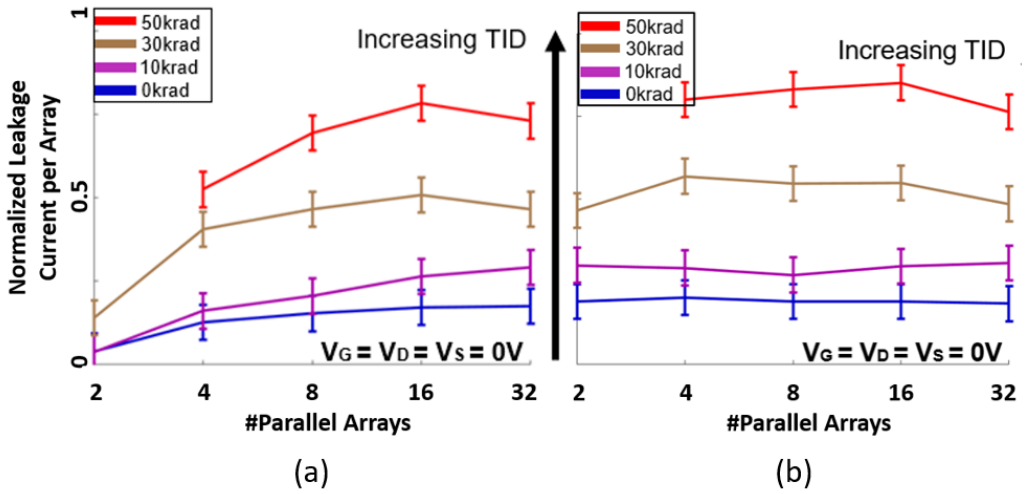


**Figure 7.7 – (a) normalized leakage divided by the number of active parallel arrays. (b) data from (a) with an empirically-found leakage offset. This offset is unique for each level of dose.**

# CHAPTER 8

## Conclusions

This work explores on-chip transient photocurrent measurement and characterization in 22FDX, a 22nm fully-depleted silicon-on-insulator technology node. Traditional off-chip measurement is not feasible in this technology due to insufficient signal-to-noise ratios from off-chip current-sensing. To resolve this challenge for 22FDX and other sub-50 nm technologies which may exhibit the same off-chip measurement challenges, an on-chip photocurrent measurement circuit design using technology-agnostic signal recovery approaches was developed. Signal recovery requirements for photocurrent in sub-50 nm technologies are demanding, but they are met through the use of several novel mixed-signal techniques, including capacitive integration and analog capacitive sampling. To demonstrate the capability to measure both primary and secondary photocurrent, the design was implemented in 22FDX and simulated in Cadence Virtuoso. The simulations mimic the in-beam behavior of photocurrent generation and indicate that the novel circuitry is effective, capturing the necessary information to recreate the photocurrent transients. Signal recovery using the digital outputs of the photocurrent measurement circuit and post-processing was shown to be effective at reconstructing the device-level photocurrent response.

In addition to transient photocurrent measurement, the circuit can be repurposed as a leakage current measurement circuit, capable of capturing the increase of total-ionizing-dose-induced leakage current. The 22FDX photocurrent measurement circuit was taped-out, incorporated in a test characterization vehicle, and irradiated up to 100 krad($SiO_2$). The total-ionizing-dose-induced leakage current increase for several NMOS targets was shown to be

comparable to direct-measurements of layout-identical targets. Finally, this circuit additionally shows promise as an on-chip dosimeter, and in combination with TID-mitigating back-bias techniques, could potentially be implemented as a circuit which calculates the level of dose and adjusts back-gate voltage to compensate accordingly.

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