ION-INDUCED SINGLE-EVENT BURNOUT MECHANISMS IN SIC POWER MOSFETS AND DIODES

By

Dennis R. Ball, II

Dissertation

Submitted to the Faculty of the

Graduate School of Vanderbilt University

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

June 30, 2020

Nashville, Tennessee

Approved:

Kenneth F. Galloway, Ph.D.

Ronald D. Schrimpf, Ph.D.

Arthur F. Witulski, Ph.D.

Michael L. Alles, Ph.D.

Joshua D. Caldwell, Ph.D.

© Copyright by Dennis R. Ball, II 2020

All Rights Reserved

DEDICATION

This dissertation is dedicated to my wife, Andrea, and sons, Easton, Rowan, and Landon.

ACKNOWLEDGEMENTS

The body of research detailed in this dissertation would not have been possible without the support of NASA, through the Early Stage Innovations (ESI) program and managed by Goddard Space Flight Center. Additional acknowledgment goes to the University Programs of Synopsys, Inc. for providing access to Technology Computer-Aided Design (TCAD) tools used in this research.

I would like to express my thanks and appreciation to my committee members for their support and enthusiasm for the research detailed in this dissertation. Dr. Ken Galloway and I were discussing my career several years ago and the possibility of pursuing a doctorate came up, and after a few minutes he looked at me and said "Well, Scooter...why not." For those that know him, you will understand why there is a period and not a question mark at the end of that quote! Dr. Galloway's encouragement and guidance have been invaluable during this research. Even more importantly, I am thankful that he has such a positive attitude and spirit. A special thank you goes to Dr. Ron Schrimpf, who is primarily responsible for my being at Vanderbilt/ISDE in the first place, and has been a mentor for the entirety of my career. Dr. Mike Alles has also been a great advisor, not only for his participation in this program, but also for the guidance that he has given me through the years. I have been extremely fortunate to have benefited directly from his interests in just about anything related to radiation in a semiconductor device, and so very much of my career has been working with him on so many different projects. Dr. Art Witulski's patience and ability to step away from his desk and pick up a pen and walk through a calculation or brainstorm an idea has been extremely helpful. I am very grateful to

Dr. Josh Caldwell and his support of my research, and his willingness to be a part of this team and my committee.

I am also very appreciative of the support and effort of the team that worked together as part of this research program. Dr. Robert Reed, Dr. Andrew Sternberg, Dr. John Hutson, Dr. Jean-Marie Lauenstein, Dr. Arto Javanainen, and Robert Johnson have been instrumental in discussions about pretty much every facet of this research. There is no "I" in "team", and while this work is my own, there is a tremendously collaborative effort among my entire committee and the other members of this research team, and I would not have gotten to this point without them.

I would also like to express my gratitude to VU RER faculty, Dr. Lloyd Massengill, Dr. Bharat Bhuva, Dr. Tim Holman, Dr. Dan Fleetwood, Dr. Jeff Kauppila, and Dr. Brian Sierawski. I have been extremely fortunate to have worked with each of them on a wide range of programs over my career as an engineer at ISDE. While this disseration is focused on one specific research area, I feel that my entire basis of knowledge is much more broad, and stems from having worked with these faculty members over the years.

I am thankful for my colleagues and co-workers at the Institute for Space and Defense Electronics. Dr. Kevin Warren, Tim Haeffner, and Mike McCurdy have all contributed to my research in some manner. I have always thought it important to understand my limitations, and being part of a team that can pretty much do anything is highly rewarding.

I am also deeply grateful to my wife, Andrea, and my sons, Easton, Rowan, and Landon. Let's face it, they are the best part of my life, and every day with my family is such an adventure.

TABLE OF CONTENTS

Page

DEDICATION iii

ACKNOWLEDGEMENTS iv

LIST OF TABLES viii

LIST OF FIGURES ix

Chapter

I. INTRODUCTION 1

II. POWER DEVICE STRUCTURE AND OPERATION 6

Power Device Structure 6
Power Device Safe Operating Area 10

III. 3D TCAD MODEL DEVELOPMENT 12

Physical Device Design 13
Electrical Breakdown Simulation 16

IV. RADIATION-INDUCED SINGLE-EVENT EFFECTS BACKGROUND 25

Space Radiation Environment 28
Single-Event Burnout - Si Power Devices 30
MOSFETs 30
Diodes 34
Derating 38
Single-Event Burnout - SiC Power Devices 39
JBS Diodes 39
MOSFETs 43
Thermal Simulation Analysis 45
Derating 48

V. IDENTIFYING COMMON TRENDS FOR SINGLE-EVENT BURNOUT IN SIC POWER MOSFETS AND DIODES 50

1200 V SiC 51
650 V - 3300 V SiC 57

VI. ION-INDUCED ENERGY PULSE MECHANISM 61

Resistive Shunt Effects . . . 61
Energy Pulse Mechanism . . . 72
Inline Resistor Effects . . . 75
Localized Thermal Effects . . . 78

VII. EVALUATION OF DEVICE VARIANTS . . . 83

MOSFET Device Variants - Epitaxial Design . . . 84
MOSFET Device Variants - Ion Simulations . . . 86

VIII. MITIGATING SINGLE-EVENT BURNOUT THROUGH DEVICE SELECTION AND CIRCUIT DESIGN . . . 93

Silicon vs. SiC . . . 94
SiC: 1200 V vs. 3300 V . . . 97
System Transmission Power Losses . . . 97
Switching MOSFET Power Losses . . . 99

IX. IMPACT AND CONCLUSIONS . . . 102

REFERENCES . . . 106

Appendix

A. POSITIVE FEEDBACK LOOP: PARASITIC BJT AND IMPACT IONIZATION . . . 113

Parasitic BJT . . . 114
Impact Ionization . . . 118

B. NEUTRON-INDUCED SECONDARY PARTICLE GENERATION . . . 127

LIST OF TABLES

Table | Page

1. Comparison of on-state resistance and rated current for two commercially available power MOSFETs, one silicon and one SiC [12], [13] 8
2. Electrical property comparison of Silicon and SiC after Choi *et al.* [14] 9
3. Parameters Used in TCAD Simulations for MOSFETs and Diodes . . . 14
4. Measured degradation and catastrophic failure regions for SiC power MOSFETs after Lauenstein *et al.* [6] 43
5. Ion Beam Characteristics with SEB_{TH} shown 53
6. TCAD-simulated maximum lattice temperature as a function of device bias and particle LET 78
7. 3D TCAD-simulated maximum lattice temperature as a function of ion strike location for ion LET (in MeV-cm^2/mg) and bias consistent with the single-event burnout threshold for 1200 V SiC JBS diode and SiC MOSFET. DNC indicates a simulation that Did Not Converge 81
8. 3D TCAD Simulation Results Indicating Positive Feedback as a function of Ion Strike Location, LET, and Bias 126

LIST OF FIGURES

Figure Page

1. Typical cross-sections for planar, vertical power junction-barrier Schottky diode and power MOSFET 7

2. Typical cross-section of a power MOSFET defining resistive paths through the device after Havanur *et al.* [11] 8

3. Electric field concept comparison of silicon and SiC as a function of distance, W_n. The area under each field curve is the junction voltage, which is equal in this example 10

4. Conceptual example of a power MOSFET being used as a switch to drive a load (left) and the safe-operating area (SOA) (right). An actual circuit will also have a diode from drain to ground for inductive current flow when the transistor is OFF 11

5. 3D TCAD model of a 1200 V SiC power MOSFET (top left) and JBS diode (top right) showing device structure (epi doping/depth). 2D-cutplanes indicating current flow in forward operation (middle) and fully-depleted epitaxial region at 1200 V (bottom) 15

6. 2D-cutplanes of the electron density for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V 18

7. 2D-cutplanes of the internal electric field for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V 19

8. 1D-cutlines of the internal electric field for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V 20

9. 2D-cutplanes of the internal electrostatic potential for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V 21

10. 1D-cutlines of the internal electrostatic potential for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V 21

11. 3D TCAD-simulated electrical avalanche breakdown as a function of reverse bias for 1200 V SiC power MOSFET and diode 23

12. 3D TCAD-simulated electrical avalanche breakdown as a function of reverse bias for 1200 V SiC power MOSFET and diode 23

13. Example of a power MOSFET in the OFF-state hit by an ion (left), forcing a high-current, high-voltage state that may be non-stable and outside of the SOA . . . 27

14. Schematic cross-sections for vertical power junction-barrier Schottky diode and power MOSFET indicating electron-hole pairs generated by the passage of a heavy ion . . . 29

15. Example of SEB during heavy ion irradiation of a power MOSFET. Sudden drain current increase indicates drain-to-source short circuit after Titus *et al.* [30] . . . 31

16. Before and after photos of SEB. Visible physical damage is a likely indicator of SEB after Titus *et al.* [30] . . . 31

17. Inherent N-P-N parasitic BJT transistor in a vertical DMOS device after Johnson *et al.* [32] . . . 32

18. Electric field distribution pre-strike (A) and post-strike (B and C) for simulated ion strike in a power MOSFET. A to B to C represents an evolution of the electric field as a function of time after Liu *et al.* [31] 33

19. Oscilloscope recording of reverse blocking current and voltage during failure. The destructive current develops in less than 10 ns after Kabza *et al.* [33]. . . . 35

20. Charge spectrum from the bombardment of a 4kV diode with 90 MeV Kr ions showing the number of events as a function of the total generated charge with increasing the applied voltage after Maier *et al.* [34]. . . . 36

21. Output currents of isothermal and non-isothermal simulations with LET = 30 MeV-cm^2/mg and V = 3500 V (top), along with maximum temperature due to self-heating (bottom) after Walker *et al.* [36]. . . . 37

22. Collected charge as a function of reverse bias voltage observed in SiC Schottky diodes after Kuboyama *et al.* [42] . . . 40

23. Measured diode current versus time during heavy-ion irradiation for two diodes, showing discrete increases in leakage current with individual heavy ions, with self-heating effect. Xenon flux was 68, and Neon was 5.7–6.1 ions/cm^2/s after Witulski *et al.* [18] . . . 41

24. SEB events for three different 1200 V JBS diodes. Xenon flux was 68, and Neon was 5.7–6.1 ions/cm^2/s. All diodes are irradiated at room temperature after Witulski *et al.* [18] . . . 41

25. Measured degradation mode thresholds as functions of applied bias and LET. The width of the line indicates minimum voltage at which burnout was observed and maximum voltage with no burnout observed after Witulski *et al.* [18] 42

26. MOSFET drain current as a function of time during irradiation A) No damage, B) Leakage current degradation, and C) Catastrophic failure after Lauenstein *et al.* [6] 44

27. Electric field and temperature distribution along ion track after Kr ion strike under 220 V of reverse bias after Kuboyama *et al.* [42] 47

28. 3D TCAD simulations of ion-induced temperature increase in SiC power MOSFET for LET = 46 MeV-cm^2/mg varying bias and hit location after McPherson *et al.* [48] 47

29. Single-event burnout voltage normalized to rated breakdown voltage as a function of ion LET for SiC Schottky diodes (top) and MOSFETs (bottom) showing that 50% device de-rating is not sufficient for survivability after Lauenstein *et al.* [45] 49

30. Single-event burnout and degradation threshold bias voltages vs. LET for 1200 V SiC power MOSFETs taken during this work and compared to published literature [19], [45], [46], [50]. 52

31. Single-event burnout and degradation threshold bias voltages vs. LET for 1200 V SiC power diodes taken during this work and compared to published literature after Witulski *et al.* [18] 53

32. Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes for data taken during this work and compared to published literature [18], [19], [45], [46], [50] 56

33. Circuit schematic for a non-destructive test technique for silicon power devices with a resistor inline between the power supply and the drain node 57

34. Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes [18], [19], [45], [46], [49], [50]. 59

35. Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes after Lichtenwalner *et al.* and Akturk *et al.* [56], [57] 60

36. 3D TCAD model of a 1200 V SiC power MOSFET (top left) and JBS diode (top right) showing device structure (epi doping/depth). 2D-cutplanes indicating current flow in forward operation (middle) and fully-depleted epitaxial region at 1200 V (bottom) 62

37. Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias . . 64

38. 2D-cutplanes in TCAD showing electron and hole current densities exceeding 1x10^7 A/cm^2 for a particle with LET = 10 MeV-cm2/mg with 500 V drain bias. 2D-cutlplanes taken at 5 ps following the ion strike. . 65

39. 2D-cutplanes in TCAD showing internal electrostatic potential and electric field ino-induced re-distribution, with electric fields exceeding 3.2 MV/cm for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 2D-cutlplanes taken at 5 ps following the ion strike. 66

40. 1D-cutline in TCAD showing pre- and post-strike electric fields exceeding 3.2 MV/cm for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike. 67

41. 1D-cutline in TCAD showing pre- and post-strike internal electrostatic potential (bottom) for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike. 68

42. 1D-cutline in TCAD showing post-strike power density for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike. 70

43. 1D-cutline in TCAD showing post-strike cumulative power density for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike. 71

44. 1D-cutline in TCAD showing post-strike power density and cumulative power density for a particle with LET = 4 and 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike. . . 73

45. TCAD calculated energy dissipation for 10 ps following the strike with the SEB$_{TH}$ conditions highlighted. 74

46. Circuit schematic for a 3D-TCAD mixed mode ion-strike simulation with a resistor inline between the power supply and the drain node 75

47. 3D TCAD mixed-mode ion-strike simulations for both the MOSFET and JBS diode using non-destructive technique for adding a resistor inline with the power supply. Ion LET=10 MeV-cm^2/mg and devices biased at 500 V 77

48. 3D TCAD simulated maximum lattice temperature for ion LET (in MeV-cm^2/mg) and bias consistent with the single-event burnout threshold for 1200 V SiC JBS diode (top) and SiC MOSFET (bottom) 80

49. 3D TCAD model of a 1200 V SiC power JBS diode showing device structure, also shown is a representative long-range ion track (top). 1D-cutlines of net doping through the epi and drain regions for each variant (bottom) 85

50. Ion-induced electron current density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias. 86

51. Ion-induced hole current density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias. 87

52. Ion-induced hole electric field re-distribution at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias. 88

53. Ion-induced total power density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias. 89

54. Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias . . 90

55. Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias . . 91

56. One-dimensional specific on-resistance versus breakdown voltage comparing silicon, silicon carbide, and gallium nitride after Gajewski *et al.* [16] 96

57. TCAD simulations of collected charge in a MOSFET for a constant amount of deposited charge but varying location and bias are shown in (a). TCAD simulations of collected charge in a diode for a constant amount of deposited charge but varying location and bias (b). For (a) and (b), a strike location of 0 is at the center of the epitaxial region near the surface between two p-doped regions. after Johnson *et al.* [75] . . . 116

58. TCAD simulations of collected charge in a MOSFET and diode for a constant amount of deposited charge in the most sensitive location but varying bias after Johnson *et al.* [75] 117

59. TCAD heavy ion simulations of SiC power MOSFET, showing single-event burnout at 800 V at LET=5 MeV-cm^2/mg with impact ionization turned on, and device recovery at other conditions. 119

60. 2D cross-section TCAD time slice 250ps after the strike occurs, showing hole current density (A/cm^2) (top), electron current density (bottom) with impact ionization turned off, for LET=5 MeV-cm^2/mg at VD=800 V. Blue indicates a current density of 1 A/cm^2 while red indicates a current density of 106 A/cm^2. 121

61. 2D cross-section TCAD time slice 250ps after the strike occurs, showing hole current density (A/cm^2) (top), electron current density (bottom) with impact ionization turned on, for LET=5 MeV-cm^2/mg at VD=800 V. Blue indicates a current density of 1 A/cm^2 while red indicates a current density of 106 A/cm^2. 122

62. Impact ionization (per cm^2-s) at the epi/drain junction at 250 ps after the strike occurs for LET=10 MeV-cm^2/mg at VD=800 V. Impact ionization rate ranges from 1e10 cm-3•s-1 (blue color) to 1e27 cm-3•s-1 (red color) 123

63. TCAD heavy ion simulations of a SiC power MOSFET, showing drain current transient as a function of LET with the drain biased at 500 V. At LETs of 20 MeV-cm^2/mg and greater, the drain current runs away, indicating a positive feedback loop between a parasitic BJT and impact ionization. 124

64. 2D cross-section of TCAD model, with arrows indicating varied ion strike locations. In all cases, ion is at normal incidence. 125

65. TCAD representation of an MRED-generated nuclear event. The shaded volumes represent the sensitive nodes of the memory device. The incident neutron enters and induces a nuclear event. The shower of secondary products includes alpha particles, protons, neutrons, gamma rays, and a carbon heavy ion after Tipton *et al.* [81] 129

66. Neutron spectrum from LANL [67] that closely matches the terrestrial neutron spectrum, and is used for MRED simulations. 130

67. Secondary particles (showing range and LET) generated from neutron environment and entering the primary sensitive volume as calculated by MRED. 131

CHAPTER I

INTRODUCTION

Growth of the global power semiconductor industry hinges upon developing new technologies and products that can meet a wide range of voltage specifications, while providing higher power efficiency in a smaller package when compared to previous technologies. Applications range from low-voltage healthcare devices to high-power space, aerospace, automotive, and defense systems. Historically, power devices were all silicon-based, however, the past two decades have shown tremendous achievements in the use of wide-bandgap materials, such as silicon carbide (SiC), with the first commercially available 1200 V SiC power junction barrier Schottky diode offered in 2006 and the first 1200 V SiC power MOSFET offered in 2011 [1].

Silicon carbide is superior to silicon due to higher breakdown electric fields, increased thermal conductivity and significantly lower on-state resistance, all of which result in size, weight, and power (SWaP), and overall cost savings [2]. Over twenty automotive companies are using SiC power MOSFETs and diodes for onboard charging systems in their electric and hybrid-electric vehicles [3] in addition to many other applications. The global SiC power semiconductor market size was valued at $302M in 2017, and projected to reach $1.1B by 2025 [4], with 90% of the market focused on terrestrial applications, and 10% devoted to aerospace and defense applications [5], which would include space systems. The SWaP benefits of SiC over silicon make these power devices ideal candidates for space-based applications. These features are of interest to both National Aeronautics and Space Administration

(NASA) and European Space Agency (ESA) for use in space vehicles, such as the Orion Spacecraft and the Venus Mobile Explorer [6], in addition to space solar arrays and a variety of other applications and interplanetary missions. However, microelectronic devices and circuits used in space may be susceptible to naturally occurring radiation, such as heavy ions.

Obtaining radiation data for semiconductor devices is an expensive, time-consuming task with single-event burnout (SEB) testing particularly challenging because of the destructive nature of the test. The safe operating area (SOA) for 1200 V SiC power MOSFETs and diodes has been characterized to a limited extent through test campaigns, however, little insight has been gained into the physical mechanism(s) that may be responsible for ion-induced single-event burnout. Understanding these mechanisms is imperative for organizations, such as NASA and ESA, for making space-flight hardware design decisions to mitigate risk of operational failure during a mission. Ion-induced radiation data for power devices reflects the response of a device from the perspective of an electrical terminal, or better defined as "on the outside looking in". Modeling and simulation tools, such as 3D Technology Aided Design (TCAD), provide the capability to explore the physical response of a device to radiation, leveraging available data to validate modeling and simulation efforts.

Historically, it has been thought that there are separate mechanisms responsible for the catastrophic failures observed in silicon power diodes (localized avalanche breakdown due to ion-induced electric field spikes) and silicon power MOSFETs (parasitic bipolar junction transistor), resulting in differing single-event burnout responses between the two types of devices. A natural assumption is that separate mechanisms are also responsible for single-event burnout in SiC power diodes and

MOSFETs. However, that is not the case. In this work, industry-generated heavy ion data is compiled and combined with new data, identifying matching single-event burnout thresholds for the 1200 V power MOSFETs and diodes. Analysis of these heavy-ion data indicates that the devices have a common mechanism responsible for the catastrophic failures.

Insight into failure mechanisms is developed through the use of 3D TCAD simulations, which are used to identify similarities in both structures during an ion event. The simulation results show a resistive shunt effect capable of generating very high localized current transients during an ion strike, and consequently, significant energy dissipation. For LET and bias conditions matching the single-event burnout threshold data, a constant amount of energy dissipation is calculated through analysis of TCAD simulation results. Ion-induced, highly-localized energy pulses are proposed as a common mechanism responsible for catastrophic single-event burnout in 1200 V SiC power MOSFETs and JBS diodes.

The 3D TCAD framework developed in this work also provides an opportunity to efficiently evaluate the effects of an ion-strike on a variety of device variants (doping and dimension). Understanding how these variants perform following an incident heavy-ion strike will provide design teams an opportunity to consider alternate device designs that may meet the mission specification or otherwise mitigate the risk associated with single-event burnout during flight. This analysis may also prove to be useful for manufacturers that are interested in exploring radiation-hardened device development, further driving innovation for device reliability.

Typically, using a commercial off-the-shelf part is less expensive than using a special radiation-hardened device. Successfully designing a power electronic circuit to

operate while minimizing the risk of single-event burnout causing catastrophic failure of the circuit is important for both space and terrestrial applications. Circuit designers must understand the environment and the mechanisms contributing to single-event burnout in order to appropriately select parts. In this work, 1200 V and 3300 V SiC power MOSFETs are compared for operation in a circuit, with insight provided into the concept of voltage derating and a trade-off analysis focused primarily on power losses during operation. Implications for part selection and circuit design show that using a 3300 V power MOSFET provides ample single-event burnout threshold margin for space applications up to 650 V for most space environments, while the 1200 V device is susceptible to single-event burnout.

In this dissertation, Chapter II provides a brief overview of vertical power device structure and electrical operation, along with introducing the electrical benefits of SiC compared to silicon power devices. The development of 3D Technology Computer-Aided Design (TCAD) models for both the 1200 V power MOSFET and JBS diode are discussed in Chapter III. This discussion provides detailed information about the physical structure (doping and dimensions) along with the electrical characteristics (current and voltage) for each device, establishing the similarity between the MOSFET and the diode. Historical concepts of single-event burnout and the effects of ion-induced charge deposition in power devices are explored in Chapter IV. This work identifies a unique similarity in the single-event burnout response of SiC power MOSFETs and JBS diodes in Chapter V, leveraging ion-induced single-event burnout data from available literature, in addition to describing data taken during this work. A novel method for analyzing ion-induced energy pulses for both diodes and MOSFETs is presented in Chapter VI. In Chapter VII,

evaluation of ion-induced effects on device variants is explored and potential trade-offs in performance are discussed. Finally, Chapter VIII provides considerations for circuit designers and risk mitigation in heavy ion environments. Chapter IX discusses the impact of this work for the radiation effects community.

There is an Appendix A for discussion about the role of the parasitic bipolar junction transistor turn-on following an ion strike in the SiC power MOSFET, and a final Appendix B providing discussion about neutron-induced secondary particle generation in SiC in a terrestrial environment.

CHAPTER II

POWER DEVICE STRUCTURE AND OPERATION

An estimated 50% of the electricity used in the world is controlled by power devices [7], with applications ranging from consumer, industrial, medical, and transportation. Efficiency and cost of systems drives innovation, with silicon power devices dominating the market for the past few decades. However, silicon power devices have proven to have significant conduction power losses for high-voltage applications due to the design of the device. Silicon carbide provides vast improvements in size, weight, and power, when compared to silicon because of the superior electrical properties of SiC over silicon [7]. This chapter discusses the general power device structure and compares silicon to SiC, while also introducing the safe operating area for power devices.

Power Device Structure

Power MOSFETs are the most commonly used power devices for a wide range of applications, such as power supplies, DC-to-DC converters, and motor controllers [8], while power diodes are commonly used in rectifying circuits [9]. Commercially available power MOSFETs and JBS diodes typically have a vertical structure which provides higher breakdown voltages, lower on-state resistance, and higher current than a lateral structure. The MOSFETs are commonly called Vertical Double-Diffused MOSFETs, or VDMOS [10] due to the double-diffusion process for creating the source and body regions. A Junction-Barrier Schottky (JBS) diode can be designed

in the same process as the MOSFET, with the exceptions of no source implant and replacing the gate stack with a Schottky contact. Typical cross-sections of each device are shown in Figure 1. Most MOSFETs are NMOSFETs with the starting wafer a

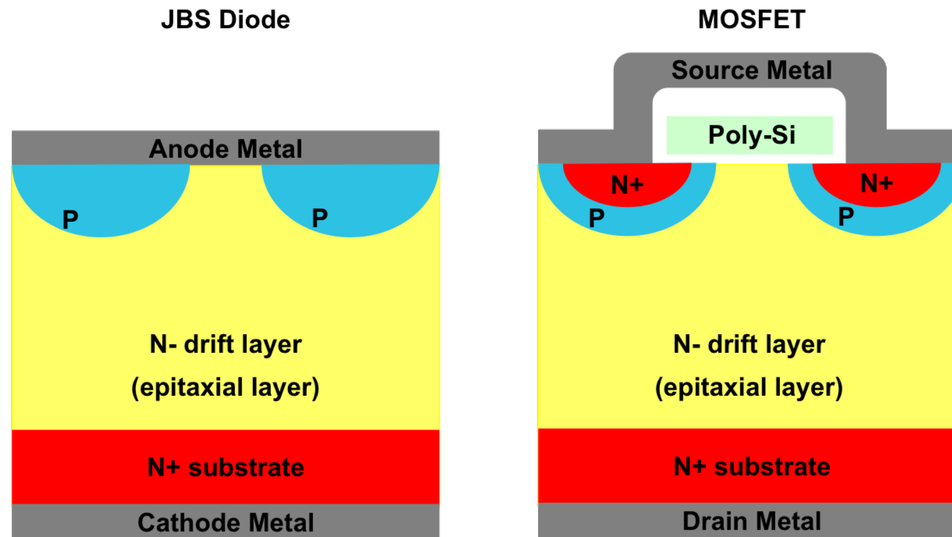


Figure 1: Typical cross-sections for planar, vertical power junction-barrier Schottky diode and power MOSFET

heavily doped n-type substrate. The n-type drift layer, the epitaxial layer or epi region, is then grown onto the substrate, and will be lightly doped. The doping of the epi region sets the breakdown voltage, with the thickness of the epi region designed to allow for full depletion of the epi region under reverse bias. Subsequent processing steps involve implanting the p-type body region and the heavily doped n-type source, followed by growing a gate oxide and depositing the back end of line metal layers. In both the JBS diode and the MOSFET, current flow is vertical when the device is ON, and when the device is OFF, the applied bias is supported across the entire epi region. In a power device, the doping and thickness of the epitaxial layer set the primary characteristics of the device with respect to breakdown voltage and current capacity. Resistance through the epi region increases as the epi thickness

increases and the doping density decreases. The resistive paths through the device are shown in Figure 2 [11], with the resistance through the epi region dominating the total resistance along the path of current flow. For silicon power devices, designing a high-voltage, low-resistance device has proven to be challenging, with an example of a silicon power MOSFET rated at 1000 V [12] and 8 A, with 1450 mΩs of on-state resistance (R_{ON}), shown in Table 1. This particular device was chosen because the rated breakdown voltage is similar to the rated breakdown voltage of the SiC power MOSFETs that are discussed in this work.

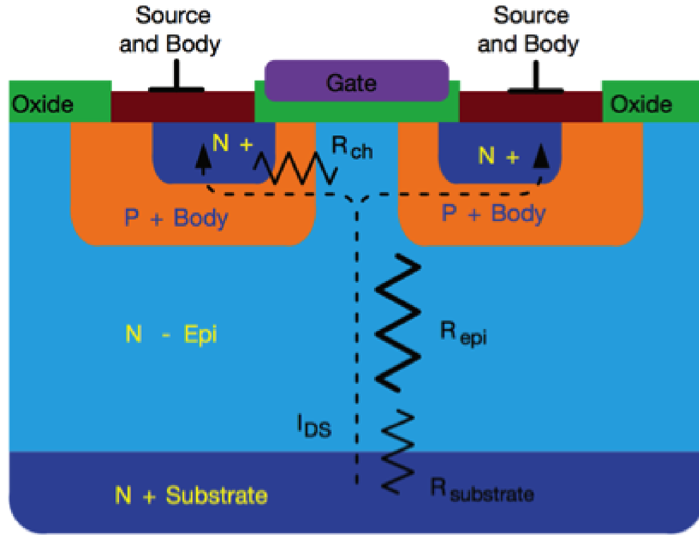


Figure 2: Typical cross-section of a power MOSFET defining resistive paths through the device after Havanur *et al.* [11]

Table 1: Comparison of on-state resistance and rated current for two commercially available power MOSFETs, one silicon and one SiC [12], [13]

Device	Material	$V_{BREAKDOWN}$ [V]	$R_{DS,ON}$ [mΩs]	I_{RATED} [A]
FQA8N100C	Si	1000	1450	8
C2M0080120D	SiC	1200	80	36

Silicon carbide (SiC) is superior to silicon for use in many power device applications due to significantly higher breakdown electric fields and significantly lower on-state resistance [2]. These benefits can be attributed to the electrical properties of SiC compared to silicon, a few of which are summarized [14] and shown in Table 2. A semiconductor with a wide bandgap requires more energy to produce carriers through impact ionization which leads to electrical breakdown than a semiconductor with a narrow bandgap. SiC has a bandgap of 3.3 eV, compared to 1.1 eV for silicon, which results in a critical electric field in SiC of 2-3 MV/cm compared to 0.2-0.3 MV/cm in silicon. This concept can be visualized by considering the peak electric field as a function of distance (W_n) for both SiC and silicon, as shown in Figure 3. For a given applied potential (the area under the electric field curve), the electric field in SiC reaches a much higher peak over a shorter distance when compared to silicon. This effect directly results in lower on-state resistance and higher drive currents for SiC compared to silicon. The electrical characteristics of SiC have resulted in commercially available high-voltage and low-resistance devices, with a 1200 V SiC MOSFET providing 36 A at 80 mΩ of on-state resistance [13], also shown in Table 1.

Table 2: Electrical property comparison of Silicon and SiC after Choi *et al.* [14]

Electrical Property	Si	SiC (4H)
Band Gap Energy (eV)	1.12	3.28
Critical Electric Field (MV/cm)	0.29	2.5
Electron Mobility (cm^2)/VS	1200	800
Hole Mobility (cm^2)/VS	490	115
Thermal Conductivity (W/cmK)	1.5	3.8
Maximum Junction Temperature (C)	150	600

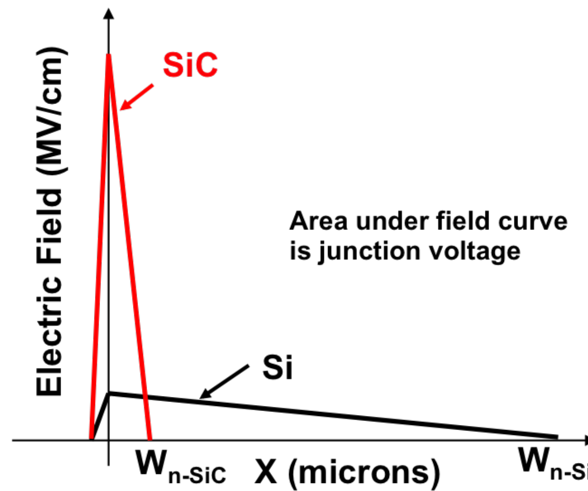


Figure 3: Electric field concept comparison of silicon and SiC as a function of distance, W_n. The area under each field curve is the junction voltage, which is equal in this example

Power Device Safe Operating Area

Power devices are intended to operate in either a high-voltage, low-current state, or a low-voltage, high-current state to prevent significant power dissipation that may impact device and/or circuit reliability. An example of a power MOSFET being used as a switch to drive a load and the current/voltage safe operating area (SOA) is shown in Figure 4. Note that this figure is conceptual, and an actual circuit will have a diode connected from the drain to ground to allow a path for inductive current to flow when the MOSFET is OFF. When the MOSFET driving the load is turned OFF, the drain is biased at the supply voltage, and the drain current through the circuit is minimized, referred to as OFF-state leakage current. As the MOSFET is slowly turned ON by increasing the gate voltage, the drain current increases significantly while the drain-to-source voltage drops. The device is stable in both OFF and ON states. During the transition from OFF to ON, the gate voltage is controlled in such

a way as not to exceed the switching speed of the device, typically in the tens to hundreds of nanoseconds for a power MOSFET [13], maintaining stability through the transition. In addition to the device and circuit being stable, power dissipation, or the product of current times voltage, is maintained in such a way that the device can continue to operate without physical damage. Significant power dissipation can result in catastrophic device failure, such as the separation of metal lines from the semiconductor surface, electromigration of metal through a metal/semiconductor interface, or thermal heating leading to metal and/or semiconductor damage.

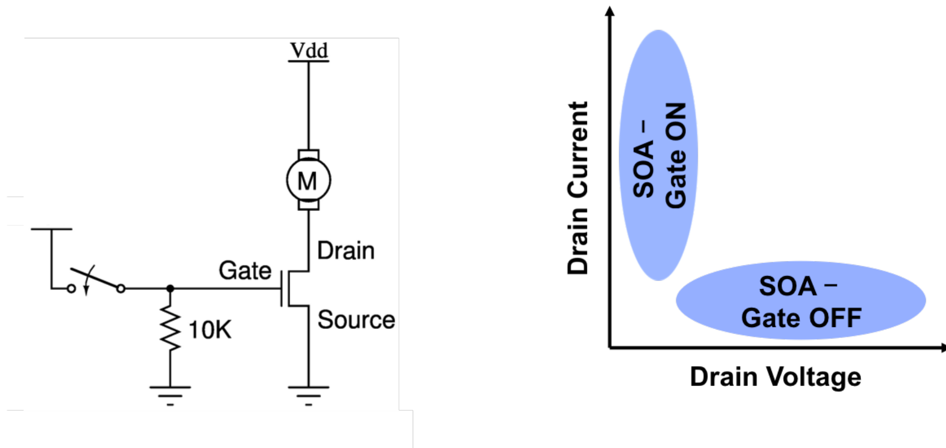


Figure 4: Conceptual example of a power MOSFET being used as a switch to drive a load (left) and the safe-operating area (SOA) (right). An actual circuit will also have a diode from drain to ground for inductive current flow when the transistor is OFF

CHAPTER III

3D TCAD MODEL DEVELOPMENT

Chapter II provided a brief overview of vertical power device structure and electrical operation, along with introducing the electrical benefits of SiC compared to silicon. In this chapter, a detailed discussion of a 1200 V SiC power MOSFET and a 1200 V JBS diode is provided, to include both physical (doping and dimension) and electrical (current and voltage) characteristics. Both the MOSFET and the JBS diode can have the same breakdown voltage, indicating that the devices share the same or very similar doping, epitaxial dimensions, and other physical geometries. Of particular importance to this work is that the rated breakdown voltage, 1200 V, is consistent between both devices, and is typically determined experimentally by device manufacturers. The data that will be shown in Chapter V is for 1200 V commercial devices. For specifying the device breakdown rating, most manufacturers use an unclamped inductive switching (UIS) test methodology (established as a JEDEC standard [15]) to determine an avalanche safe operating area (SOA) for the SiC devices. In these devices, there are zero failures in 1000 hours at low avalanche conditions, 1200 V at 150 C, hence, the 1200 V rated breakdown voltage [16].

Electrical data, both before and after radiation exposure, provide insight into the behavior of a semiconductor device from an external point of view, where measurement equipment can characterize current and voltage. 3D Technology Computer-Aided Design (TCAD) tools provide an opportunity to investigate internal device physics, such as current density, electric field, and impact ionization. TCAD

tools are finite-element based solvers for carrier diffusion and transport, solving Poisson's and the electron and hole continuity partial differential sets of coupled equations. The remainder of this chapter will discuss the physical 3D model, followed by the electrical breakdown operation.

Physical Device Design

Typically, power devices are designed to take advantage of a large die area, for example, 2 mm x 3 mm. Either a honeycomb or a striped cell design is commonly used and a device is composed of many cells in parallel. 3D TCAD models of a single cell, 1200 V SiC power MOSFET and JBS diode, Figure 5 (top), were developed in the Synopsys Sentaurus suite of TCAD tools, version K-2015.06, [17], based on information from published literature [18], [19]. The devices have an epitaxial thickness of 10 μm, with doping of 8x10^{15} cm^{-3} N-type, with an additional 15 μm of highly-doped N+ drain (the highly-doped drain is truncated in Figure 5 for visualization purposes). Otherwise, the models shown in Figure 5 are to-scale, with the thickness of the epitaxial region indicated for guidance. Additional parameters are listed in Table 3.

Both devices have the same P-type body doping at the surface of the device, seen more clearly in the 2D-cutplanes, also shown in Figure 5. In the JBS diode, after implanting the P-type body doping, the surface metallization is deposited. The JBS diode has been designed in such a way that the device can operate as a P-i-N diode when reverse-biased, and as a Schottky diode when forward-biased [20], with representative electron current flow indicated in Figure 5 (middle). The MOSFET has a highly doped (N+), source region implanted, and the source metal contacts

both the N+ source and the P-type body. This is an effective option for grounding the body to the source. A gate oxide of 50-100 nm is deposited over the center of the structure, with polysilicon covering the gate oxide to control the channel regions, with representative electron current flow indicated in Figure 5 (middle). In both the diode and the MOSFET, applying positive voltage to the drain results in a depletion region forming in the epitaxial region, and at 1200 V, the entire epitaxial region is depleted, see Figure 5 (bottom). Consequently, vertical structure, doping, and dimensions, of both the diode and the MOSFET are nearly identical.

Table 3: Parameters Used in TCAD Simulations for MOSFETs and Diodes

Parameter	Value
4H-SiC	Bandgap = 3.26 eV
P-Body Doping/Depth	1x10^{19} cm^{-3}, 1 μm
N-Epi Doping/Depth	8x10^{15} cm^{-3}, 10 μm
N+Drain Doping/Depth	1x10^{19} cm^{-3}, 15 μm

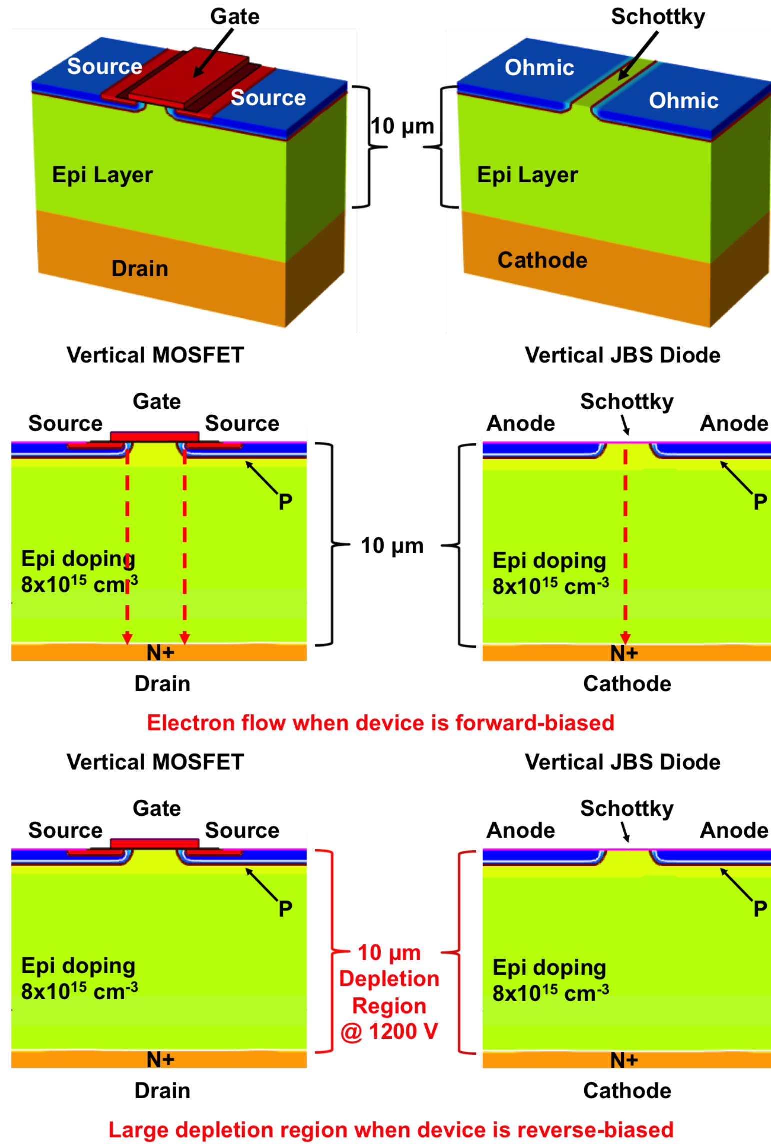


Figure 5: 3D TCAD model of a 1200 V SiC power MOSFET (top left) and JBS diode (top right) showing device structure (epi doping/depth). 2D-cutplanes indicating current flow in forward operation (middle) and fully-depleted epitaxial region at 1200 V (bottom)

Electrical Breakdown Simulation

As discussed previously, a power device is susceptible to single-event burnout when the device is OFF. Although device forward characteristics are very interesting, the reverse characteristics are more important to single-event burnout. Under this bias condition, there exists a very large depletion region in which charge can be deposited. In addition, the presence of a strong electric field is responsible for impact ionization and carrier generation in normal electrical operation, along with providing a mechanism for rapidly moving radiation-induced charge out of the depletion region. For the remainder of this dissertation, the N+ heavily doped substrate will be referred to as the drain, which is consistent with MOSFET terminology. In a diode, this region is called a cathode, but for sake of comparison to the MOSFET in both text and plots, the cathode will also be referred to as a drain.

For electrical breakdown, positive voltage is applied to the drain of the device, and the current flowing through the drain is monitored. For lab measurements, compliance is set for the current in order to protect both the measurement equipment and the device under test (DUT). In simulation, there are no such restrictions. As the depletion region is formed at any P-N junction in a semiconductor, and as the voltage across the junction increases, the depletion region grows, described by

$$X_D = \sqrt{\left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)(\phi_i - V_a)\right]} \tag{1}$$

where ϵ_s is the permittivity of SiC, q is the electronic charge, N_a is the acceptor doping concentration in the p-type body, N_d is the donor doping concentration is the n-type epitaxial region, ϕ_i is the built-in potential at the P-N junction, and V_a is the externally applied bias across the P-N junction [21]. The built-in potential is

described by

$$\phi_i = \frac{kT}{q} ln \frac{N_a N_d}{n_i^2} \tag{2}$$

where k is Boltzmann's constant, T is the temperature in Kelvin and n_i is the intrinsic carrier concentration of SiC, which is $5 \times 10^{-9} cm^{-3}$ [22]. In a step (one-sided or abrupt) P-N junction, there exists a large change in dopant level magnitude. For power device, the P-type body is typically doped 3-5 orders of magnitude higher than the N-type epitaxial region, essentially forming a step junction from P-type to N-type. As shown in Table 3, the P-type body is doped slightly more than 3 orders of magnitude higher than the N-type epitaxial region. This results in the depletion region extending significantly into the N-type epitaxial region, effectively setting the maximum depletion region thickness as the thickness of the epitaxial region. This can be seen in a series of 2D-cutplanes of electron density as a function of drain bias, shown in Figure 6. With the drain at 500 V, the depletion region (light blue) is 8 μm wide, and at 1200 V, the epitaxial region is fully depleted at 10 μm wide. Due to the N+ drain region, the depletion region can extend no further, evidenced by the 1600 V condition which shows no increase in depletion region thickness.

The charge density in a depletion region is described by Poisson's equation

$$\frac{d\mathcal{E}}{dx} = \frac{\rho}{\varepsilon_s} = \frac{q}{\varepsilon_s} N_d \tag{3}$$

which can be integrated to find the electric field, $\mathcal{E}$

$$\mathcal{E}(x) = -\frac{q}{\varepsilon_s} N_d (x - x_n) \tag{4}$$

and as shown Equation 4, the electric field varies linearly within the depletion region. Both of these relationships are shown in Figure 7, which is a series of 2D-cutplanes

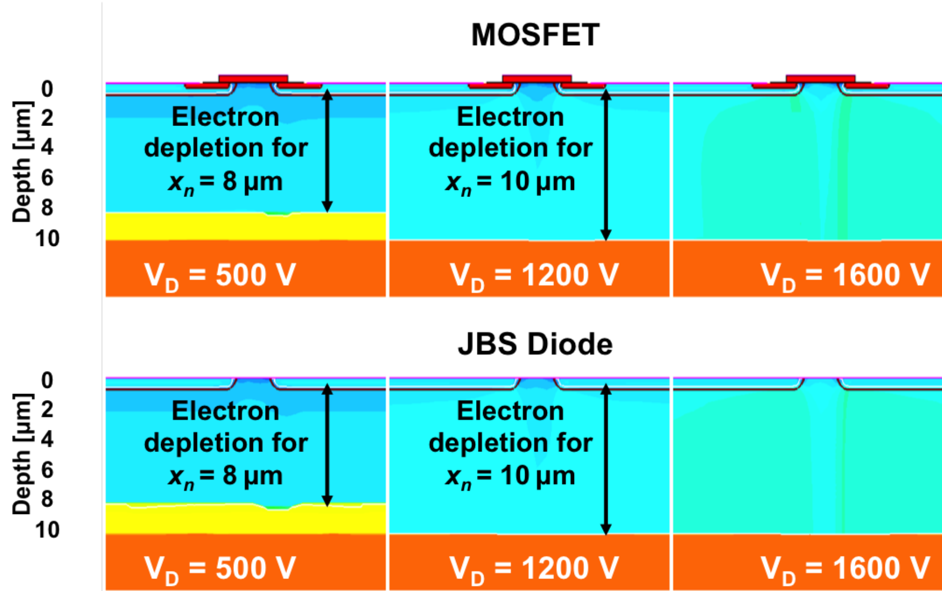


Figure 6: 2D-cutplanes of the electron density for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V

showing the internal electric field for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V. At 500 V, the electric field is linearly graded over the epitaxial region, with an ε_{max} of 1.6 MV/cm at the corner of the P-type body. As the drain voltage increases to 1200 V and then to 1600 V, ε_{max} increases to 2.8 MV/cm and 3.2 MV/cm, respectively. Once the N-type epitaxial region becomes fully depleted, with no additional area in which the depletion layer can grow, the electric fields at the corners of the P-type body increase rapidly, shown in Figure 7. This mechanism is even more evident when plotted as a series of 1D-cutlines, shown in Figure 8. The electric field is linear throughout the entire epitaxial region, and at 500 V, extends slightly over 8 μm. At 1200 V, there is a clear truncation of the electric field at the epitaxial region and N+ drain interface, where the electric field drops to 0 V/cm. However, at the P-type body and epitaxial region interface, the electric field has reached a maximum value. This is further established as the drain voltage

is increased to 1600 V, and as noted above, has reached an $\mathcal{E}_{max}$ of 3.2 MV/cm.

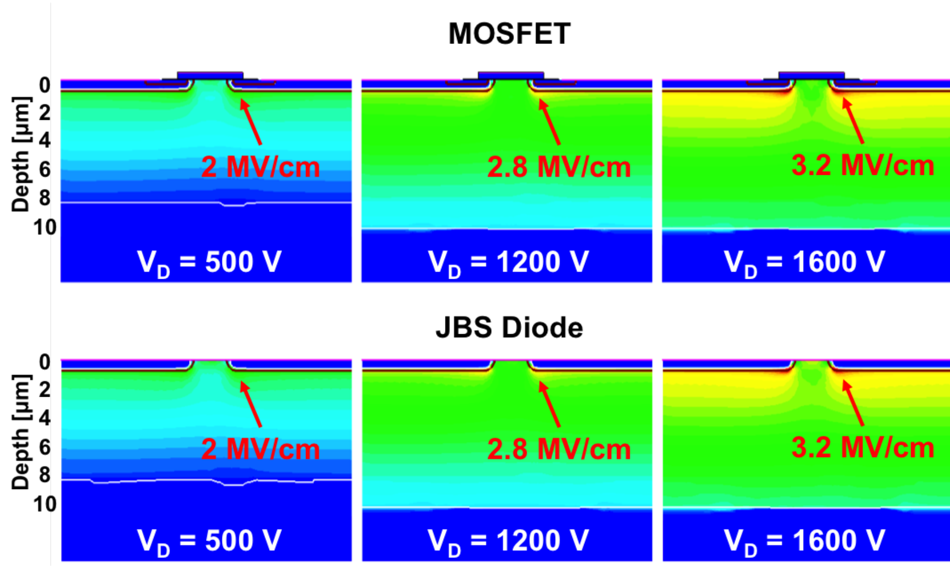


Figure 7: 2D-cutplanes of the internal electric field for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V

The electrostatic potential in the epitaxial region is obtained from the electric field using

$$\frac{d(\phi_i - V_a)}{dx} = -\mathcal{E} \tag{5}$$

which is integrated to give the total potential across the P-N junction by

$$\phi_i - V_a = \frac{qN_d x_n^2}{2\varepsilon_s} \tag{6}$$

This concept is highlighed in Figure 9, which is a series of 2D-cutplanes showing the internal electrostatic potential for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V. At 500 V, the depletion region width (shown as a white line on the contour plot) extends slightly over 8 μm. When the drain voltage is increased to 1200 V, the 10 μm wide epitaxial region is fully depleted. Once the epitaxial region is fully depleted, it can extend no farther because of the N+ drain region. 1D-cutlines of the electrostatic potential for both the MOSFET and diode

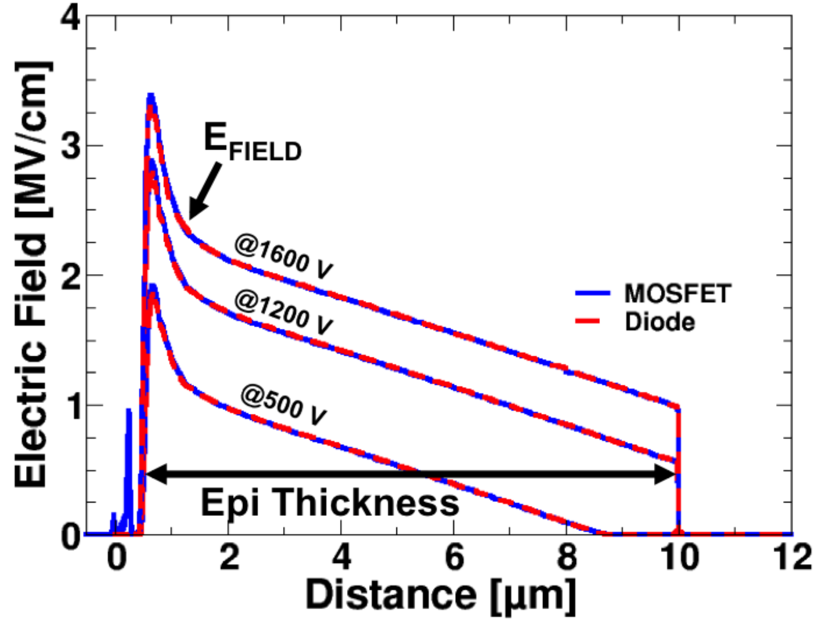


Figure 8: 1D-cutlines of the internal electric field for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V

are shown in Figure 10. In all bias conditions, the entire externally applied voltage is dropped over the epitaxial region, with the slope changing significantly as the drain voltage increases.

This discussion provides the basis for designing a vertical power device. In particular, the epitaxial doping determines the slope of the electric field under a given externally applied voltage. For the 1200 V SiC power device structure, the epitaxial doping was set so that the epitaxial region can be fully depleted at 1200 V, while limiting the maximum electric field, given by

$$\mathcal{E}_{max} = \frac{2(\phi_i - V_a)}{x_n} \tag{7}$$

which results in creating mobile carriers in a process known as impact ionization. Impact ionization occurs when a mobile carrier is accelerated by an electric field in a

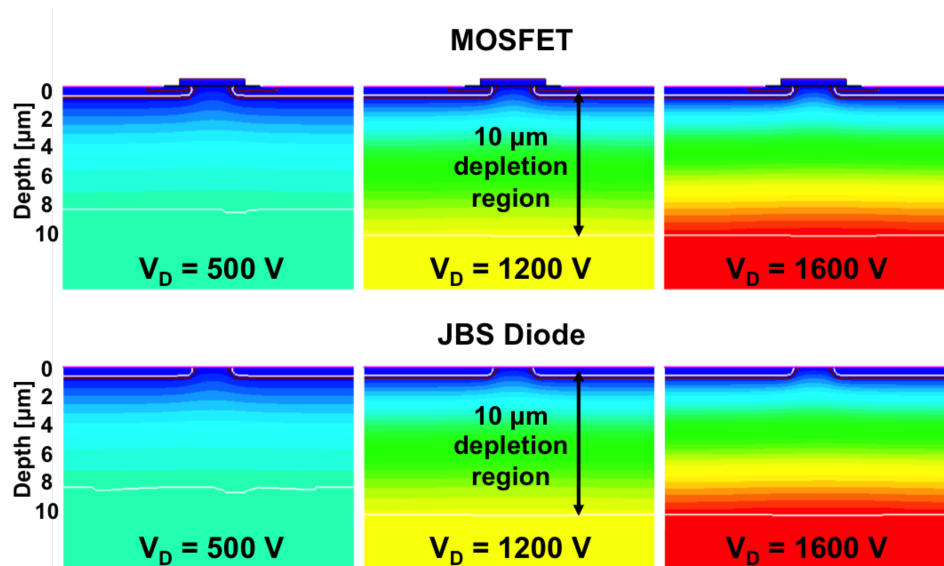


Figure 9: 2D-cutplanes of the internal electrostatic potential for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V

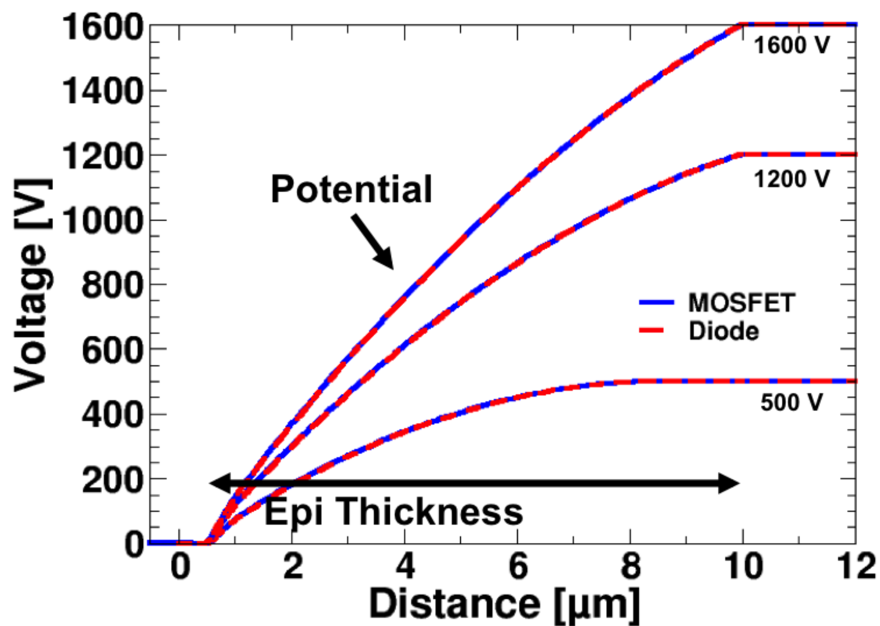


Figure 10: 1D-cutlines of the internal electrostatic potential for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V

depletion region, and a collision occurs between mobile carriers and electrons in the semiconductor lattice with enough energy to free additional electron-hole pairs. This is an avalanching effect can result in very high conduction (current flow). Impact ionization rates are exponentially related to electric field, and while impact ionization can occur with any electric field, as the electric field increases, impact ionization does as well, and with the carrier generation rate described by

$$G^{ii} = \alpha_n n v_n + \alpha_p n v_p \tag{8}$$

where n/p are the available free carriers, v_n/v_p is the carrier velocity, and α_n/α_p are the avalanche coefficients [17]. For the simulations in this work, the Okuto-Crowell Model was selected for avalanche coefficients, where α is described by

$$\alpha = a\mathcal{E}^{\gamma} exp(-\frac{b^{\delta}}{\mathcal{E}}) \tag{9}$$

where a, b, γ, and δ are fitting parameters [17]. This concept is highlighted in Figure 11, a series of 2D-cutplanes showing the impact ionization rates for both the MOSFET and the diode, when biased at 500 V, 1200 V, and 1600 V. The impact ionization rate as a function of position in each device is shown in Figure 11. At 500 V, impact ionization is low, and the rate increases significantly as the drain voltage is increased. When this field reaches approximately 3.2 MV/cm, defined as the critical field, avalanche breakdown can occur, and is consistent with ranges of electric field required for avalanche breakdown in 4H-SiC [23].

3D TCAD electrical breakdown simulation results as a function of reverse bias are shown in Figure 12 for the 1200 V SiC power MOSFET and JBS diode. Both devices were simulated in a reverse-bias condition up to 2000 V, and the simulation results in Figure 12 show that both devices enter avalanche breakdown with approximately

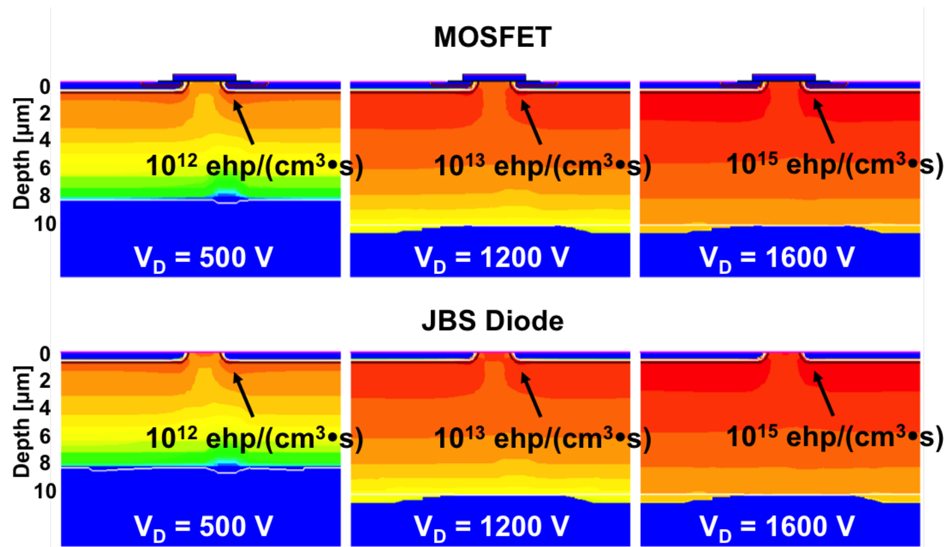


Figure 11: 3D TCAD-simulated electrical avalanche breakdown as a function of reverse bias for 1200 V SiC power MOSFET and diode

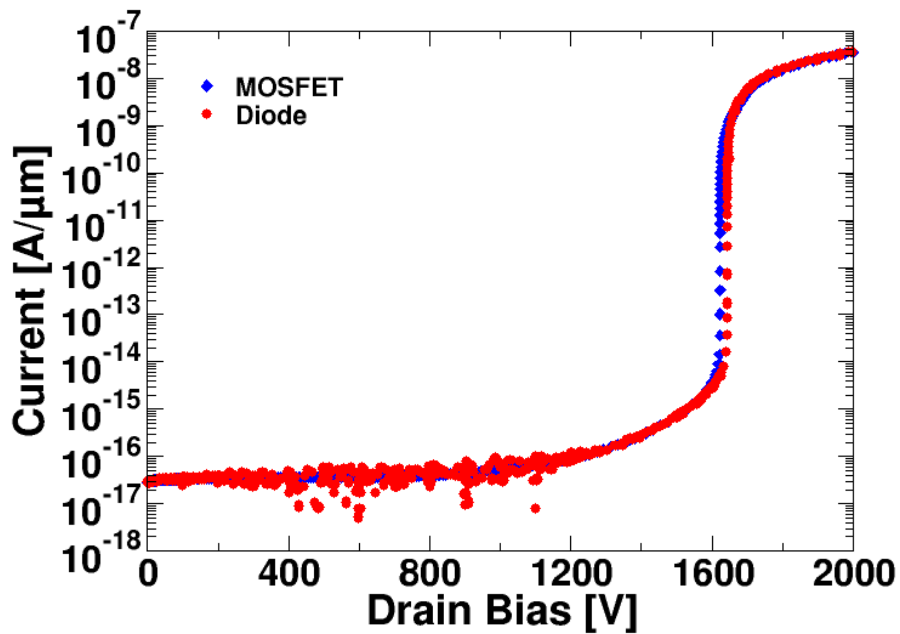


Figure 12: 3D TCAD-simulated electrical avalanche breakdown as a function of reverse bias for 1200 V SiC power MOSFET and diode

the same current-voltage relationships. Physically and electrically, these two devices are very similar.

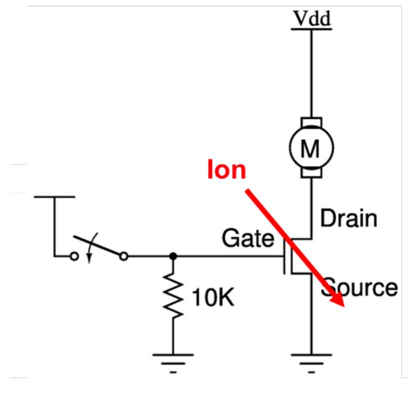
CHAPTER IV

RADIATION-INDUCED SINGLE-EVENT EFFECTS BACKGROUND

Single-event burnout (SEB) is a phenomenon where a power MOSFET or diode, transitions from a stable, low-current state to non-recoverable, high-current state as a result of heavy-ion radiation exposure. This phenomenon was first reported in 1986 for a silicon power MOSFET [24]. An illustration of a power MOSFET in the OFF-state being hit by an ion and the transition of the device into an unstable operating region is shown in Figure 13. The ion, which deposits charge in the form of electron-hole pairs, acts as a current source, forcing the device into a high-current, high-voltage state that may be outside the safe operating area (SOA). The severity of the ion event is a function of particle energy and device bias, with a small deviation outside the SOA likely to result in a single-event transient (SET) of either current or voltage, or both. However, if the event is more severe, it may render the device permanently inoperable, typically as a result of significant current flow that may cause metal line failure, separation of semiconductor material interfaces, or excessive temperatures exceeding the melting point of materials in the device.

Although power MOSFETs and diodes are structurally very similar, it has generally been thought that there are separate mechanisms responsible for the catastrophic failures observed in silicon power diodes (localized avalanche breakdown due to ion-induced electric field spikes) and silicon power MOSFETs (parasitic bipolar junction transistor). The remainder of this chapter will detail the historical concepts driving single-event burnout in both types of devices, including some discussion on modeling

techniques. This discussion is very important for this work for a variety of reasons. First, silicon power diodes are much more radiation tolerant than silicon power MOSFETs due to the differing mechanisms driving single-event burnout. Significant effort has been dedicated to understanding these differences through modeling and analysis, providing significant insight into the physical mechanisms behind single-event burnout in silicon power devices. Second, while the SiC MOSFETs and diodes have been characterized through test campaigns (though far less so than silicon devices), little insight has been gained for the physical mechanism(s) that may be responsible for ion-induced single-event burnout. This dissertation identifies that the long-standing concepts for silicon single-event burnout are not specifically applicable to SiC single-event burnout, resulting in describing a new mechanism for single-event burnout in SiC diodes and MOSFETs, while also developing a simulation methodology to capture this mechanism. Third, with silicon power MOSFETs significantly less susceptible to single-event burnout than diodes, much effort has been focused on increasing the single-event burnout tolerance of the MOSFETs, with much less attention on the diodes. SiC power MOSFETs and power diodes are equally susceptible to single-event burnout, and this work will demonstrate the potential to increase the single-event burnout tolerance for both devices using the same techniques.



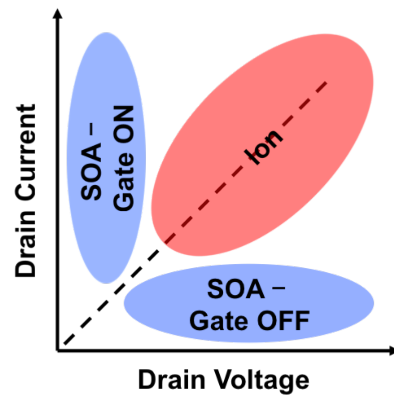


Figure 13: Example of a power MOSFET in the OFF-state hit by an ion (left), forcing a high-current, high-voltage state that may be non-stable and outside of the SOA

Space Radiation Environment

The Galactic Cosmic Ray (GCR) background radiation environment that exists in space consists of many high-energy, charged particles [25] that are capable of interacting with the materials used in microelectronic devices and circuits. Many of these energetic charged particles will produce free electron-hole pairs in a semiconductor material as the particle interacts with the crystal lattice. As the ion passes through the semiconductor, a plasma of electron-hole pairs is created, and the energy deposition is defined as the linear energy transfer (LET), which has units of [(energy/distance)/(mass/volume)]. The energy deposition can also be defined as stopping power which has units of [energy/distance]. The charge generated in the semiconductor is dependent on the original particle energy and the mass of the semiconductor, and can be calculated as

$$Q\,[pC] = \frac{LET\left[\frac{MeV-cm^2}{mg}\right] * \rho\left[\frac{mg}{cm^3}\right] * 1.6 \times 10^{-5}}{G\,[eV]} = L\left[\frac{pC}{\mu m}\right] * X\,[\mu m] \qquad (10)$$

where the units of each variable is indicated in the brackets and Q is the total charge deposited along the particle path length. LET is the linear energy transfer of the ion, ρ is the density of the semiconductor material, and G is the electron-hole pair generation energy. This relationship can be rearranged to show the stopping power, which is L, along the ion path length, X. In silicon, the bandgap is 1.1 eV, and in SiC, the bandgap is 3.3 eV. Energy deposited in excess of the bandgap energy has the potential to create an electron-hole pair, however, much of the energy is thermalized in the lattice, requiring an average energy that is 2-3 times larger than the bandgap to create an electron-hole pair. In silicon, an average of 3.6 eV is required [26], [27],

and in SiC, an average of 7.5 eV is required [28], [29].

In a semiconductor device, when a P-N junction is reverse-biased, a depletion region is formed. As the reverse-bias increases, the depletion region increases in width, and the electric field across the depletion region increases accordingly. Electron-hole pairs created by an ion passing through the depletion region are separated by the electric field, and holes move towards the p-type region, while electrons move towards the n-type region. A drawing of the ion passing through a depletion region and generating electron-hole pairs is shown in Figure 14, with the electrons moving to the n-type region and the holes moving to the p-type region. The currents that arise at the device terminals from the carrier movement is called ion-induced transient current and is a function of the magnitude of the electric field and the density of electron-hole pairs generated by the ion.

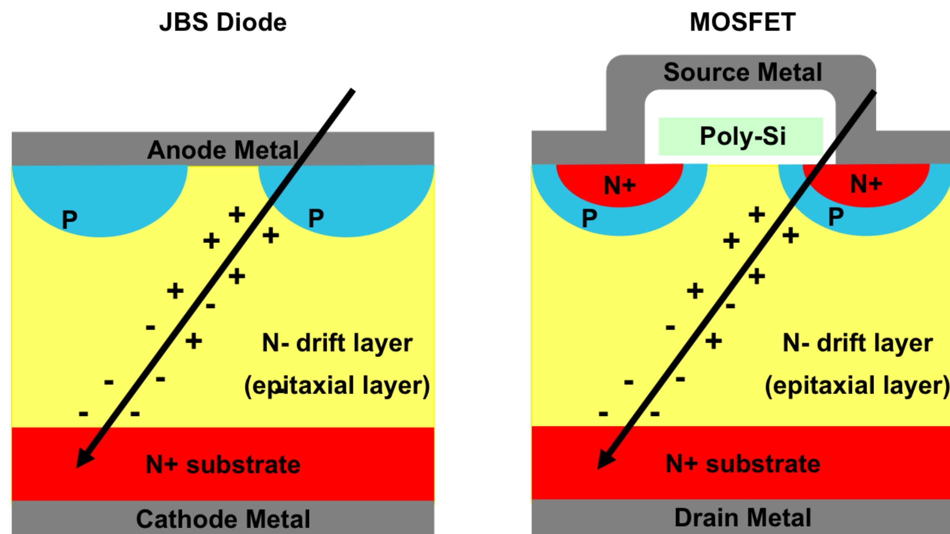


Figure 14: Schematic cross-sections for vertical power junction-barrier Schottky diode and power MOSFET indicating electron-hole pairs generated by the passage of a heavy ion

Single-Event Burnout - Si Power Devices

MOSFETs

A single-event burnout current signature for a silicon power MOSFET during heavy ion irradiation is shown in Figure 15 [30]. The MOSFET is reverse biased in a steady state condition. Approximately 50 ns after the ion strike, the drain current shows a virtually instantaneous rise until the current compliance of the measurement system is reached, while the gate current remains unchanged. This indicates that a resistive short has been created between the drain and the source. The gate current remains relatively unchanged, indicating that the gate is undamaged. This is a classic example of drain-to-source single-event burnout in a power MOSFET [30]. Typically for single-event burnout, physical damage can be seen on the die, as shown in Figure 16 [30]. In this example, the die prior to single-event burnout appears pristine, and following single-event burnout, there is a visible crater on the surface of the die. Visible damage, combined with either a drain-to-source or a drain-to-gate short circuit is evidence of a single-event burnout event.

Single-event burnout in silicon power MOSFETs has historically been attributed to a positive feedback loop with avalanche carrier generation and the turn-on of a parasitic NPN bipolar transistor [24]. A visual interpretation of the parasitic BJT is shown in Figure 17, with the collector (drain), base (body), and emitter (source) labeled. In a typical power device configuration, the body and source are shorted together by the common metallization, so the body voltage has no ability to rise and forward-bias the body-source P-N junction. However, when the passage of a heavy-ion deposits charge in the device, lateral current flow along the P-type body

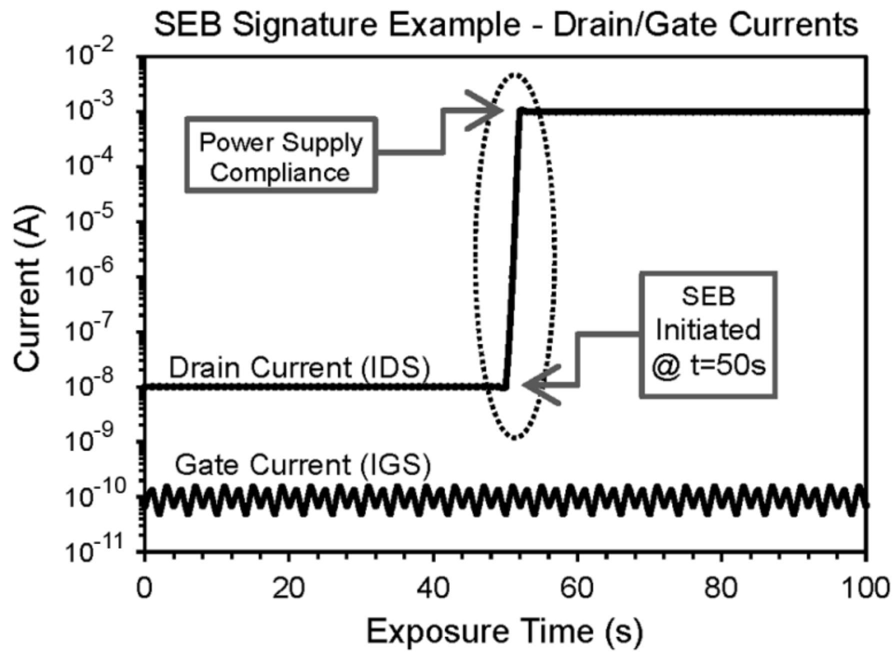


Figure 15: Example of SEB during heavy ion irradiation of a power MOSFET. Sudden drain current increase indicates drain-to-source short circuit after Titus *et al.* [30]

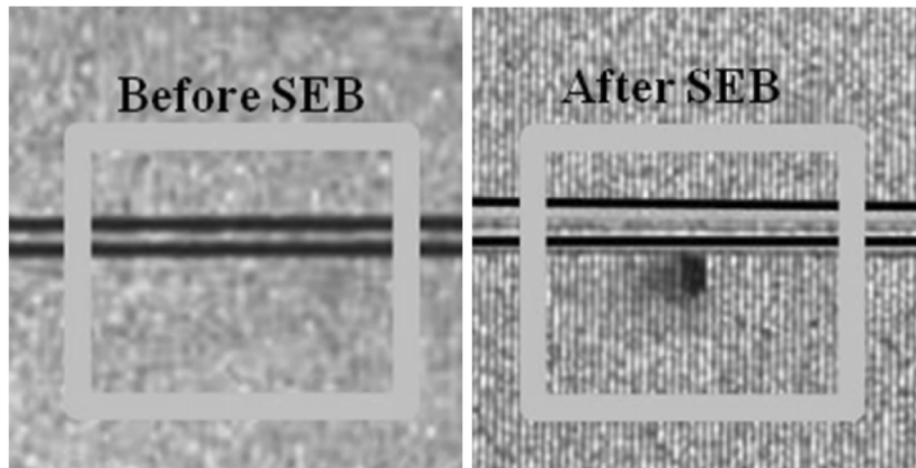


Figure 16: Before and after photos of SEB. Visible physical damage is a likely indicator of SEB after Titus *et al.* [30]

region allows the body voltage to rise, forward-biasing the body-source P-N junction, turning on the parasitic BJT. This occurs simultaneously with the avalanche carrier generation due to the high electric fields present in the device, which can be seen in TCAD simulation results from Liu *et al.* in Figure 18 [31]. These simulation results show the internal electric field is redistributed during the ion strike, peaking at the interface between the epitaxial and drain regions. The positive feedback loop between the parasitic BJT and the avalanching carriers, each with a positive gain, results in a condition where high current and high voltage are sustained sufficiently to physically damage the device through metal/semiconductor separation at the contact, burnout of metal lines, or thermal meltdown of the silicon.

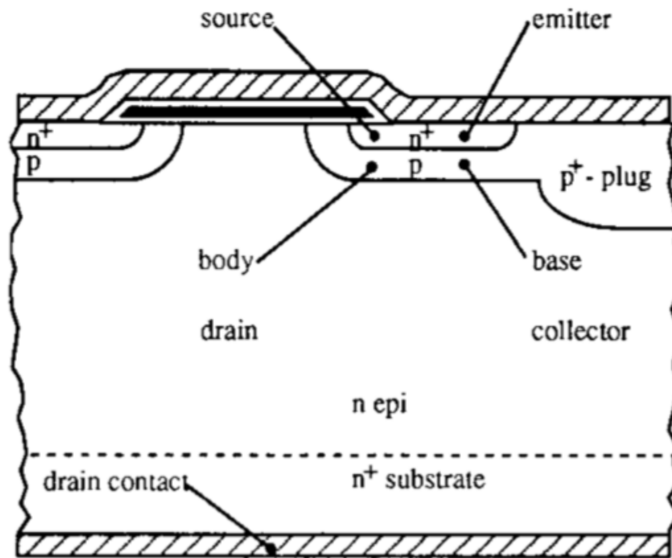


Figure 17: Inherent N-P-N parasitic BJT transistor in a vertical DMOS device after Johnson *et al.* [32]

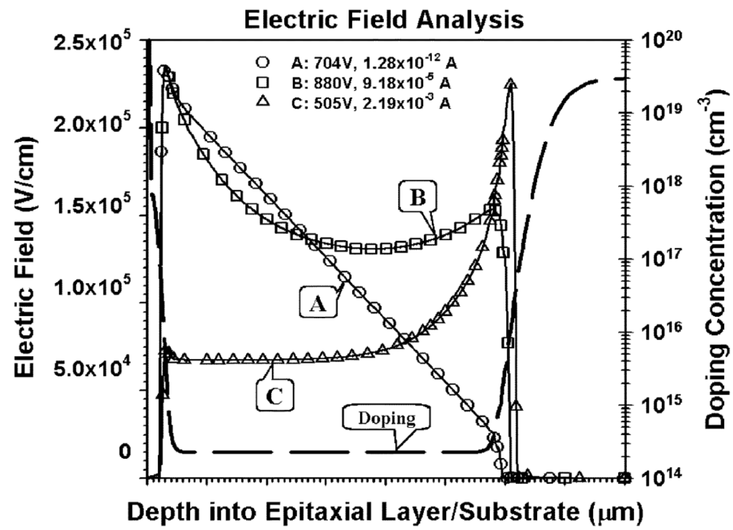


Figure 18: Electric field distribution pre-strike (A) and post-strike (B and C) for simulated ion strike in a power MOSFET. A to B to C represents an evolution of the electric field as a function of time after Liu *et al.* [31]

Diodes

In 1994, Kabza *et al.* reported the first single-event burnout in silicon power diodes [33], with the single-event burnout signature shown in Figure 19. The current shows a virtually instantaneous rise until current compliance of the measurement system is reached. The corresponding decrease in functionality of the diode to block the externally applied voltage indicates a resistive short created between the anode and the cathode. In addition to the electrical characteristics, Kabza reported "the failure pattern consisted of a spontaneous short without prior indication; the devices exhibited a pin hole size molten channel from cathode to anode". The physical damage in the silicon power diodes appeared to be consistent with physical damage observed in silicon power MOSFETs. However, in a silicon power diode, there is no parasitic NPN bipolar present, suggesting that the mechanism for single-event burnout in a silicon power diode is not the sameas that in silicon power MOSFETs. In the same work, Kazba presented 2D cylindrical TCAD simulations for charge deposition in a diode, concluding that the ion-induced charge resulted in re-distributed internal electric fields that were larger in magnitude than the pre-strike electric fields. Simultaneously, high current densities, combined with the increased electric fields contribute to very high local power densities, likely to cause local temperature increases and self-heating [33].

In 1998, Maier *et al.* investigated the impact of avalanche multiplication (which is exponentially dependent on electric field) on single-event burnout in silicon power diodes [34]. Charge generated in a silicon power diode from a single ion was measured with a charge-sensitive preamplifier, and the results are shown in Figure 20 [34]. At low voltages, below 850 V, a single charge collection peak is observed corresponding

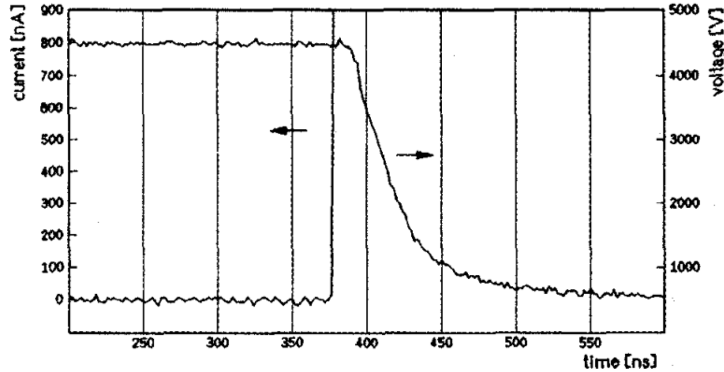


Figure 19: Oscilloscope recording of reverse blocking current and voltage during failure. The destructive current develops in less than 10 ns after Kabza *et al.* [33].

to the direct energy loss of the ion. As the voltage increases, the charge collection peak both broadens and shifts, with the shift interpreted as a amplification of charge carriers from avalanche multiplication. Once the voltage is increased past 1100 V, all deposited charge contributes to avalanche carrier generation.

In 2002, Walker *et al.* presented Figure 21, showing TCAD simulation results in a diode for an ion with LET = 30 MeV-cm^2/mg and applied bias of 3500 V. A non-isothermal simulation, Figure 21 (top), shows an increase in lattice temperature to the point at which intrinsic carrier concentrations begin to dominate the current response. The increased current forces increased self-heating, further increasing the intrinsic carrier density, and completing the positive feedback loop. In comparison, an isothermal simulation shows a current transient that eventually dies out as all of the excess carriers in the system recombine. Further, the temperature in the non-isothermal simulation is monitored during the simulation, and shown in Figure 21 (bottom). This simulation result indicates clear thermal runaway, and the device may be permanently damaged from either sustained current through the metal lines or melting of the silicon, or both. Albadri *et al.* [35] presented a comprehensive

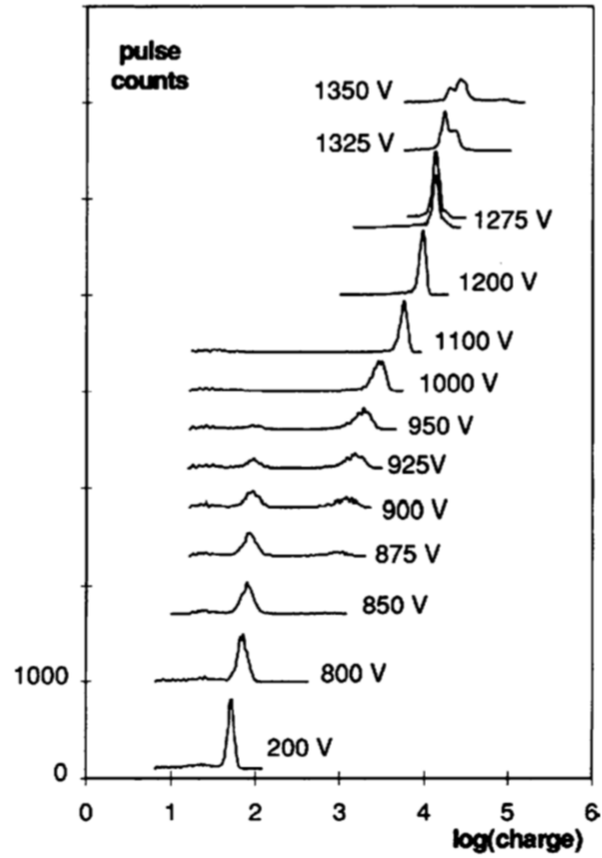


Figure 20: Charge spectrum from the bombardment of a 4kV diode with 90 MeV Kr ions showing the number of events as a function of the total generated charge with increasing the applied voltage after Maier *et al.* [34].

analysis of single-event burnout in silicon power diodes and power MOSFETs in 2006, concluding that silicon power diode single-event burnout results from thermal effects, while power MOSFET single-event burnout results from the turn-on of a parasitic BJT .

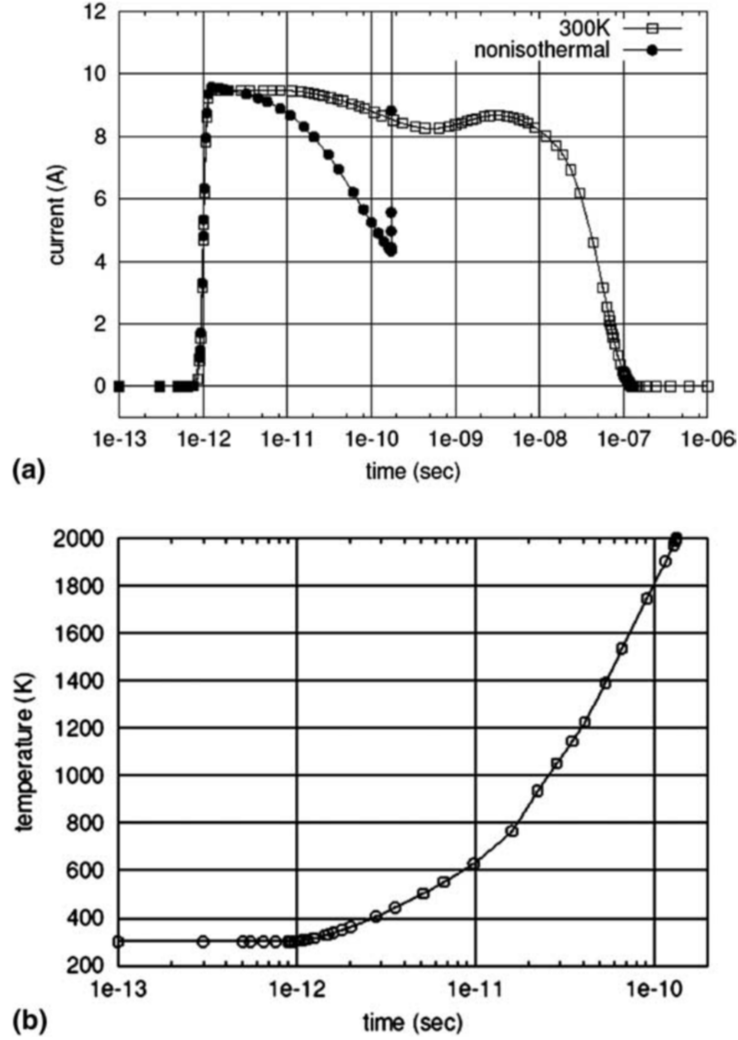


Figure 21: Output currents of isothermal and non-isothermal simulations with LET = 30 MeV-cm^2/mg and V = 3500 V (top), along with maximum temperature due to self-heating (bottom) after Walker *et al.* [36].

Derating

Derating is an approach used to reduce operating conditions sufficiently that the survivability of a power device is maximized for a given environment. NASA defines it as "derating is the reduction of electrical and thermal stresses applied to a part during normal operation in order to decrease the degradation rate and prolong its expected life [37]." In a single-event environment, a "rule of thumb" is to derate the operating voltage of a device/circuit by a given percentage, such as 75%, 50%, or 25% [38]. Derating can also provide sufficient margin where part-to-part variability is a concern, however, the penalty for derating comes in the form of reduction in device performance. In power MOSFETs, safe-operating areas for single-event burnout are typically established by testing with ions that have an atomic number (Z) $>$ 35 and LET $>$ 37 MeV-cm^2/mg [39], and a common derating practice for radiation-hardened devices to survive those conditions are to use 75% of the rated breakdown voltage, with 50% the lower bound to provide additional margin for part-to-part variation [40], [37]. Casey *et al.* irradiated 38 silicon power Schottky diodes from 9 vendors and a wide range of rated breakdown voltages, and concluded that the entire list of parts did not show single-event burnout or any other permanent damages when derated to 50% of the breakdown voltage [41]. With no derating, almost half of the parts survived. In general, derating trends for silicon power devices correlate to the mechanisms driving single-event burnout in MOSFETs and diodes. MOSFETs require larger derating due to the parasitic BJT turn-on, while diodes can tolerate less derating because the thermal runaway is driven by higher voltages.

JBS Diodes

A important work was published in 2006 by Kuboyama *et al.* [42] for SiC Schottky diodes, investigating single-event burnout through charge collection and leakage current measurements. Kuboyama identified unexpected damage in Schottky diodes from heavy ion irradiation, resulting in permanent increases in leakage current. This phenomenon had never been observed in silicon devices. As the device bias was increased, destructive single-event burnout was observed, with no sustainable positive feedback mechanism for current multiplication, such as a parasitic BJT. As discussed above, this is also unique due to the inherent radiation tolerance of silicon diodes.

Kuboyama described three regions of device response for the SiC diodes as a function of reverse bias and the parameters of heavyion exposure: 1) nondestructive charge collection; 2) permanent leakage current degradation; and 3) catastrophic failure. An example of non-destructive charge collection is shown in Figure 22 [42]. In this region, collected charge can be reproduced during each exposure, with no permanent damage to the device. In each of these irradiation events, the ion deposits charge, and the collected charge is measured from the diode Schottky contact during the event.

The second region of device response defined by Kuboyama is permanent leakage current degradation, and is clearly seen in data from Witulski *et al.* in Figure 23 [18]. In order to see discrete leakage steps, the beam flux was tuned to be very low, between 5 and 100 ions/cm^2/s. The data shows significant discrete steps in leakage current while the beam was ON, and when the beam turned OFF, no additional

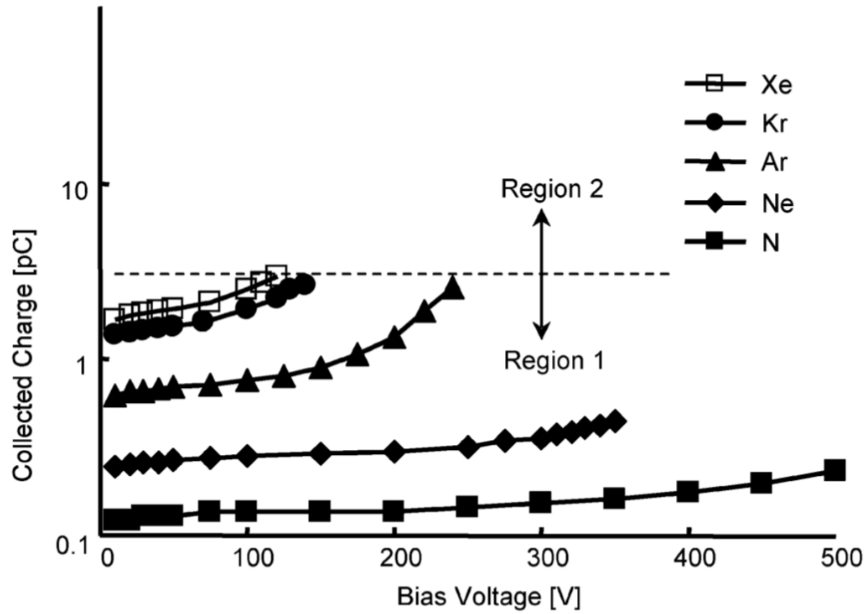


Figure 22: Collected charge as a function of reverse bias voltage observed in SiC Schottky diodes after Kuboyama *et al.* [42]

leakage increases were seen. This data supports additional studies for leakage current in SiC diodes [43], [44].

The third region of device response defined by Kuboyama is catastrophic failure, and can be seen in data from Witulski in Figure 24 [18]. In these irradiation exposures, the beam was turned on while the devices were biased, and the drain current monitored as a function of time. Catastrophic failure was determined by a singularly large jump to the compliance state of the measurement equipment, typically 4-5 orders of magnitude larger than the leakage current just before failure.

Witulski produced the first work defining the leakage and single-event burnout thresholds as a function of ion LET and device bias in Figure 25 [18]. The curve shows a nonlinear dependence on LET, with a significant "knee" at LET=10 MeV-cm^2/mg, where the curve changes slope. The boundaries in this data set illustrate

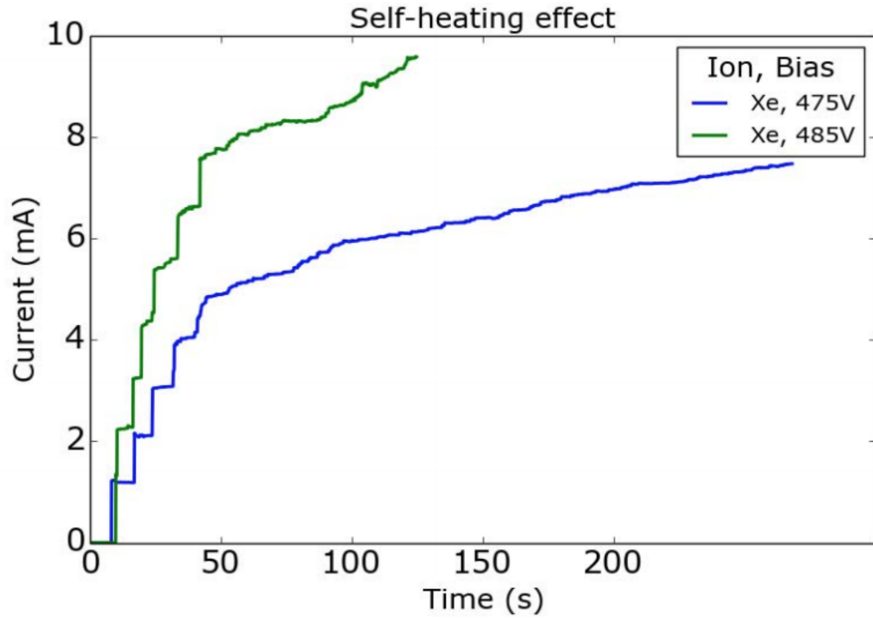


Figure 23: Measured diode current versus time during heavy-ion irradiation for two diodes, showing discrete increases in leakage current with individual heavy ions, with self-heating effect. Xenon flux was 68, and Neon was 5.7–6.1 ions/cm^2/s after Witulski *et al.* [18]

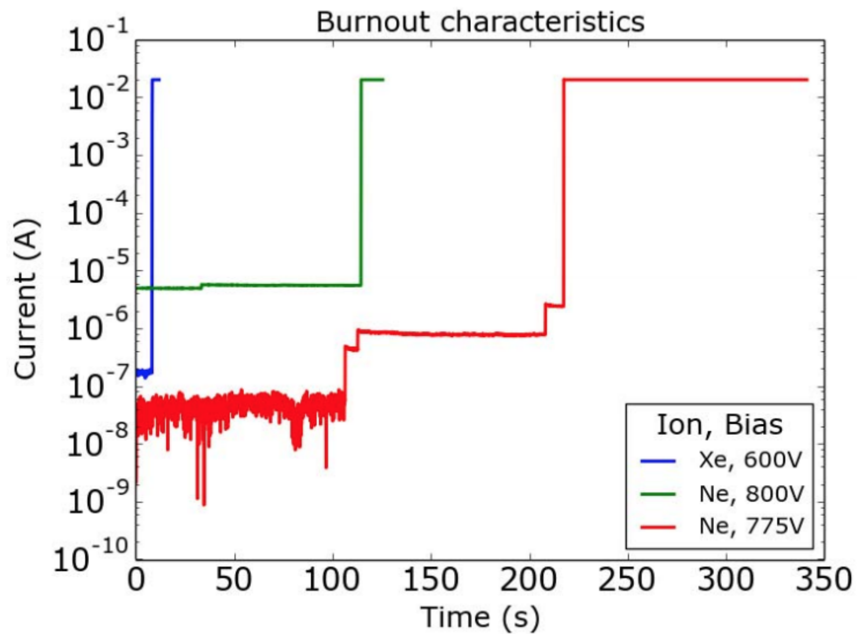


Figure 24: SEB events for three different 1200 V JBS diodes. Xenon flux was 68, and Neon was 5.7–6.1 ions/cm^2/s. All diodes are irradiated at room temperature after Witulski *et al.* [18]

the three regions defined by Kuboyama, non-destructive, permanent leakage, and catastrophic failure.

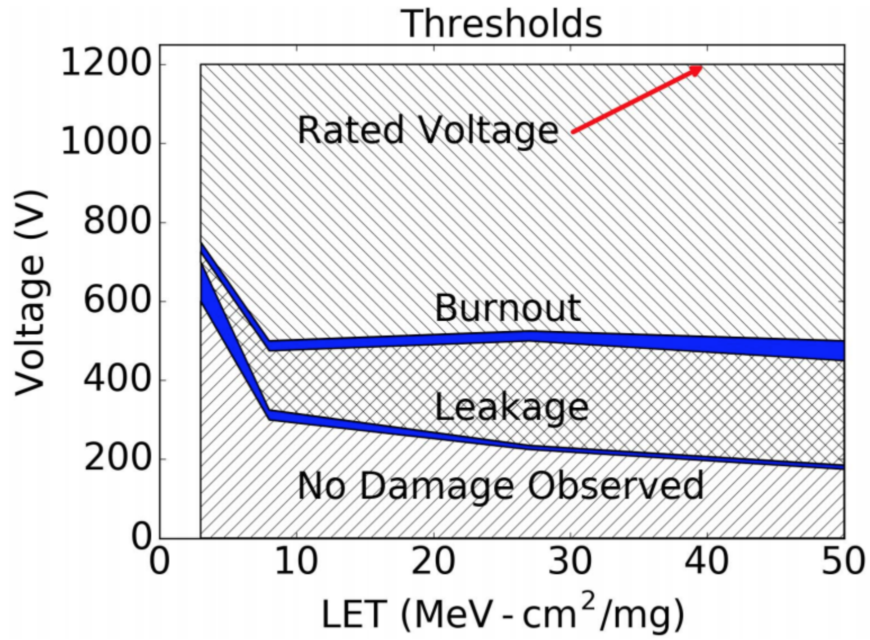


Figure 25: Measured degradation mode thresholds as functions of applied bias and LET. The width of the line indicates minimum voltage at which burnout was observed and maximum voltage with no burnout observed after Witulski *et al.* [18]

MOSFETs

In 2014, Lauenstein *et al.* identifed that SiC power MOSFETs have both permanent leakage current degradation and catastrophic failure due to ion irradiation, similarly to the Schottky diodes [45]. Mizuta *et al.* published similar data in 2014 [46] supporting Lauenstein's findings. A more comprehensive data set was published by Lauenstein *et al.* in 2017, with data shown in Table 4 establishing the single-event burnout threshold as a function of ion species. The data shown in Figure 26 show drain current as a function of time during irradiation, indicating regions of no damage (A), leakage current degradation (B), and catastrophic failure (C). These data are consistent with the trends shown by Witulski *et al.* [18] for the JBS diodes.

Table 4: Measured degradation and catastrophic failure regions for SiC power MOSFETs after Lauenstein *et al.* [6]

Ion	Device	Rated Voltage	Max V_{DS} No Damage	Onset V_{DS}: I_D, I_G Degradation $I_G = I_D$	$I_D > I_G$	Min V_{DS} Sudden SEE
1110 MeV Ag	M1	1200	$50 < V_{DS} < 75$	$200 \leq V_{DS} < 225$	$350 < V_{DS} < 400$	$500 < SEB \leq 600$
	M6	1200	$25 < V_{DS} < 50$	$50 < V_{DS} < 100$	not found	SEE ≤600 (see Xe)
996 MeV Xe	M1	1200	$50 < V_{DS} < 75$	$200 < V_{DS} < 300$	$400 < V_{DS} < 425$	$450 < SEB \leq 500$
	M2A	1200	$40 < V_{DS} < 50$	< 182	*$400 < V_{DS} < 500$	$600 < SEB \leq 700$
	M2B	1200	$50 < V_{DS} < 60$	< 182	$300 < V_{DS} < 400$	not found (> 500)
	M2C	3300	$50 < V_{DS} < 75$	n/a†	$325 < V_{DS} < 350$	$600 < SEB \leq 800$
	M5	1200	$40 < V_{DS} < 50$	< 182	$200 < V_{DS} < 400$	$400 \leq SEE \leq 600$
	M6	1200	not found	not found	not found (≤ 500)	SEE >500 (see Ag)
566 MeV Cu	M5	1200	$70 < V_{DS} < 80$	$200 < V_{DS} \leq 400$	not found (> 400)	$400 < SEB \leq 600$

*Onset > 400 V based on 4 samples irradiated to low, $1x10^3$ cm^{-2}, fluence
†Latent gate damage only; during beam exposure, all events resulted in $I_D > I_G$

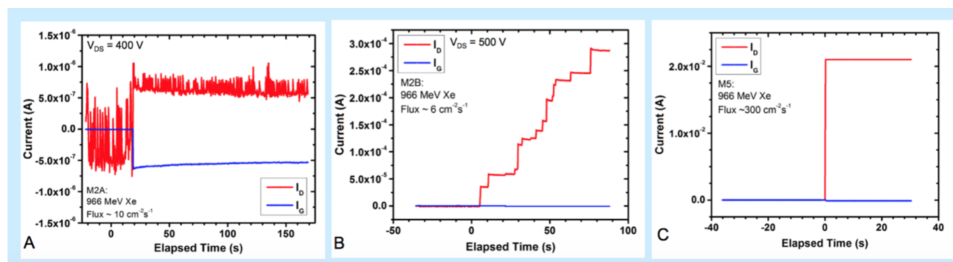


Figure 26: MOSFET drain current as a function of time during irradiation A) No damage, B) Leakage current degradation, and C) Catastrophic failure after Lauenstein *et al.* [6]

Thermal Simulation Analysis

Due to the history of silicon power diodes with thermal runaway driving single-event burnout, effort has been made to explore the same effect in SiC diodes. Kuboyama *et al.* explored thermal effects using TCAD simuation in 2006, with results shown in Figure 27 for an ion strike of LET = 42 MeV-cm^2/mg at 220 V reverse bias in a SiC diode. The simulated results show a maximum electric field of 7.7x10^6 V/cm shortly after the ion strike, and a maximum temperature of 2680 K. Kuboyama noted that at this temperature, the intrinsic carrier density of SiC is 5.9x10^{18} which is lower than the carrier density along the ion track, therefore not sufficient for thermal runaway. As discussed previously, in silicon, the increase in temperature and the corresponding increase in intrinsic carrier density result in a positive feedback loop driving thermal runaway. This effect did not appear to be driving single-event burnout in SiC diodes at that time. Similar results were presented in other works, notably Witulski *et al.* where it was concluded using TCAD simulations that local temperature increases to 2600 K at 500 V for LET of 40 MeV-cm^2/mg and greater [18]. Similar TCAD simulation results were published by McPherson *et al.* in 2019 for LET = 49MeV-cm^2/mg and temperatures reaching 3000 K [47]. Abbate *et al.* presented TCAD simulation results in 2015 for LET = 28 MeV-cm^2/mg indicating temperatures of 1500° Celsius (1773 K) when biased at 500 V, and reaching almost 10000° Celsius when biased at 900 V.

In very recent work, Kuboyama *et al.* in 2019 showed that thermal runaway may be possible in SiC Schottky diodes for LET = 62 MeV-cm^2/mg and 200 V, when thermionic transmission of carriers through the Schottky barrier were considered in conjunction with the avalanche generation during the strike, causing a positive

feedback loop. Kuboyama *et al.* are continuing efforts to refine and update models, however, it is interesting to note that traditional behaviors are not likely to cause positive feedback scenarios. Thermionic transmission through a Schottky barrier is required to provides a source of carriers.

These results for ion-induced thermal rise in SiC diodes are consistent among multiple authors and multiple simulation tools in the fact that higher LET ions can cause significant thermal rise to temperatures exceeding that of the SiC sublimation point. However, no results have been shown for low LET strikes. The data presented above indicate that diodes show single-event burnout at LET as low as 2 MeV-cm^2/mg. In general, low LET particles have a significantly lower charge density along the core of the track, and likely do not result in significant thermal increase as do the higher LET particles. This suggests that there is another mechanism causing single-event burnout.

Similar results have been published for a 1200 V SiC power MOSFET by McPherson *et al.* in 2019, showing that an ion with LET = 46 MeV-cm^2/mg can result in a temperature rise to over 3000 K at the interface between the epitaxial and drain regions [48]. Again, this is a high LET particle, and similar to the diodes, data for the MOSFETs shows low LET single-event burnout.

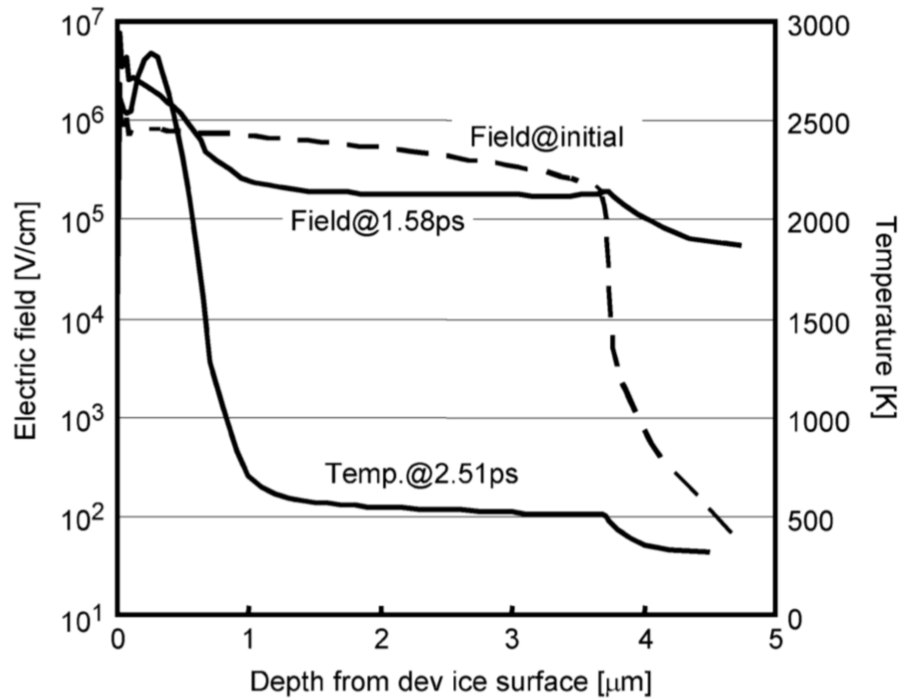


Figure 27: Electric field and temperature distribution along ion track after Kr ion strike under 220 V of reverse bias after Kuboyama *et al.* [42]

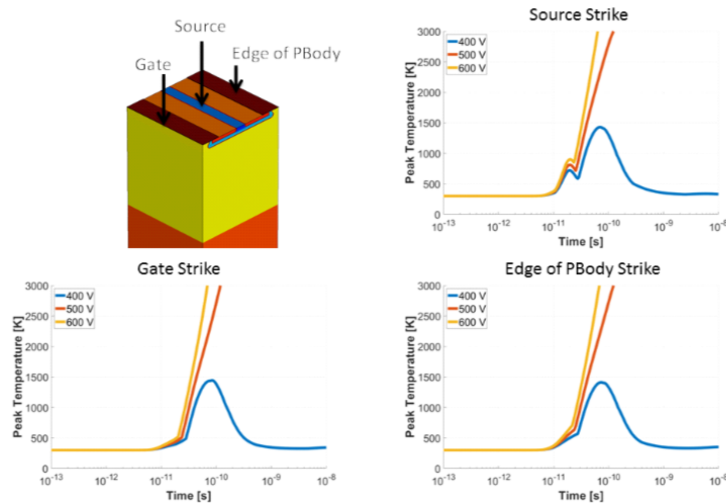


Figure 28: 3D TCAD simulations of ion-induced temperature increase in SiC power MOSFET for LET = 46 MeV-cm^2/mg varying bias and hit location after McPherson *et al.* [48]

Derating

In 2017, Lauenstein *et al.* concluded that SiC power MOSFETs and JBS diodes evaluated at that time showed catastrophic single-event burnout at a maximum of 60% of the rated breakdown voltage and permanent leakage degradation down to 10% of the rated breakdown voltage. The data shown in Figure 29 is for the bias required for single-event burnout and normalized to the rated breakdown voltage as a function of ion LET for JBS diodes (top) and MOSFETs (bottom) [49]. It is apparent that 60% of the rated breakdown voltage is the maximum voltage that can be applied to a SiC device before showing single-event burnout for a 1200 V device, and that provides little to no margin for error. A 70% derating provides approximately 100 V of margin before suceptibility to single-event burnout. However, at 80% derating, all devices would appear to survive ion-induced single-event burnout.

This is in sharp contrast to conclusions from Casey *et al.* for silicon Schottky diodes, which showed that at 100% of the rated breakdown voltage, almost half of the diodes survived, and at 50% de-rating, all devices survived irradiation. Establishing a "rule of thumb" for de-rating SiC power devices is challenging at best, particularly when considering leakage degradation in addition to single-event burnout.

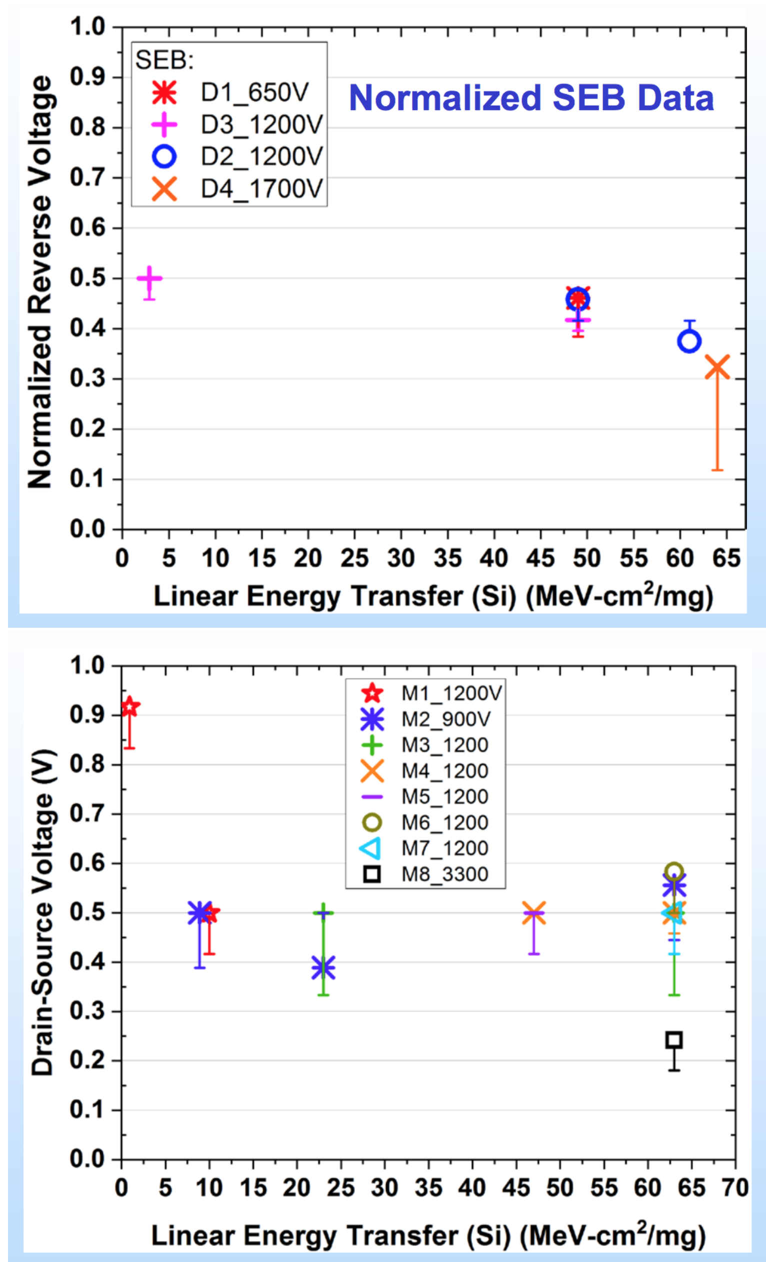


Figure 29: Single-event burnout voltage normalized to rated breakdown voltage as a function of ion LET for SiC Schottky diodes (top) and MOSFETs (bottom) showing that 50% device de-rating is not sufficient for survivability after Lauenstein *et al.* [45]

CHAPTER V

IDENTIFYING COMMON TRENDS FOR SINGLE-EVENT BURNOUT IN SIC POWER MOSFETS AND DIODES

Obtaining radiation data for semiconductor devices is an expensive, time-consuming task with single-event burnout (SEB) testing particularly challenging because the destructive nature results in devices that are no longer functional. The safe operating area (SOA) for 1200 V SiC power MOSFETs and diodes has been modestly characterized through test campaigns, however, little insight has been gained for the physical mechanism(s) that may be responsible for ion-induced single-event burnout. Understanding these mechanisms is imperative for organizations making space-flight hardware design decisions to mitigate risk of operational failure during a mission. Ion-induced radiation data for power devices reflects the response of a device from the perspective of an electrical terminal, or better defined as "on the outside looking in."

This chapter is focused on analyzing ion-induced single-event burnout data for commercially manufactured 1200 V SiC power MOSFETs and JBS diodes. This data is a compilation of data taken specifically for this work along with data from literature. These data sets indicate that a common mechanism is responsible for single-event burnout in MOSFETs and diodes. In addition, single-event burnout data from 650 V to 3300 V SiC MOSFETs and diodes has also been gathered from literature, and is compared to the 1200 V data, showing a clear trend that increasing epitaxial thickness and lighter epitaxial doping results in a higher single-event burnout

threshold. Terrestrial neutron-induced single-event burnout data for these devices, available in engineering and scientific literature, also support both of these concepts.

1200 V SiC

Single-event burnout data taken as part of this work is shown in Figure 30 for the 1200 V SiC power MOSFET with $R_{DS,ON}$ = 80 mΩs [19], [50]. The irradiation tests were performed at the Lawrence Berkeley National Laboratory (LBNL) 88-inch cyclotron [51] and at the RADEF facility [52] at the University of Jyvaskyla, Finland. For all tests, the ion beam was at normal incidence and in vacuum. The characteristics of the ion beams used are given in Table 5. The energy and range of the heavy ions were chosen to sufficiently penetrate the entire epitaxial region of the device. During irradiation, the MOSFET source and gate were grounded, and the drain biased. All data presented in this work are for heavy ions at normal incidence, however SiC power devices have a significant single-event burnout dependence on angle [53], [49], and while angular effects are not analyzed in this work, it is important to note that heavy ions at normal incidence are the worst case.

The observed single-event burnout threshold (SEB_{TH}) data are shown in Figure 30 and in Table 5. These data are compared to published data [46], [45], also for the 1200 V MOSFET. The trends of the data presented in this work match the trends evident in the previously published data, where the onset voltage for single-event burnout failure threshold increases significantly at decreasing LET. Data from Mizuta [46] observe an SEB_{TH} at 600 V for Ne ions at LET = 6.9 MeV-cm^2/mg and at 900 V for N ions at LET = 3.6 MeV-cm^2/mg. Higher LET data (23 to 66 MeV-cm^2/mg) are from Lauenstein [45], indicating an SEB_{TH} of 500 V. Both published data sets

are consistent with data taken in this work. A key takeaway from these data sets is that the SiC power MOSFETs fail at voltages that are 50% of the rated breakdown voltage of 1200 V for LET > 5 MeV-cm^2/mg.

In addition to single-event burnout, permanent damage is manifested as an increase in drain leakage current with higher LET ions similar to that observed in SiC Schottky Barrier diodes [18]. No leakage current increase was observed for lower LET ions including protons [6] before single-event burnout was observed.

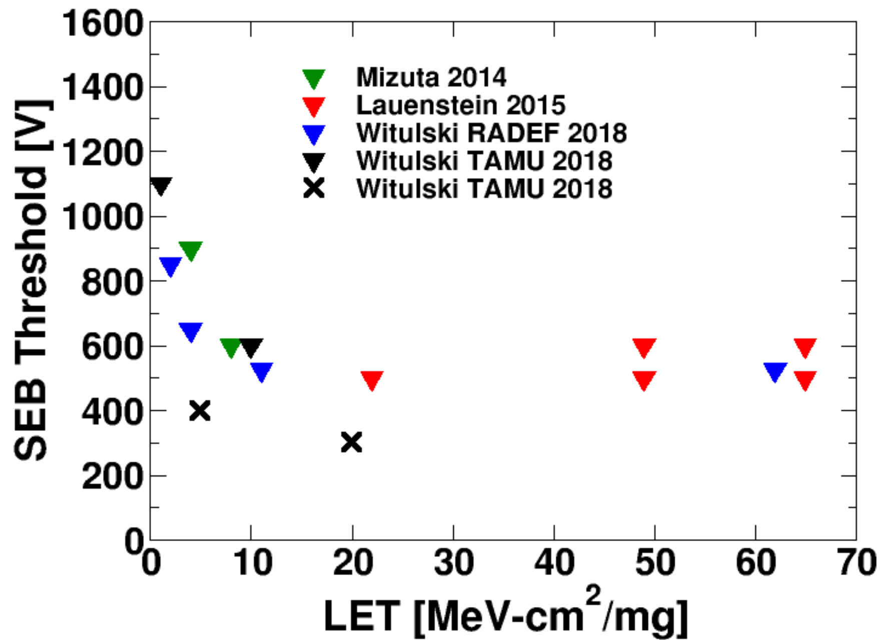


Figure 30: Single-event burnout and degradation threshold bias voltages vs. LET for 1200 V SiC power MOSFETs taken during this work and compared to published literature [19], [45], [46], [50].

Single-event burnout data from published literature is shown in Figure 31 for a commercially available 1200 V SiC JBS diode [18]. The heavy-ion irradiations were performed at the Texas A&M Cyclotron [54] using the 15-MeV/amu cocktail, with sufficient energy and range to fully penetrate the entire epitaxial region of the

Table 5: Ion Beam Characteristics with SEB_{TH} shown

Facility	Ion	Energy [MeV]	LET [MeV-cm^2/mg]	SEB_{TH} [V]
LBNL	B	108	1	1100
LBNL	Ar	400	10.4	600
RADEF	N	139	2	850
RADEF	Ne	186	3.9	650
RADEF	Ar	373	10.8	525
RADEF	Xe	1217	62.4	525

device. The trends of the diode single-event burnout data appear to closely match the data shown in Figure 30 for the MOSFET. At high LET, less than 50% of the rated breakdown voltage is required for single-event burnout, while at low LET, the voltage approaches the rated value.

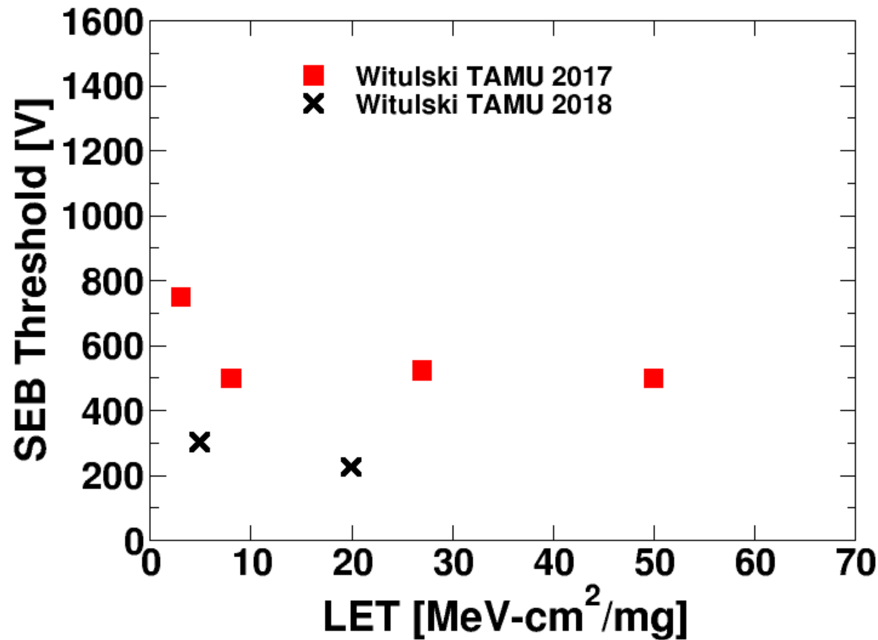


Figure 31: Single-event burnout and degradation threshold bias voltages vs. LET for 1200 V SiC power diodes taken during this work and compared to published literature after Witulski *et al.* [18]

As discussed in Chapter IV, it has generally been thought that there are separate

mechanisms responsible for the catastrophic failures observed in silicon power diodes (localized avalanche breakdown due to ion-induced electric field spikes) and silicon power MOSFETs (parasitic bipolar junction transistor). A natural assumption is that separate mechanisms are also responsible for single-event burnout in SiC power diodes and MOSFETs. However, the data presented in Figure 30 and Figure 31 show that 1200 V SiC power MOSFETs and 1200 V JBS diodes have the same SEB_{TH} as a function of ion LET. These data sets are combined in Figure 32, showing the unique similarity of single-event burnout for the MOSFET and diode. single-event burnout in silicon power MOSFETs has been linked to the parasitic bipolar junction transistor, which is an integral part of the device structure a discussed in Chapter IV. Some success has been achieved in simulating single-event burnout in SiC power MOSFETs by assuming that impact ionization, coupled with the parasitic bipolar junction transistor, results in a positive-feedback loop during an ion event causing single-event burnout [19], and discussed in detail in Appendix A. However, power diodes do not have a positive-feedback loop related to a parasitic bipolar structure, suggesting that there is another mechanism responsible for single-event burnout.

Additional single-event burnout data taken in this work at at Texas A&M University Cyclotron (TAMU) for SiC MOSFETs are shown in Figure 32 [50], using a non-destructive test technique in an attempt to suppress single-event burnout. The LET considered is 20 MeV-cm^2/mg at normal incidence, and the device was at room temperature. A resistor was inserted inline between the power supply and the drain node in an attempt to limit current and allow the drain node voltage to drop below critical levels required for single-event burnout. This is shown schematically in Figure 33. Data shown in Figure 32 indicate that this test technique was not

effective in suppressing single-event burnout using a 100 kΩ resistor (for LET = 20 MeV-cm^2/mg, single-event burnout occurred at the same voltage, with or without the resistor). Similar data were presented previously, indicating that inserting a 1 MΩ resistor inline with the drain of a 1200 V SiC power MOSFET had little to no impact on ion-induced degradation in the device [45]. Kuboyama *et al.* showed that this technique was also shown to be ineffective for 600 V SiC Schottky diodes [42]. These data indicate that single-event burnout is occurring faster than the RC time constant of the system. If the single-event burnout mechanism occurred at times longer than the RC time constant of the circuit, then inserting a resistor should have provided some protection. In addition, these data suggest that the energy stored in the device is contributing to the damage.

The MOSFETs and diodes also show the same degradation threshold (bias at which the device off-state leakage current begins to increase) as a function of ion LET in Figure 32 [50]. This data was also taken at Texas A&M University Cyclotron for this work. Although leakage current degradation is not a focus of this work, it is extremely important to note that the MOSFET and diode again show virtually identical behavior, as they do for single-event burnout. This further reinforces the idea of a common mechanism resulting in single-event damage for both devices.

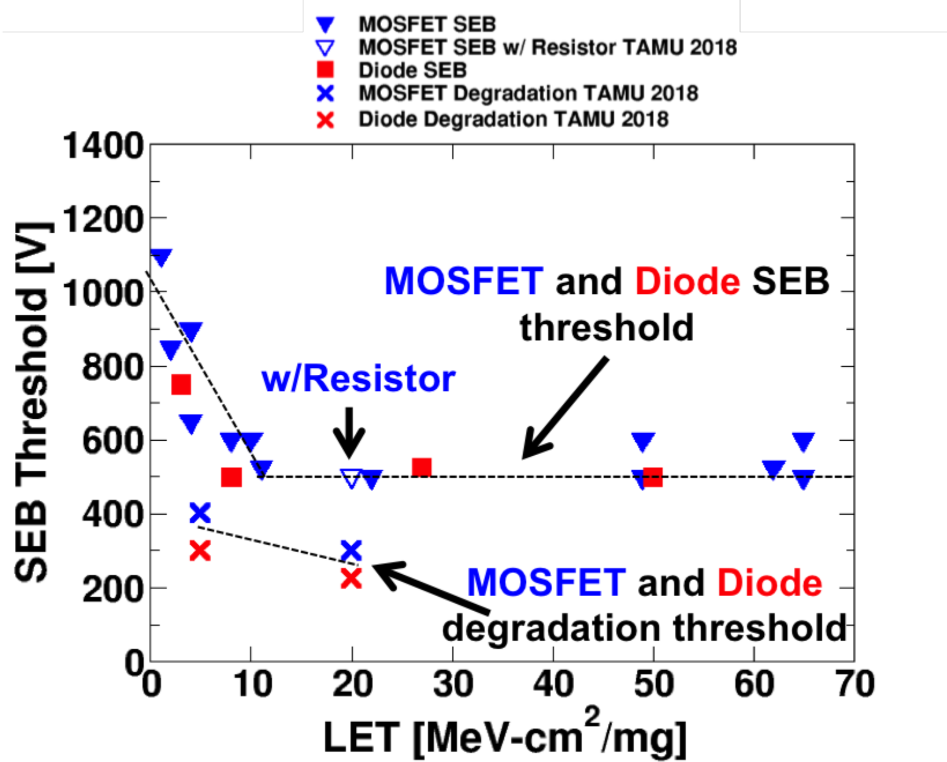


Figure 32: Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes for data taken during this work and compared to published literature [18], [19], [45], [46], [50]

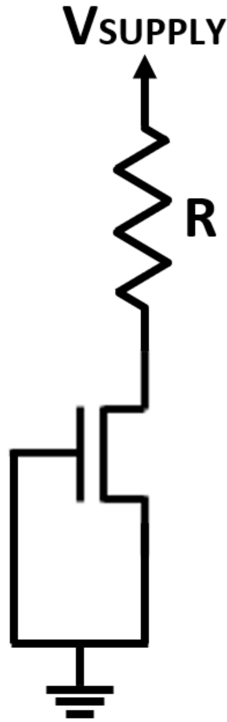


Figure 33: Circuit schematic for a non-destructive test technique for silicon power devices with a resistor inline between the power supply and the drain node

650 V - 3300 V SiC

The impact of epitaxial thickness and doping on rated breakdown voltage was discussed in Chapters II and III. A thicker, more lighly-doped epitaxial region results in a higher breakdown voltage while a thinner, more heavily-doped epitaxial region results in a lower breakdown voltage. The 1200 V power MOSFET was the first commercially viable SiC device for market consumption, available in 2006. Since that time, manufacturers have developed reliable, commercially available SiC devices ranging from 650 V to 1700 V rated breakdown voltage, with experimental devices up to 10 kV. Due to the newness of these devices, much less effort has been expended to test these devices for single-event burnout. However, limited data exist, and are shown in Figure 34, and compared to the 1200 V data. The single-event burnout data

shown are for 650 V and 1700 V JBS diodes, 900 V commercial power MOSFETs, and experimental 3300 V power MOSFETs [49]. The 650 V diode shows single-event burnout at 300 V and the 1700 V diode shows single-event burnout at 525 V. The 900 V MOSFET shows single-event burnout at 375 V, and the 3300 V MOSFET shows single-event burnout at 825 V. These data show a clear dependence of SEB_{TH} on rated breakdown voltage, which is directly a function of epitaxial thickness and doping.

In addition, Zhu *et al.* published data on multiple 1200 V equivalent device variants [55]. The data sets were sparse, and were taken for a single particle LET = 60 MeV-cm^2/mg. 16 device variants were compared to the production-ready 1200 V device. The details of the variants were discussed generically, but with no fine detail, such as specific dimensions or dopings. The data presented showed that the SEB_{TH} for the production-ready 1200 V device is approximately 500 V, consistent with the data presented in Figure 32. The data presented for the 16 variants showed that the SEB_{TH} ranges between 1000-1200 V [55].

Terrestrial neutron-induced single-event burnout data has been published by a SiC manufacturer [56], [57], and is compiled in Figure 35 for 1200 V MOSFETs and JBS diodes along with 900 V, 1700 V, and 3300 V MOSFETs. Data presented shows that the 1200 V MOSFET and 1200 V JBS diode have matching FIT rates, suggesting that a common mechanism is causing single-event burnout for two devices with the same rated breakdown voltage. These data also show a clear dependence of SEB_{TH} on rated breakdown voltage, again indicating that single-event burnout is a function of epitaxial thickness and doping.

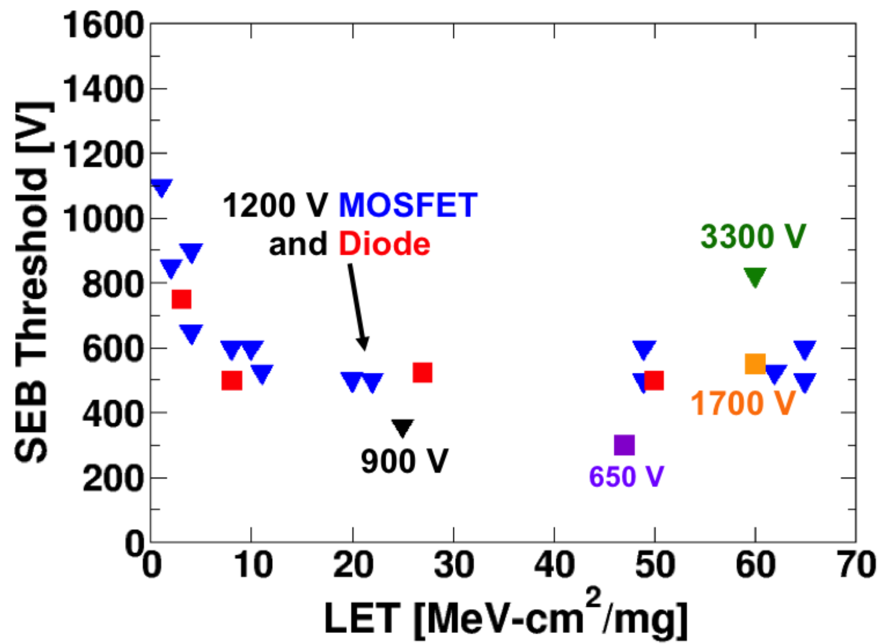


Figure 34: Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes [18], [19], [45], [46], [49], [50].

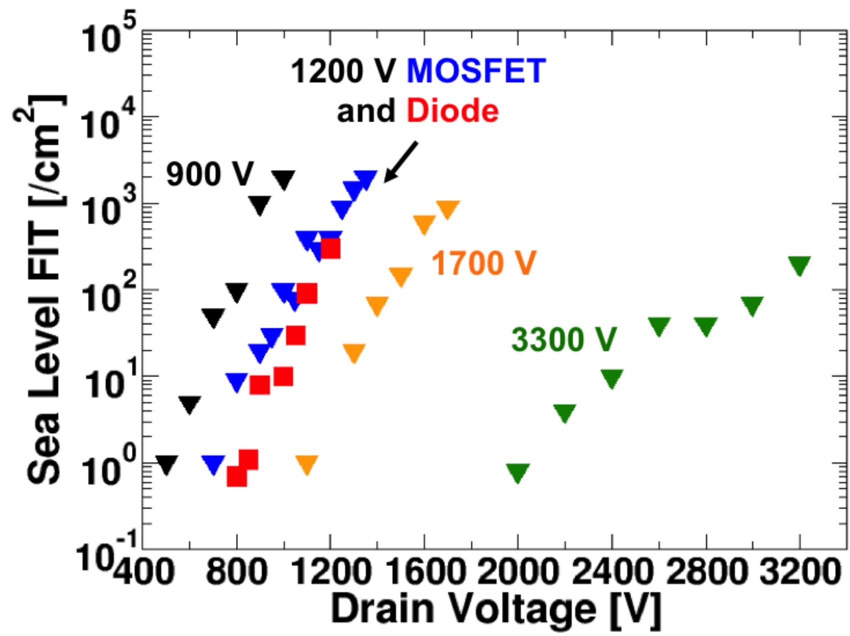


Figure 35: Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes after Lichtenwalner *et al.* and Akturk *et al.* [56], [57]

CHAPTER VI

ION-INDUCED ENERGY PULSE MECHANISM

Data presented in Figure 32 show that 1200 V SiC power MOSFETs and 1200 V JBS diodes have the same ion-induced single-event burnout threshold (bias at which single-event burnout may occur) as a function of ion LET. The devices also show the same degradation threshold (bias at which the device off-state leakage current begins to increase) as a function of ion LET. Similarly, the 1200 V SiC power MOSFET and 1200 V JBS diode have the same terrestrial neutron-induced single-event burnout threshold, shown in Figure 35. Analysis of these data indicate that the devices share a common mechanism responsible for the catastrophic failures. In addition to single-event burnout, the devices have very similar degradation thresholds suggesting a common mechanism responsible for degraded performance. In this chapter, 3D TCAD simulations are used to identify a resistive shunt effect capable of generating very high localized current transients, and consequently, significant energy dissipation in both structures. For LET and bias conditions matching the ion-induced single-event burnout threshold data, a constant amount of energy dissipation is calculated through analysis of TCAD simulation results. Similarly, a constant amount of energy dissipation is calculated for conditions matching the degradation threshold data.

Resistive Shunt Effects

An ion deposits ionizing energy in a semiconductor device by generating electron-hole pairs and creating a plasma track through the device. At very short times, the

ion track has an extremely high density of electrons and holes, and acts as a shunt, or low resistance path, between two regions [21-23]. In a vertical power MOSFET, an ion strike at normal incidence can create a shunt between the source and the drain. In a power JBS diode, the shunt is between the anode and the cathode.

The 3D TCAD models for the 1200 V SiC power MOSFET and JBS diode discussed in Chapter III are used for charge deposition simulations. In TCAD, an ion is modeled by generating a column of electron-hole pairs that is deposited in the structure. A representative arrow is overlayed on the 3D models in Figure 36 showing the approximate location of the ion track. It is assumed that the LET of the ion is constant along the entire path, and the charge is deposited spatially with a 50 nm Gaussian profile and temporally with a 2 ps Gaussian profile, which is discussed in more detail in Appendix ??.

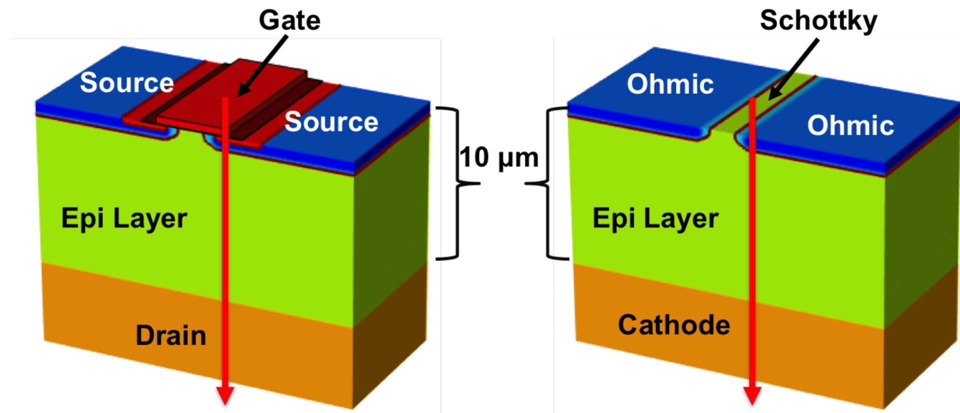


Figure 36: 3D TCAD model of a 1200 V SiC power MOSFET (top left) and JBS diode (top right) showing device structure (epi doping/depth). 2D-cutplanes indicating current flow in forward operation (middle) and fully-depleted epitaxial region at 1200 V (bottom)

The low resistance path of the shunt results in a localized current spike for the device, as illustrated in Figure 37 using 3D TCAD simulation results for an ion with

LET = 10 MeV-cm^2/mg and a drain bias of 500 V for both the 1200 V SiC power MOSFET and the 1200 V JBS diode. For approximately 100 ps after the ion strike occurs, the current transients for both devices behave identically, while at longer time scales they begin to deviate.

Avalanche breakdown, coupled with a parasitic BJT in a positive feedback loop in the MOSFET, is suggested as the reason for the simulated runaway drain current, and is discussed in greater detail in Appendix A. However, the JBS diode has no such parasitic structure, and at longer times, the charge from the ion is collected or recombines and the device appears to recover in simulation. Yet the single-event burnout data presented in Chapter V show that the SiC power MOSFETs and diodes have matching single-event burnout thresholds, suggesting that there is a common mechanism responsible for the failures. Further, the common mechanism likely occurs at short times on the order of picoseconds, shown by simulation to be the timeframe in which the MOSFET and diode behave similarly.

The internal ion-induced effects can be seen as a series of 2D-cutplanes for the MOSFET and JBS diode at 5 ps after the strike has occurred. Electron and hole current densities are shown in Figure 38 and are on the order of 1×10^7 A/cm^2 at 5 ps after the strike has occurred (current densities fall off to 1 A/cm^2 approximately 3 μm away from the ion core for electrons and a few hundred nanometers for holes). The ion-induced redistribution of the electrostatic potential and the electric fields are shown in Figure 39, with 1D-cutlines taken along the center of the ion track, shown in Figure 40 and Figure 41. The ion strike is centered above the corner of the P-type body region, where the pre-strike maximum electric field is located [9,18]. This point in time, 5 ps, corresponds to the peak current transient shown in Figure 37,

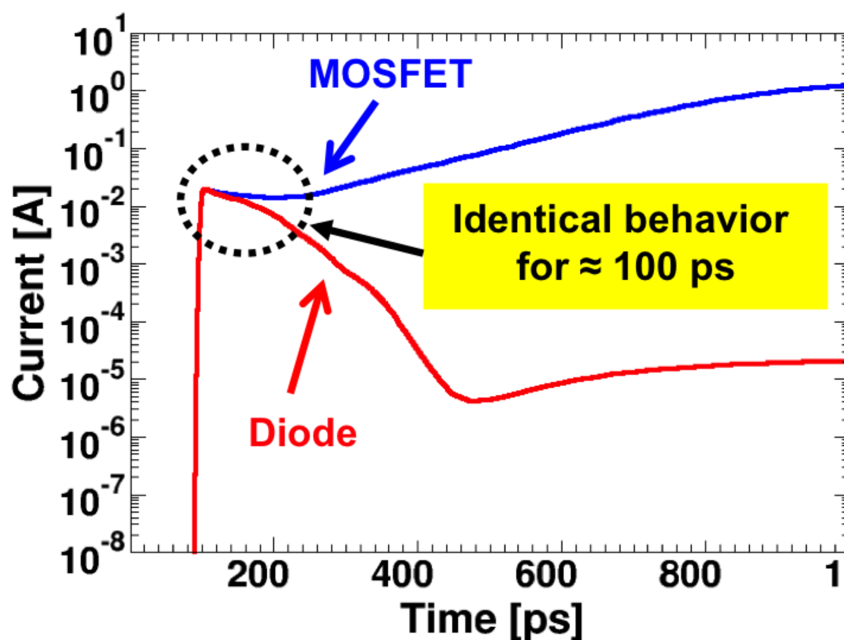


Figure 37: Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias

which is identical for both the MOSFET and JBS diode. For both devices, the peak electric field immediately after the ion strike is approximately 3.2 MV/cm, which is the critical electric field ($\mathcal{E}_{CRIT}$) required for avalanche breakdown shown in Chapter III. The ion strike redistributes the potential in a way that leads to avalanche breakdown conditions at the junction between the epitaxial region and the heavily doped drain.

This can be seen in greater detail through 1D-cutlines, taken along the center of the ion track as shown in Figure 40 and Figure 41, which compare the pre- and post-strike electric fields and potentials. This effect has also been discussed for silicon power DMOSFETs [58].

At this point in time in the simulation, the charge deposited by the ion has generated a low-resistance path, or shunt, through the MOSFET and JBS diode. However, this low-resistance path is not a linear resistor over the entire epitaxial region; rather,

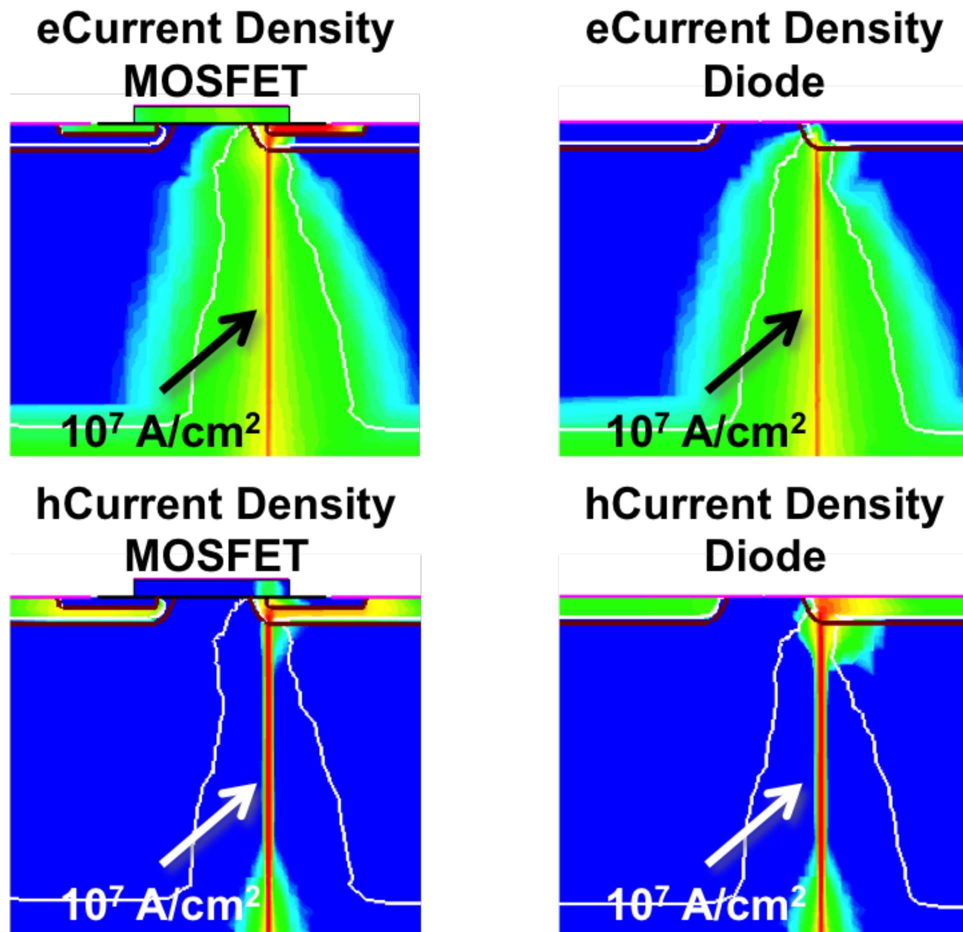


Figure 38: 2D-cutplanes in TCAD showing electron and hole current densities exceeding 1x10^7 A/cm^2 for a particle with LET = 10 MeV-cm2/mg with 500 V drain bias. 2D-cutlplanes taken at 5 ps following the ion strike.

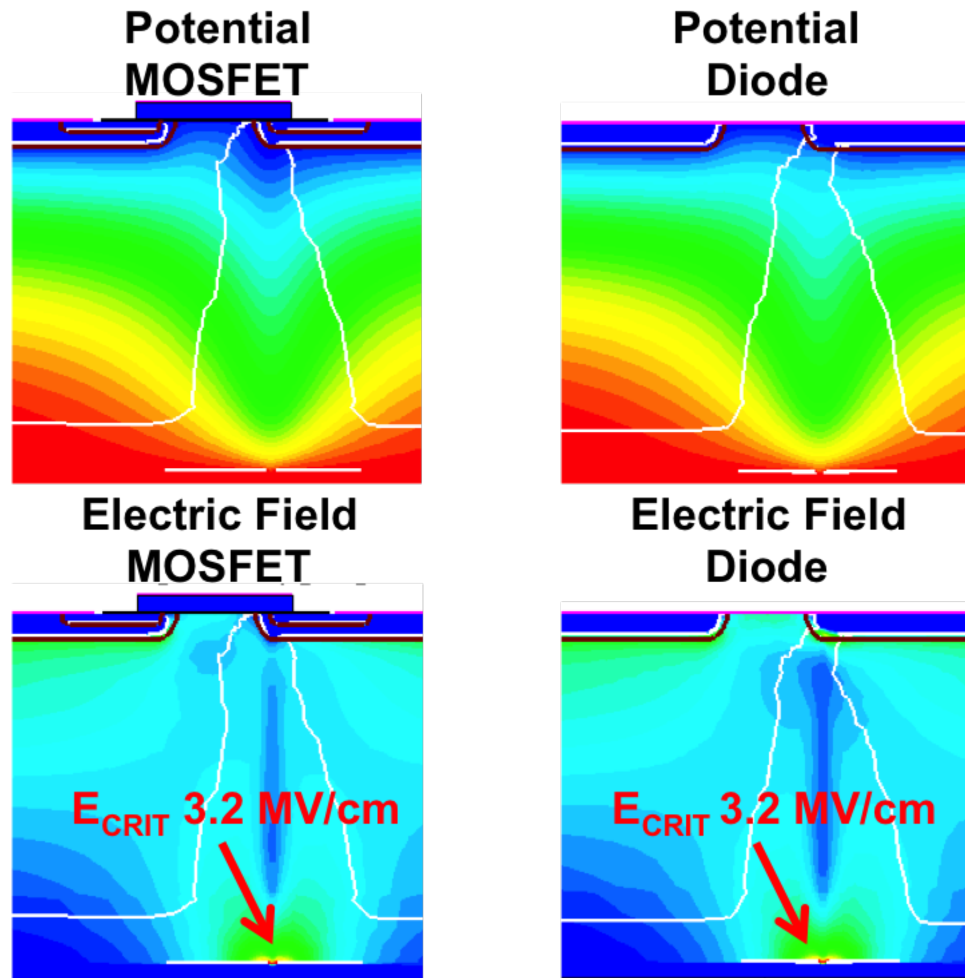


Figure 39: 2D-cutplanes in TCAD showing internal electrostatic potential and electric field ino-induced re-distribution, with electric fields exceeding 3.2 MV/cm for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 2D-cutlplanes taken at 5 ps following the ion strike.

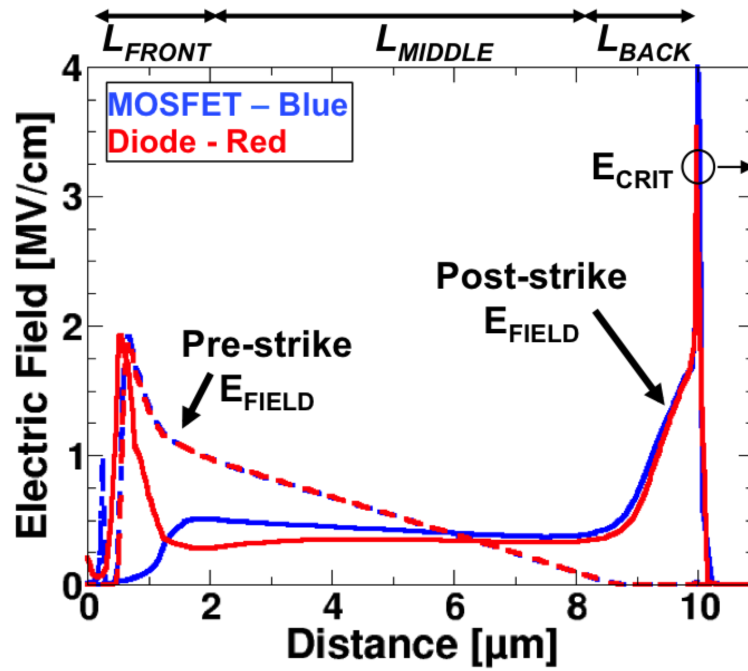


Figure 40: 1D-cutline in TCAD showing pre- and post-strike electric fields exceeding 3.2 MV/cm for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

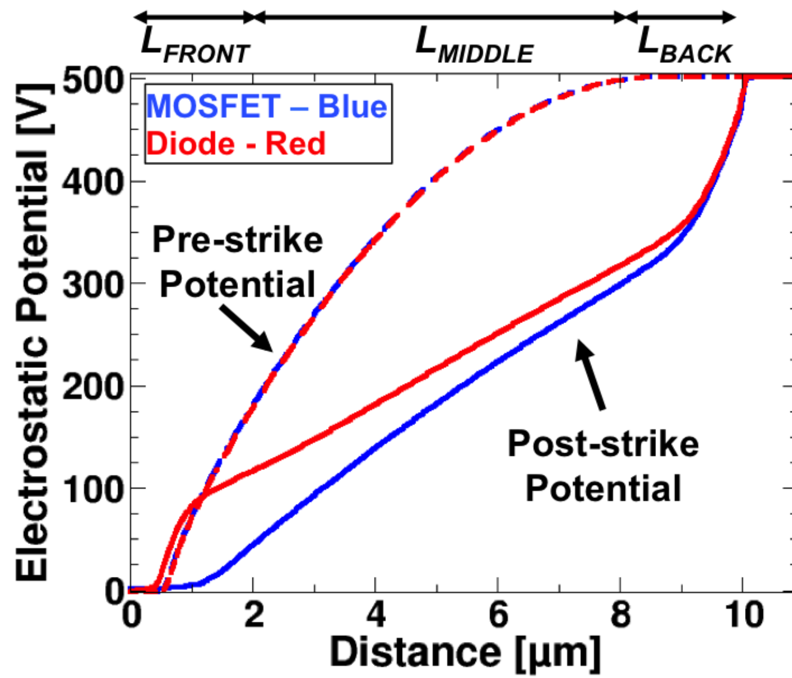


Figure 41: 1D-cutline in TCAD showing pre- and post-strike internal electrostatic potential (bottom) for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

three distinct conductive regions have developed due to non-equilibrium conditions and each region can be defined in terms of length in Equation 11 as:

$$L_{EPI} = L_{FRONT} + L_{MIDDLE} + L_{BACK} \tag{11}$$

with L_{BACK} shown in Figure 40 as the region with the greatest peak electric field and gradient (greatest change in potential), located near the junction where the lightly-doped epitaxial layer meets the heavily doped drain. The surface region, defined as L_{FRONT}, also shows a sharply peaked electric field and gradient. However, the middle of the epi region, defined as L_{MIDDLE}, has a significantly lower electric field and very low gradient (small change in potential). The low gradient of L_{MIDDLE} defines this region independently from L_{FRONT} and L_{BACK}. The total power dissipation during the event can be described by

$$PowerDensity[W/cm^3] = J[A/cm^2] \cdot \mathcal{E}[V/cm] \tag{12}$$

where J is the current density and $\mathcal{E}$ is the electric field, with units for each shown in brackets. The power density is along the core of the ion track is shown in Figure 42. In both the MOSFET and diode, power is primarily dissipated at the interface between the epitaxial region and the heavily doped drain.

The total power density along the ion track can be described by

$$TotalPowerDensity[W/cm^2] = \int (J[A/cm^2] \cdot \mathcal{E}[V/cm])dx \tag{13}$$

and is shown in Figure 43, indicating that approximately 40% of the power is dissipated in the region defined as L_{BACK} (2 μm) and 15% in the region defined as L_{FRONT} (1 μm), with only 35% attributed to the region of L_{MIDDLE} (7 μm). Almost half of the total power dissipated during the ion strike occurs at the junction between the epitaxial region and the heavily doped drain.

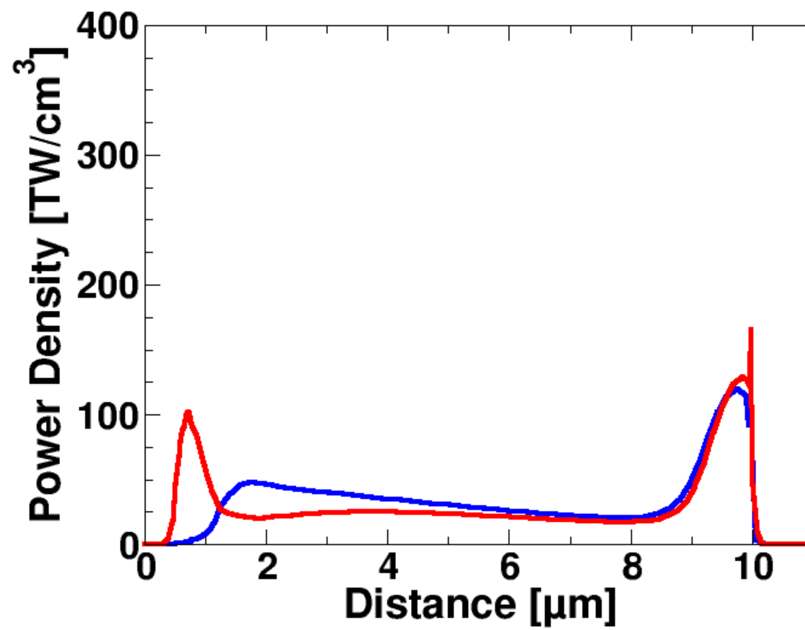


Figure 42: 1D-cutline in TCAD showing post-strike power density for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

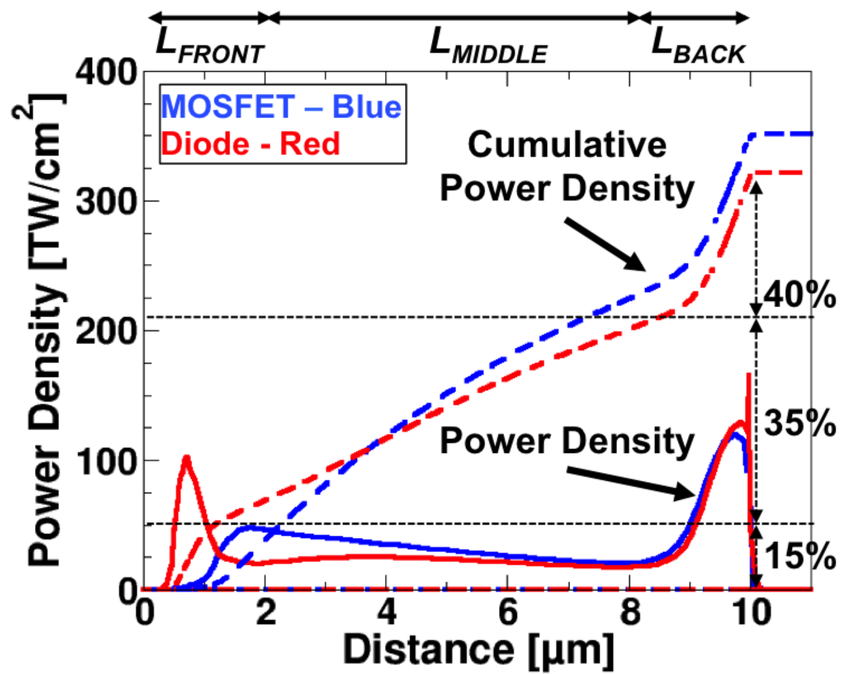


Figure 43: 1D-cutline in TCAD showing post-strike cumulative power density for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

Energy Pulse Mechanism

Power MOSFETs and diodes are designed specifically to block high voltages in the off-state and conduct high currents in the on-state. In normal operation, high current and high voltage do not exist at the same time (at least not for very long!). During an ion-initiated event, the device begins with high voltage dropped across the epitaxial region and the ion quickly increases the current, possibly leading to excessive power dissipation. TCAD simulations are used to generate power density curves for a range of ion LETs and device biases, for both the MOSFET and JBS diode, with examples shown in Figure 44 comparing two LET values at a fixed bias. The power density vs. position curves for both the MOSFET and diode exhibit the same overall shape in all cases, however, the magnitude of the power density increases with increasing LET and bias. This sensitivity can be more easily analyzed by integrating the power density spatially (to account for volume) across the entire epi region of the ion track and temporally (to account for time) to determine the amount of energy dissipated during each event described by

$$Energy[J] = \int\int (J[A/cm^2] \cdot \mathcal{E}[V/cm] \cdot A_{ION}[cm^2])dxdt \qquad (14)$$

where A_{ION} is the area of the ion track. For this work, the area of the ion track is assumed to be constant across ion LET, with the gaussian rolloff parameter defined as 50 nm. The calculated energy during each event is shown in Figure 45. For bias and LET conditions consistent with the experimentally-determined single-event burnout thresholds shown in Figure 32, the energy dissipated during the 10 ps immediately following the event ranges from 2-3 nJ, as shown in Figure 45 (depicted by the yellow region). For example, an ion strike for LET = 2 MeV-cm^2/mg and 1300 V results

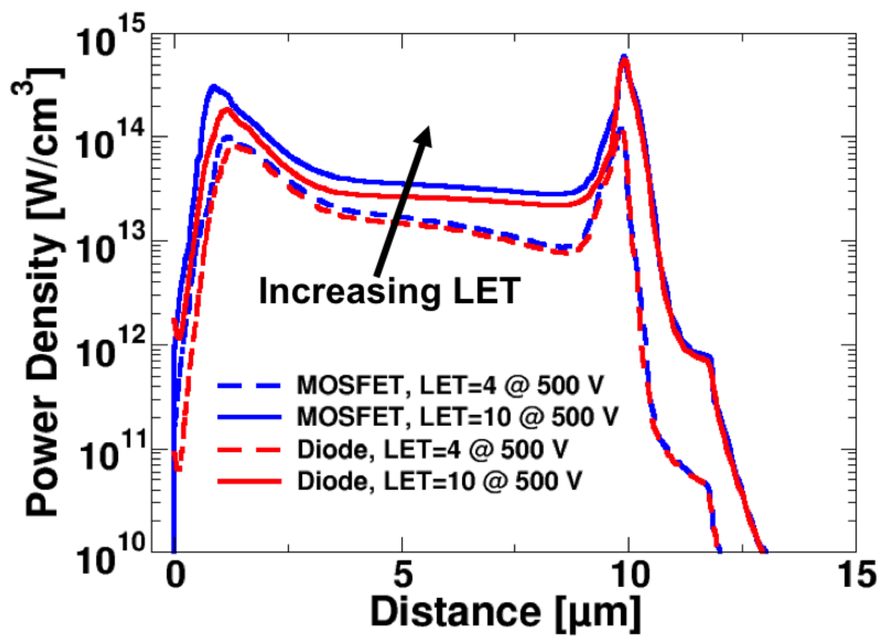


Figure 44: 1D-cutline in TCAD showing post-strike power density and cumulative power density for a particle with LET = 4 and 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

in 2.5 nJ/2.4 nJ in the MOSFET/JBS diode, while LET = 10 MeV-cm^2/mg at 500 V results in 2.6 nJ/2nJ in the MOSFET/JBS diode. For events that are above the single-event burnout threshold, more energy is dissipated, and for events that are below the single-event burnout threshold, less energy is dissipated (pink region in Figure 45). For events that occur at bias and LET conditions consistent with experimentally-determined degradation threshold, the result is virtually identical to the single-event burnout analysis, just lower in magnitude, suggesting that single-event burnout is a catastrophic form of what has been termed degradation. In all cases, this energy dissipation occurs over 10 ps, which is a very short time, considering that power devices have switching speeds on the order of microseconds. Also in all cases, both the MOSFET and the JBS diode behave almost identically.

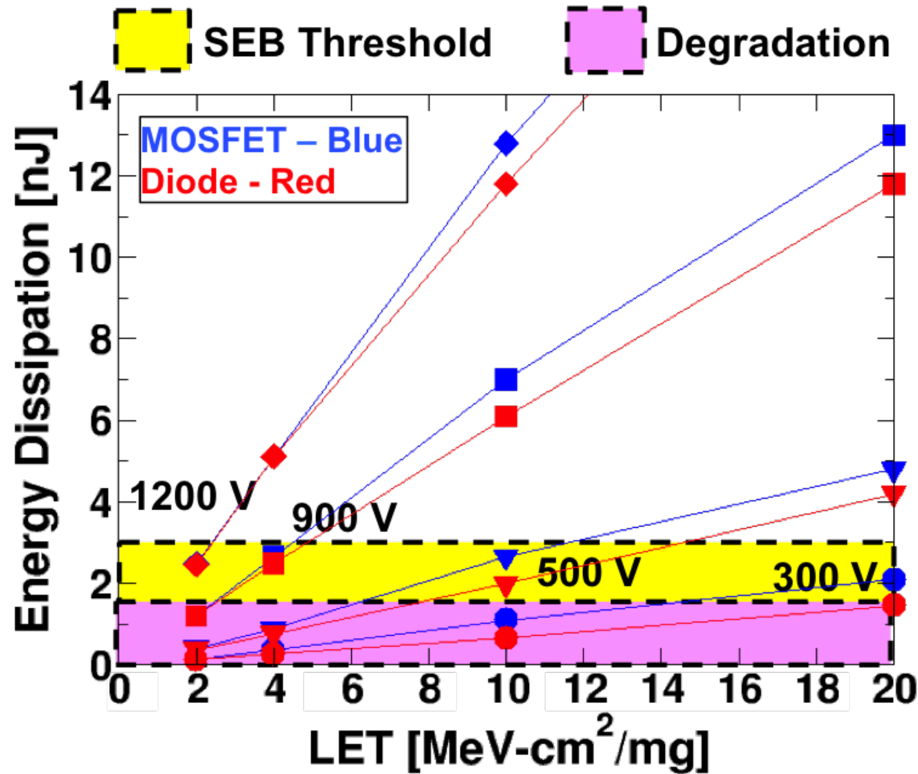


Figure 45: TCAD calculated energy dissipation for 10 ps following the strike with the SEB_{TH} conditions highlighted.

Inline Resistor Effects

Due to the short timeframes of ion-induced transients, experimentally measuring localized energy pulses is challenging and perhaps impossible considering the highly-localized aspect of the events. For example, a typical avalanche stress test pulses an entire device (i.e., die area 2 mm x 3 mm) with current transients lasting tens of microseconds [16], compared to ps-ns timeframes for single-events in volumes limited to hundreds of nanometers. A non-destructive test technique of inserting a resistor in line with the drain was not effective for mitigating single-event burnout in these devices, as shown in Figure 32, and seen in other work [45], [42]. Due to the time constant of the circuit, if the single-event burnout failures resulting from transients occur on the order of nanoseconds to microseconds, then inserting a resistor should have provided some protection.

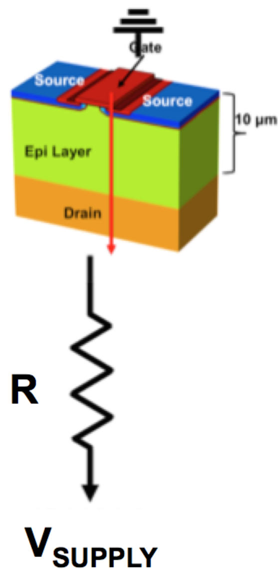


Figure 46: Circuit schematic for a 3D-TCAD mixed mode ion-strike simulation with a resistor inline between the power supply and the drain node

3D TCAD mixed-mode simulations (schematic shown in Figure 46), indicate that

connecting a resistor in line between the drain and power supply works as designed for the MOSFET, with results shown in Figure 47, provided that the device can survive at least a nanosecond following the ion strike. In simulation, the inline resistor has allowed the bias across the MOSFET to decrease, effectively decreasing both avalanching and parasitic BJT responses, and the drain current shows a recovery. The inline resistor does not impact the simulated response of the diode to any measurable degree. For time scales on the order of tens of picoseconds, the simulated ion-induced current pulse is identical for both the MOSFET and diode, independent of the inline resistor. As noted above, data shows no impact on single-event burnout by adding an inline resistor. Thus, data shown in Figure 32 and in other work [45], combined with TCAD simulations, indicate that the inline resistor provides no benefit and confirms that damage is occurring on a time scale faster than the time constant of the device. The response time of the R/C loaded circuit is far too slow to suppress the energy pulses that result in catastrophic single-event burnout or degradation. It also indicates that the destructive energy is from the local stored die capacitance rather than the externally applied voltage source.

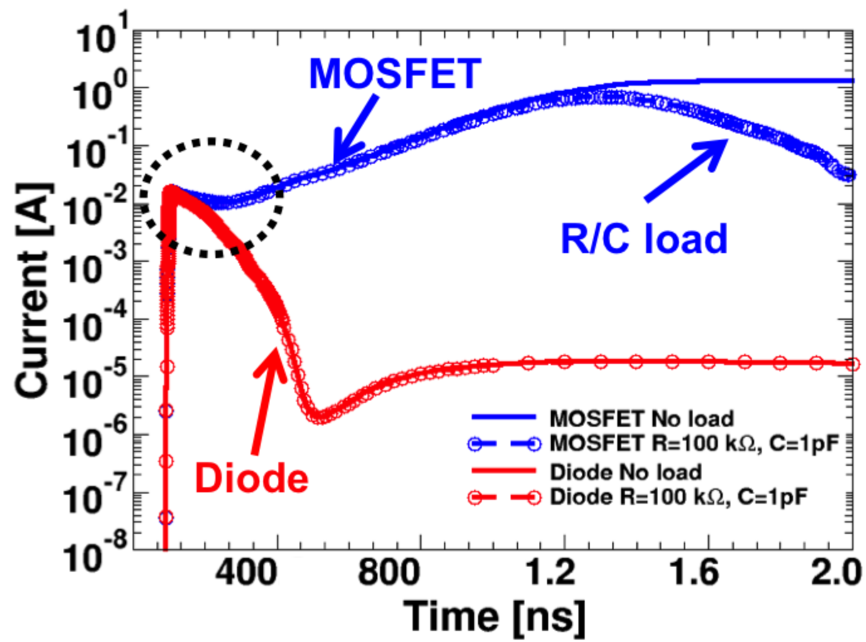


Figure 47: 3D TCAD mixed-mode ion-strike simulations for both the MOSFET and JBS diode using non-destructive technique for adding a resistor inline with the power supply. Ion LET=10 MeV-cm^2/mg and devices biased at 500 V

Localized Thermal Effects

As current flows in a semiconductor device, the power dissipated can lead to increased lattice temperatures. As discussed throughout this dissertation, a device is normally operated in such a way to minimize internal power dissipation, but an ion-strike can result in significant localized power dissipation. Ion-induced thermal effects have been simulated by multiple authors using multiple simulation tools and the results are consistent in the fact that higher LET ions can cause significant thermal rise to temperatures exceeding that of the SiC sublimation point (3000 K). However, the published results are focused on a high LET, high bias conditions and was discussed in detail in Chapter IV and briefly summarized again in Table 6 and organized by increasing particle LET. Based on the simulated results from literature, for LET $\geq$ 35 MeV-cm^2/mg, lattice temperatures reaching the sublimation point of SiC are possible. However, the impact of low LET particles on lattice temperature has not been investigated fully.

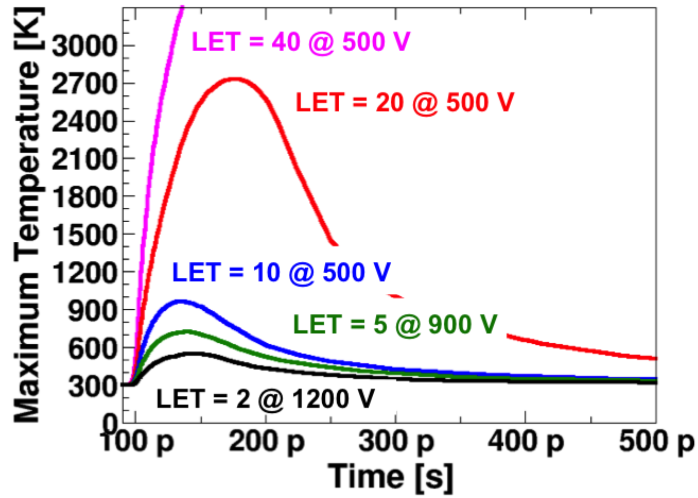
Table 6: TCAD-simulated maximum lattice temperature as a function of device bias and particle LET

Device	Bias [V]	LET [MeV-cm^2/mg]	Temperature [K]	Reference
Diode	500	28	1,773	[59]
Diode	800	35	$\geq$ 3,000	[47]
Diode	500	40	2,600	[18]
Diode	220	42	2680	[42]
Diode	200	62	$\geq$ 10,000	[60]
MOSFET	500	46	$\geq$ 3000	[48]

For this dissertation, thermodynamic 3D TCAD simulations were run for bias and LET conditions matching those of the single-event burnout threshold shown in Figure 32. Thermodynamic simulations compute the lattice temperature, and

describe self-heating due to current flow in the device. For the 1200 V SiC diode, the simulated maximum lattice temperature is shown in Figure 48 for a strike directly to the center of the device, at the Schottky contact, which was determined to be the worst case strike location in other works. For an LET = 2 MeV-cm^2/mg @ 1200 V, ion data shows single-event burnout. The maximum lattice temperature from simulation for those conditions is 530 K. The maximum lattice temperature increases to 950 K for an LET = 10 MeV-cm^2/mg @ 500 V. Up to an LET = 10 MeV-cm^2/mg, there does not appear to be any significant thermal increase sufficient to catastrophically damage SiC. At an LET = 20 MeV-cm^2/mg and 500 V, the maximum lattice temperature reaches 2700 K, very near the sublimation point of SiC, and an LET = 40 MeV-cm^2/mg drives it above and beyond 3000 K. Similar results are shown in Figure **??** for the 1200 V SiC MOSFET, for a hit location at the corner of the p-body and epitaxial region, and for LET $\leq$ 10 MeV-cm^2/mg, lattice temperature stays below 1100 K, while LET $\geq$ 20 MeV-cm^2/mg results in significantly higher lattice temperatures.

These simulation results for both the diode and the MOSFET show a clear dependence of lattice temperature on particle LET. Additional simulation results are shown in Table 3 where maximum lattice temperature is a function of ion strike location at the LET/bias conditions consistent with the single-event burnout threshold. For all hit locations, low LET particles do not generate a significant increase in lattice temperature. This is due to the low charge density along the core of the track when compared to the high LET particles, which do result in significantly higher lattice temperatures.This indicates that single-event burnout from thermal rise in the SiC lattice is unlikely from low LET particles. However, at higher LETs, thermal effects may contribute to damage, both degradation and single-event burnout.



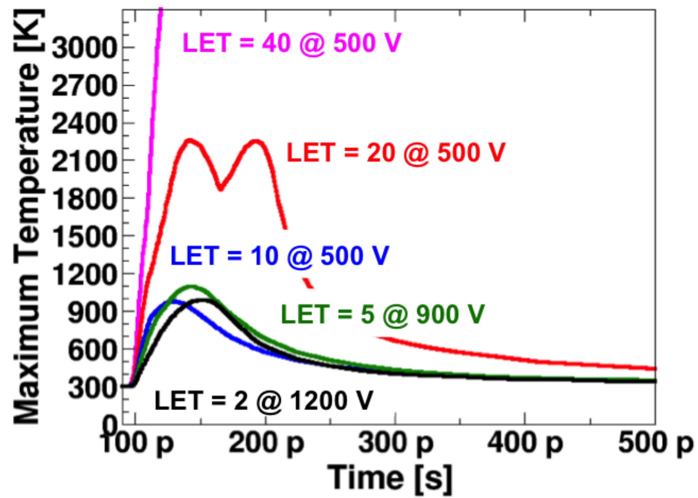
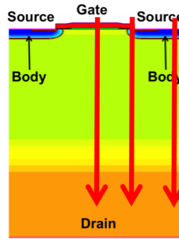


Figure 48: 3D TCAD simulated maximum lattice temperature for ion LET (in MeV-cm^2/mg) and bias consistent with the single-event burnout threshold for 1200 V SiC JBS diode (top) and SiC MOSFET (bottom)

It is important to note that these simulations only take into account heating in the SiC lattice. As discussed in the ion-induced energy pulse analysis, there is significant current flowing in the device and through the contacts. The simulator treats the contact as an ideal heat sink. In reality, large currents are flowing across the SiC/metal interfaces. Interfaces between semiconductors and metals/oxides may be susceptible to damage at far lower temperatures than the SiC can tolerate, in addition to other effects such as electromigration or metal delamination.

Table 7: 3D TCAD-simulated maximum lattice temperature as a function of ion strike location for ion LET (in MeV-cm^2/mg) and bias consistent with the single-event burnout threshold for 1200 V SiC JBS diode and SiC MOSFET. DNC indicates a simulation that Did Not Converge



	Diode		
LET @ Bias	Center Gate	Source/Body	Body/Drain
2 @ 1200	550	690	707
5 @ 900	720	820	844
10 @ 500	970	990	1030
20 @ 500	2700	1900	2010
40 @ 500	$\geq$ 3000	3800	$\geq$ 2300
	MOSFET		
LET @ Bias	Center Gate	Source/Body	Body/Drain
2 @ 1200	DNC	990	700
5 @ 900	DNC	1100	840
10 @ 500	650	975	1030
20 @ 500	DNC	2200	1953
40 @ 500	$\geq$ 4600	$\geq$ 4600	$\geq$ 4600

To conclude this chapter, ion-induced, highly-localized energy pulses are proposed as the common mechanism responsible for catastrophic single-event burnout in 1200

V SiC power MOSFETs and JBS diodes. As discussed earlier, analysis of heavy-ion data indicates that these devices have matching single-event burnout thresholds suggesting that there is a common mechanism responsible for the catastrophic failures. 3D TCAD simulations are used to identify similarities in both structures during an ion event showing a resistive shunt effect capable of generating very high localized current transients, and consequently, significant energy dissipation. For LET and bias conditions matching the single-event burnout threshold data, a constant amount of energy dissipation is calculated through analysis of TCAD simulation results. A non-destructure test technique of using an inline resistor does have any impact on the extremely fast (50 ps) response of either the diode or the MOSFET in simulation, which agrees with data showing the inline resistor is ineffective. Simulated ion-induced lattice heating is also explored for bias/LET conditions matching those of the single-event burnout threshold, indicating that for LET under 20 MeV-cm^2/mg, there is insufficient localized thermal rise in the SiC lattice to account for catastrophic damage.

CHAPTER VII

EVALUATION OF DEVICE VARIANTS

As shown earlier in this work, high-voltage SiC power MOSFETs and junction barrier Schottky (JBS) diodes are susceptible to device degradation due to increased leakage currents and single-event burnout due to heavy-ion exposure in space and terrestrial neutron irradiation. Increasing the reliability of SiC power devices by mitigating these effects, typically through process modifications, is a high priority. Both the heavy ion data, shown in Figure 34, and the neutron data, shown in Figure 35, indicate that voltage rating significantly impacts the single-event burnout threshold, with higher voltage ratings resulting in higher SEB_{TH}. In power devices, increased epitaxial region thickness and lower epitaxial doping results in higher rated breakdown voltage, with little to no change for the surface structure and metalization. single-event burnout data indicate that increased epitaxial thickness and lighter doping results in increased single-event burnout survivability.

In this chapter, 3D TCAD heavy ion simulation results are analyzed for three power MOSFETs designs using the methodology developed in Chapter VI showing the power dissipation after an ion strike is capable of causing single-event burnout in SiC power MOSFETs and diodes. Analysis using this technique suggests that the 3300 V MOSFET provides almost 50% reduction in total power dissipated along the ion track core compared to a 1200 V MOSFET, confirming the trends shown in the data. The third simulated MOSFET is a dual-epi 1200 V design using a buffer layer (which is a well-known semiconductor design technique for reducing abrupt junctions),

which shows no improvement in power dissipated along the ion track core, although it does mitigate electric field peaks during the ion event.

MOSFET Device Variants - Epitaxial Design

The 1200 V baseline device was discussed in Chapter III. Two additional device variants were selected for simulation based on an evaluation of the currently available data and previously published literature. In all variants, the surface structure remains unchanged. The first variant is based on an experimental 3300 V SiC power MOSFET with an epi doping of 2×10^{15} cm−3, and a thickness of 30 μm [16], [61]. The second variant is a dual epi design using a buffer layer approximately 2 μm thick, after McPherson *et al.*. This design was suggested as an improvement in single-event burnout robustness for heavy ion exposure by reducing the peak electric field that develops during an ion strike at the junction between the epitaxial and drain regions [48]. The use of buffer layers in SiC devices has also been documented in literature for a variety of device structures [62], [63], [64], [65], [66]. McPherson *et al.* did not provide detailed doping levels for their buffer layer design, however, it can be assumed to be approximately 1-2 orders of magnitude higher than the epitaxial doping level. For this work, the doping level of the buffer layer was selected to be 1 $\times 10^{17}$ cm^{-3} and this variant is referred to as the 1200 V Dual Epi. 1D-cutlines of the epitaxial and substrate doping, with dimensions, are shown in Figure 49. Note that the epitaxial doping is almost an order of magnitude lower and the epitaxial thickness is three times wider for the 3300 V device when compared to the 1200 V device.

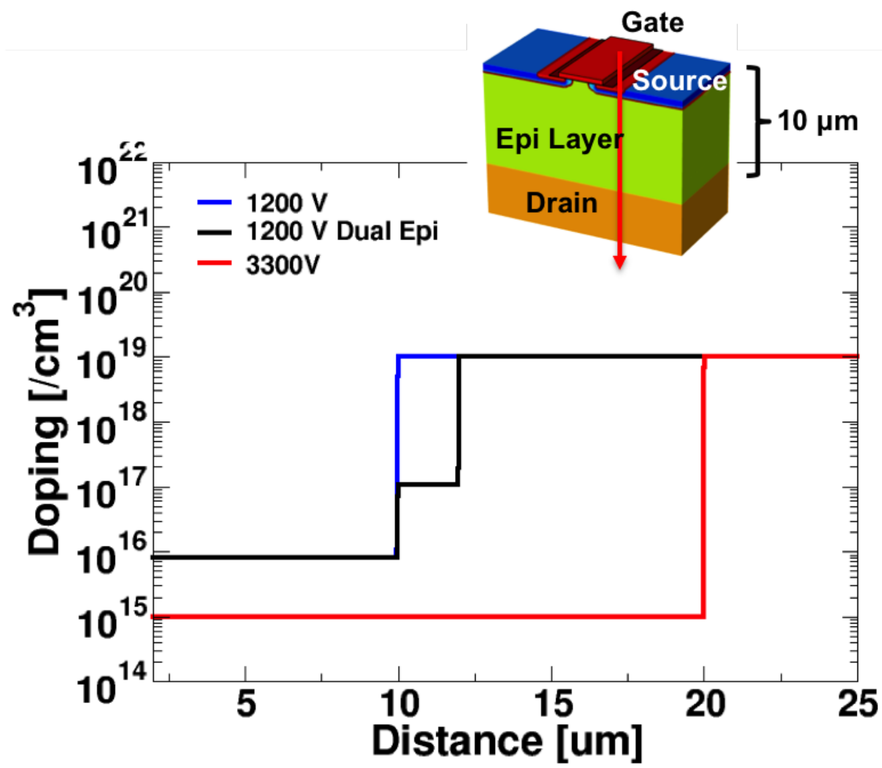


Figure 49: 3D TCAD model of a 1200 V SiC power JBS diode showing device structure, also shown is a representative long-range ion track (top). 1D-cutlines of net doping through the epi and drain regions for each variant (bottom)

MOSFET Device Variants - Ion Simulations

As shown previously, during an ion-strike, the 1200 V device enters a region of operation with both high current and high voltage, leading to excessive localized power dissipation. 3D TCAD simulations were performed for an ion with LET of 10 MeV-cm^2/mg and a reverse bias of 500 V for each of the two MOSFET design variants, and compared to the 1200 V device. Simulation results are shown in Figure 50 and Figure 51 for the electron and hole current densities, respectively. For each variation of the 1200 V device, the peak current densities are approximately equal. However, the peak current densities for the 3300 V device are approximately half as large as the 1200 V device.

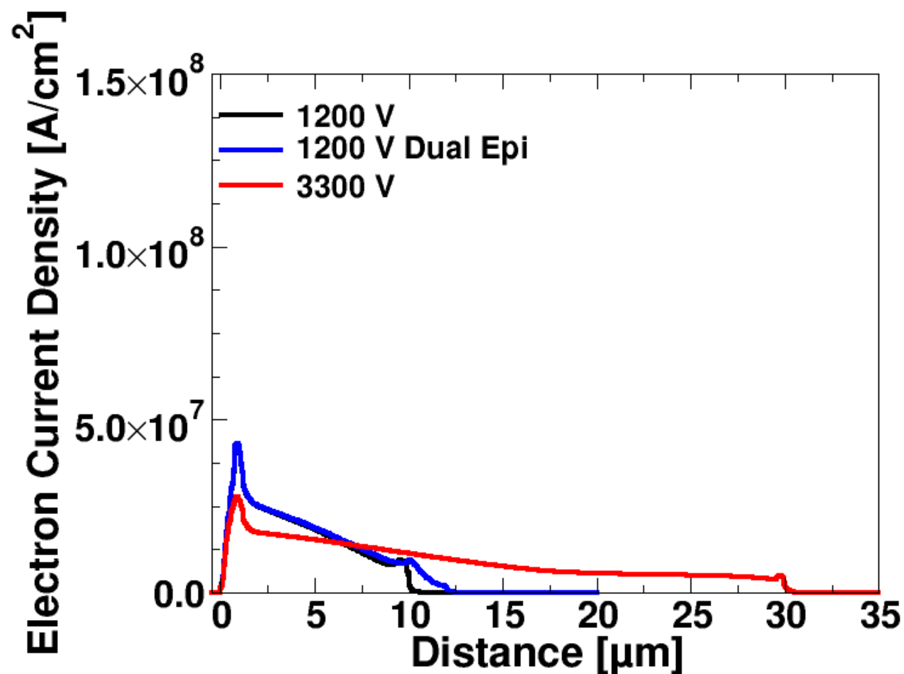


Figure 50: Ion-induced electron current density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias.

The ion-induced shunt effect also results in electric field redistribution during

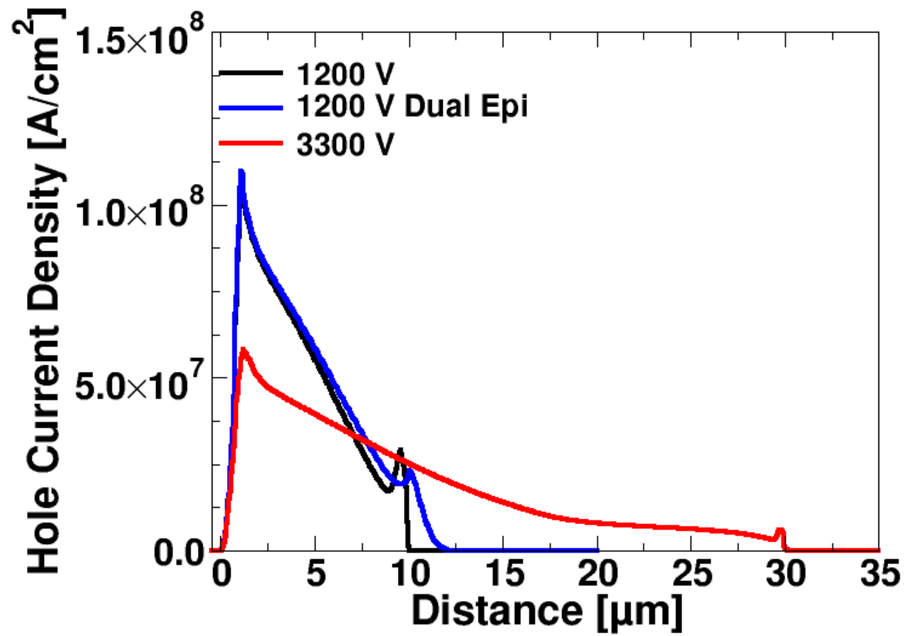


Figure 51: Ion-induced hole current density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias.

the event. Simulated results are shown in Figure 52 for each of the devices. The general trends are the same for each device, with the electric field showing a spike at the interface between the epitaxial and drain regions. For the 1200 V and 3300 V devices, the magnitude of the electric field spike is above the critical electric field for electrical breakdown. In the 1200 V Dual Epi device variant, the electric field spike remains lower than the pre-strike peak electric field, but the electric field for the first 8 μm of the epitaxial region is slightly higher than the 1200 V device. As previously discussed, the integral of the electric field curve is the externally applied bias, and for the spike at the interface between the epitaxial and drain regions to decrease, then the electric field must increase in another region.

The simulated power density along the core of the track is shown in Figure 53 at

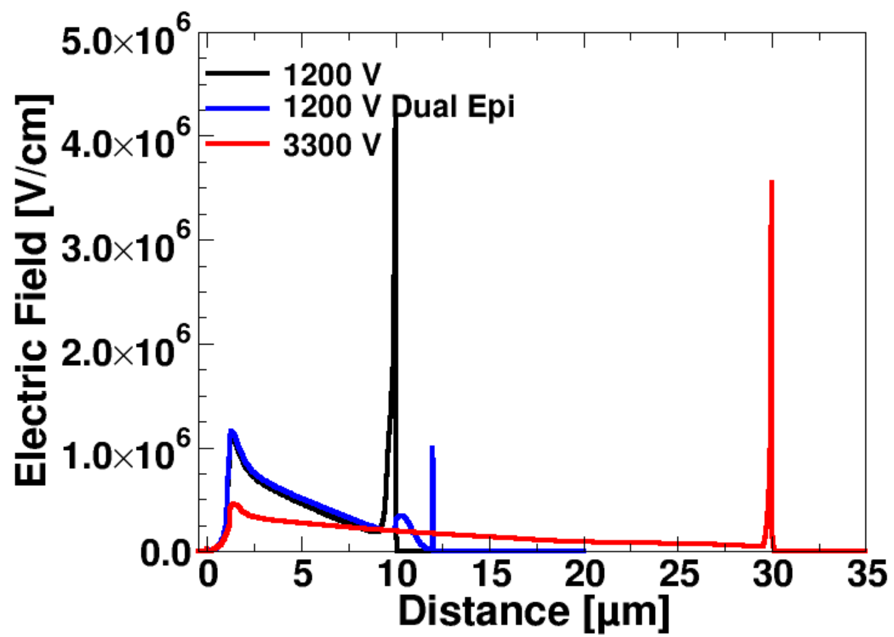


Figure 52: Ion-induced hole electric field re-distribution at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias.

20 ps following the ion strike. These simulation results show that the 1200 V devices have virtually identical characteristics, while the peak power density in the 3300 V device is decreased by almost an order of magnitude, although it does extend an additional 20 μm until terminating at the interface between the epitaxial and drain regions.

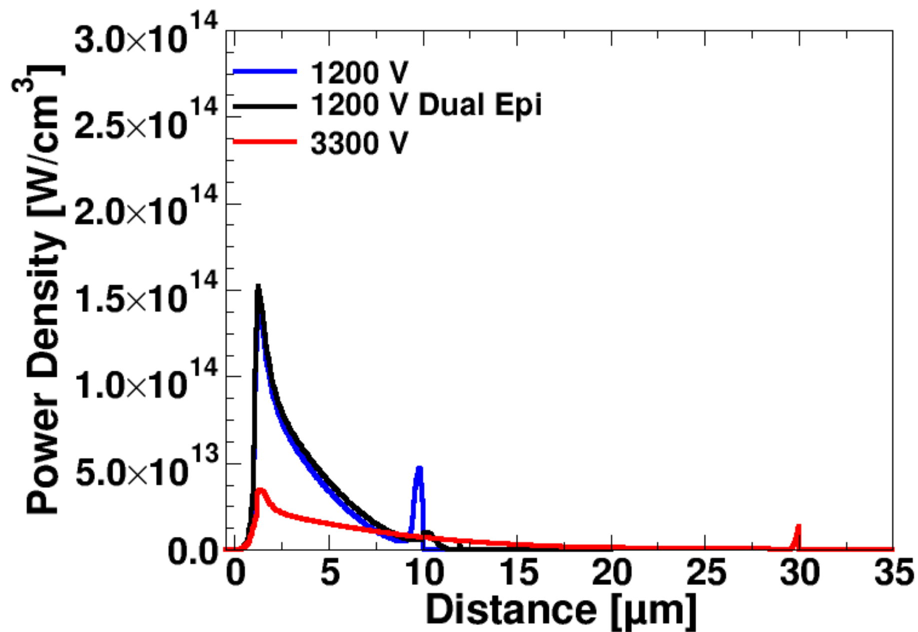


Figure 53: Ion-induced total power density at 20 ps following the strike for SiC power MOSFETs for particle with LET=10 MeV-cm2/mg and 500 V drain bias.

This can be further analyzed by integrating across the epitaxial thickness, showing cumulative power density dissipated along the core of the ion track, shown in Figure 54. The total power for the 1200 V Dual Epi design is slightly higher than the total power in the baseline device. In contrast, the 3300 V device shows a dramatic 51% reduction in total power during the ion strike compared to the 1200 V baseline device. The increased epitaxial thickness and lower epitaxial doping result in lower

peak electric fields and lower total current during the strike compared to the other two devices. Increasing the thickness of the epitaxial region reduces the total power dissipation resulting from the ion strike, confirming the trends seen in data.

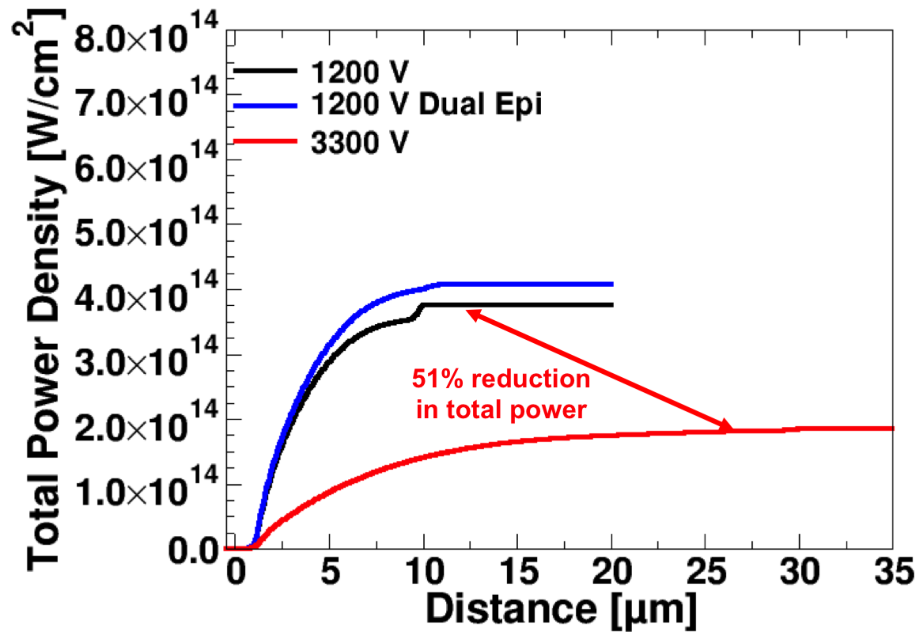


Figure 54: Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias

3D TCAD simulations are used to generate total power density for a range of ion LETs (2-60 MeV-cm^2/mg) and device biases (100 V – 1200 V). The simulated data is shown in Figure 55 for the 1200 V and 3300 V device designs. The 3300 V device showed an average of 49% reduction in total power when compared to the 1200 V device. This is extremely important because the total power dissipated during the ion event is consistently lower in the 3300 V device when compared to the 1200 V device, indicating improvements across the entire range of ion LET and device bias. The power dissipation savings are not restricted to any particular subset of the range,

rather, they encompass it entirely.

Also of note is that each of the device variants show trends matching the ion-induced single-event burnout data shown in Figure 32, which has a strong inflection point with a slope change for the single-event burnout threshold. This is highlighted in Figure 55 by the dashed line which shows the single-event burnout threshold for the 1200 V device. For the 3300 V device, the curve lies safely in the "green" region, which denotes the safe operating area. While this is not intended to predict a single-event burnout threshold for the 3300 V device, it is consistent with the measured data showing that a thicker, and more lightly-doped epitaxial region result in a higher single-event burnout threshold.

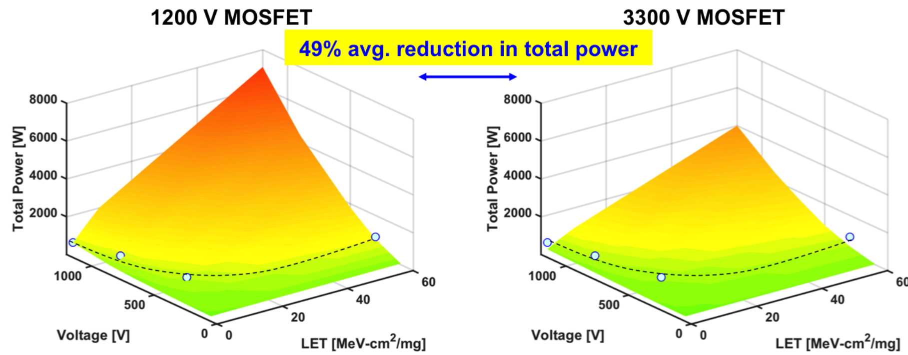


Figure 55: Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias

Simulation results are analyzed for three power MOSFET designs. The 3300 V MOSFET provides almost 50% reduction in total power dissipated along the ion track core compared to a 1200 V MOSFET, agreeing with the trends shown in the data. The third MOSFET is a dual-epi 1200 V design using a buffer layer, which shows no reduction in the power dissipated along the ion track core as compared to the 1200

V baseline, although it does reduce the electric field peak during the ion event.

CHAPTER VIII

MITIGATING SINGLE-EVENT BURNOUT THROUGH DEVICE SELECTION AND CIRCUIT DESIGN

Successfully designing a power electronic circuit to operate while minimizing the risk of single-event burnout causing catastrophic failure of the circuit is important for both space and terrestrial applications. Circuit designers must understand the environment and the mechanisms contributing to single-event burnout in order to appropriately select components. The components are then used in a specific circuit topology with an appropriate voltage derating in order to survive the intended or expected environment.

In Chapter IV, the concept of derating was introduced for SiC power devices, which is typically based on the rated breakdown voltage for a device. In Chapter VII, ion-induced burnout was analyzed comparing 1200 V and 3300 V SiC power MOSFETs showing that the 3300 V MOSFET has an almost 50% reduction in total power dissipated along the ion track core compared to a 1200 V MOSFET. This analysis supported data shown in Chapter V indicating that increased rated breakdown voltage results in increased single-event tolerance. In this chapter, a brief comparison of silicon versus SiC devices and the implications for circuit designs will be discussed to establish the benefits of using SiC over silicon. Further analysis for SiC part selection will focus on power losses at the transistor level when selecting a 3300 V device over a 1200 V device. These power losses can be mitigated by using multiple devices in parallel, which presents additional tradeoff choices of increased cost, weight, area, and

cross-section for an ion strike. However, increasing the operating voltage of the circuit results in fewer system power distribution losses. Implications for circuit design show that using a 3300 V power MOSFET provides ample single-event burnout threshold margin for space applications up to 600 V up to an LET of 60 MeV-cm^2/mg, while the 1200 V device is susceptible to single-event burnout with these parameters. In a terrestrial environment, the 3300 V device can safely operate up to 2000 V with little risk of neutron-induced single-event burnout.These concepts will be the focus of the remainder of this chapter.

Silicon vs. SiC

Silicon carbide (SiC) is superior to silicon for use in many power device applications due to significantly higher breakdown electric fields and significantly lower on-state resistance [2]. These benefits can be attributed to the electrical properties of SiC compared to silicon, a few of which were summarized [14] and shown previously in Table 1. For a given applied potential (the area under the electric field curve), the electric field in SiC can reach much higher peaks over much shorter distances when compared to silicon. This effect directly results in lower on-state resistance and higher drive currents for SiC compared to silicon. For traditional silicon power devices, designing a high-voltage, low-resistance device has proven to be challenging, with the state-of-the-art MOSFETs rated at 1000 V [12] and 8 A, with 1450 mΩs of on-state resistance (R_{ON}). The characteristics of SiC have yielded commercially available high-voltage and low-resistance devices, with a 1200 V SiC MOSFET providing 36 A at 80 mΩ of on-state resistance [13]. This comparison can be seen in Figure 56, which shows specific on-resistance versus breakdown voltage for SiC and silicon [16].

These data are theoretical curves assuming that the only source of on-resistance is due to the lightly-doped epitaxial region. In practice, the measured on-resistance is a function of the channel, the substrate, metallization, and die area as discussed previously. However, the theoretical curves succinctly show the differences between the lightly-doped epitaxial regions SiC and silicon for a 1-D analysis. Using the above two devices as examples, a 1000 V silicon epitaxial region will have 100 mΩs-cm^2 of on-resistance, while a 1200 V SiC has 2-3 mΩs-cm^2 of on-resistance. Data-driven derating (70%) of the 1200 V SiC MOSFET suggests that operating at 400 V is sufficient for mitigating single-event burnout. Conventional derating (50%) for silicon MOSFETs suggest that 500 V operating voltage is sufficient for mitigating single-event burnout [67]. A simple 1-D solution of Ohm's law using the derating voltages results in the SiC supplying 160,000 A/cm^2 while the silicon can only supply 5000 A/cm^2. To achieve the same current supply as a SiC device, the silicon die area would need to be 30X the size of the SiC die area. The size and weight penalties for using silicon compared to SiC are too large to ignore for most applications.

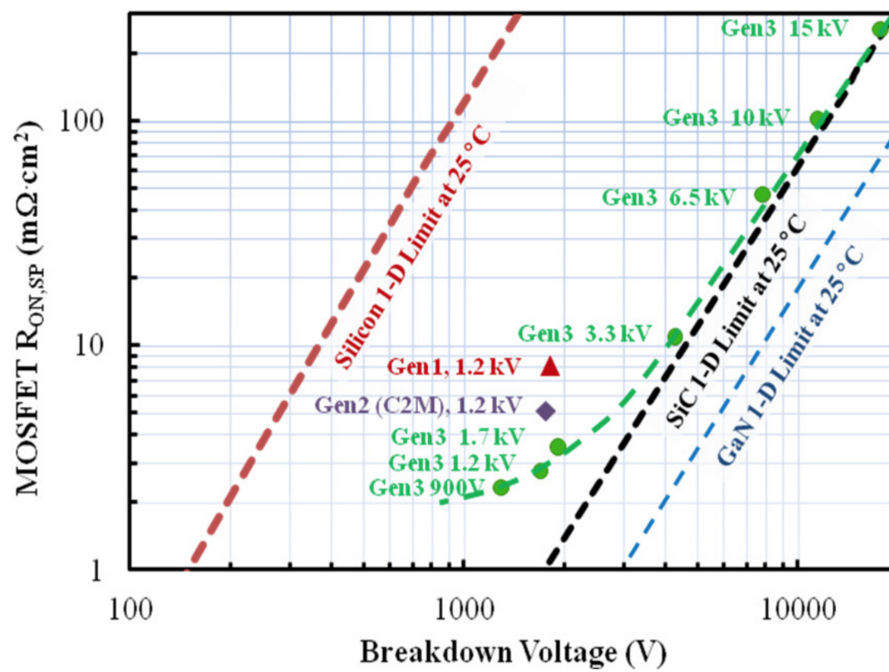


Figure 56: One-dimensional specific on-resistance versus breakdown voltage comparing silicon, silicon carbide, and gallium nitride after Gajewski *et al.* [16]

SiC: 1200 V vs. 3300 V

System Transmission Power Losses

A circuit design for an application that may be susceptible to single-event burnout typically has a 20-25% safety margin in supply voltage for survivability [68]. Single-event burnout data for the 1200 V SiC power MOSFET showed failures at 500 V, while the 3300 V SiC power MOSFET showed failures at 825 V [6]. This equates to 400 V and 650 V supply for a space-based application to accommodate a 20% safety margin for the 1200 V and 3300 V MOSFETs, respectively. For electric power transmission, increased operating voltages result in a reduction in energy lost in the system. For a given amount of power being transmitted, as voltage increases, current must decrease, shown by

$$P_{TRANS} = I_{TRANS} \cdot V_{TRANS} \tag{15}$$

where I_{TRANS} is the specified transmission current and V_{TRANS} is the transmission voltage of the system. Power loss is calculated by

$$P_{LOST} = I_{TRANS}^2 \cdot R_{TRANS} \tag{16}$$

where R_{TRANS} is the resistance of the system transmission lines. Assuming the transmitted power is the same in both cases, and using simple substitution with these two equations, comparing a 400 V bus and a 650 V bus gives

$$P_{LOST@650V} = 0.36 \cdot P_{LOST@400V} \tag{17}$$

indicating that increasing the supply voltage from 400 V to 650 V results in a significant savings of transmission losses in the system. In addition, smaller gauge

wire can be used for lower current levels, saving mass in the system. Although both the 1200 V and 3300 V devices can easily accommodate 650 V, ion data shows that the 1200 V device is susceptible to single-event burnout for LET > 5 MeV-cm^2/mg, while the 3300 V device does not show failure up to an LET = 60 MeV-cm^2/mg.

A similar comparison can be made for terrestrial applications where neutron-induced single-event burnout is a concern. The lowest voltage at which the 1200 V SiC power MOSFET shows single-event burnout due to cosmic ray neutrons is 700 V, compared to 2000 V for the 3300 V power MOSFET. Increasing the bus voltage from 700 V to 2000 V shows almost 90% savings in transmission losses, shown by

$$P_{LOST@2000V} = 0.12 \cdot P_{LOST@700V} \tag{18}$$

Using a higher rated breakdown voltage device is not a novel concept, and has been used historically for heavy ion environments. George *et al.* extensively covered statistical responses of power MOSFETs for single-event burnout, noting that in one specific example with a 24 V supply, selecting an 80 V power MOSFET would not be acceptable, while the 100 V device would satisfy the system requirements provided that the resulting power efficiency losses were tolerable [68]. In most engineering decisions, there are inherent trade-offs. In this work, examining trade-offs for using 1200 V versus 3300 V MOSFETs provides a starting point for a circuit/system design. The following analysis is not intended to be exhaustive, because there are so many designs and applications where these parts may be viable. Rather, this analysis will focus on a general concept of power losses in a switching SiC MOSFET comparing the 1200 V and 3300 V MOSFETs.

Switching MOSFET Power Losses

The total power loss in a MOSFET is a sum of the switching loss, the conduction loss, and the gate charge loss, and shown by [7]

$$P_{MOSFET} = P_{ON} + P_{SW} + P_G \tag{19}$$

where P_{ON} is the conduction loss, P_{SW} is the switching loss, and P_G is the gate charge loss. When a MOSFET is ON, or conducting, power is dissipated in the device as current flows through the resistive semiconductor and metallization, and is proportional to the on-state resistance, $R_{DS,ON}$. With increasing $R_{DS,ON}$, conduction losses increase and can be described by

$$P_{ON} = I_{ON}^2 \cdot R_{DS,ON} \tag{20}$$

and as shown, conduction losses are proportional to $R_{DS,ON}$. $R_{DS,ON}$ for the 1200 V SiC power MOSFET is 2-3 mΩs-cm^2 and for the 3300 V device is 10 mΩs-cm^2, suggesting that $P_{ON,3300V}$ is approximately 3X larger than $P_{ON,1200V}$.

As the MOSFET is turned ON and OFF, or switching, intrinsic parasitic capacitances store and dissipate energy during each transition and can be described by

$$P_{SW} = C_{MOSFET} \cdot V_{IN}^2 \cdot f_{SW} \tag{21}$$

where C_{MOSFET} is the combined capacitance of the gate capacitance and the drain-to-source capacitance, and f_{SW} is the switching frequency. Assuming die area and operating voltage are equal between the 1200 V and 3300 V devices, then $P_{SW,3300V}$ is approximately 3X larger than $P_{SW,1200V}$ because the drain-to-source capacitance in the 3300 V device is 3X the drain-to-source capacitance in the 1200 V device due to the 3X thicker epitaxial region.

Gate charge loss is described by

$$P_G = Q_G \cdot V_{GS} \cdot f_{SW} \tag{22}$$

where Q_G is the gate electric charge and V_{GS} is the gate drive voltage. Again, assuming the die area is equal between both devices, P_G is the same using either device. Additionally, P_G is typically 1-2 orders of magnitude lower than either conduction or switching loss, so even considering a larger die area, the impact of gate charge loss is negligible.

One goal of a designer is to balance conduction and switching losses [69]. For a circuit designed using a 1200 V MOSFET with balanced conduction and switching losses, swapping in a 3300 V device with the same die area results in a 2X increase in total power loss through the MOSFET, with negligible penalties in size/weight.

For applications where an increase in size/weight/cost do not significantly impact the application, increasing the die area by a factor of three will reduce $R_{DS,ON}$, and P_{ON} by a factor of three. SiC is also particularly well suited for operating multiple devices in parallel, which is an alternate option to reduce $R_{DS,ON}$. In either case, a 3X increase in the surface area will generally result in a 3X increase in device cross-section heavy ion interaction, although, to the point of this discussion, single-event burnout will not be a risk due to an appropriately selected bus voltage.

Implications for component selection and circuit design show that using a 3300 V power MOSFET provides ample single-event burnout threshold margin for space applications up to 650 V and up to an LET of 60 MeV-cm^2/mg, while the 1200 V device is susceptible to single-event burnout. In a terrestrial environment, the 3300 V device can safely operate up to 2000 V with little risk of cosmic ray neutron-induced

single-event burnout. An obvious design tradeoff is increased total power loss at the transistor level, which may be mitigated by fewer losses at the system level due to the increased bus voltage. Additionally, using a 3300 V device with a larger die area, or three devices in parallel, results in decreasing total power loss while potentially increasing cost, weight, area, and cross-section for an ion strike. For applications where single-event burnout cannot be tolerated, using higher rated devices should be considered.

CHAPTER IX

IMPACT AND CONCLUSIONS

Growth of the global power semiconductor industry hinges upon developing new technologies and products that can meet a wide range of voltage specifications, while providing higher power efficiency in a smaller package when compared to previous technologies. Silicon carbide is superior to silicon for power devices due to higher breakdown electric fields, increased thermal conductivity and significantly lower on-state resistance, all of which result in size, weight, power (SWaP), and overall cost savings. The SWaP benefits of SiC over silicon make these power devices desirable candidates for space-based applications. However, microelectronic devices and circuits used in space may be susceptible to naturally occurring space radiation, such as cosmic ray heavy ions.

Obtaining radiation test data for semiconductor devices is an expensive, time-consuming task with single-event burnout (SEB) testing particularly challenging because of the destructive nature of the test. The safe operating area (SOA) for 1200 V SiC power MOSFETs and diodes has been characterized to a limited extent through test campaigns, however, little insight has been gained into the physical mechanism(s) that may be responsible for ion-induced single-event burnout. Understanding these mechanisms is imperative for organizations for making space-flight hardware design decisions to mitigate risk of operational failure during a mission. Ion-induced radiation data for power devices reflects the response of a device from the perspective of an electrical terminal, or better defined as “on the outside looking in”. Modeling

and simulation tools, such as 3D Technology Aided Design (TCAD), provide the capability to gain insight into the physical response of a device to radiation, leveraging available data to validate modeling and simulation efforts.

This work has advanced the state-or-the-art in four key areas: identifying a trend for single-event burnout in SiC power MOSFETs and diodes, exploring physical failure mechanisms for that trend, evaluating device variants, and analyzing device voltage derating and selection for a circuit design.

Historically, it has been shown that there are separate mechanisms responsible for the catastrophic failures observed in silicon power diodes (localized avalanche breakdown due to ion-induced electric field spikes) and silicon power MOSFETs (parasitic bipolar junction transistor), resulting in differing single-event burnout responses between the two types of devices. A natural assumption is that there would be separate mechanisms responsible for single-event burnout in SiC power diodes and MOSFETs. However, this is not the case. In this work, heavy ion data has been compiled and combined with new data, identifying matching single-event burnout thresholds for the 1200 V power MOSFETs and diodes. Analysis of these heavy-ion data indicates that the devices have a common mechanism responsible for the catastrophic failures.

Insight into failure mechanisms is developed through the use of 3D TCAD simulations, which are used to identify similarities in both structures during an ion event. The simulation results show a resistive shunt effect capable of generating very high localized current transients during an ion strike, and consequently, significant energy dissipation. For LET and bias conditions matching the single-event burnout threshold data, a constant amount of energy dissipation is calculated through analysis

of TCAD simulation results. Ion-induced, highly-localized energy pulses are proposed as a common mechanism responsible for catastrophic single-event burnout in 1200 V SiC power MOSFETs and JBS diodes.

The 3D TCAD framework developed in this work provides an opportunity to efficiently evaluate the effects of an ion-strike on a variety of device variants (doping and dimension). Understanding how these variants perform following an incident heavy-ion strike will provide design teams an opportunity to consider alternate device designs that may meet the mission specification or otherwise mitigate the risk associated with single-event burnout during flight. This analysis may also prove to be useful for manufacturers that are interested in exploring radiation-hardened device development, further driving innovation for device reliability. 3D TCAD heavy ion simulation results have been analyzed for comparing commercial 1200 V and experimental 3300 V power MOSFETs. The results showed that the 3300 V MOSFET provides almost 50% reduction in total power dissipated along the ion track core compared to a 1200 V MOSFET, agreeing with the trends shown in the data.

Typically, using a commercial off-the-shelf part is less expensive than using a special radiation-hardened device. Successfully designing a power electronic circuit to operate while minimizing the risk of single-event burnout causing catastrophic failure of the circuit is important for both space and terrestrial applications. Circuit designers must understand the environment and the mechanisms contributing to single-event burnout in order to appropriately select parts. In this work, 1200 V commercially available and 3300 V experimental SiC power MOSFETs are compared for operation

in a circuit, with insight provided into the concept of voltage derating and a trade-off analysis focused primarily on power losses during operation. Implications for part selection and circuit design show that using a 3300 V power MOSFET provides ample single-event burnout threshold margin for space applications up to 650 V for most space environments, while the 1200 V device is susceptible to single-event burnout. In a terrestrial environment, the 3300 V device can safely operate up to 2000 V with little risk of neutron-induced single-event burnout. An obvious design trade-off is increased total power loss at the transistor level, which may be mitigated by fewer losses at the system level due to the increased bus voltage. Additionally, using a 3300 V device with a larger die area, or three devices in parallel, results in decreasing total power loss while potentially increasing cost, weight, area, and cross-section for an ion strike. For applications where single-event burnout cannot be tolerated, using higher rated devices should be considered.

REFERENCES

[1] "Wolfspeed," https://www.wolfspeed.com/why-wolfspeed.

[2] A. Elasser and T. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[3] "Automotive is Driving the SiC Power Market," https://www.electronicdesign.com/, Jul. 2018.

[4] "Silicon Carbide Power Semiconductors Market Size, Share and Growth," https://www.alliedmarketresearch.com/silicon-carbide-sic-power-semiconductors-market.

[5] "Power Electronics Market Size & Share — Industry Analysis Report, 2025," https://www.grandviewresearch.com/industry-analysis/power-electronics-market.

[6] J.-M. Lauenstein, M. C. Casey, K. A. LaBel, S. Ikpe, A. D. Topper, E. P. Wilcox, H. Kim, and A. M. Phan, "Single-Event Effects in Silicon Carbide Power Devices," *Proceedings NASA NEPP Electronics Technology Workshop*, pp. 1–15, Jun. 2015.

[7] B. J. Baliga, *Advanced Power Mosfet Concepts*, 2010.

[8] Alpha and Omega Semiconductor, "Power MOSFET Basics," pp. 1–10.

[9] "Power Diodes — Half wave and Full wave Bridge Rectifier," Jun. 2015.

[10] L. Harrison, "An introduction to Depletion-mode MOSFETs," p. 12.

[11] S. Havanur and P. Zuk, "Power MOSFET Basics Understanding Superjunction Technology," p. 5.

[12] "FQA8N100C: Power MOSFET, N-Channel, QFET®, 1000 V, 8.0 A, 1.45 Ω, TO-3P," https://www.onsemi.com/products/discretes-drivers/mosfets/fqa8n100c.

[13] "Worldwide Leader in SiC MOSFETs — Wolfspeed," https://www.wolfspeed.com/power/products/sic-mosfets.

[14] H. Choi, "Overview of Silicon Carbide Power Devices," p. 6.

[15] "ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: — JEDEC," https://www.jedec.org/standards-documents/docs/jesd-24-5.

[16] D. A. Gajewski, B. Hull, D. J. Lichtenwalner, S.-H. Ryu, E. Bonelli, H. Mustain, G. Wang, S. T. Allen, and J. W. Palmour, "SiC power device reliability," in *2016 IEEE International Integrated Reliability Workshop (IIRW)*, Oct. 2016, pp. 29–34.

[17] "Synopsys — EDA Tools, Semiconductor IP and Application Security Solutions," https://www.synopsys.com/.

[18] A. F. Witulski, R. Arslanbekov, A. Raman, R. D. Schrimpf, A. L. Sternberg, K. F. Galloway, A. Javanainen, D. Grider, D. J. Lichtenwalner, and B. Hull, "Single-Event Burnout of SiC Junction Barrier Schottky Diode High-Voltage Power Devices," *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 256–261, Jan. 2018.

[19] A. F. Witulski, D. R. Ball, K. F. Galloway, A. Javanainen, J.-M. Lauenstein, A. L. Sternberg, and R. D. Schrimpf, "Single-Event Burnout Mechanisms in SiC Power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 65, no. 8, pp. 1951–1955, Aug. 2018.

[20] D. T. Barbieri, "SiC Schottky Diode Device Design: Characterizing Performance & Reliability," https://www.wolfspeed.com/.

[21] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 1977.

[22] "Appendix C: Major Physical Properties of Common SiC Polytypes," in *Fundamentals of Silicon Carbide Technology.* John Wiley & Sons, Ltd, 2014, pp. 521–524.

[23] A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, "Ionization rates and critical fields in 4H silicon carbide," *Applied Physics Letters*, vol. 71, no. 1, pp. 90–92, Jul. 1997.

[24] A. E. Waskiewicz, J. W. Groninger, V. H. Strahan, and D. M. Long, "Burnout of Power MOS Transistors with Heavy Ions of Californium-252," *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1710–1713, Dec. 1986.

[25] W. Schimmerling, "The space radiation environment: An introduction." p. 6.

[26] J. L. Wirth and S. C. Rogers, "The Transient Response of Transistors and Diodes to Ionizing Radiation," *IEEE Transactions on Nuclear Science*, vol. 11, no. 5, pp. 24–38, Nov. 1964.

[27] L. W. Massengill, "SEU Modeling and Prediction Techniques," in *IEEE Nuclear and Space Radiation Effects Conference Short Course Text*, 1993.

[28] S. K. Chaudhuri, K. J. Zavalla, and K. C. Mandal, "Experimental determination of electron-hole pair creation energy in 4H-SiC epitaxial layer: An absolute calibration approach," *Applied Physics Letters*, vol. 102, no. 3, p. 031109, Jan. 2013.

[29] A. Lo Giudice, F. Fizzotti, C. Manfredotti, E. Vittone, and F. Nava, "Average energy dissipated by mega-electron-volt hydrogen and helium ions per electron-hole pair generation in 4H-SiC," *Applied Physics Letters*, vol. 87, no. 22, p. 222105, Nov. 2005.

[30] J. L. Titus, "An Updated Perspective of Single Event Gate Rupture and Single Event Burnout in Power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1912–1928, Jun. 2013.

[31] S. Liu, M. Boden, D. A. Girdhar, and J. L. Titus, "Single-Event Burnout and Avalanche Characteristics of Power DMOSFETs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3379–3385, Dec. 2006.

[32] G. H. Johnson, J. H. Hohl, R. D. Schrimpf, and K. F. Galloway, "Simulating single-event burnout of n-channel power MOSFET's," *IEEE Transactions on Electron Devices*, vol. 40, no. 5, pp. 1001–1008, 1993.

[33] H. Kabza, H.-J. Schulze, Y. Gerstenmaier, P. Voss, J. Schmid, F. Pfirsch, and K. Platzoder, "Cosmic radiation as a cause for power device failure and possible countermeasures," in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, May 1994, pp. 9–12.

[34] K. H. Maier, A. Denker, P. Voss, and H. W. Becker, "Single event burnout of high-power diodes," 1998.

[35] A. M. Albadri, R. D. Schrimpf, K. F. Galloway, and D. G. Walker, "Single event burnout in power diodes: Mechanisms and models," *Microelectronics Reliability*, vol. 46, no. 2, pp. 317–325, 2006.

[36] D. G. Walker, T. S. Fisher, A. M. Al-badri, and R. D. Schrimpf, "Simulation of Single-Event Failure in Power Diodes," in *ASME 2002 International Mechanical Engineering Congress and Exposition*. American Society of Mechanical Engineers Digital Collection, Jun. 2008, pp. 39–45.

[37] D. K. Sahu, "EEE-INST-002: Instructions for EEE Parts Selection, Screening, Qualification, and Derating," *NASA NEPP*, p. 338, Apr. 2008.

[38] L. Scheick, "Testing guideline for single event gate rupture (SEGR) of power MOSFETs," Pasadena, CA : Jet Propulsion Laboratory, National Aeronautics and Space Administration, 2008., Technical Report, Feb. 2008.

[39] J.-M. Lauenstein, M. C. Casey, E. P. Wilcox, A. M. Phan, H. S. Kim, A. D. Topper, R. L. Ladbury, and K. A. LaBel, "Recent Radiation Test Results for Trench Power MOSFETs," in *2017 IEEE Radiation Effects Data Workshop (REDW)*, Jul. 2017, pp. 1–8.

[40] J.-M. Lauenstein, R. L. Ladbury, N. Goldsman, H. S. Kim, D. A. Batchelor, and A. M. Phan, "Interpreting Space-Mission LET Requirements for SEGR in

Power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3443–3449, Dec. 2010.

[41] M. C. Casey, J.-M. Lauenstein, R. L. Ladbury, E. P. Wilcox, A. D. Topper, and K. A. LaBel, "Schottky Diode Derating for Survivability in a Heavy Ion Environment," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2482–2489, Dec. 2015.

[42] S. Kuboyama, C. Kamezawa, N. Ikeda, T. Hirao, and H. Ohyama, "Anomalous Charge Collection in Silicon Carbide Schottky Barrier Diodes and Resulting Permanent Damage and Single-Event Burnout," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3343–3348, Dec. 2006.

[43] A. Javanainen, K. F. Galloway, V. Ferlet-Cavrois, J.-M. Lauenstein, F. Pintacuda, R. D. Schrimpf, R. A. Reed, and A. Virtanen, "Charge Transport Mechanisms in Heavy-Ion Driven Leakage Current in Silicon Carbide Schottky Power Diodes," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 208–212, Jun. 2016.

[44] A. Javanainen, K. F. Galloway, C. Nicklaw, A. L. Bosser, V. Ferlet-Cavrois, J.-M. Lauenstein, F. Pintacuda, R. A. Reed, R. D. Schrimpf, R. A. Weller, and A. Virtanen, "Heavy Ion Induced Degradation in SiC Schottky Diodes: Bias and Energy Deposition Dependence," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 415–420, Jan. 2017.

[45] J.-M. Lauenstein, M. C. Casey, A. J. Topper, E. T. Wilcox, H. S. Kim, A. M. Phan, and K. A. LaBel, "Single-Event Effects in Silicon and Silicon Carbide Power Devices," *Proceedings NASA NEPP Electronics Technology Workshop*, pp. 1–18, Jun. 2014.

[46] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of Single-Event Damages on Silicon Carbide (SiC) Power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1924–1928, Aug. 2014.

[47] J. A. McPherson, P. J. Kowal, G. K. Pandey, T. P. Chow, W. Ji, and A. A. Woodworth, "Heavy Ion Transport Modeling for Single-Event Burnout in SiC-Based Power Devices," *IEEE Transactions on Nuclear Science*, vol. 66, no. 1, pp. 474–481, Jan. 2019.

[48] J. A. McPherson, C. Hitchcock, T. P. Chow, W. Ji, and A. A. Woodworth, "Mechanisms of Heavy Ion-Induced Single Event Burnout in 4H-SiC Power MOSFETs," *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, p. 1, Sep. 2019.

[49] J.-M. Lauenstein and M. Casey, "Taking SiC Power Devices to the Final Frontier: Addressing Challenges of the Space Radiation Environment," *Proceedings NASA NEPP Electronics Technology Workshop*, pp. 1–36, Jun. 2017.

[50] D. R. Ball, K. F. Galloway, R. A. Johnson, M. L. Alles, A. L. Sternberg, B. D. Sierawski, A. F. Witulski, R. A. Reed, R. D. Schrimpf, J. M. Hutson, A. Javanainen, and J.-M. Lauenstein, "Ion-Induced Energy Pulse Mechanism for Single-Event Burnout in High-Voltage SiC Power MOSFETs and Junction Barrier Schottky Diodes," *IEEE Transactions on Nuclear Science*, vol. 67, no. 1, pp. 22–28, Jan. 2020.

[51] "88-Inch Cyclotron," http://cyclotron.lbl.gov/.

[52] "RADiation Effects Facility," https://www.jyu.fi/.

[53] A. Javanainen, M. Turowski, K. F. Galloway, C. Nicklaw, V. Ferlet-Cavrois, A. Bosser, J.-M. Lauenstein, M. Muschitiello, F. Pintacuda, R. A. Reed, R. D. Schrimpf, R. A. Weller, and A. Virtanen, "Heavy-Ion-Induced Degradation in SiC Schottky Diodes: Incident Angle and Energy Deposition Dependence," *IEEE Transactions on Nuclear Science*, vol. 64, no. 8, pp. 2031–2037, Aug. 2017.

[54] "Cyclotron Institute - Nuclear Science at Texas A&M University," https://cyclotron.tamu.edu/.

[55] X. Zhu, J.-M. Lauenstein, A. Bolonikov, B. Jacob, A. Kashyap, K. Sariri, and Y. Chen, "Radiation Hardness Study on SiC Power MOSFETs," *International Conference on Silicon Carbide and Related Materials (ICSCRM)*, p. 1, Sep. 2017.

[56] A. Akturk, R. Wilkins, J. McGarrity, and B. Gersey, "Single Event Effects in Si and SiC Power MOSFETs Due to Terrestrial Neutrons," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 529–535, Jan. 2017.

[57] D. J. Lichtenwalner, B. Hull, E. Van Brunt, S. Sabri, D. A. Gajewski, D. Grider, S. Allen, J. W. Palmour, A. Akturk, and J. McGarrity, "Reliability studies of SiC vertical power MOSFETs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, pp. 2B.2–1–2B.2–6.

[58] S. Liu, M. Boden, D. A. Girdhar, and J. L. Titus, "Single-Event Burnout and Avalanche Characteristics of Power DMOSFETs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3379–3385, Dec. 2006.

[59] C. Abbate, G. Busatto, P. Cova, N. Delmonte, F. Giuliani, F. Iannuzzo, A. Sanseverino, and F. Velardi, "Analysis of Heavy Ion Irradiation Induced Thermal Damage in SiC Schottky Diodes," *IEEE Transactions on Nuclear Science*, vol. 62, no. 1, pp. 202–209, Feb. 2015.

[60] S. Kuboyama, E. Mizuta, Y. Nakada, H. Shindou, A. Michez, J. Boch, F. Saigné, and A. Touboul, "Thermal Runaway in SiC Schottky Barrier Diodes Caused by Heavy Ions," *IEEE Transactions on Nuclear Science*, vol. 66, no. 7, pp. 1688–1693, Jul. 2019.

[61] B. Pushpakaran and S. Bayne, *Modeling And Electrothermal Simulation Of Sic Power Devices: Using Silvaco© Atlas*. World Scientific, Mar. 2019.

[62] A. Mihaila, F. Udrea, G. Amaratunga, and G. Brezeanu, "A comprehensive analysis of breakdown mechanisms in 4H-SiC MOSFET and JFET," in *2000 International Semiconductor Conference. 23rd Edition. CAS 2000 Proceedings (Cat. No.00TH8486)*, vol. 1, Oct. 2000, pp. 185–188 vol.1.

[63] Y. Wang, M. Lin, X.-J. Li, X. Wu, J.-Q. Yang, M.-T. Bao, C.-H. Yu, and F. Cao, "Single-Event Burnout Hardness for the 4H-SiC Trench-Gate MOSFETs Based on the Multi-Island Buffer Layer," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4264–4272, Oct. 2019.

[64] X. Zhou, Y. Jia, D. Hu, and Y. Wu, "A Simulation-Based Comparison Between Si and SiC MOSFETs on Single-Event Burnout Susceptibility," *IEEE Transactions on Electron Devices*, vol. 66, no. 6, pp. 2551–2556, Jun. 2019.

[65] X. Zhou, Y. Tang, Y. Jia, D. Hu, Y. Wu, T. Xia, H. Gong, and H. Pang, "Single-Event Effects in SiC Double-Trench MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 66, no. 11, pp. 2312–2318, Nov. 2019.

[66] X. Zhang and M. Wang, "Simulation of high power step-buffer 4H silicon carbide metal semiconductor field effect transistor," in *2018 International Conference on Electronics Technology (ICET)*, May 2018, pp. 1–5.

[67] "MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES — JEDEC," https://www.jedec.org/standards-documents/docs/jesd-89a.

[68] J. S. George, D. A. Clymer, T. L. Turflinger, L. W. Mason, S. Stone, R. Koga, E. Beach, K. Huntington, J.-M. Lauenstein, J. Titus, and M. Sivertz, "Response Variability in Commercial MOSFET SEE Qualification," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 317–324, Jan. 2017.

[69] EETimes, "EETimes - Calculating power loss in switching MOSFETs -," Aug. 2011.

[70] G. Johnson, J. Palau, C. Dachs, K. Galloway, and R. Schrimpf, "A review of the techniques used for modeling single-event effects in power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 546–560, Apr. 1996.

[71] G. Soelkner, W. Kaindl, M. Treu, and D. Peters, "Reliability of SiC Power Devices Against Cosmic Radiation-Induced Failure," *Materials Science Forum*, vol. 556-557, pp. 851–856, Sep. 2007.

[72] M. C. Casey, J.-M. Lauenstein, A. D. Topper, E. P. Wilcox, H. Kim, A. M. Phan, and K. A. LaBel, "Single-Event Effects in Silicon Carbide Power Devices," *Proceedings NASA NEPP Electronics Technology Workshop*, p. 15, Jun. 2013.

[73] A. Bolotnikov, P. Losee, A. Permuy, G. Dunne, S. Kennerly, B. Rowden, J. Nasadoski, M. Harfman-Todorovic, R. Raju, F. Tao, P. Cioffi, F. J. Mueller, and L. Stevanovic, "Overview of 1.2kV – 2.2kV SiC MOSFETs targeted for industrial power conversion applications," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2015, pp. 2445–2452.

[74] X. Zhang, "FAILURE MECHANISM INVESTIGATION FOR SILICON CARBIDE POWER DEVICES," Ph.D. dissertation.

[75] R. A. Johnson, A. F. Witulski, D. R. Ball, K. F. Galloway, A. L. Sternberg, E. Zhang, L. D. Ryder, R. A. Reed, R. D. Schrimpf, J. A. Kozub, J.-M. Lauenstein, and A. Javanainen, "Enhanced Charge Collection in SiC Power MOSFETs Demonstrated by Pulse-Laser Two-Photon Absorption SEE Experiments," *IEEE Transactions on Nuclear Science*, vol. 66, no. 7, pp. 1694–1701, Jul. 2019.

[76] T. Shoji, S. Nishida, K. Hamada, and H. Tadano, "Analysis of neutron-induced single-event burnout in SiC power MOSFETs," *Microelectronics Reliability*, vol. 55, no. 9, pp. 1517–1521, Aug. 2015.

[77] M. Allenspach, C. Dachs, G. Johnson, R. Schrimpf, E. Lorfevre, J. Palau, J. Brews, K. Galloway, J. Titus, and C. Wheatley, "SEGR and SEB in n-channel power MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2927–2931, Dec. 1996.

[78] R. Baumann, "Soft errors in advanced computer systems," *IEEE Design Test of Computers*, vol. 22, no. 3, pp. 258–266, May 2005.

[79] R. A. Weller, M. H. Mendenhall, R. A. Reed, R. D. Schrimpf, K. M. Warren, B. D. Sierawski, and L. W. Massengill, "Monte Carlo Simulation of Single Event Effects," *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 1726–1746, Aug. 2010.

[80] R. A. Reed, R. A. Weller, M. H. Mendenhall, D. M. Fleetwood, K. M. Warren, B. D. Sierawski, M. P. King, R. D. Schrimpf, and E. C. Auden, "Physical Processes and Applications of the Monte Carlo Radiative Energy Deposition (MRED) Code," *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1441–1461, Aug. 2015.

[81] A. D. Tipton, X. Zhu, H. Weng, J. A. Pellish, P. R. Fleming, R. D. Schrimpf, R. A. Reed, R. A. Weller, and M. Mendenhall, "Increased Rate of Multiple-Bit Upset From Neutrons at Large Angles of Incidence," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 3, pp. 565–570, Sep. 2008.

[82] J. F. Ziegler, "Terrestrial cosmic rays," *IBM J. Res. Dev.*, 1996.

Appendix A

POSITIVE FEEDBACK LOOP: PARASITIC BJT AND IMPACT IONIZATION

Silicon-based power MOSFETs, on exposure to heavy-ion irradiation, may experience catastrophic failure, either single-event gate rupture (SEGR) or single-event burnout (SEB), above a certain gate and/or drain bias. These failures are well understood with the latter linked to the parasitic bipolar junction transistor, which is an integral part of the device structure [32], [70], [31], [30].

SiC power MOSFETs may also undergo catastrophic single-event burnout when exposed to energetic heavy ions or protons [71], [72], [46], [6], [73], [56]. Lauenstein et al. [6] points out that two types of ion-induced single-event effects are observed in SiC power MOSFETs: degradation and catastrophic failure. They also say that "at this time the primary failure mode is unclear and that "Signatures are similar across manufacturers and part types: [the] mechanism is more fundamental than geometry or process quality." There have also been some previous efforts at modeling single-event burnout and SEGR effects in SiC power MOSFETs [74].

In this Appendix, the role of the parasitic bipolar turn-on in a 1200 V SiC power MOSFET during an ion strike is discussed. As previously discussed in Chapter IV single-event burnout in silicon power MOSFETs has historically been attributed to a positive feedback loop with avalanche carrier generation and the turn-on of a parasitic NPN bipolar transistor. In a typical operating mode, the body and source of the MOSFET are shorted together by the common metallization, so the body voltage has no ability to rise and forward-bias the body-source P-N junction. However, when the

passage of a heavy-ion deposits charge in the device, lateral current flow along the P-type body region allows the body voltage to rise, forward-biasing the body-source P-N junction, turning on the parasitic BJT. This occurs simultaneously with the avalanche carrier generation due to the high electric fields present in the device. The positive feedback loop between the parasitic BJT and the avalanching carriers, each with a positive gain, results in a condition where high current and high voltage are sustained sufficiently to physically damage the device through metal/semiconductor separation at the contact, burnout of metal lines, or thermal meltdown of the silicon. Although the parasitic BJT does not appear to be the dominant mechanism contributing to single-event burnout in SiC power devices, it is still an integral part of the device. 3D TCAD simulations are used to understand the dependence of the parasitic BJT turn-on and the avalanche generation from impact ionization as a function of ion linear energy transfer (LET) and reverse bias voltage.

Parasitic BJT

The details of the 3D TCAD SiC power MOSFET and diode devices were discussed in Chapter III. TCAD simulations were used to investigate the activation of the parasitic BJT in the MOSFET, and comparing results to the diode which has no parasitic BJT [75]. In these simulations, the ion strike location was varied across the surface of the devices in 250 nm steps, with an LET = 20 MeV-cm^2/mg) and varying the bias from 10 V up to 250 V. The ion did not fully penetrate the epitaxial region, rather it was truncated at 2 μm into the device, sufficient to deposit charge entirely through the P-type body region and activating the parasitic BJT, without shorting the source to the drain. In addition, bias conditions were sufficiently low that with

impact ionization models turned ON, there was not sufficient avalanching of carriers due to low electric fields. Charge collected on the drain node as a function of bias and strike position is shown in Figure 57, with MOSFET collected charge on the drain in (A), diode collected charge on the drain in (B). These results clearly show that collected charge in the diode is constant, and independent of both hit location and bias. In the MOSFET, the parasitic BJT is activated, resulting in an amplification of charge that is dependent on both hit location and bias. The most sensitive location is the the corner of the P-type body region, discussed in earlier chapters. This location is the farthest from the source contact, resulting in the maximum series resistance between the deposited charge and the contact and allowing the P-type body region potential to rise during the ion strike. For the worst case strike location, collected charge is compared for the MOSFET and diode as a function of bias in Figure 58. For a drain voltage less than 20 V, both the MOSFET and diode collect approximately the same amount of charge because the parasitic BJT has not been activated. As the bias increases, the P-type body potential rises, increasing the base-emitter voltage, and driving the amplification of charge in the MOSFET.

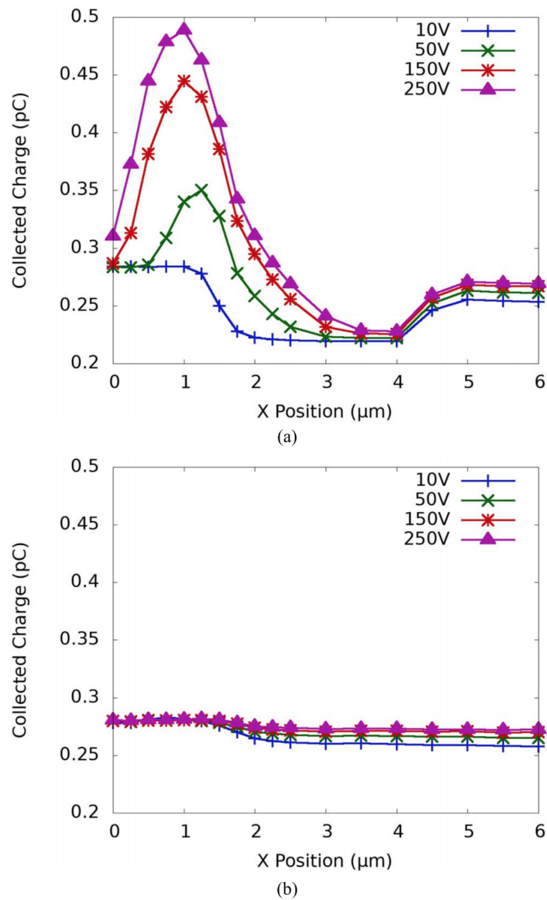


Figure 57: TCAD simulations of collected charge in a MOSFET for a constant amount of deposited charge but varying location and bias are shown in (a). TCAD simulations of collected charge in a diode for a constant amount of deposited charge but varying location and bias (b). For (a) and (b), a strike location of 0 is at the center of the epitaxial region near the surface between two p-doped regions. after Johnson *et al.* [75]

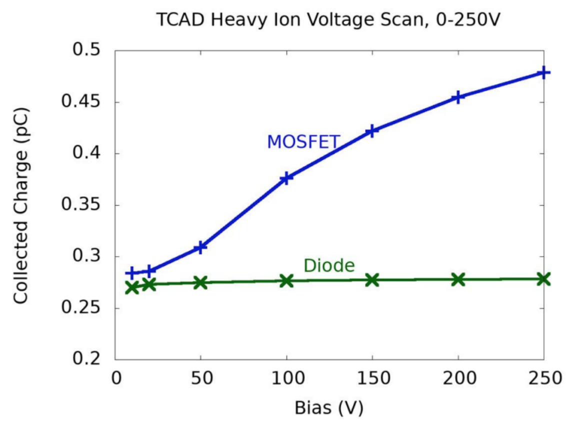


Figure 58: TCAD simulations of collected charge in a MOSFET and diode for a constant amount of deposited charge in the most sensitive location but varying bias after Johnson *et al.* [75]

Impact Ionization

The details of the 3D TCAD SiC power MOSFET device were discussed in Chapter III. The single-event simulation matrix varied the heavy ion charge deposition from 0.007 pC/μm to 0.042 pC/μm (which can be converted to LET = 1 MeV-cm^2/mg to 60 MeV-cm^2/mg), and drain bias from 400 V to 1600 V, in 100 V increments. The heavy ion strike occurs 100 ps after the simulation begins, giving the device simulation ample time to achieve steady state, and the Gaussian track radius is 50 nm spatially with a 2 ps Gaussian rise/fall time parameter. Impact ionization models developed specifically for 4H-SiC [17], which are critical for simulating breakdown, were employed. Thermal equations (lattice heating) were not considered for this study.

Figure 59 shows the simulated heavy-ion induced drain current as a function of time for LET = 5 MeV-cm^2/mg at 700 V and 800 V drain bias, with and without impact ionization turned on. When the device is biased at 800 V and impact ionization is turned OFF, the ion-induced drain current transient shows a sharp peak, followed by a characteristic recovery as mobile carriers recombine. In this case, the parasitic BJT has turned ON, but with no impact ionization to generate holes to supply the base current, there is no positive feedback path. With impact ionization turned ON, the drain current shows a slight recovery as the device moves from drift collection into a state where impact ionization can begin to supply holes to the base of the BJT, driving the gain higher, and the drain current increases indefinitely due to the positive gain in the system. With the impact ionization model turned ON, but at a lower bias of 700 V, the drain current transient does not show a runaway event, however, it is significantly more pronounced than the case with impact ionization turned OFF. In

this condition, there is still an activated parasitic BJT and generation of carriers from impact ionization, but the gain of the system is too low to show a runaway current event.

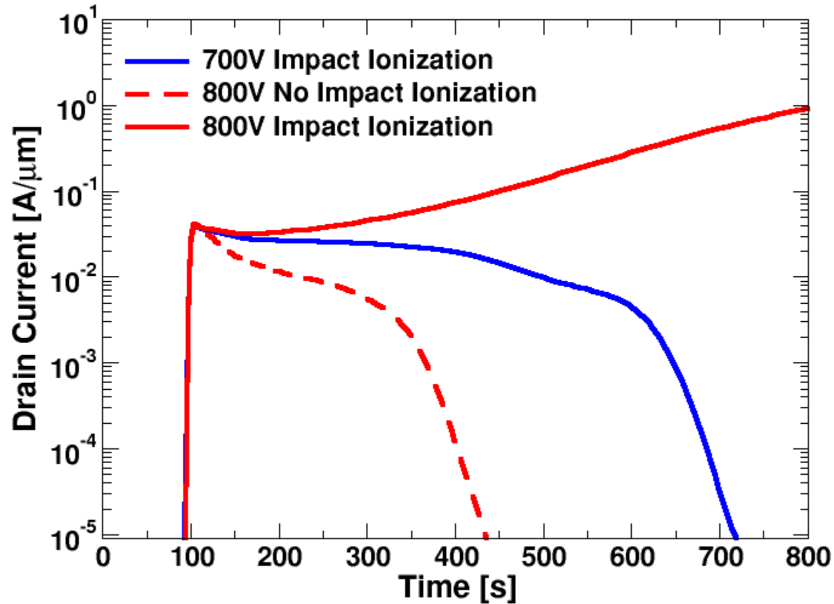


Figure 59: TCAD heavy ion simulations of SiC power MOSFET, showing single-event burnout at 800 V at LET=5 MeV-cm^2/mg with impact ionization turned on, and device recovery at other conditions.

The importance of the parasitic bipolar transistor to the positive feedback loop is apparent in Figure 60 and Figure 61 which show 2D cross-section TCAD time slices 250 ps after the strike occurs, or 350 ps of simulation time to correspond to the curves in Figure 59. This time was chosen to highlight the differences between the two cases. Much earlier, and the two cases look very similar and hard to distinguish any significant differences. Much later and the impact ionization simulation has advanced so far that the device has started to become flooded with carriers and is difficult to use as a comparison against the no impact ionization case. Figure 60 shows hole

current density (A/cm^2) (top) and electron current density (bottom) without impact ionization turned on, for LET = 5 MeV-cm^2/mg at VD = 800 V. Figure 61 illustrates a 2D cross-section TCAD time slice after the strike occurs, with hole current density (A/cm^2) (top) and electron current density (A/cm^2) (bottom) with impact ionization turned on, again for LET = 5 MeV-cm^2/mg at VD = 800 V. Both electrons and holes exhibit significantly higher current densities with the impact ionization model active, revealing the presence of a cylinder of current from the ion strike on the source down to the highly-doped drain region. Without impact ionization turned on in the simulation, there is no sustainable source of carriers for positive gain in the system. With the impact ionization model turned ON, the significant increase in current density compared to the simulation without impact ionization is a result of avalanche multiplication at the epi/substrate junction, as shown in Figure 62. The condition for impact ionization is created by charge carrier transport following the strike, and is initiated by localized high electric fields arising from the drain bias. The charge carriers flooding the epi region cause the maximum electric field to relocate from the p-body/epi junction (pre-strike) to the epi/substrate junction as shown by the current generation profile in Figure 59, with impact ionization rate shown in Figure 62. In this simulation, the parasitic BJT turns on and the electric field is high enough that impact ionization can begin, such that carrier multiplication occurs quickly. In other device structures, it may be possible to initiate this process without the effective gain of the parasitic bipolar [76]. In Figure 59, the current from the generated carriers shorts the source to the drain. The electron and hole current flow is a direct path from source to drain, and the avalanching effects cause the currents to continue increasing, leading to a runaway current event. In a TCAD simulation,

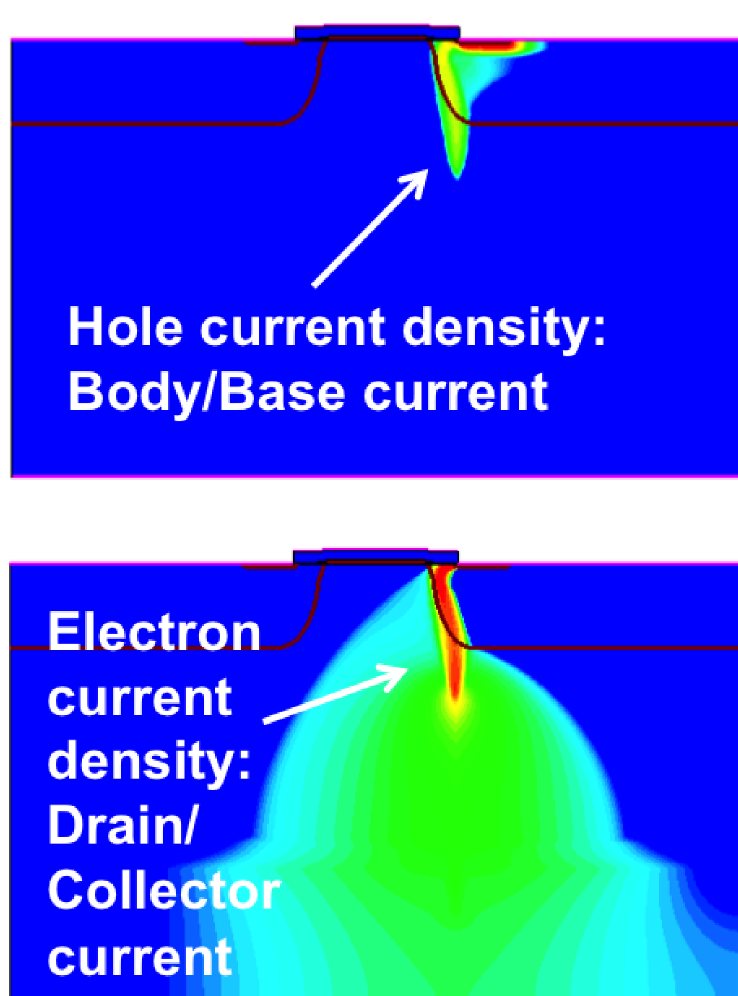
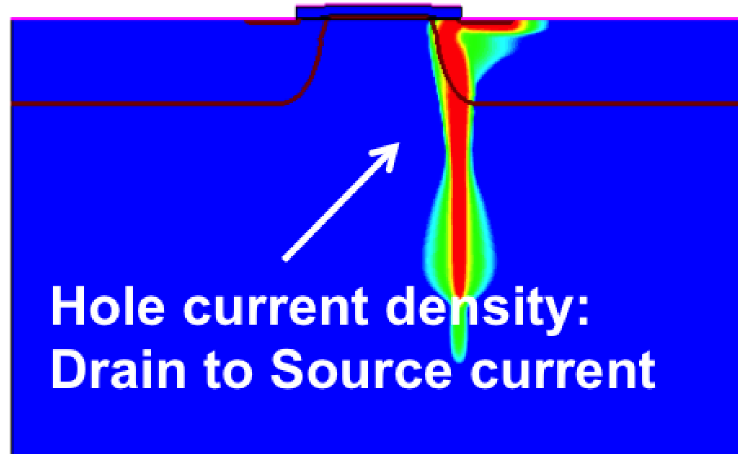


Figure 60: 2D cross-section TCAD time slice 250ps after the strike occurs, showing hole current density (A/cm^2) (top), electron current density (bottom) with impact ionization turned off, for LET=5 MeV-cm^2/mg at VD=800 V. Blue indicates a current density of 1 A/cm^2 while red indicates a current density of 106 A/cm^2.



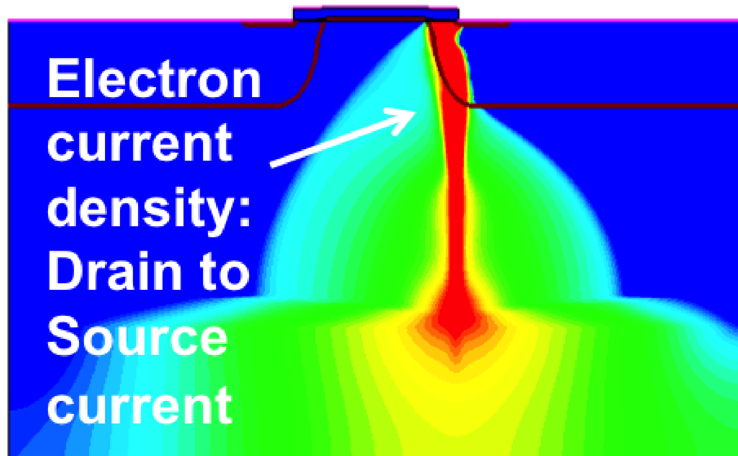


Figure 61: 2D cross-section TCAD time slice 250ps after the strike occurs, showing hole current density (A/cm^2) (top), electron current density (bottom) with impact ionization turned on, for LET=5 MeV-cm^2/mg at VD=800 V. Blue indicates a current density of 1 A/cm^2 while red indicates a current density of 106 A/cm^2.

there is no way to differentiate between parasitic BJT current and current generated from avalanching carriers. Thus, it is important to simulate both cases, with and without impact ionization, to understand the mechanisms causing failure. TCAD

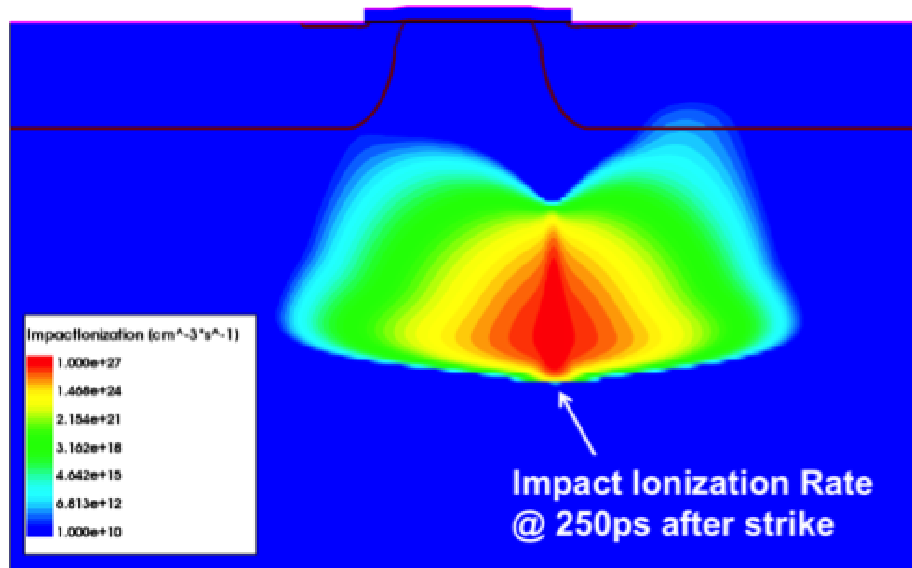


Figure 62: Impact ionization (per cm^2-s) at the epi/drain junction at 250 ps after the strike occurs for LET=10 MeV-cm^2/mg at VD=800 V. Impact ionization rate ranges from 1e10 cm-3•s-1 (blue color) to 1e27 cm-3•s-1 (red color)

simulation results shown in Figure 63 further illustrate that the positive feedback loop is a function of device reverse bias and ion LET. The ion is assumed to pass through the source, body and drain. The bias is fixed at 500 V and the LET is varied from 1 to 60 MeV-cm^2/mg. These simulation results show drain current transients as a function of time. At 500 V, positive feedback does not occur at an LET of 10 MeV-cm^2/mg or below, but does occur at LETs of 20 MeV-cm^2/mg and above.

In addition to bias and LET dependence, runaway drain current events in SiC power MOSFETs also depend on strike location, similar to silicon power MOSFETs [77]. Figure 64 shows representative strike locations, with all strikes at normal incidence. The simulated effects of ion strike location are shown in Table 8 for

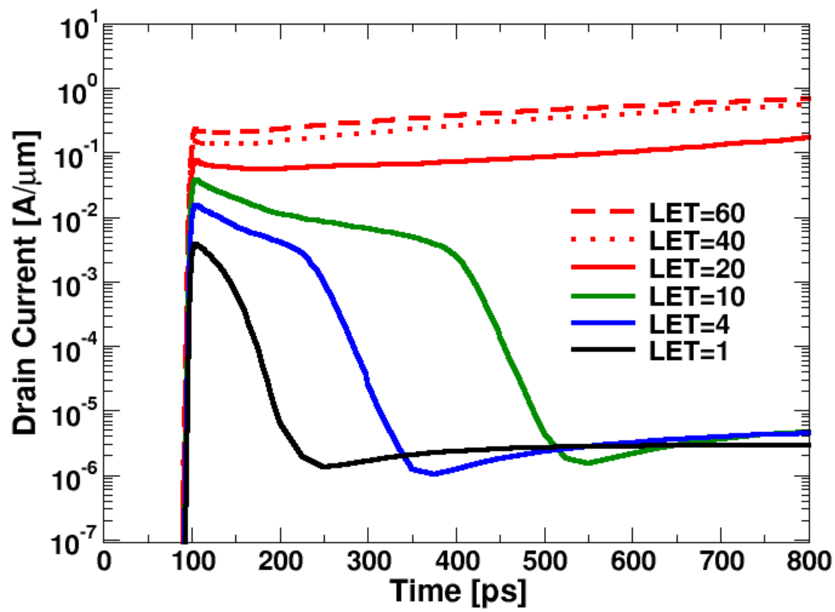


Figure 63: TCAD heavy ion simulations of a SiC power MOSFET, showing drain current transient as a function of LET with the drain biased at 500 V. At LETs of 20 MeV-cm^2/mg and greater, the drain current runs away, indicating a positive feedback loop between a parasitic BJT and impact ionization.

a variety of LET and bias conditions. For a given bias, increasing LET over the threshold value leads to an increasing area of sensitivity. This occurs because the charge generated by the ion strike must be sufficient to turn on the parasitic bipolar transistor locally. As the strike location moves farther from the sensitive area, the particle LET must increase so that the deposited charge that diffuses to the sensitive region is sufficient to trigger both the parasitic BJT and impact ionization. Combined with a suitable electric field, the parasitic BJT can turn on and carrier avalanching can drive a runaway current event.

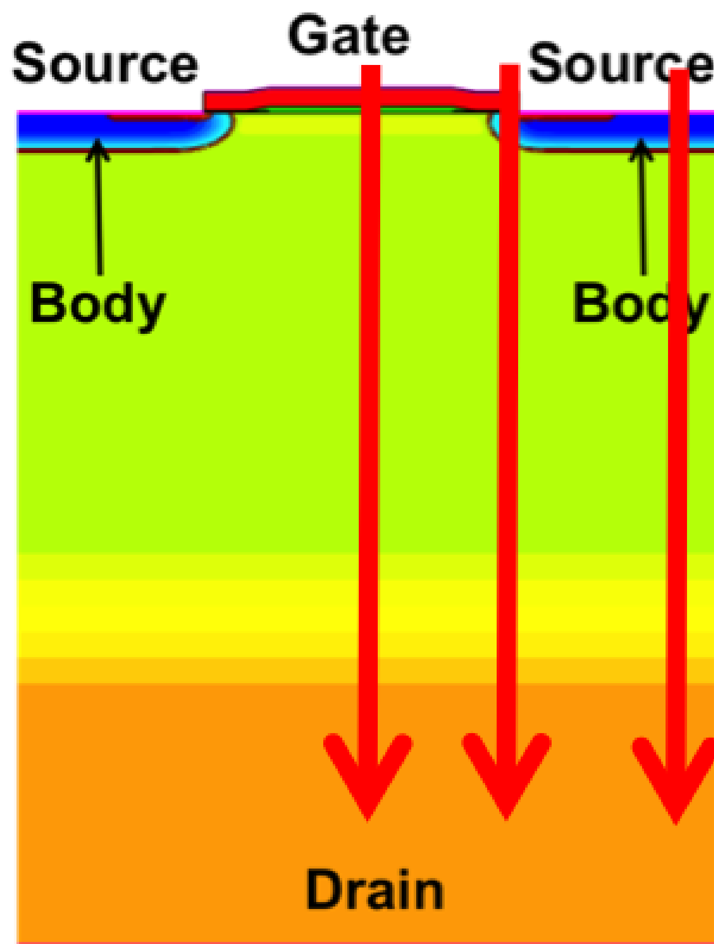


Figure 64: 2D cross-section of TCAD model, with arrows indicating varied ion strike locations. In all cases, ion is at normal incidence.

Table 8: 3D TCAD Simulation Results Indicating Positive Feedback as a function of Ion Strike Location, LET, and Bias

Location	Center Gate	Source/Body	Body/Drain
LET=4 @ 1400 V	No	Yes	No
LET=10 @ 800 V	No	Yes	No
LET=20 @ 500 V	No	Yes	No
LET=60 @ 500 V	Yes	Yes	Yes

Single-event burnout in silicon power MOSFETs occurs as a result of impact ionization driving rapidly escalating current flow in a device, ultimately leading to the device failing catastrophically. For vertical power devices, there is an inherent parasitic bipolar junction transistor (BJT) that can turn on during a single-event strike, amplifying the current that is flowing, initiating impact ionization, and ultimately leading to device breakdown. Although the effects of impact ionization are well understood in silicon devices, SiC devices exhibit different characteristics due to the wider bandgap. It is important to use impact ionization models in TCAD. With impact ionization models turned OFF, considerable ion-generated current flows in the device, but mobile carriers recombine and the device recovers. With impact ionization models turned ON and coupled with the activiation of the parasitic BJT (seen by examining the hole and electron current densities in Figure 61), the heavy-ion generated carriers are sufficient to raise the potential in the body, forward biasing the body/source junction, and providing a path for holes to flow into the source in the form of base current. As the simulation progresses, the carriers recombine, and the parasitic BJT turns off because there is no sustainable injection of charge and the device will recover.

Appendix B

NEUTRON-INDUCED SECONDARY PARTICLE GENERATION

As a neutron passes through a semiconductor material, a collision with the nucleus of an atom can result secondary reaction product (alpha, proton, or ion) that is ionizing and capable of creating electron-hole pairs in the semiconductor. For terrestrial microelectronics, neutrons can greatly impact the reliability of a circuit or device [78] when a collision occurs and charge is deposited. An estimated 50% of the electricity used in the world is controlled by power devices [7], with applications ranging from consumer, industrial, medical, and transportation. Thus, for terrestrial applications for SiC power devices, neutron-induced single-event burnout is a reliability concern [57].

This dissertation is focused on ion-induced single-event burnout for SiC power devices, with analysis showing that 3300 V power devices are less susceptible to catastrophic failure than a 1200 V device. Terrestrial neutron-induced single-event burnout data (shown in Figure 35) also supports this analysis. It is interesting to consider neutron-induced charge deposited in the SiC devices as it relates to the devices discussed in previous chapters. The impact of the terrestrial neutron environment bombarding a semiconductor material can be investigated through simulations using a radiation transport tool called Monte Carlo Radiative Energy Deposition (MRED) [79], [80]. Tipton *et al.* used MRED to generate neutron-induced secondary products in a 90 nm bulk silicon SRAM, with an example of a secondary product reaction shown in Figure 65. Neutron-induced secondary particles

are isotropic and largely independent of the direction of the neutron, wich is seen in Figure 65 where the incident neutron results in a shower of alphas, protons, and a carbon ion.

In this dissertation, MRED is used to identify secondary particles from terrestrial neutron-induced nuclear reactions in a SiC target. In order to understand the distribution of recoil products from nuclear reactions produced when SiC is exposed to neutrons, a target with a cross-sectional area of 2 mm x 3 mm (the size of the die) with a depth of 30 μm was used for initial MRED radiation-transport simulations. The structure also has a 1 μm tungsten overlayer to provide a reasonable representation of back end of line materials (the actual BEOL is not known). The neutron environment used for the MRED simulations matches that of the Los Alamos National Laboratory (LANL) spallation neutron source, whose energy distribution closely matches that of terrestrial neutrons [67], [82]. The distribution of the terrestrial neutron spectrum as a function of energy is shown in Figure 66. An event-weighting technique defined in [79] allowed the high energy, low flux portion of the spectrum to be analyzed accurately. MRED simulations were run for the entire 2 mm x 3 mm x 30 μmm block of SiC to establish the likelihood of secondary particles depositing energy in the epitaxial region. In Figure 67, the range and LET of secondary particles generated in the SiC by incoming neutrons are shown. For this illustration, only secondary particles with an LET greater than 1 MeV-cm^2/mg are recorded. This limit was defined based on the lowest recorded heavy ion LET that caused single-event burnout, see Figure 32. The range of LET values that are presented from MRED simulations extends from an LET of 1 MeV-cm^2/mg up to an LET of almost 15 MeV-cm^2/mg. Based on heavy ion data, this range of LET values (and deposited energy) is well within the range

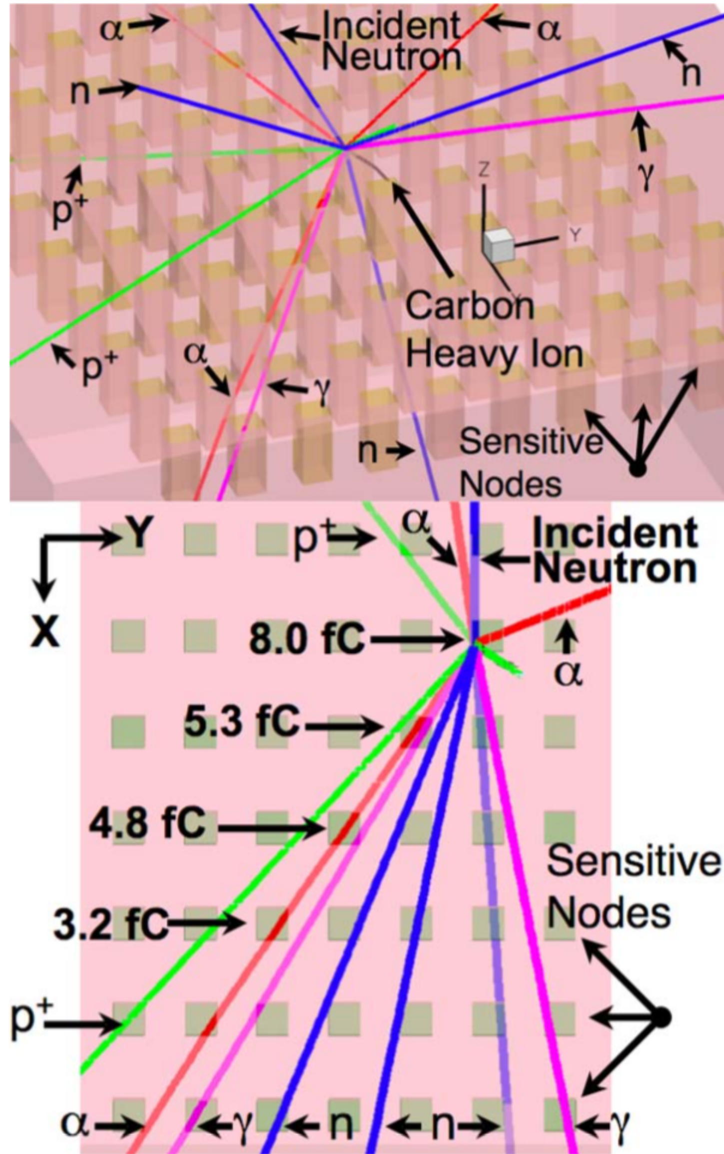


Figure 65: TCAD representation of an MRED-generated nuclear event. The shaded volumes represent the sensitive nodes of the memory device. The incident neutron enters and induces a nuclear event. The shower of secondary products includes alpha particles, protons, neutrons, gamma rays, and a carbon heavy ion after Tipton *et al.* [81]

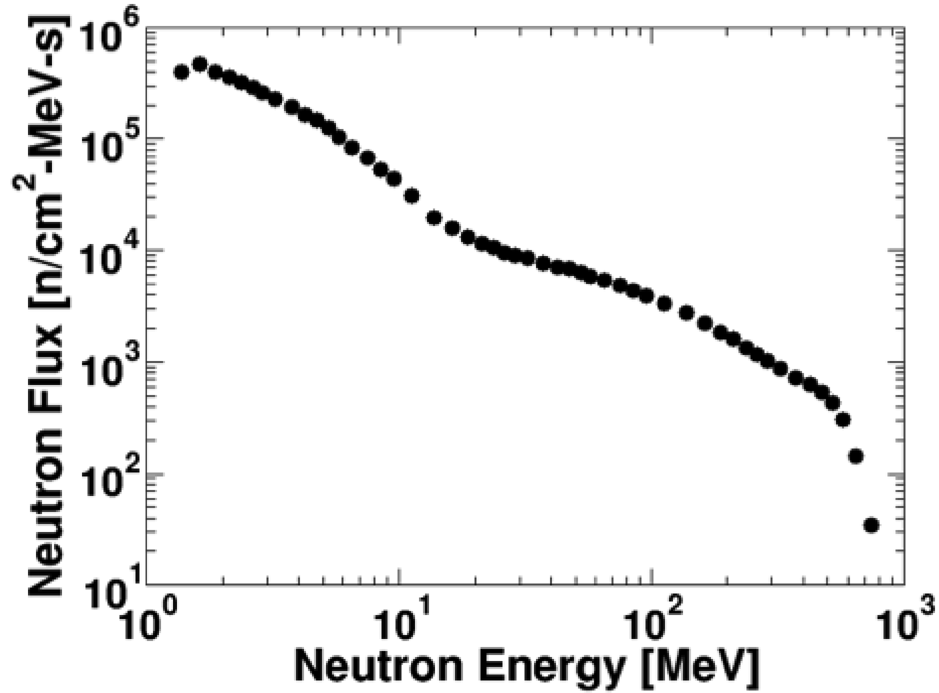


Figure 66: Neutron spectrum from LANL [67] that closely matches the terrestrial neutron spectrum, and is used for MRED simulations.

required for single-event burnout. Further analysis of the simulation results shown in Figure 67 indicates that many of these secondary particles have a much shorter range than the heavy ions from LBNL and RADEF. Out of 55,000 simulated secondary reaction events, 80% of them had a range of 5 μm or less, and 65% have a range of 2 μm or less. As noted previously, the thickness of the epitaxial region in the 1200 V device is 10 μm, and the thickness in the 3300 V device is 30 μm. These results indicate that a significant majority of the charge deposited after a nuclear reaction occurs in a volume that is significantly smaller than the epitaxial region. This is consistent with the neutron-induced single-event burnout data that shows the 3300 V device requires significantly higher applied bias (2000 V) than the 1200 V device (800 V) before catastrophic failure. At 800 V, the depletion region in the 1200 V device penetrates the entire thickness of the epitaxial region. For the 3300 V device,

when biased at 2000 V, the entire epitaxial region is depleted. For a given amount of charge deposited from a neutron-induced collision, each device needs to have the eptixial region fully depleted for single-event burnout. The key takeaway from these simulation results is that neutron-induced secondary particle can sufficiently deposit energy consistent with the energy required for single-event burnout, in addition to having ranges that can fully penetrate the epitaxial region.

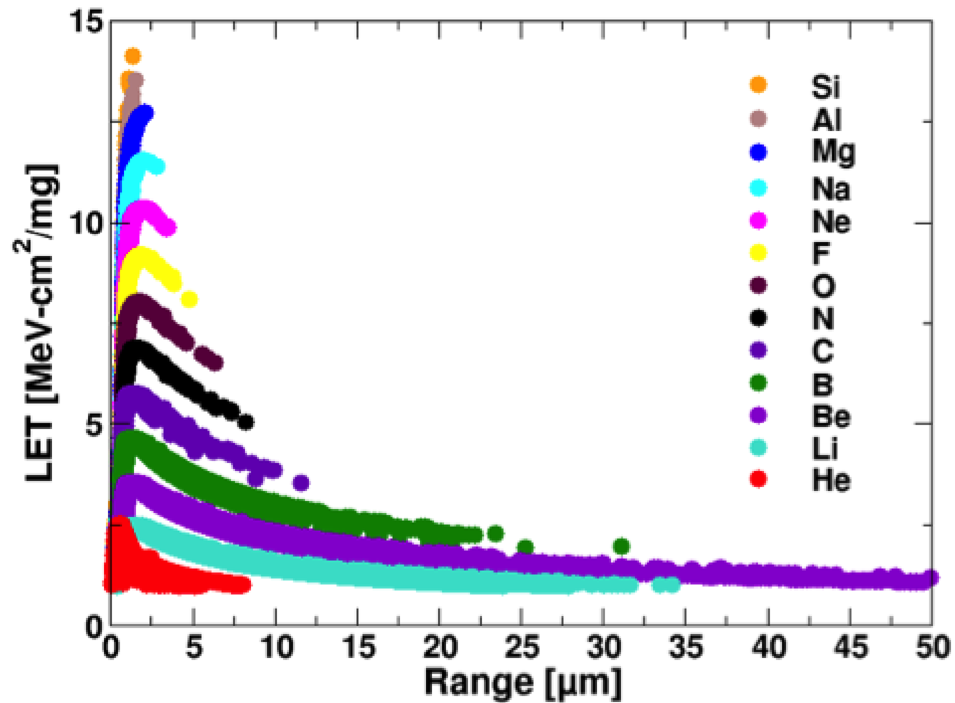


Figure 67: Secondary particles (showing range and LET) generated from neutron environment and entering the primary sensitive volume as calculated by MRED.