DUAL INTERLOCKED LOGIC: A RADIATION-HARDENED-BY-DESIGN TECHNIQUE FOR SINGLE-EVENT LOGIC ERRORS

By

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CHAPTER I

INTRODUCTION

Modern computing systems for terrestrial, military and space applications are facing ever increasing demands for higher throughput while still meeting constraints for radiation hardness, reliability and power. Each of these constraints impose significant design challenges and often an improvement in one area trades off as a degradation in another. At advanced technology nodes, the foremost problem faced by integrated circuit (IC) and system designers is power consumption. With ICs operating at gigahertz frequencies and facing increased transistor densities, reduction in power density and consumption has become a major focus of recent electronic systems. Innovations in circuit design and architecture for performance and power management (e.g., utilization of parallelism as an approach to improve circuit/system performance, aggressive use of power down of inactive transistors, etc.), as well as utilization of multiple types of transistors (high performance with high leakage and low performance with low leakage), are needed to design chips with both the desired performance and power dissipation [1]. For CMOS technologies, power consumption is proportional to the square of the supply voltage (and linearly proportional to nodal capacitances and operating frequencies). As a result, designers often use reduction in supply voltage as the first option against increasing power consumption at the IC and system level. Reduced power supply operations have the undesirable consequence of increasing electrical delays and increasing vulnerability to single-event soft errors.

A major contributor to soft errors in electronics are single event transients (SETs)

generated in combinational logic. This is especially true as technology scales to nanometer dimensions and designers push towards decreased supply voltages and higher operating frequencies, both of which increase the probability that an SET will cause a soft error. The general goal of this research is to elucidate the mechanisms and failure-modes governing the production and propagation of SETs in low-voltage, advanced technology applications, and provide novel RHBD designs and guidelines aimed at reducing SET-induced soft errors.

This dissertation covers the measurement, characterization and mitigation of digital single-event transients in two advanced technologies, 32nm SOI and 16nm/14nm bulk finFET. Chapter II consists of general background information for single-event radiation effects, low power design techniques and SET mitigation techniques. Chapter III details the investigation of SETs in low-power, voltage-scaled integrated circuits, including the impact of voltage shifters and the efficacy of filter-based SET hardening. Chapter IV presents the design and validation of a novel radiation-hardened-by-design (RHBD) combinational logic topology.

Appendix A details the current status of Vanderbilt's SET characterization and measurement methodologies. Appendix B presents heavy-ion induced SET data from both 32nm SOI and 16nm/14nm bulk finFET logic gates, but focuses primarily on the plethora of data at the 16nm/14nm node.

CHAPTER II

BACKGROUND

The possibility of cosmic radiation interacting with a semiconductor device to produce undesirable effects was first postulated by Wallmark and Marcus in 1962, although it had been known for some time that radiation from other sources affected semiconductor devices [2]. The first observation of errors due to cosmic radiation was in 1975 by Binder, Smith and Holman [3]. Since then, extensive research has been performed to understand how radiation affects electronics.

Radiation Effects Overview

Radiation effects generally fall into three categories: total ionizing dose (TID), displacement damage (DD) and single event effects (SEE). TID is a long-term cumulative effect which can lead to increased leakage current, shifts in threshold voltage or even functional failures. DD is caused when radiation interacts with the lattice structure to produce defects. The effects of DD are similar to TID. SEE are prompt effects due to an ionizing particle interacting with the material, which is called a single event (SE). SEE can be further categorized into soft errors and hard errors. Hard errors are typically destructive and can lead to single event latchup (SEL), single event burnout (SEB) or single event gate rupture (SEGR). Soft errors may manifest themselves as single event upsets (SEU) or single event transients (SET). SETs are temporary voltage glitches that arise at a circuit node due to a single ionizing event. SETs compete with the nominal signals in a circuit and can cause incorrect data to

be stored in a storage element. SEU are defined as the corruption of a logic state in a storage element due to the direct interaction of a single event with the storage element. However, in most cases SEU are caused by an SET being generated and captured inside the circuitry of a storage element. This work is focused on single event effects, especially single event transients.

Single Event Effects

A common topology for generic, synchronous logic is shown in Fig. 1, in which combinational logic is intermixed with storage elements. The logic is synchronous because data flow from one storage element, through combinational logic, to the next storage element is controlled by a common clock. A single event may occur in one of the combinational logic gates or in a storage element. If a single event occurring inside a storage element flips the logic state stored on the node, it is called a single event upset (SEU). If a single event occurs within a combinational logic gate, it may give rise to a temporary voltage signal called a single event transient (SET). An SET within the combinational logic of synchronous circuitry can propagate to a storage element and result in a SEU if certain timing criteria are met. An SET will be latched as an SEU if it is present at the latch's data input port within one setup time before the capturing clock edge or a hold time after the capturing clock edge as illustrated in Fig. 2. The summation of the setup and hold times of the latch along with the SET duration form what is known as the window of vulnerability. Due to the window of vulnerability, both the clock frequency and SET duration critically affect the probability of an SET being latched. As clock frequency increases, the window of vulnerability consumes more of the clock's period, thus leading to a higher

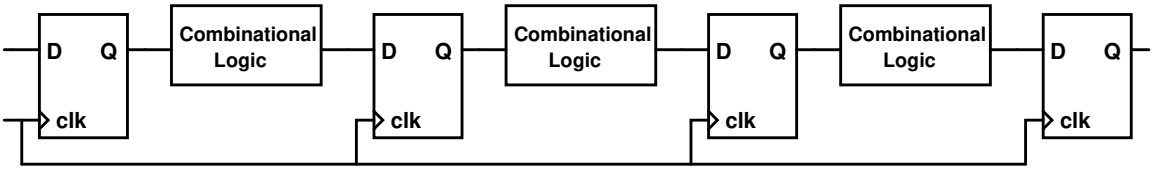


Figure 1: Generic pipelined synchronous digital system.

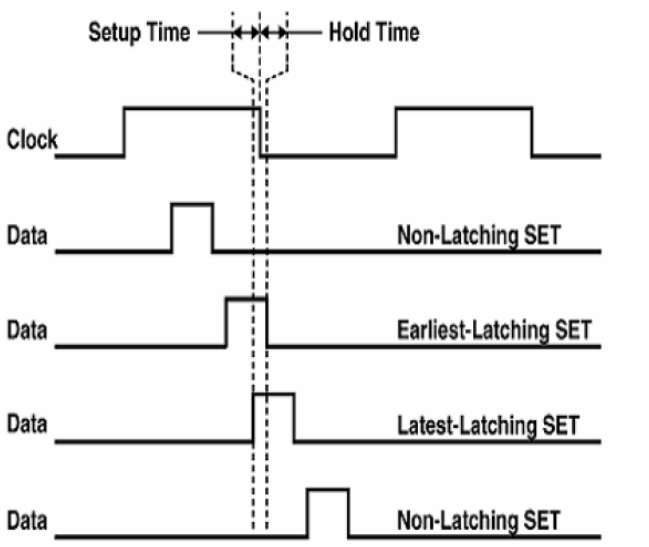


Figure 2: Window of vulnerability for latching an SET. (after [4])

probability that an SET will be latched.

Previous work has shown that the latching probability of an SET depends linearly on clock frequency [5], and that for modern high-speed designs, the soft error rate due to SETs may overcome the rate due to direct SEU. This effect is graphically shown in Fig. 3. The duration of an SET is also a critical factor in determining the probability of upset. As can be seen in Fig. 2, a longer SET duration results in a higher probability of being latched by essentially increasing the window of vulnerability. It is important to note that even for a direct strike to a storage element, an SET is first generated internally and then latched as an SEU. Thus, the understanding of SET generation and propagation is fundamental to all SEE soft error types. Several factors can influence the SET duration such as temperature, supply voltage, threshold voltage,

drive strength, load capacitance, LET, etc. Many of these factors can be related back to drive strength, and thus understanding the mechanism relating drive strength to SET duration is critical. A portion of this work is focused on understanding this link.

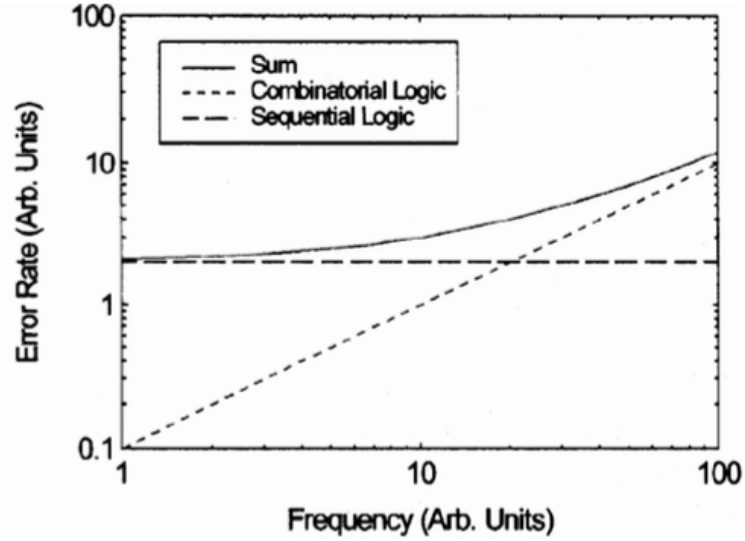


Figure 3: Relative contributions of errors from combinational and sequential logic. As operating frequency increases combinational errors become the dominant contributor to soft errors. (after [5])

Power Consumption in Digital Circuits

One of the most important design parameters in modern digital designs is power density. As integrated circuits (ICs) continually scale in both size and performance, removing the heat from the IC has become an increasing problem and often limits the performance. Power consumption in digital ICs can generally be grouped into two categories: static and dynamic power. Static power is the energy consumed when the circuit is in a stable logic state. Dynamic power is the energy consumed as the circuit transitions from one logic state to the next. In order to understand how to design circuits that consume less power, it is critical to understand the physical mechanisms

governing power consumption.

Static power consists of multiple components. The junction between the transistor diffusion and the substrate form a parasitic diode. When this diode is reverse biased, as is the case for the NMOS drain diffusion in an OFF inverter, a reverse bias leakage current is established due to minority carrier diffusion and drift near the edge of depletion regions. The reverse biased leakage current is modeled by,

$$I_{rbdl} = A \cdot J_s \cdot (e^{V_{bias}/V_{th}} - 1) \tag{1}$$

where A is the area of the junction, J_s is the reverse saturation current density, V_{bias} is the voltage across the junction and V_{th} is the thermal voltage.

Subthreshold leakage is another component of static power which occurs when the gate to source voltage is below the threshold voltage of the transistor. Weak inversion in the channel is one contributer to this leakage. When there is weak inversion in the channel, carriers can diffuse along the surface. This effect is most significant when the gate to source voltage is near the threshold voltage. Drain-induced barrier leakage (DIBL) also contributes to subthreshold leakage at high drain biases by effectively lowering the threshold voltage of the device. Electrical punch-through can also occur at high drain biases if the drain and source depletion regions encroach on one another. The combination of all of these subthreshold currents can be modeled as,

$$I_{sub} = I_0 \cdot e^{\frac{V_G - V_S - V_{T0} - \gamma V_S + \eta V_{DS}}{n V_{th}}} (1 - e^{\frac{-V_{DS}}{V_{th}}}) \tag{2}$$

where n is the subthreshold swing coefficient constant, γ is the linearized body effect coefficient, η is the DIBL coefficient and I_0 is the technology dependent subthreshold leakage.

Dynamic power consists of two parts: switching and short-circuit power. Switching power is the energy consumed from charging and discharging the load capacitor when the logic gate transitions from Vdd to 0. The switching power can be calculated using

$$P_{sw} = ACV^2 f \tag{3}$$

where C is the load capacitance, V is the supply voltage, f the switching frequency and A is the activity factor ($0 \leq A \leq 1$) since not every gate switches on every clock cycle. Short-circuit power is the energy consumed during a switching cycle due to both the NMOS and PMOS transistors being partially on for a short amount of time because of their finite switching times.

Low Power Design Techniques

Several techniques have been developed to reduce static and dynamic power such as: gate sizing, clock gating, voltage/frequency scaling, multi-Vt designs, adaptive body-biasing and power gating.

Since dynamic power is proportional to the load capacitance, one straightforward approach to reducing dynamic power is to reduce the logic gate size. As the logic gate size is reduced, the capacitance and thus the power are both reduced. However these power savings come with the tradeoff of increased delay.

Clock gating is another useful technique to reduce dynamic power. This technique arises from the fact that often large groups of storage elements may depend on a single enable value. Significant power can be wasted when storage elements are clocked without their data input changing. Clock-gating essentially ANDs the original clock with the enabling signal to form a new clock that is only active when the inputs to

the storage elements are more likely to change.

A third, highly common technique to reduce both static and dynamic power is voltage scaling. As the supply voltage is decreased, the dynamic power goes down proportional to the square of the voltage while also reducing the leakage power. The tradeoff in this case is speed and noise margins. In order to circumvent the effect of the reduced speed while still maintaining low power operation, ICs can be partitioned into voltage islands, where each voltage island is operated at the lowest voltage that still allows it to meet timing requirements. Logic signals that traverse from one voltage island to another must have their voltage level translated using a voltage level shifter in order to prevent static current flow that can arise when a low voltage gate cannot fully turn on a high voltage gate.

Multi-Vt designs can also be quite effective in reducing power, especially leakage power. As the threshold voltage of a device increases, the subthreshold leakage decreases because the device is able to be more effectively turned OFF. Once again, the tradeoff is speed since higher Vt devices inherently have longer delays. Similarly to voltage scaling, different portions of the design can utilize different threshold voltage devices in order to optimize the power and speed tradeoff.

Adaptive body-biasing is another power reduction technique which utilizes the relationship between threshold voltage and power. However, instead of statically choosing a single Vt device, the Vt is actively modulated by controlling the body bias via the well. One drawback of this technique is that in order to be effective it must use either a dual or triple-well technology.

Lastly, power gating is an extremely useful technique for reducing leakage power in idle blocks of the design. In power gated designs there is a permanent power rail

connected to the supply ports and a virtual power rail connected to the logic. These two rails are connected by large, power-gating transistors. When the logic block is active, the power-gating transistors are ON and the virtual power rail is connected to the permanent power rail. However, when the logic block is in idle mode, the power-gating transistors are switched OFF, disconnecting the permanent rail from the virtual rail. By cutting off power to the idle blocks, leakage power is drastically reduced.

SET Mitigation Techniques

The radiation-hardened-by-design (RHBD) community has put forth much effort to address the problem of SETs, and numerous techniques have been developed to mitigate the effect of SETs, which can generally be grouped into two categories: temporal mitigation and spatial mitigation. Temporal mitigation techniques involve a direct tradeoff between circuit speed and hardness since hardness is gained by inserting circuit delays proportional to the duration of the SET to be mitigated. Spatially redundant techniques circumvent the speed penalty of temporal techniques by incorporating multiple copies of the logic and using majority voting circuitry. However, spatially redundant techniques induce significant area and power penalties.

One of the most popular SET hardening techniques is triple modular redundancy (TMR), which has both a spatial and temporal topology. The spatially redundant topology is shown in Fig. 4, which consists of three copies of logic, voting circuitry and memory cells. This topology seeks to maximize performance (speed) by not incorporating any delays and relying solely on triplicated logic. The temporally

redundant TMR technique is shown in Fig. 5 and consists of voting logic, combinational logic, delay cells and triplicated memory cells. Each memory cell receives data that has been delayed by a different amount, either none, ΔSET or 2ΔSET. The amount of delay, ΔSET, corresonds to the maximum SET duration that needs to be mitigated. Although temporal TMR saves power and space compared to spatial TMR, the tradeoff is that temporal TMR adds clock overhead by an amount equal to two times the maximum SET duration that needs to be mitigated [6].

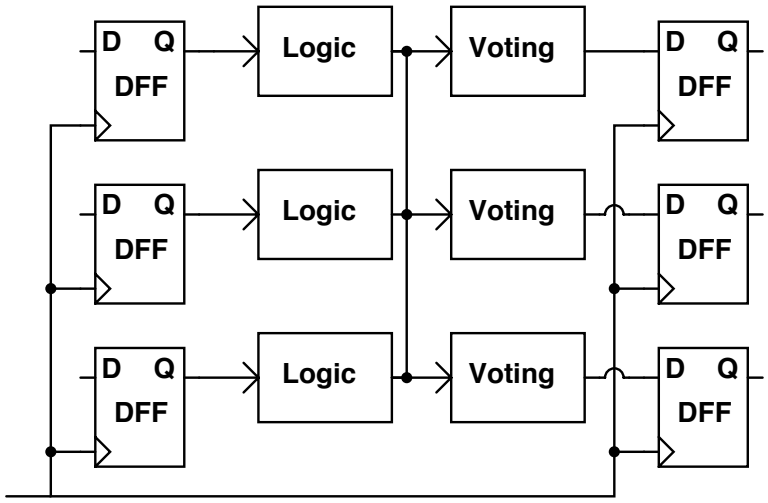


Figure 4: Block diagram of a spatially redundant TMR topology which does not require any a priori knowledge of the SET. [6]

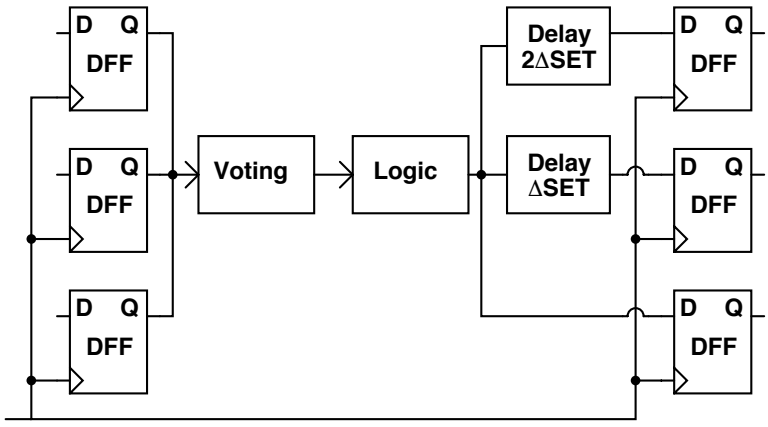
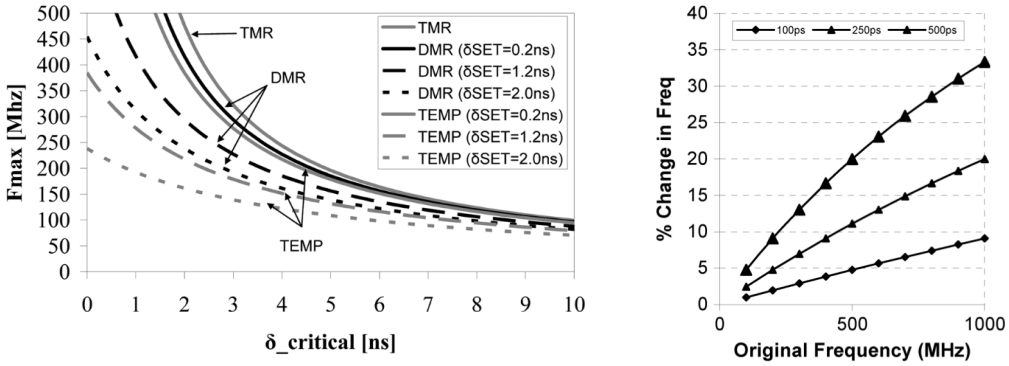


Figure 5: Block diagram of a hybrid spatial/temporal redundant TMR topology which is dependent on the duration of the SET. [6]



(a) (b)

Figure 6: (a)Maximum operating frequency for TMR, DMR and temporal sampling latches which include a voting circuitry delay of 0.1 ns [8].(b) Degradation of operating frequency as a function of SET duration for guard gate based mitigation. [7].

Several other SET mitigation schemes have been proposed that incorporate a mixture of spatial and temporal redundancy such as the temporal sampling latch by Mavis and Eaton [4], guard gates by Balasubramanian *et al.* [7] and dual modular redundancy by Teifel [8]. As can be seen in Figs. 6a and 6b, any technique incorporating delays inherently limits the maximum operating frequency of the circuit. As long as SET durations are much shorter than the desired clock period, temporally redundant techniques are an attractive solution to mitigating SETs since they have low area and power overheads. However, as operating frequencies increase to the point that the clock periods approach SET durations, temporally redundant techniques become impractical and the only remaining viable solution is spatial TMR. This research proposal will introduce a new SET mitigation technique that has less area and power overhead than spatial TMR and does not have the speed overhead of temporally redundant techniques.

CHAPTER III

TEMPORAL MITIGATION IN LOW POWER CIRCUITS

Delay-based SET Mitigation at Reduced Voltages

Single event effects are known to be enhanced for standard logic operating at sub-nominal supply voltages. As the supply voltage decreases, SET pulse widths increase, leading to a higher likelihood that they will be latched as an SEU. There have been numerous papers published on the effect of supply voltage on SET pulse widths; however, the mechanisms relating supply voltage to SET pulse width have not been explicitly laid out.

There are multiple factors that affect the efficacy of filter-based hardening techniques at low voltages SET duration, SET cross section and logic gate delay. It is known that both the electrical delay of a logic gate and SET duration increase with decreased bias; however, it is unknown whether they increase at the same rate since they are related to voltage through different physical processes. If SET duration increases at a faster rate than electrical delay, it could be detrimental to filter-based hardening at low voltages. This detrimental effect is possibly compounded by the corresponding increase in logic gate sensitive area at decreased voltages.

Fig. 7 shows an example of how the effectiveness of a filter decreases as the supply voltage decreases. The intersection of the the filter delay value with the SET cross section curve gives the cross section of unfiltered transients. A 50-ps filter at 0.8 V produces an unfiltered SET cross section of $3x10^{-}10$ cm^2. As the supply voltage decreases, the filter delay changes to 175 ps due to increased electrical delay, but

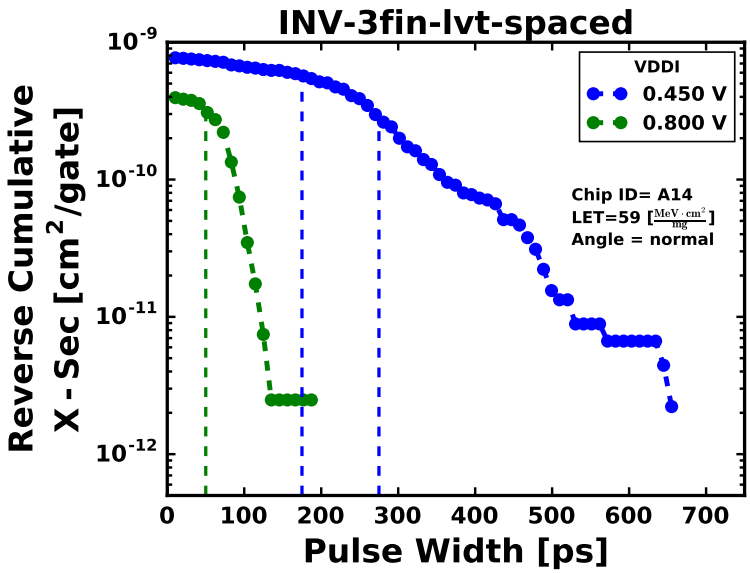


Figure 7: Reverse cumulative cross section represents the cross section of generating an SET with duration greater than or equal to the x-axis value. These data were collected from the heavy-ion irradiation of 14nm bulk finFET inverter chains. The green dashed line corresponds to a filter designed with a delay of 50 ps at 0.8 V. The cutoff increases to 175 ps as the bias decreases to 0.45 V, represented by the middle dashed line. The cross section of unfiltered SETs, represented by the intersection of the filter delay and the cross section curve, increases as the bias decreases from 0.8 V to 0.45 V.

the cross section of unfiltered SETs increases to 5x10^{-}10 cm^2. The filter delay would need to be increased to 275 ps in order to maintain the same cross section of unfiltered SETs as the 50-ps filter at 0.8 V. By elucidating the underlying mechanisms relating supply voltage with SET duration and logic gate delay, this research shows that the decrease in filter effectiveness for near-threshold biases is due to the increase in logic gate sensitive area, and that it is not compounded by a rapid increase in SET duration.

Mechanisms of Voltage Scaling for Inverter Delay and SET Duration

Inverter Delay

The electrical delay of an inverter has been studied extensively, and the mechanisms controlling the supply voltage dependency of the delay are well understood. The physical process underlying the electrical delay is the discharge of a loading capacitor by the drive current of a transistor. The voltage dependence of this process is evident in both the voltage-dependent charge on the capacitor as well as the voltage-dependent drive current of the active transistor. The equations governing the delay through two inverters in a series are given by

$$t_{HL} = \left[\frac{2(V_{Tn} - 0.1V_{DD})}{V_{DD} - V_{Tn}} + \ln\left(\frac{2(V_{DD} - V_{Tn})}{0.1V_{DD}} - 1\right)\right] \cdot \frac{C_{load}}{\beta_n(V_{DD} - V_{Tn})} \tag{4}$$

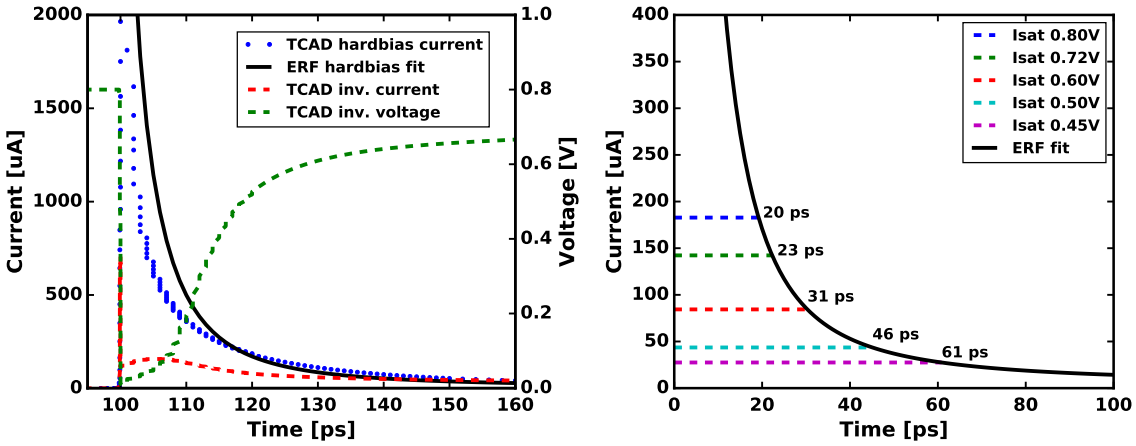
$$t_{LH} = \left[\frac{2(|V_{Tp}| - 0.1V_{DD})}{V_{DD} - |V_{Tp}|} + \ln\left(\frac{2(V_{DD} - |V_{Tp}|)}{0.1V_{DD}} - 1\right)\right] \cdot \frac{C_{load}}{\beta_n(V_{DD} - |V_{Tp}|)} \tag{5}$$

where V_{Tn} and V_{Tp} are the NMOS and PMOS threshold voltages, V_{DD} supply voltage, C_{load} output capacitance and β_n and β_p are the transconductance constants [9].

SET Duration

It is commonly known that SET duration increases with decreased bias, and it is understood that bias and duration are related through the current of the unstruck restoring device dissipating the charge generated in the struck device [10, 11, 12]. However, the drive current of the inverter alone is not sufficient to explain the voltage dependence of SETs. It has been shown that the duration of the SET nodal current

plateau created by the balance of the unstruck device restoring current and the single-event charge collection photocurrent is a good estimate for the duration of the SET voltage pulse [10, 11, 12]. It has also been shown through 3D-TCAD that the current plateau in an inverter configuration recovers at a time corresponding to the intersection of the magnitude of the restoring current and the profile of the drain current due to diffusion for the hard-biased configuration [10]. If the diffusion current profile for the hard-biased configuration can be accurately modeled, then the voltage dependence of SETs can be extracted based on the intersection described above.



(a) (b)

Figure 8: The hard-biased single-event diffusion current generated in the struck device is modeled well by an error function as described by Kauppila [13]. These simulations were performed with 3-fin LVT devices at a supply voltage of 0.8 V. In both cases, the NMOS device was struck with an LET of 10 MeV·cm^2/mg. For the inverter configuration, a 3-fin LVT PMOS was modeled to complete the inverter. (b) An estimate of the SET pulse width can be obtained by locating the intersection of the drive current of the restoring device with the model for the current in the hard-biased case. The saturation currents were obtained from SPICE simulations using the 16nm/14nm PDK.

Figs. 8a and 8b illustrate the concept. In Fig. 8a the drain current due to a single event strike on a 16nm/14nm 3-fin NMOS device is modeled using 3D-TCAD for both hard-bias and inverter configurations. The current from the inverter configuration

exhibits the characteristic plateau, and the voltage recovery coincides with the current plateau intersecting the hard-bias current. The hard-bias diffusion current has been modeled with an error function, also shown in Fig. 8a, as described by Kauppila [14]. Fig. 8b shows the same error function fit along with the saturation current of a 3-fin PMOS device (restorative device) at several different supply voltages. The saturation currents were obtained from SPICE simulations using the 14nm PDK. The intersection of the saturation current with the diffusion current model can be used to estimate the SET pulse width and thus identify the voltage dependence of SETs. Fig. 8b shows that as the supply voltage decreases, the saturation current does decrease as expected, but that the SET duration increases mainly due to the profile of the error fit which is due to diffusion current.

Experimental Details

A test DUT for autonomously capturing SETs at reduced supply voltages was designed in a 16nm/14nm bulk FinFET technology. Similar to previous SET test chips, it consists of target logic, a propagation network and an SET capture circuit. Table 6 summarizes the logic gates used in this work. Three different variants of inverter designs are utilized. The base inverter, INV-3f-LVT, is a 3 fin, low threshold voltage (Vt) design. The INV-6f-LVT inverter differs only in fin count (six instead of three) from the base design. The INV-3f-RVT inverter differs only in threshold voltage (RVT instead of LVT) from the base design, where RVT is a higher threshold voltage than LVT.

The target logic is constructed similarly to previous designs, utilizing short logic chains combined in parallel by a balanced OR tree. In order to minimize propagation

Table 1: Description of target logic for low voltage heavy-ion results.

Name	Logic Type	Total Fins	Fingers	Threshold Voltage	Gates Per Chain	Total Gates
inv-3f-lvt	inverter	3	1	low	22	11264
inv-6f-lvt	inverter	6	2	low	20	10240
inv-3f-rvt	inverter	3	1	regular	22	11264

induced pulse broadening, chain lengths are limited to less than 23 gates each [9]. Logic gates are spaced four poly pitches apart, which for the 16nm/14nm finFET generation corresponds to 280 nm (70 nm poly pitch) [10]. The inverters used in the work have equally sized PMOS and NMOS transistors. The 3-fin inverters use transistors with drawn active areas having dimensions of three fin pitches by two poly pitches which corresponds to 126 nm (3x42 nm) and 140 nm (2x70 nm). The 6-fin inverter uses transistors with drawn active areas having dimensions of three fin pitches by four poly pitches which corresponds to 126 nm (3x42 nm) and 280 nm (4x70 nm) [10].

The test DUT was irradiated in vacuum at Lawrence Berkeley National Laboratory (LBNL) using the 10 MeV/u cocktail at normal incidence and at room temperature. Data were collected for target logic supply voltages ranging from 0.45 V to 0.8 V and LETs ranging from 0.9 (B) to 59 (Xe) MeV·cm^2/mg. All circuits other than target logic were operated at nominal voltage of 0.8 V for all tests.

Low Voltage Heavy-Ion Induced SET Results

Data from the irradiation of the three logic targets from Table 6 using 10 MeV/u Si, Cu and Xe ions across a range of target supply voltages are shown in Figs. 9 - 11.

These data can be used to independently reveal the SET dependence on supply

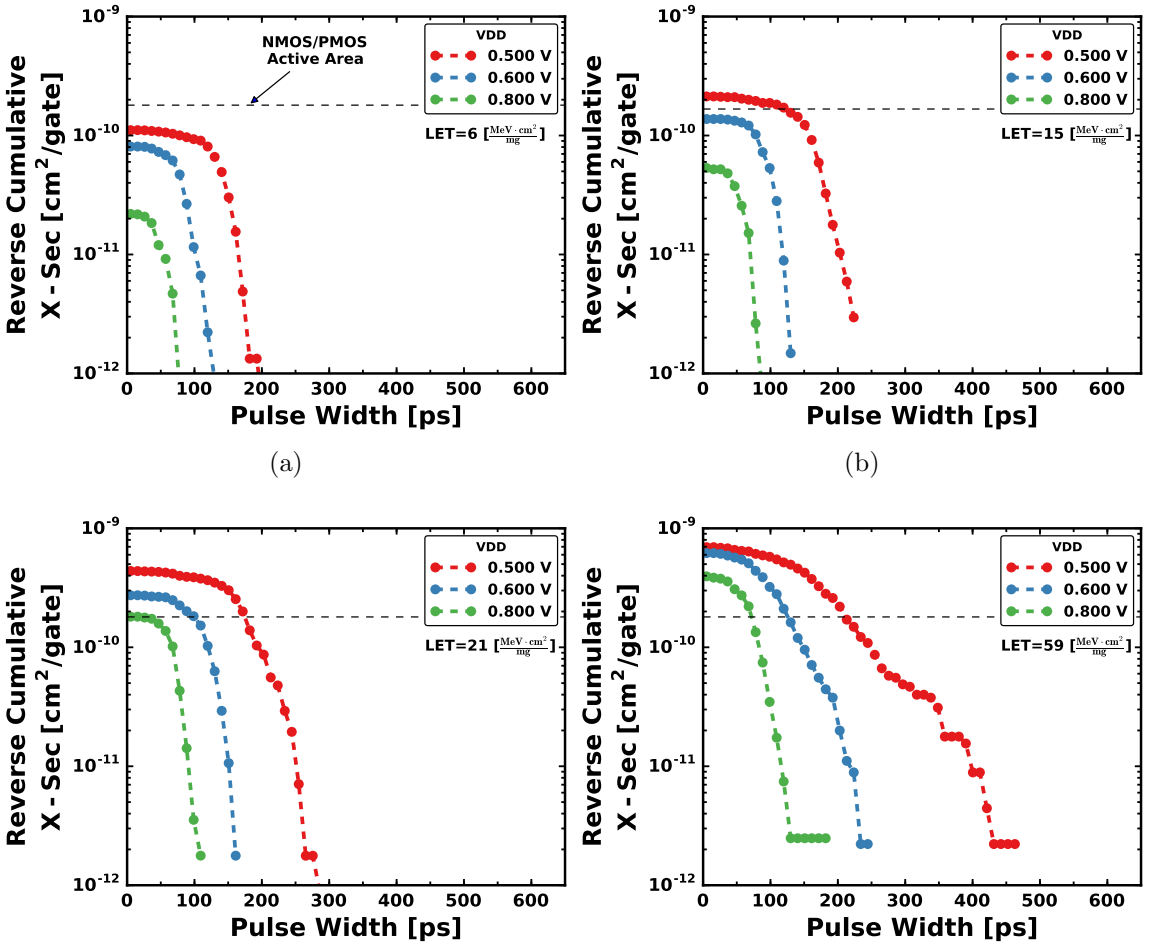


Figure 9: Impact of supply voltage and LET on the SET cross section from the heavy-ion irradiation of a three-fin, low-threshold-voltage inverter (INV-3f-lvt target from Table 6). Irradiations shown are with 10 MeV/u Si, Ar, Cu and Xe ions at normal incidence with LETs of 6,15, 21 and 59 MeV·cm^2/mg respectively. The flat dashed line represents the drawn active area of one NMOS or PMOS transistor used in the inverter design.

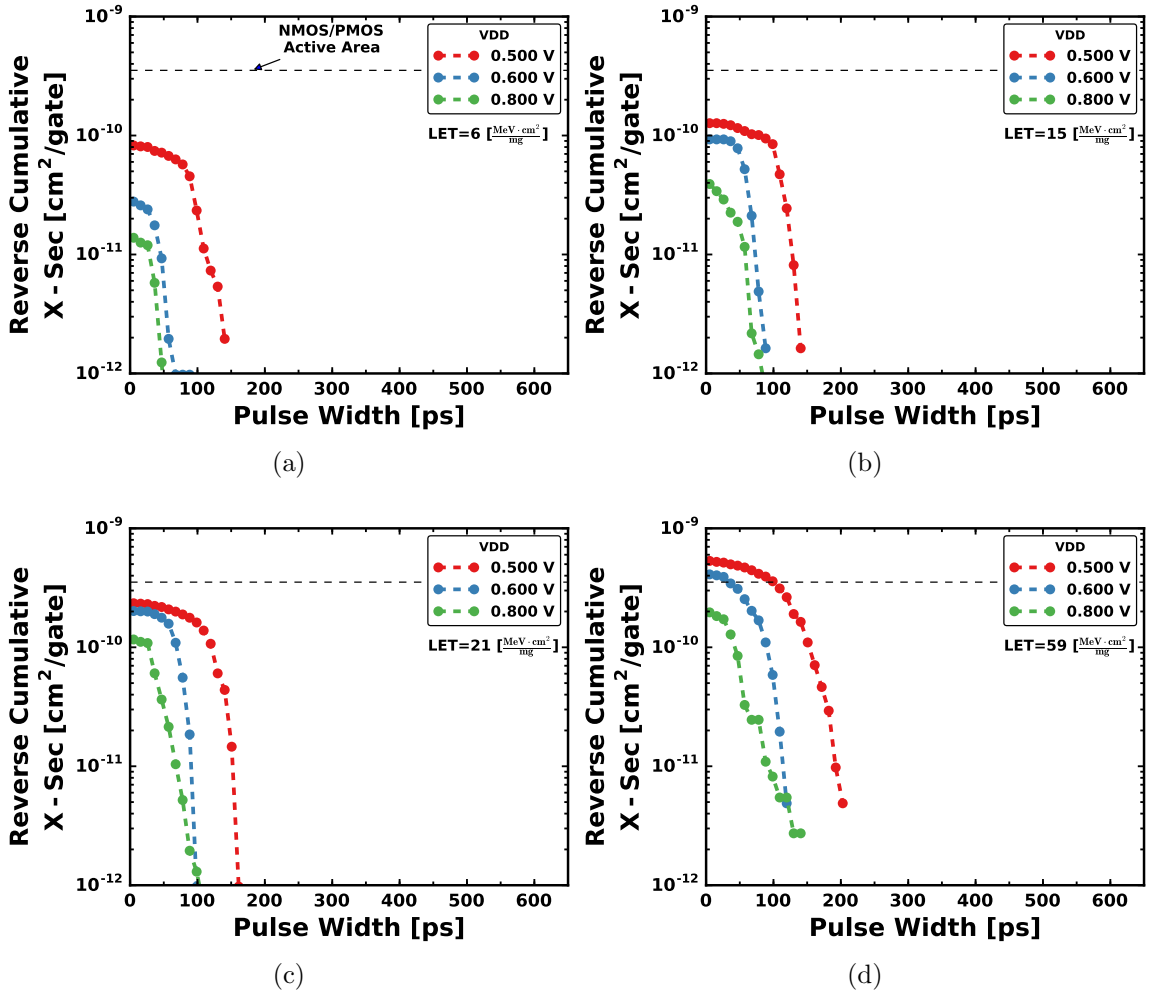


Figure 10: Impact of supply voltage and LET on the SET cross section from the heavy-ion irradiation of a six-fin, low-threshold-voltage inverter (INV-6f-lvt target from Table 6). Irradiations shown are with 10 MeV/u Si, Ar, Cu and Xe ions at normal incidence with LETs of 6,15, 21 and 59 MeV·cm^2/mg respectively. The flat dashed line represents the drawn active area of one NMOS or PMOS transistor used in the inverter design.

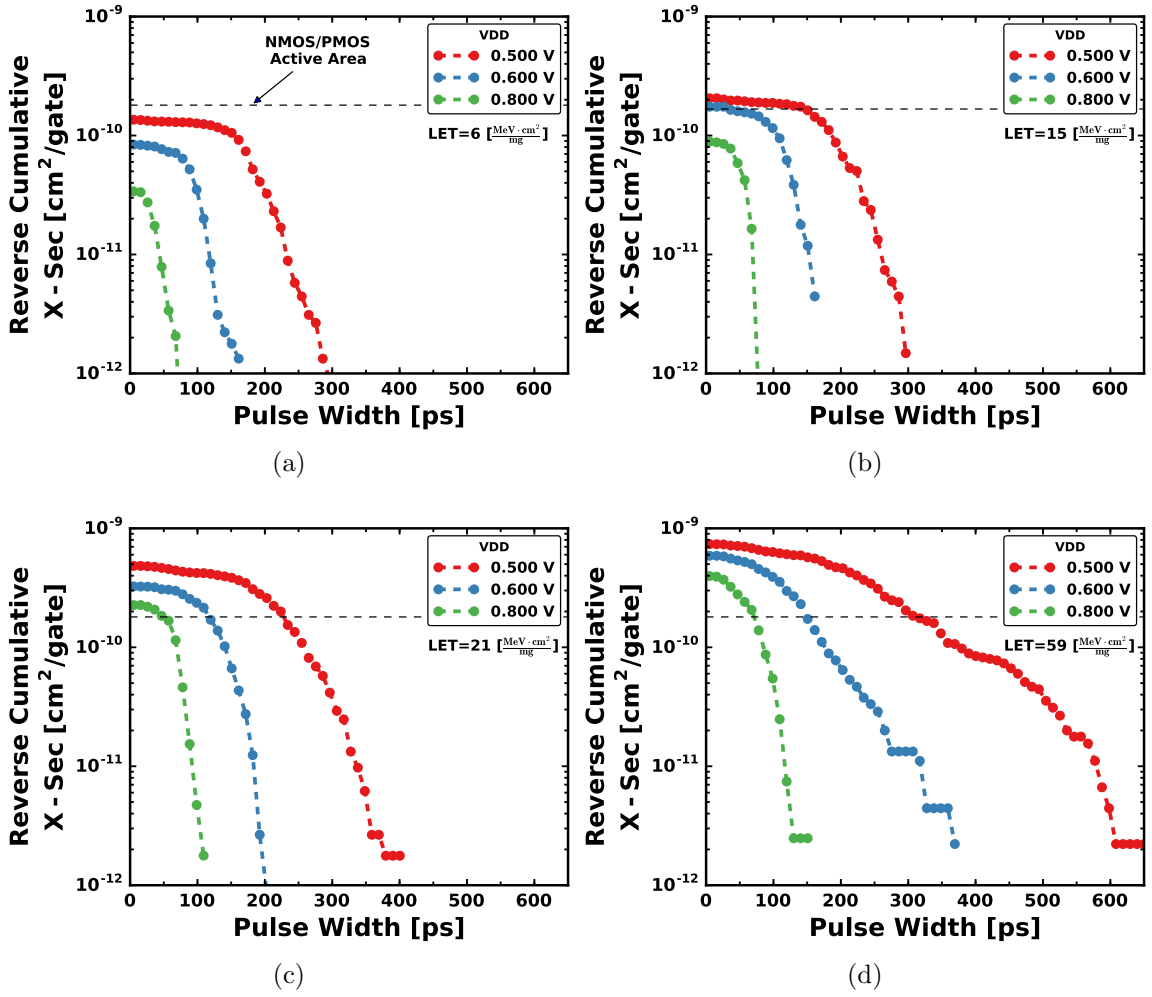


Figure 11: Impact of supply voltage and LET on the SET cross section from the heavy-ion irradiation of a three-fin, regular-threshold-voltage inverter (INV-3f-rvt target from Table 6). Irradiations shown are with 10 MeV/u Si, Ar, Cu and Xe ions at normal incidence with LETs of 6,15, 21 and 59 MeV·cm^2/mg respectively. The flat dashed line represents the drawn active area of one NMOS or PMOS transistor used in the inverter design.

Table 2: LET threshold for measuring an SET across several bias conditions. SET measured (Y). No SET measured (N). LET is given in [MeV·cm^2/mg] for the two lowest LET heavy-ions used.

LET	0.9 (B)				2.2 (O)
VDD [V]	0.5	0.6	0.65	0.8	0.8
inv-3f-lvt	Y	Y	N	N	Y
inv-6f-lvt	N	N	N	N	Y
inv-3f-rvt	Y	Y	N	N	Y

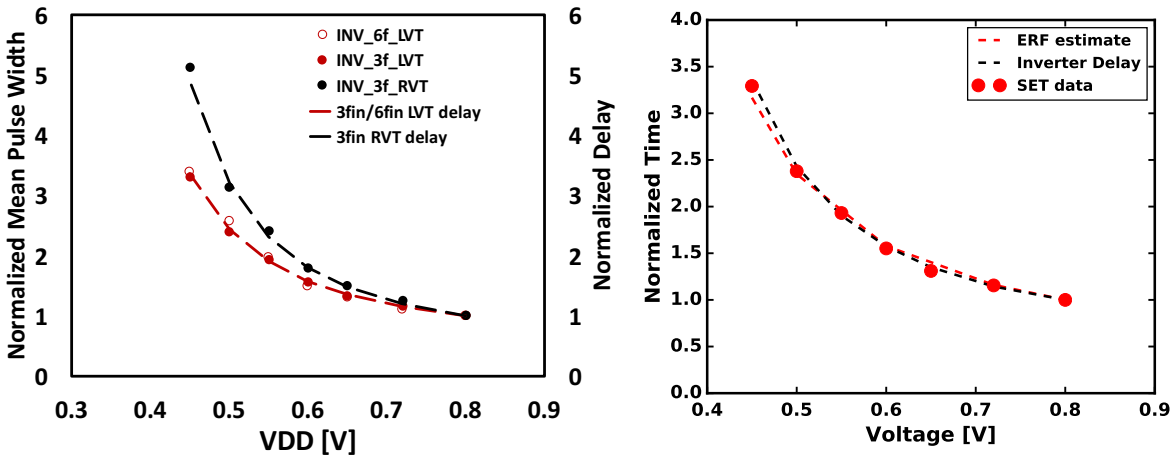
voltage through drive current variations due to threshold voltage and device width (fin count). It is clearly evident in these data that as the restoring drive current decreases due to supply voltage, fin count or threshold voltage, there is a corresponding increase in both SET duration and cross section. The increase in SET duration is readily understood by the fact that the reduced restoring current takes longer to dissipate the single-event deposited charge, and thus restore the voltage at the output node. The increase in cross section (or sensitive area) for reduced restoring currents is due to the reduction in the amount of charge needed to discharge the output node (i.e. critical charge). This reduction in critical charge naturally leads to a larger sensitive area. As critical charge decreases, LET threshold also decreases. Table 2 states whether or not an SET was measured for a given bias and LET combination. SETs were measured from all targets at an LET of 2.2 MeV·cm^2/mg with a bias of 0.8 V and below. No SETs were measured from the 6-fin LVT inverter at an LET of 0.9 MeV·cm^2/mg regardless of bias. SETs were measured from both 3-fin inverters at an LET of 0.9 MeV·cm^2/mg for biases at and below 0.6 V but not for biases above 0.6 V. The data in Table 2 can be used to evaluate the LET threshold for an SET that was above the minimum measurable pulse width for the measurement circuit (i.e. 11ps). SETs below 11ps will be produced at lower LETs.

As the LET increases there is an increase in both SET duration and cross section across all biases. The drawn active area of one NMOS or PMOS transistor is imposed on the plots of Figs. 9 - 11. At an LET of 6 MeV·cm^2/mg, the cross sections of all three inverter types are below the drawn active area. As LET increases to 59 MeV·cm^2/mg, the cross sections increase above the drawn active area. When the cross section is above the drawn active area, it is possible that pulse quenching can occur if the logic gates are adjacent to one another. In this work, the logic gates are spaced apart by four poly pitches (280nm) in order to reduce the effect of pulse quenching.

SET Duration and Inverter Delay

The SET duration is a critical parameter in RHBD approaches utilizing temporal mitigation techniques. Fig. 12a shows the mean pulse width from experimental SET distributions for the three inverters described in Table 6 for biases ranging from 0.45 V to 0.8 V collected at an LET of 21 MeV·cm^2/mg. At least 200 SETs were measured for each distribution in order to produce a good statistical mean. The data in Fig. 12 have been normalized to their value at 0.8 V in order to elucidate the dependency on voltage. Both the 3-fin and 6-fin LVT inverters show the same dependency on voltage, while the 3-fin RVT inverter shows a slightly steeper trend. The simulated electrical delay of inverter chains designed with the same inverters described in Table 6 are also shown in Fig. 12a. The 3-fin and 6-fin LVT inverters have the same electrical delay as expected since both drive strength and output capacitance scale proportionally with fin count. Due to the difference in threshold voltage, the 3-fin RVT electrical delay increases faster with decreased voltage compared to the LVT inverter as expected. Interestingly, the SET data for the LVT and RVT inverters

overlay their corresponding electrical delays, showing that SET duration increases at practically the same rate as electrical delay. Fig. 12b shows why this is the case using the 3-fin LVT inverter as an example. In Fig. 12b, the normalized mean SET and electrical delay for a 3-fin LVT inverter is shown, just as in Fig. 12a. Additionally, the SET pulse widths estimated from Fig. 8b are also shown normalized to the 0.8 V value. The estimate using the error function fit overlays both the data and the inverter delay, thus showing why the SET duration increases in a similar way to the electrical delay. There is strong agreement between the modeled and experimental pulse widths, thus verifying the SET duration voltage dependency that arises due to the restoring device overcoming the single-event diffusion current.



(a) (b)

Figure 12: (a) The mean experimental SET pulse width scales proportionally to inverter delay across bias. The dashed lines represent the delay of an inverter for that operating point normalized to the delay at 0.8 V. The circles represent the mean of the SET distribution for that operating point normalized to the mean at 0.8V. These data were collected with an LET of 21 MeV·cm^2/mg. (b) The mean experimental SET pulse width scales with bias due to the duration of the current plateau of the restoring device in an inverter. The ERF (error function) estimate represents the normalized estimated pulse width from Fig. 8b.

The data presented in this work is the first time SETs from logic gates have been

captured on-chip in a bulk finFET technology. However, the results and analyses presented are not specific to the measured technology. It is expected that other nano-scale bulk technologies will exhibit similar trends with voltage scaling. Silicon-on-insulator (SOI) technologies may not exhibit the same characteristics due to their limited charge collection volumes and varying levels of channel depletion. In bulk technologies, a decrease in critical charge leads to a larger sensitive area since the device can collect charge from strikes further away in the bulk silicon [15]. In SOI technologies, especially for high LETs, a decrease in critical charge may not lead to a larger sensitive area since the collection volume (i.e. body or channel region) is electrically isolated from the bulk silicon [16].

Impact on Temporal-Based Hardening Techniques

Temporal SET mitigation techniques can be very effective in reducing errors due to SETs. Conventionally, temporal techniques utilize filter or delay cells to remove any voltage glitch less than the delay or cutoff of the filter. Shown in Fig. 13 are two exemplar techniques utilizing delay cells for SET mitigation [4, 7]. Delay cells are also used internally in some hardened storage elements [17]. Although delays can be implemented by increasing nodal capacitance, a common area-efficient method is to utilize a chain of inverters, typically in combination with a guard gate (also known as C-element) [7, 17]. There are three factors that affect the efficacy of filter-based hardening techniques at low supply voltages: SET duration and SET cross section, and the electrical delay. In order for the delay cell to effectively mitigate an SET, the delay of the cell must be equal to or greater than the duration of the SET. As supply voltage decreases, both cell delay and SET duration increase. As shown above,

the electrical delay and mean SET duration scale in a similar manner with supply voltage. This bodes well for filter-based RHBD techniques, since filters would become less efficient if the SET duration were to increase more rapidly than electrical delay with reductions in supply voltage.

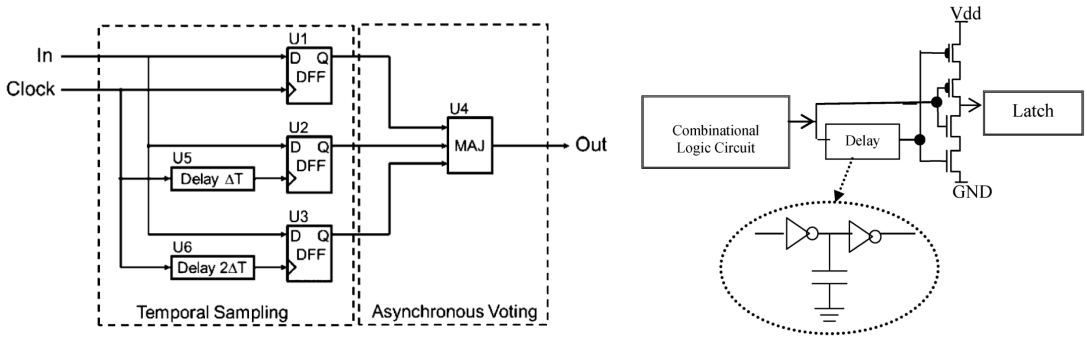
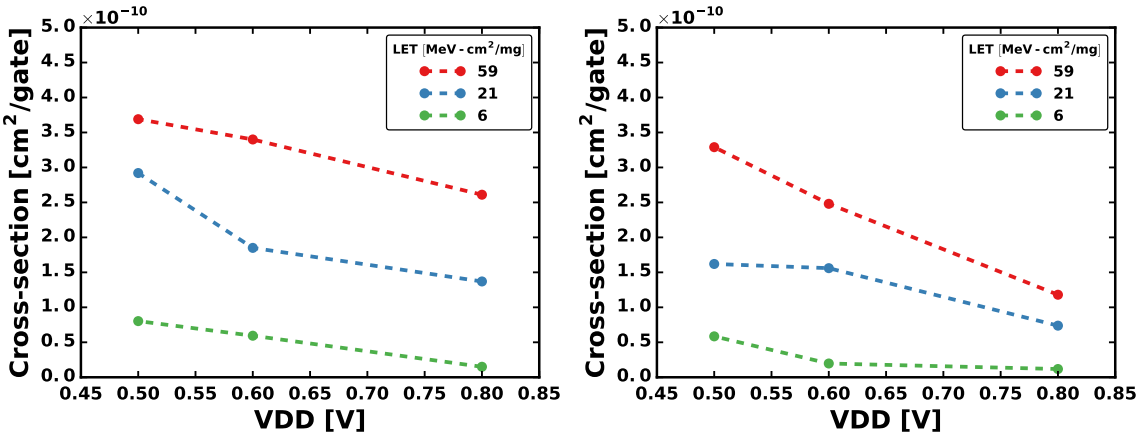
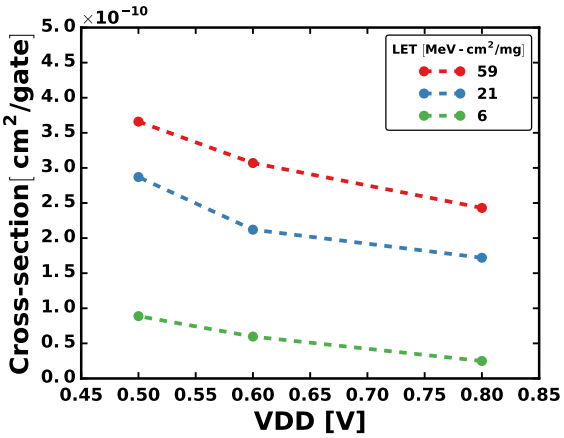


Figure 13: (a) RHBD technique utilizing delays to mitigate SETs via temporal sampling [4]. (b) Example utilizing delays to harden against SETs via filtering through a guard-gate element [7].

The second factor affecting filter-based techniques is the increase in the sensitive area of a logic gate as supply voltage decreases, as experimentally shown in Fig. 7. Each data point represents the cross section for generating an SET with a duration greater than or equal to the value on the x-axis. Overlaying the filter cutoff duration is a convenient way to represent the cross section of unfiltered SETs. Since a filter eliminates SETs less than the filter delay, the intersection of the filter delay with the reverse cumulative cross section curve represents the cross section of all SETs longer than the filter cutoff (i.e. unfiltered SETs). Although the filter cutoff increases at a similar rate with the mean SET duration, it is not enough to additionally compensate for the increase in SET cross section. Fig. 14 shows the cumulative SET cross section calculated at the mean of the SET distributions (see Table 3) shown in Figs. 9-11,



(a) (b)



(c)

Figure 14: The cumulative SET cross section calculated at the mean of the SET distributions shown in Figs. 9-11 (see Table 3 for mean pulse widths), covering both bias and LET. The plot in (a) is for inv-3f-lvt, (b) is for inv-6f-lvt and (c) is for inv-3f-rvt. Although the electrical inverter delay tracks with the mean SET pulse width, there is an increased SET cross section calculated at the mean SET pulse width due to increased sensitive area.

covering both bias and LET. It is clear from these data that even if the filter delay tracks the mean SET pulse width as supply voltage decreases, the cross section of unfiltered transients will still increase due to increased sensitive area, and this trend holds true across LET.

For applications operating at reduced and variable supply voltages and needing

Table 3: Mean SET pulse widths from distributions in Figs. 9-11 used to calculate cross sections in fig. 14. LET is given in MeV·cm^2/mg and the mean pulse width is given in picoseconds.

	VDD	LET = 59	LET = 21	LET = 6
inv-3f-lvt	0.8 V	60	57	42
	0.6 V	96	97	69
	0.5 V	162	153	120
inv-6f-lvt	0.8 V	39	34	26
	0.6 V	58	58	33
	0.5 V	106	99	76
inv-3f-rvt	0.8 V	56	55	29
	0.6 V	118	110	82
	0.5 V	235	190	163

SET robustness, these data reveal that the delay element should be designed to meet the cross section requirement of the lowest intended operating voltage. The mean SET pulse widths given in Table 3 may act as a guide for choosing an appropriate filter delay. Choosing a delay less than the mean SET duration offers minimal gain in terms of cross section reduction, whereas delays above the mean offer maximum tradeoff between delay and cross section reduction [18].

A practical solution to overcoming the increased sensitive area at low voltages is to use a delay element whose propagation delay has a stronger voltage dependence than the surrounding logic. For example, if the delay element is designed with logic gates having a higher threshold voltage than the logic gates from which the SETs are generated, then the filter cutoff of the delay element will increase more rapidly with decreased voltage than the SET duration of the lower threshold voltage logic. Other delay element schemes such as the use of current starved or stacked inverters may be tuned to have a stronger voltage dependency as well [17].

CHAPTER IV

DUAL INTERLOCKED LOGIC

The radiation-hardened-by-design (RHBD) community has put forth much effort to address the problem of SETs, and numerous techniques have been developed to mitigate the effect of SETs, which can generally be grouped into two categories: temporal mitigation and spatial mitigation. Temporal mitigation techniques involve a direct tradeoff between circuit speed and hardness since hardness is gained by inserting circuit delays proportional to the duration of the SET to be mitigated. Spatially redundant techniques circumvent the speed penalty of temporal techniques by incorporating multiple copies of the logic and using majority voting circuitry. However, spatially redundant techniques induce significant area and power penalties. This research has led to the development of a new hardening technique with manageable layout area and speed penalty.

The hardening technique developed in this work leverages concepts from the cascode voltage switch logic (CVSL) family and a RHBD technique known as interlocked feedback, similar to dual interlocked storage cell (DICE) latches, to develop a new logic topology that is robust to SETs. A traditional DICE latch schematic is shown in Fig. 15, where the feedback paths are interlocked to mitigate single-node upset susceptibility [19]. The DICE latch immunity to single-node upsets is due to distributed logic storage across four separate circuit nodes and the restoring property of redundant, interlocked feedback loops.

The schematic of a generic CVSL gate, where the gate is comprised of a

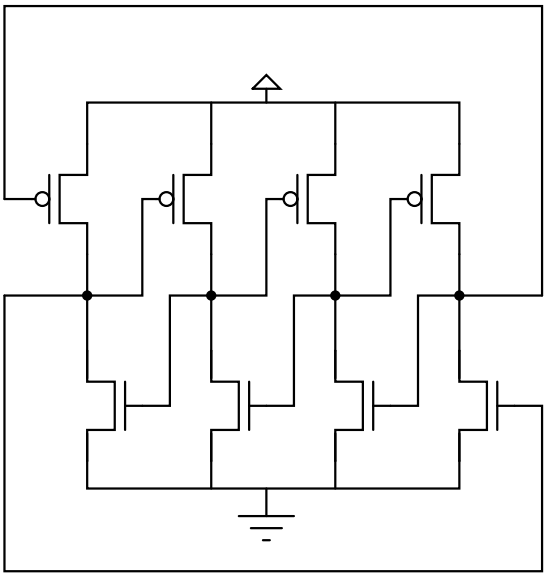


Figure 15: The latching core of a DICE flip flop, illustrating one implementation of interlocked feedback [19].

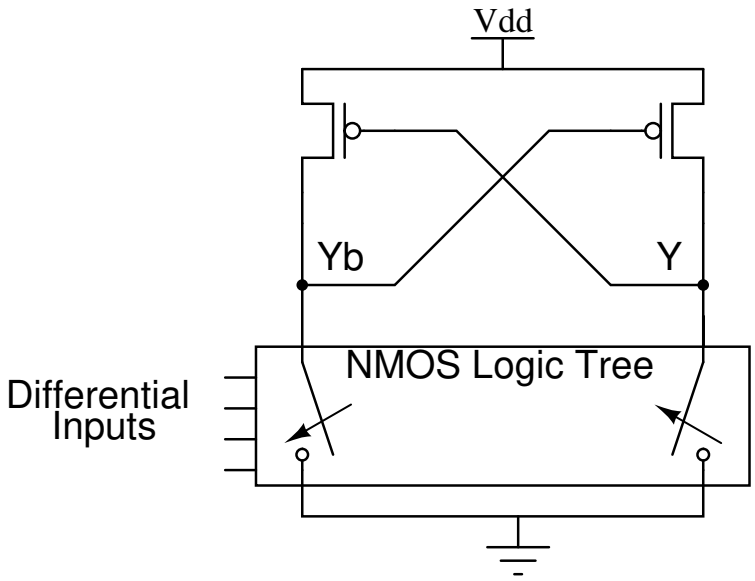


Figure 16: Schematic for a generic CVSL gate [20].

cross-coupled PMOS pair driven by complementary NMOS logic trees capable of implementing any boolean function, is shown in Fig. 16 [20]. The CVSL family is a differential logic family in that it requires both a true and complement input, and produces both a true and complement output. One advantage of CVSL is its fast switching speed, which is due to the fact that the signal is taken as the difference between its two outputs as opposed to just a single output. This research revealed that the cross-coupled PMOS pair in CVSL has the potential to be hardened via interlocked feedback.

SET mitigation in combinational logic can take various forms such as preventing an SET from originating, shortening the SET or masking the propagation of the SET to subsequent gates. Concerning the last form of mitigation, previous works have examined the ability of an SET to propagate through both static CMOS and traditional CVSL gates [21, 22, 23, 24]. Static CMOS gates have repeatedly been shown to allow SETs to propagate unhindered down a chain of logic gates, given that specific timing characteristics are met [21, 22]. Traditional CVSL gates have also been examined concerning SET propagation, although only in simulation. Casey *et al.* concluded that CVSL NAND gates do not propagate an SET that results in a 010 transition [23]. Hatano *et al.* showed via simulation that CVSL gates have an increased tolerance to SETs compared to static CMOS, but that they are still capable of propagating SETs in some cases [24]. To the authors knowledge, no previous work has experimentally examined heavy-ion-induced SETs in CVSL gates. Although traditional CVSL gates do have some single node robustness, they are still vulnerable to dual-node strikes, which can occur at high angles of incidence or due to charge sharing. This work shows via simulation and heavy-ion broad-beam exposure

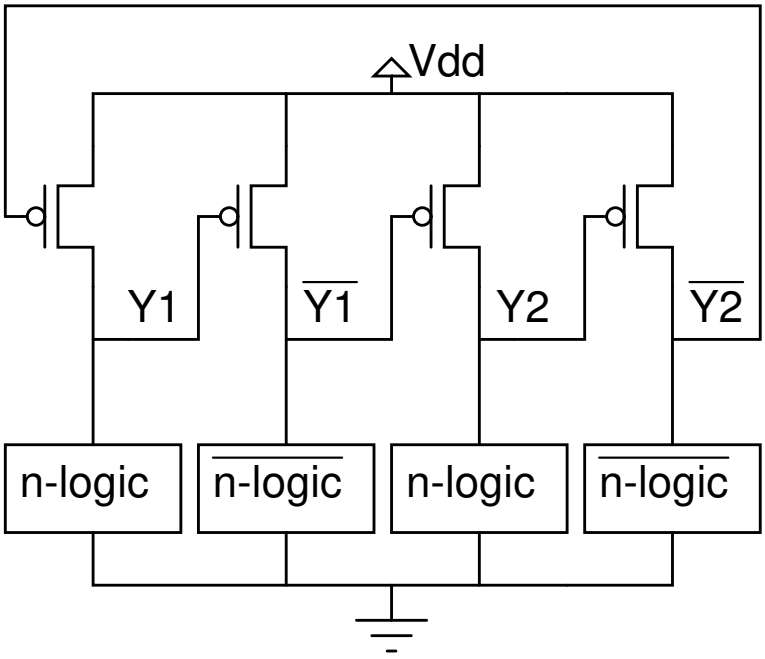


Figure 17: Dual Interlocked Logic (DIL), a novel SET hardened combinational logic topology. Nodes Y1, $\overline{Y1}$, Y2, and $\overline{Y2}$ are differential outputs that are passed to the next gate or latch. N-logic and n-logic bar are complementary NMOS logic trees capable of implementing any boolean function.

that CVSL gates are vulnerable to dual-node strikes. The hardened logic topology described in this work is shown to be an improvement over both static CMOS and traditional CVSL in that it prohibits the propagation of SETs of any polarity or duration and is robust to single- and dual-node strikes.

Hardening Technique Description

Termed Dual Interlocked Logic (DIL), the topology consists of four PMOS devices connected in an interlocked feedback fashion. Redundant NMOS differential logic trees, represented by n-logic and $\overline{\text{n-logic}}$ in Fig. 17, drive the interlocked PMOS devices. DIL gates require at least two sets of differential inputs and generate two sets of differential outputs (Y1, $\overline{Y1}$ and Y2, $\overline{Y2}$), which are connected to the inputs of the subsequent gate. When an SET occurs at one of the output nodes, at most

one adjacent output node is also perturbed. Figs. 18-21 provide an intuitive example of how the DIL topology works for the case of a single-node strike in an inverter. A transient generated as the result of an ion striking a single node in the first inverter initially produces a full-rail transition on one output node and a mid-rail transition on an adjacent node. The outputs of the next inverter are minimally affected by these transitions as shown in Fig. 21.

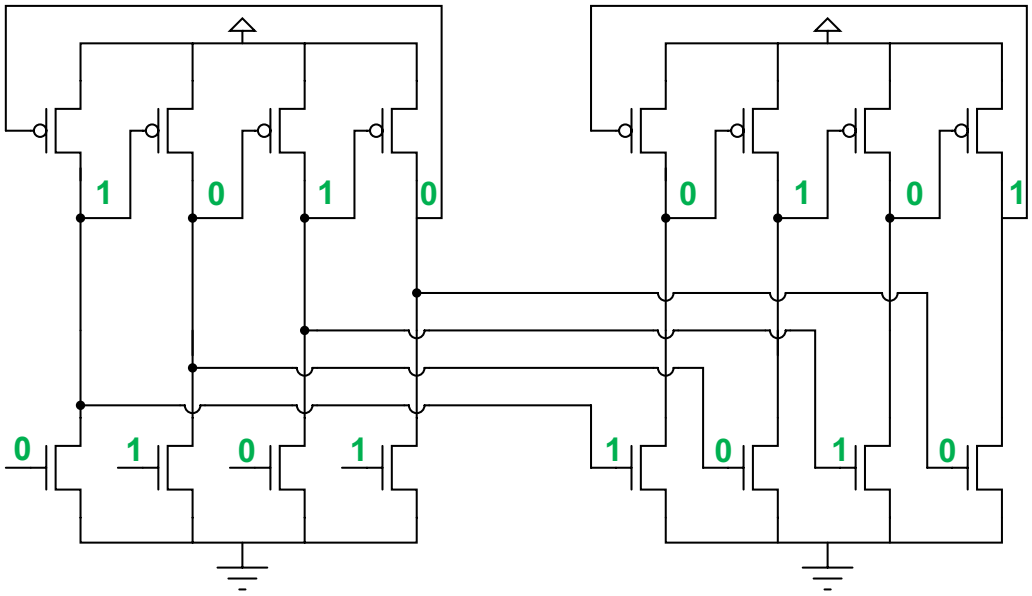


Figure 18: Intuitive fault injection example of the hardening technique presented in this work. Shown are two serially-connected hardened inverters are shown in their normal states.

Comparison to Other Logic Topologies

As with any RHBD technique, there are trade-offs in speed, area and/or power in order to gain radiation robustness. In this work, the DIL topology is compared against CVSL and traditional static CMOS logic across four metrics: delay, area, power and SET sensitivity Each metric is calculated based on a NAND2 gate in a 16nm/14nm bulk finFET technology generation. The results of the comparison are

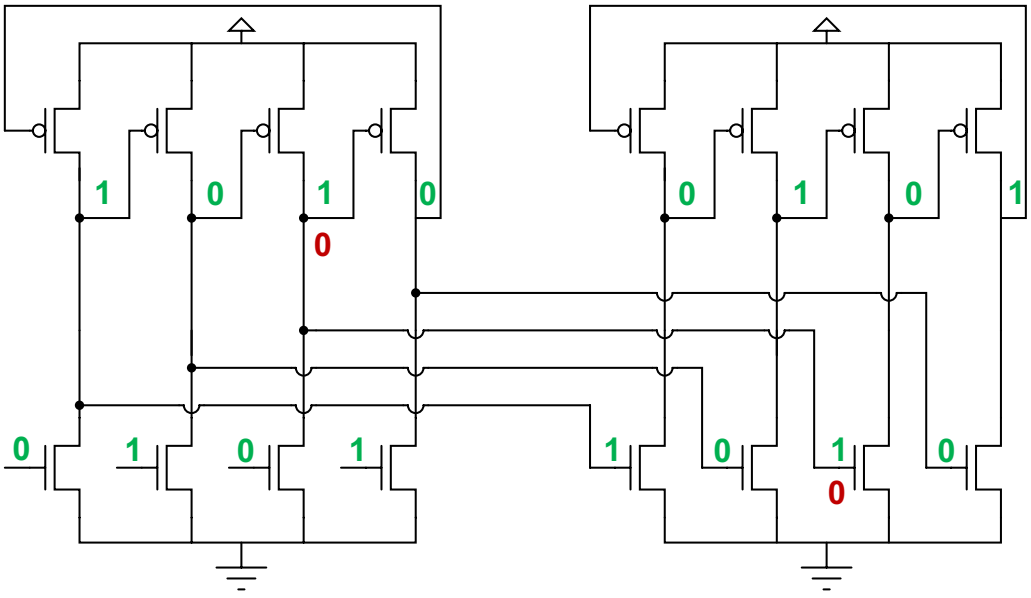


Figure 19: Intuitive fault injection example of the hardening technique presented in this work. The circuit state immediately after a single event that causes an output node on the first inverter to transition from 1 to 0 is shown, where green represents an unaltered logic state and red represents a perturbed node.

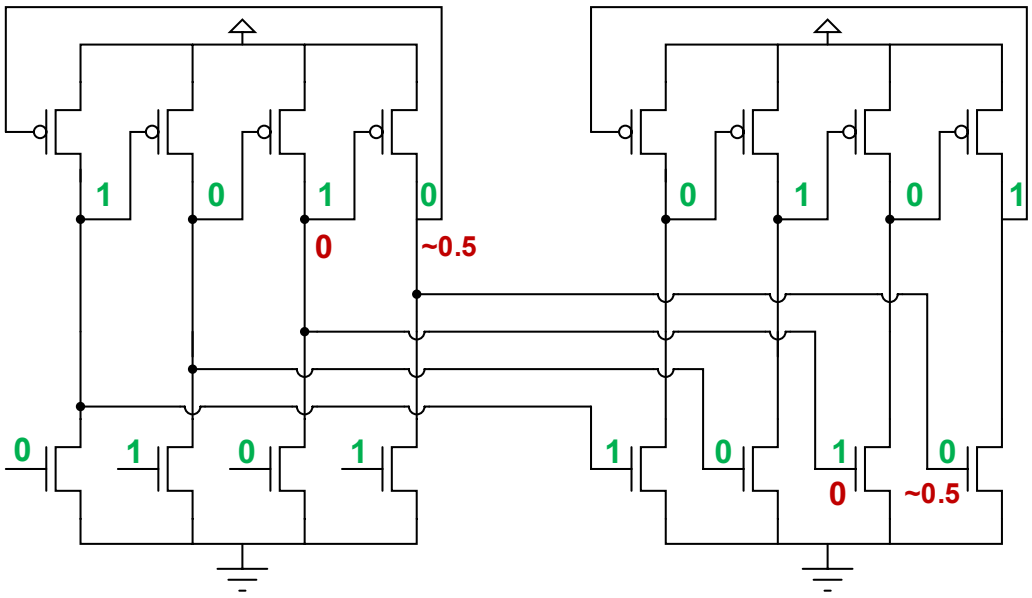


Figure 20: Intuitive fault injection example of the hardening technique presented in this work. The transition from 1 to 0 causes the adjacent output node on the first inverter to transition from 0 to 0.5 (an intermediate voltage determined by the relative drive strengths of the ON PMOS and ON NMOS in that branch).

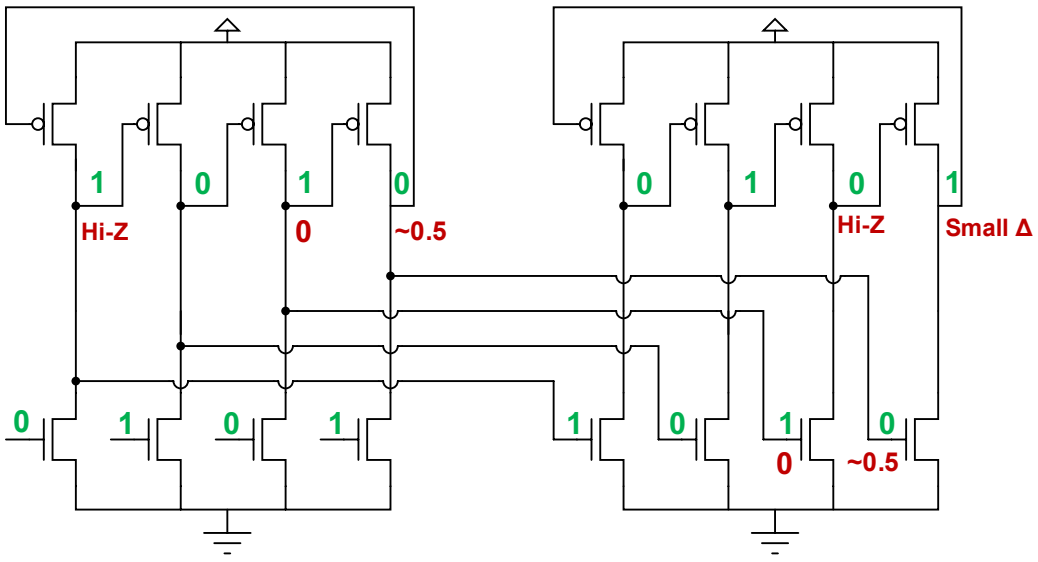


Figure 21: Intuitive fault injection example of the hardening technique presented in this work. The result of the transient in the first inverter causes one of the outputs in the second inverter to become high impedance (Hi-Z) with no change in its logic state, and the adjacent node in the second inverter has only a small change (Small). The other two outputs in the second inverter remain unchanged.

shown in Table 4.

A common metric for speed is average propagation delay, which is the average time between an input and output transition measured at 50% of the logical high voltage. Compared to CMOS, CVSL and DIL have 2.3X longer propagation delays; however, as technology scales and switching times decrease, this speed tradeoff becomes more acceptable. For example, assuming a 16nm/14nm bulk finFET technology node and a logic depth of 25 propagation delays per clock cycle, all three logic topologies are capable of operating in the low GHz range. Since the SET robustness of the DIL topology is due partially to redundancy, there is an inherent area penalty from the increased number of transistors. Compared to the CMOS NAND2 gate, the CVSL gate is 1.4X larger and the DIL gate is 2.6X larger.

However, as commercial silicon technology scales leading to increased transistor

density, area penalties become less of a critical design constraint. Power density is becoming an increasingly important design constraint with technology scaling. The power metric in Table 4 is based on the average power per clock cycle at a frequency of 1 GHz for 100% data activity (i.e. each gate switches once per clock cycle). Compared to CMOS, CVSL and DIL incur a 1.6X and 3.2X power penalty respectively. It is important to note that the CMOS gate is a commercially optimized design, whereas the CVSL and DIL gates are first iteration designs.

Techniques have been developed to reduce both the power consumption and propagation delay of CVSL gates, and these techniques are also directly applicable to DIL gates [25]. Although CVSL and DIL topologies exhibit undesirable area and electrical trade-offs compared to CMOS logic, they do exhibit highly desirable benefits in terms of SET robustness. Static CMOS logic has repeatedly been shown to be sensitive to SETs as a result of ion strikes to a single node [22]. CVSL gates have been shown to be more robust than CMOS logic to single node strikes; however, they are still vulnerable to dual node strikes. DIL gates exhibit superior radiation performance to both CVSL and CMOS logic in that they are robust to both single-node strikes, and dual-node strikes. While DIL gates do have triple node sensitivity to SETs, with proper layout techniques the sensitive nodes can be designed in such a way that the probability of a single ion passing through all three nodes is greatly reduced.

Comparison to Triple Modular Redundancy

One of the most prolific RHBD techniques is triple modular redundancy (TMR), which has both a spatial and temporal form [6, 8]. Spatial TMR is the most robust

Table 4: Trade-off comparison for CMOS, CVSL and DIL topologies. The metric, t_{pd}, is the average propagation delay.

	CMOS	**CVSL**	**DIL**
t_{pd}	1X	2.3X	2.3X
Area	1X	1.4X	2.6X
Power	1X	1.6X	3.2X
SET Sensitivity	Single Node	Dual Node	Single Node

form in that it triplicates the logic, memory cells and the voting circuitry. It is capable of mitigating an SET of any duration that is the result of a single-node strike, although it is still vulnerable to multi-node strikes and clock tree errors. The main penalties of spatial TMR are area and power, which are at least 3X greater than a non-TMR system. Temporal TMR relies on temporally triplicated logic paths rather than physically triplicated paths. It consists of three copies of the memory cells, one voting circuit and one logic path that feeds into three delayed data paths. One data path is not delayed, the middle data path is delayed by an amount equal to the longest SET to be mitigated, and the third data path is delayed by an amount equal to twice the longest SET to be mitigated. This technique has less of an area and power penalty than spatial TMR, but the integrated delay paths limit the maximum operating frequency and require prior knowledge of the SET duration to be mitigated. In order to know the SET duration, extensive testing in a specific technology and environment must be performed. RHBD techniques which do not depend on the SET duration are more easily portable to new technologies, applications and environments than those that do depend on the SET duration.

DIL shares with spatial TMR the benefit of not needing information about the SET duration, in that it can mitigate an SET of any duration that is a result of a single-node or dual-node strike. DIL has the added benefit of not needing to triplicate

any logic paths or memory cells because its redundancy is internal to the logic gate.

Table 5 compares the area, power and delay for an exemplar synchronous system consisting of ten NAND2 gates between memory cells. For comparison, DIL, spatial TMR and temporal TMR were applied to an unhardened baseline system. The block diagrams for DIL, spatial TMR and temporal TMR are shown in Figs. 34, 23 and 24 respectively. The baseline system consists of two commercial D flip-flops (FF) with ten commercial NAND2 logic gates. The DIL system uses differential DICE FFs to gain single-node robustness in the memory cells. Both TMR systems use the same gates as the baseline system along with a majority voter circuit comprised of three AND2 gates and one OR3 gate [8]. The delay circuit for the temporal TMR system was designed using current starved inverters, and the target SET duration to be mitigated was 150 ps. Power is calculated based on the average power per clock cycle at a frequency of 1 GHz for 100% data activity (i.e. each gate switches once per clock cycle).

Table 5: Comparison of single-node robust synchronous systems.

	Baseline (no RHBD)	**DIL w/ DICE**	**Spatial TMR**	**Temporal TMR**
Area	1X	2.8X	3.9X	3.5
Power	1X	2.4X	3.7X	4.6
Delay	1X	2.3X	1.5X	14.8
Technology Agnostic	n/a	yes	yes	no

Shown in Table 5, the DIL/DICE hardening technique is the most area efficient hardening approach of the three. In terms of power, DIL is better than spatial TMR and comparable to temporal TMR. In terms of delay, spatial TMR and DIL are both far better than temporal TMR. The power consumption in the DIL gate is due largely

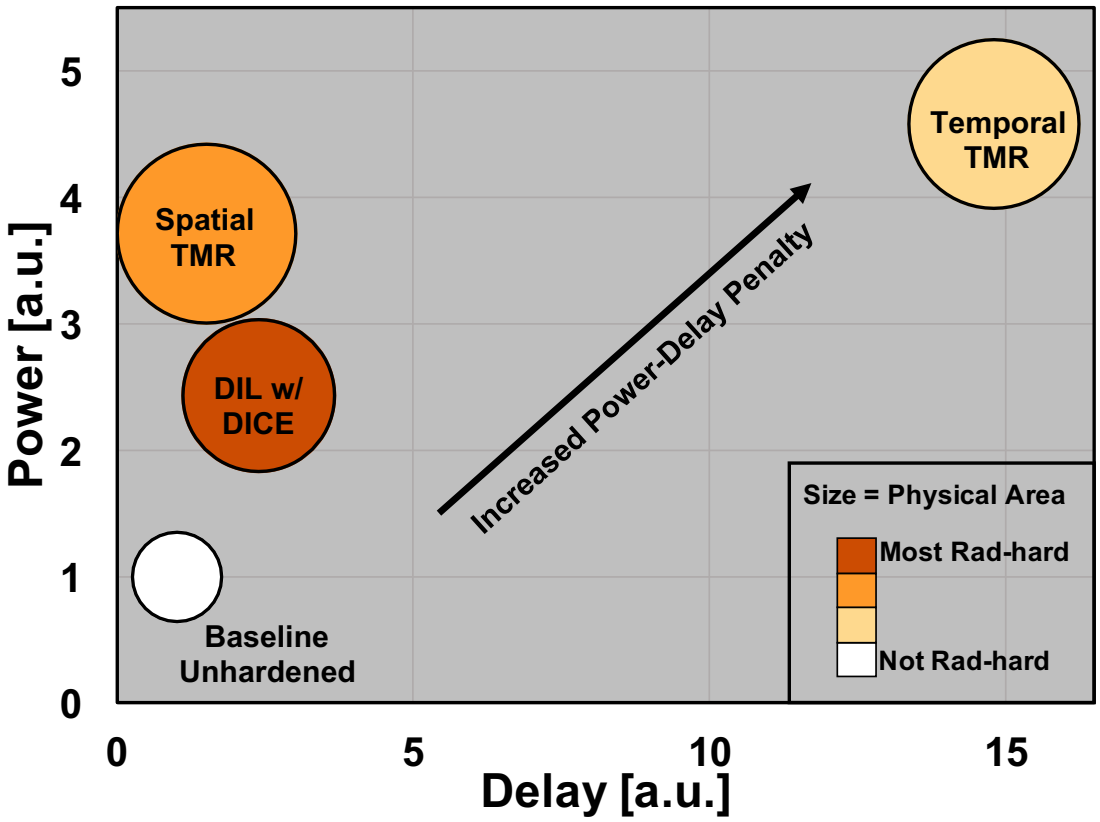


Figure 22: Power and delay tradeoff for several RHBD techniques based on the metrics in Table 5. The size of each circle corresponds to the physical area of the technique.

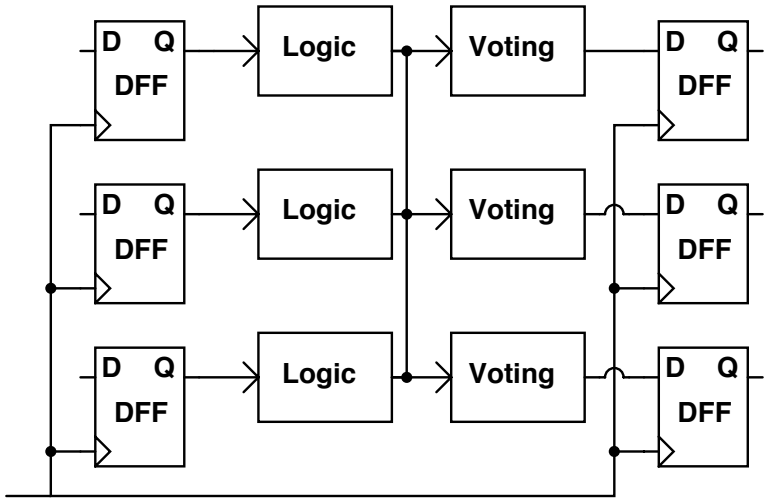


Figure 23: Block diagram of the spatial TMR topology used for comparison in Table 5. The voting blocks were designed using three AND2 gates and one OR3 gate. The logic blocks were comprised of ten NAND2 gates. All logic gates and memory cells utilized were commercially optimized.

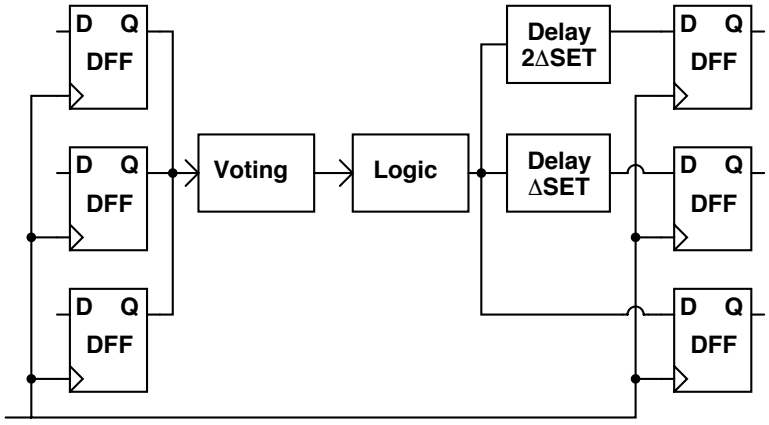


Figure 24: Block diagram of the temporal TMR topology used for comparison in Table 5. The voting block was designed using three AND2 gates and one OR3 gate. The logic block was designed using ten NAND2 gates. The delay (Δ SET) blocks was designed using current starved inverters with a total delay of 150 ps for ΔSET and 300 ps for 2ΔSET. All logic gates and memory cells utilized were commercially optimized.

to dynamic power consumption from typical output capacitance charging/discharging as well as shoot-through current. The shoot-through current arises because the NMOS and PMOS devices are not switched simultaneously. The NMOS devices are turned on first, and they must overcome the PMOS drive current to discharge the output nodes. While the output node is discharging, both the NMOS and PMOS devices are temporarily on at the same time. Since both devices are on, a path is formed between the positive voltage supply and ground. This path is the source of the additional shoot-through current. Simulations at an operating frequency of 1 GHz and 100% data activity show that the dynamic power consumption, including the shoot-through current, is 150 times greater than the static power consumption. The previous comparisons have been made based on simulations for an advanced 16nm/14nm bulk finFET node. For older technologies, the trade-offs from Table 4 will be similar. For the comparisons in Table 5, the comparisons will be similar except for the case of temporal TMR. For temporal TMR, the area, power and delay penalty will likely be

even greater due to increased transient duration at older technology nodes, which can average 500 to 800 ps [26].

Heavy-Ion Simulation Analysis

In order to investigate the robustness of the DIL hardening technique, circuit-level SPICE simulations of DIL-based circuits have been performed using the process design kit (PDK) for the 16nm/14nm bulk finFET technology generation. Ionizing particle strikes were carried out using the bias-dependent single-event (SE) compact model developed by Kauppila *et al.* [27, 14]. This bias-dependent SE model utilizes proven bias-dependent SE methods and has been calibrated to the PDKs being used and validated with heavy-ion data . For the simulations, chains of four serially connected NAND2 gates designed using either standard CMOS, CVSL or DIL were used. Both single-node and multi-node strikes were simulated. Each simulation was carried out twice, once for an LET of 6 MeV$\cdot$cm^2/mg and once for an LET of 60 MeV$\cdot$cm^2/mg. Additionally,all simulations were performed at nominal voltage (0.8 V), the NAND2 gates were implemented using the same designs that were physically implemented on the 16nm/14nm TCV test chip.

Single-node Simulation Analysis

First, the single-node robustness of each logic topology is investigated. For the purpose of analysis, a worst-case simulation was performed by striking one of the parallel transistors in the first NAND gate. This is worst case because it requires the restoring current to come from the stacked transistors as opposed to the parallel transistors. Stacked transistors exhibit lower restoring currents than

parallel transistors when when transistors are similarly sized. Fig. 25 shows the results of a single-node strike in the standard CMOS gate. As expected, a transient is generated in the first gate and is able to propagate to the last gate without any attenuation or masking. Fig. 26 shows the results of a single-node strike in the CVSL gate. A full-rail transient occurs in the first gate on the struck node, and, due to the feedback in the CVSL gate, a small secondary transient is produced on the unstruck node in the first gate. The transient from the first gate is not able to propagate to the fourth gate. Fig. 27 shows the results of a single-node strike in the DIL gate. A transient is generated at the output of the first gate, similar to the transient generated in the CVSL gate, but it is not able to propagate to the output of the last gate. The simulation analysis shown in Figs. 25 - 27 is for an input condition of 0.8 V on the stacked transistors. For thoroughness, all iterations of input conditions and transistor strikes were simulated at both an LET of 6 MeV$\cdot$cm^2/mg and 60 MeV$\cdot$cm^2/mg. The results were very similar and support the conclusion that standard CMOS logic is sensitive to single-node strikes and both CVSL and DIL exhibit single-node robustness.

Multi-node Simulation Analysis

In addition to the single-node analysis in the previous section, a thorough multi-node simulation analysis has been performed for the CVSL and DIL gates since both gate topologies exhibited single-node robustness. For each of the simulated logic chains, two nodes were struck simultaneously, corresponding to the same two nodes that were targeted during broad-beam irradiation, as discussed in a later section. The simulation is for an ion whose path crosses two nodes and is not

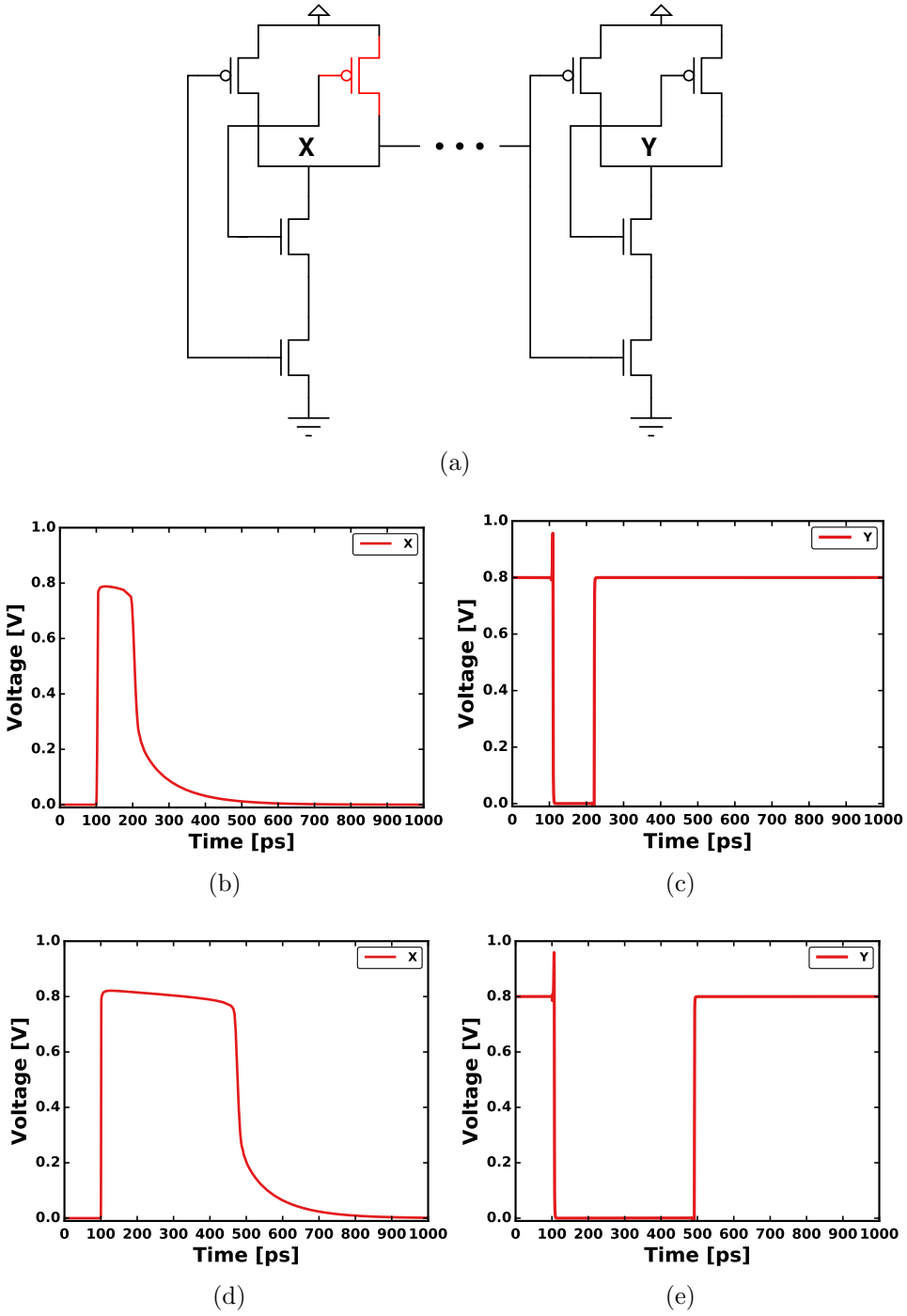


Figure 25: SEE simulation results for a single-node strike in a standard NAND chain, shown schematically in (a), using the 16nm/14nm SEE model with an LET of 6 MeV·cm^2/mg and 60 MeV·cm^2/mg [13]. In (b) the voltage at node X, resulting from a strike on the PMOS transistor in the first gate is shown for an LET of 6 MeV·cm^2/mg. The output of the fourth gate, node Y, is shown in (c). The transient produced at X is able to propagate to the output of the fourth gate. Similar results are shown in (d) and (e) for an LET of 60 MeV·cm^2/mg.

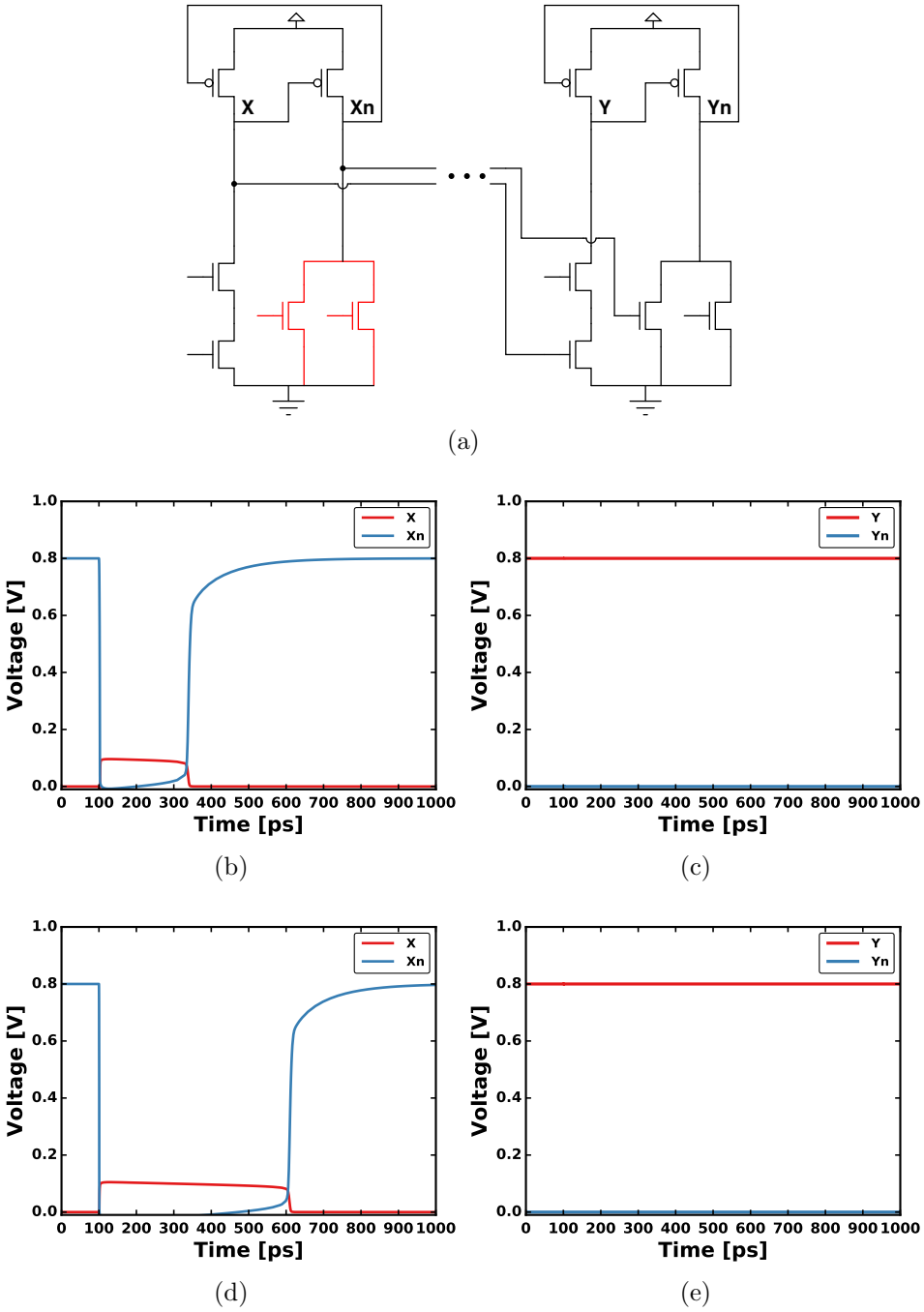


Figure 26: SEE simulation results for a single-node strike in a CVSL NAND chain, shown schematically in (a), using the 16nm/14nm SEE model with an LET of 6 MeV·cm^2/mg and 60 MeV·cm^2/mg [13]. In (b) the voltage at node Xn, resulting from a strike on the parallel NMOS transistors in the first gate is shown for an LET of 6 MeV·cm^2/mg. The output of the fourth gate, node Y, is shown in (c). The transients produced at X and Xn are not able to propagate to the output of the fourth gate. Similar results are shown in (d) and (e) for an LET of 60 MeV·cm^2/mg.

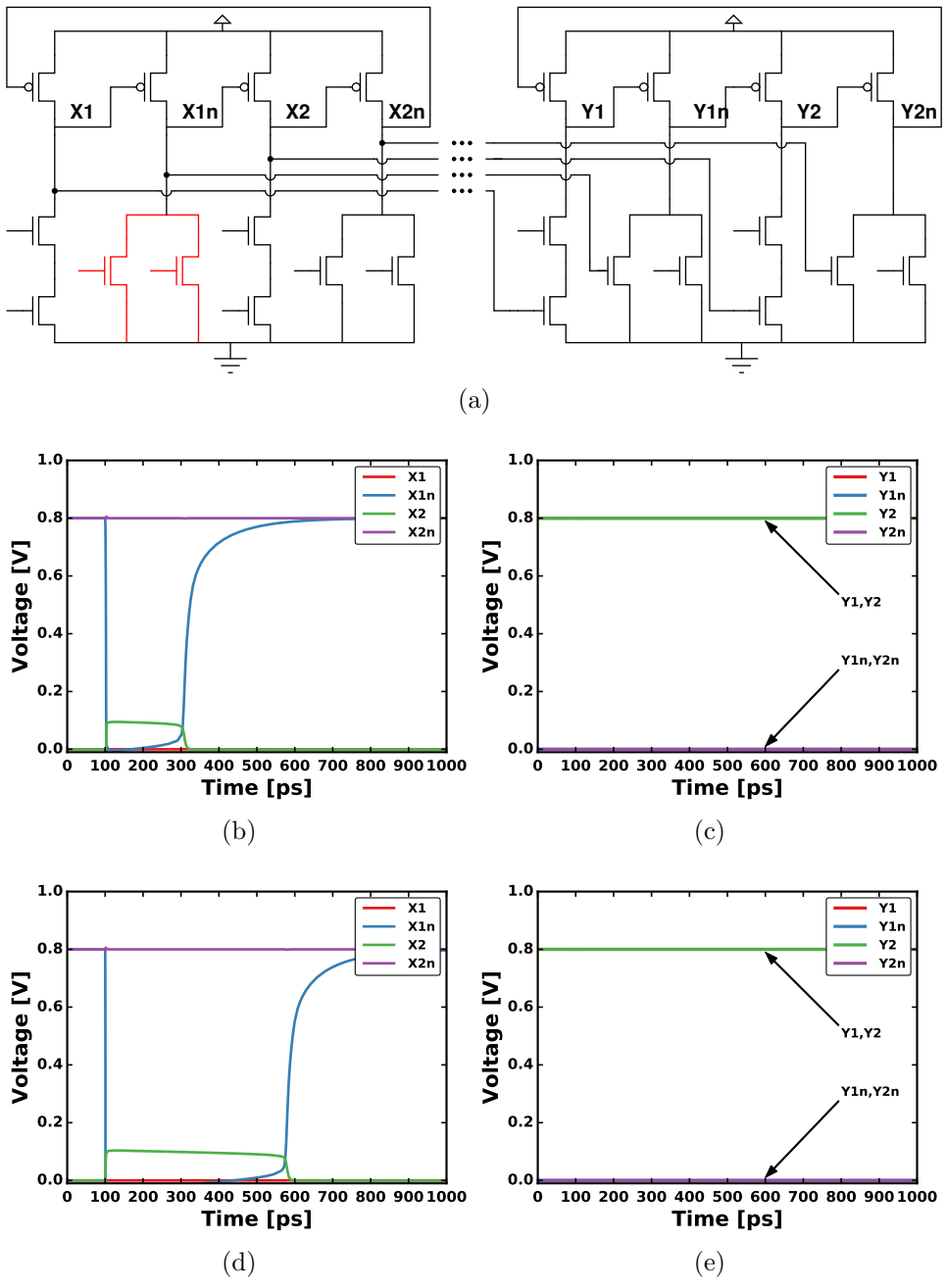


Figure 27: SEE simulation results for a single-node strike in a DIL NAND chain, shown schematically in (a), using the 16nm/14nm SEE model with an LET of 6 MeV·cm^2/mg and 60 MeV·cm^2/mg [13]. In (b) the voltage at all of the outputs (X1, X1n, X2, X2n) resulting from a strike on one set of parallel NMOS transistors in the first gate are shown for an LET of 6 MeV·cm^2/mg. The voltage at the outputs (Y1, Y1n, Y2, Y2n) of the fourth gate are shown in (c). The transients produced at X1n and X2 are not able to propagate to the output of the fourth gate. Similar results are shown in (d) and (e) for an LET of 60 MeV·cm^2/mg.

intended to simulate charge sharing from a normally incident strike. Both an LET of 4.6 MeV·cm^2/mg and 60 MeV·cm^2/mg were used for simulation purposes; however, it is the 4.6 MeV·cm^2/mg results that correspond directly to the heavy-ion data in a subsequent section. Fig. 28 shows the simulated results of a dual-node strike in the CVSL NAND gate. Full-rail transients are generated at both of the struck nodes in the first gate. As these transients propagate along the chain they are not masked by the CVSL gates. By the time the SET generated in the first gate propagates to the fourth gate, it has transformed into a signal that is unrecognizable from a standard digital signal. Thus a dual-node strike in CVSL is capable of producing a transient that has indefinite propagation characteristics. Fig. 29 shows the simulated results of a dual-node strike in the DIL NAND gate. Similar to the CVSL gate, full-rail transients are produced at two of the outputs of the first gate. However, unlike CVSL, these transients are masked by the built-in redundancy of the DIL topology. As seen in Fig. 29, the outputs of the fourth gate remain unchanged even when exposed to a dual-node strike. Similar simulations were performed for all iterations of dual-node strike combinations. There was no combination in which the DIL gate produced at transient that was able to propagate indefinitely. The results in Figs. 28 and 29 are indicative of all strike combinations; however, they were primarily chosen in order to coordinate with the heavy-ion results.

Experimental Setup

A test chip with on-chip SET pulse measurement circuitry was designed and fabricated at the 16nm/14nm bulk finFET technology generation. Test ICs were tested both electrically and in heavy-ion broad-beam. Details of the test chip design

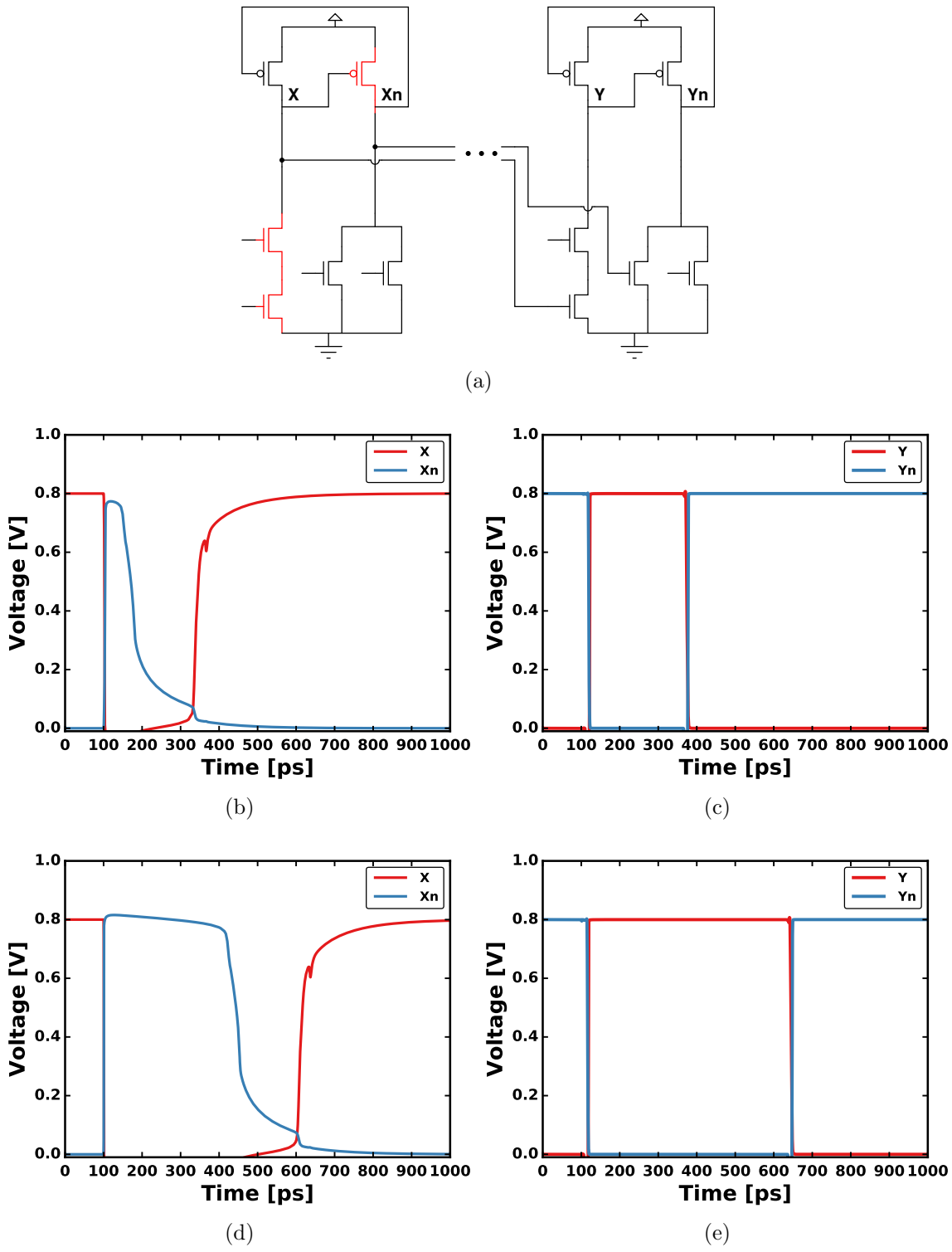


Figure 28: SET simulation results for a standard CVSL NAND chain (a) using the 16nm/14nm bias dependent SEE model with an LET of 4.6 MeV·cm^2/mg [27, 14]. Shown in (b) are simulated voltages at nodes X and Xn, resulting from a simultaneous dual-node strike in the first gate. The voltages at nodes Y and Yn of the fourth gate are depicted in (c). As shown by the simulated outputs, the SET produced at X and Xn is able to propagate to both outputs of the fourth gate.

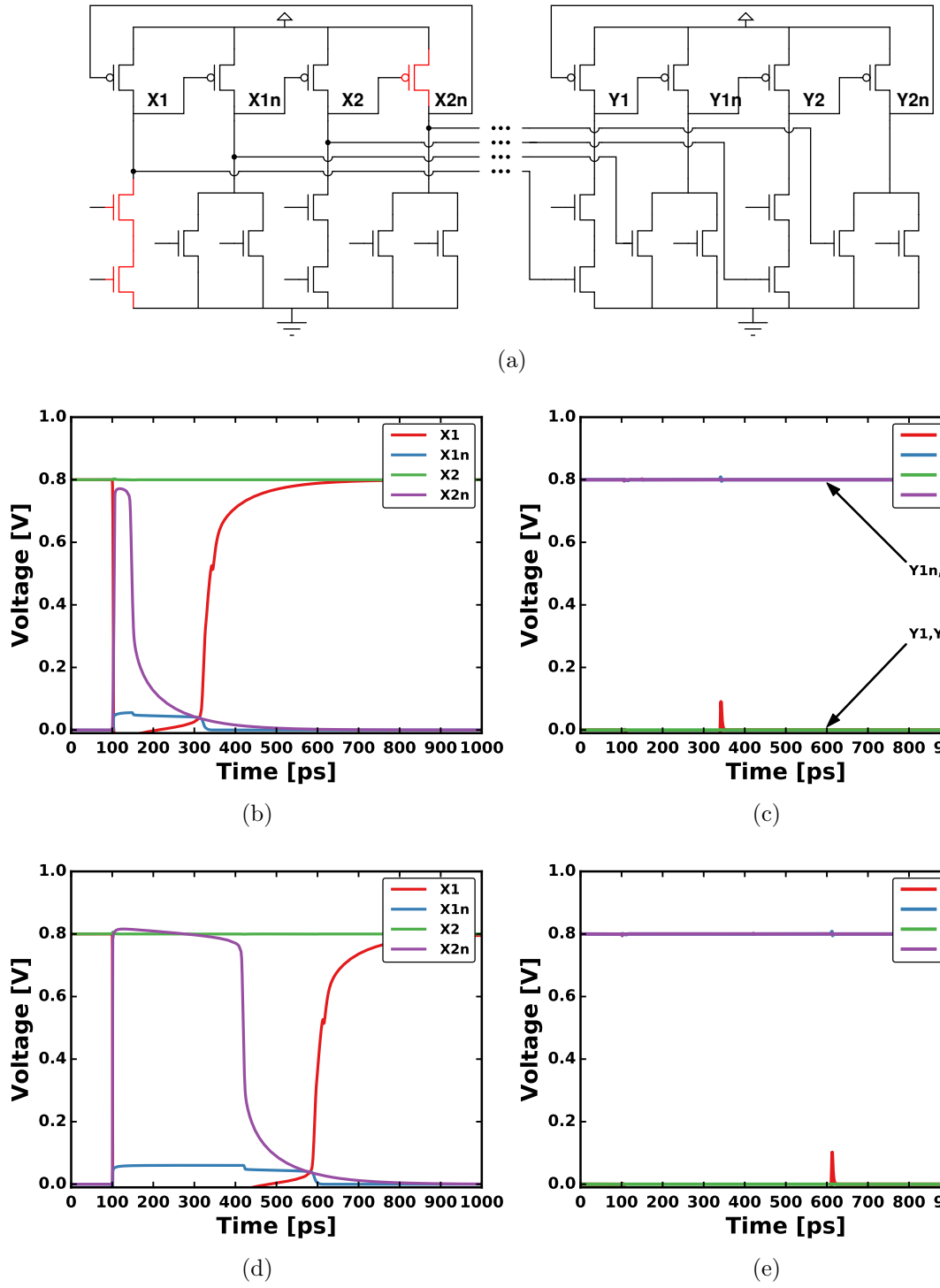
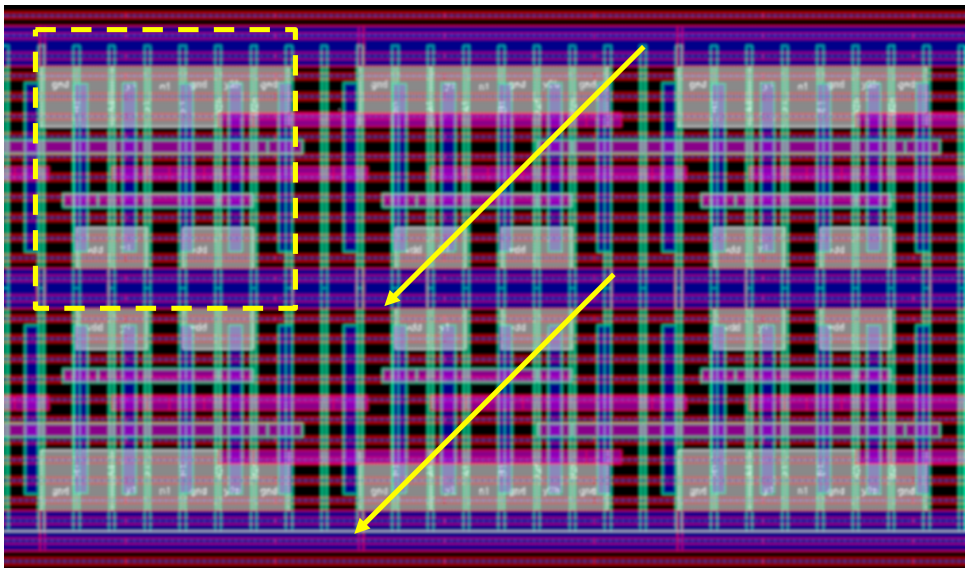


Figure 29: SET simulation results for a DIL NAND chain (a) using the 16nm/14nm bias dependent SEE model with an LET of 4.6 MeV·cm^2/mg [27, 14]. Shown in (b) are simulated voltages at struck nodes X1 and X2n and unstruck nodes X1n and X2. Simulated voltages at all of the output nodes of the fourth gate (i.e., Y1, Y1n, Y2, Y2n) are shown in (c). Due to the use of the DIL hardening technique, the SET produced in the first gate is not able to propagate to the fourth gate.

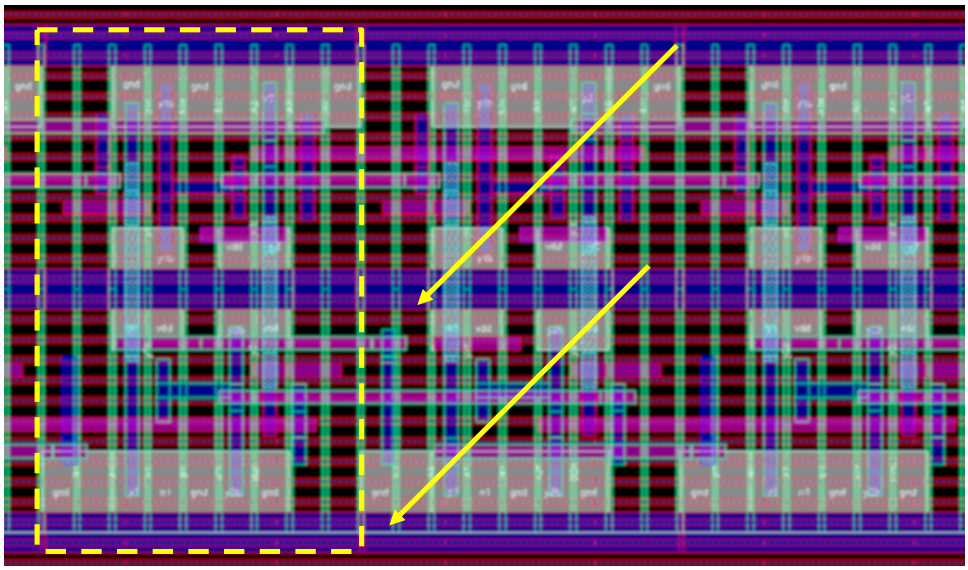
methodologies are discussed in Chapter A. As relevant to this work, the target circuitry includes chains of 2-input CVSL NAND gates, 2-input DIL NAND gates, as well as several static inverter designs. To ensure electrical functionality, pulses of known width were injected into the inverter and DIL chains using an on-chip pulse generator and successfully measured using on-chip pulse capture circuitry. The test structures were irradiated using Lawrence Berkeley National Labs 88" cyclotron with 16 MeV/u Si ions (LET @ 0° = 4.6 MeV·cm^2/mg) at both normal incidence and at 80° tilt with a range of roll angles. Irradiations were carried out at room temperature, nominal supply voltage (0.8 V) and to a minimum fluence of 1x10^8 ion/cm^2. Approximately 30 to 50 transients were recorded for the CVSL chain in each run. At normal incidence, the ion passes through only one sensitive node in each topology. Since the DUT was elevated above the surface of the package and bond-wires were only present on two sides, very high tilt angles were possible. At high tilt angles it is possible for a single ion to pass through multiple nodes. A tilt angle of 80° was chosen in order to ensure a dual-node strike in both the DIL and CVSL chains, corresponding to the two struck nodes in the SE simulations presented in 28 and 29. The 16 MeV/u cocktail at LBNL was chosen in order to ensure that the ions had enough penetration depth to pass through the back-end-of-line material and both nodes in the logic gates. Si ions were chosen for this test, which have a max range of 274 µm in silicon.

Heavy-Ion Results and Discussion

In order to make a fair comparison, the CVSL and DIL gates, shown in Fig. 30, have very similar physical layouts and node spacing, the main difference being in



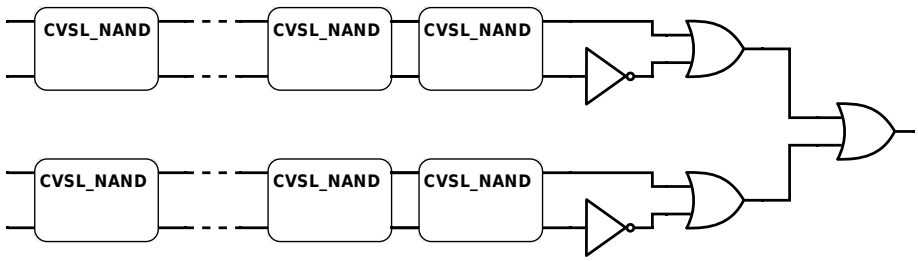
(a)



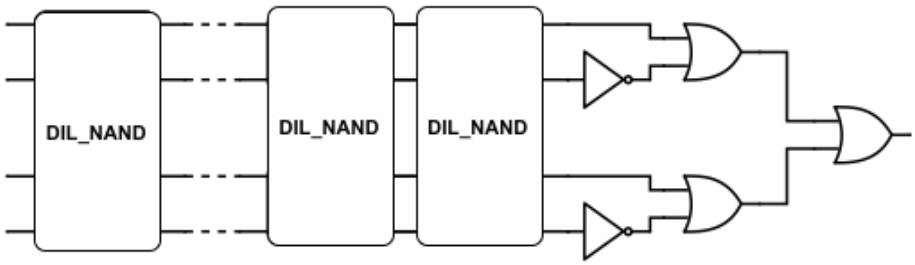
(b)

Figure 30: The physical layout of a portion of the CVSL NAND2 target chain and b.) DIL NAND2 target chain. The dashed boxes represent one logic gate cell. The arrows indicate a roll orientation of 45°.

their wiring configurations. Since both DIL and CVSL produce differential signals, standard static CMOS logic had to be incorporated at the output of each CVSL/DIL chain in order to combine their differential output into a single-ended output for the on-chip measurement circuit. An alternative approach would be to send each output



(a)



(b)

Figure 31: The schematic diagram of the a.) CVSL NAND2 target chains and b.) DIL NAND2 target chain. Combinational CMOS logic was incorporated at the end of the chains in order to combine the differential outputs into a single-end output for the on-chip pulse capture circuit. The logic was selected such that a perturbation on any one of the output lines of the CVSL or DIL gates would be captured (i.e. no logical masking).

to a separate measurement circuit, but space and input/output limitations restricted this configuration. The schematic for each logic chain along with the combining logic is shown in Fig. 31. The contribution of SETs from the static CMOS logic at the end of the DIL and CVSL chains are indistinguishable from SETs generated within the DIL and CVSL gates themselves, thus making it difficult to draw conclusions from looking at each chain independently. However, by comparing the DIL and CVSL chains to an all-static logic target structure (i.e., inverter chain), it is possible to identify additional sensitivities. At normal incidence all three logic topologies should be similar in cross section since the standard CMOS is single-node sensitive. At a tilt angle of 80°, the CVSL chain should show increased cross section over normal

incidence since it is sensitive to dual-node strikes, and the DIL chain should not change in cross section.

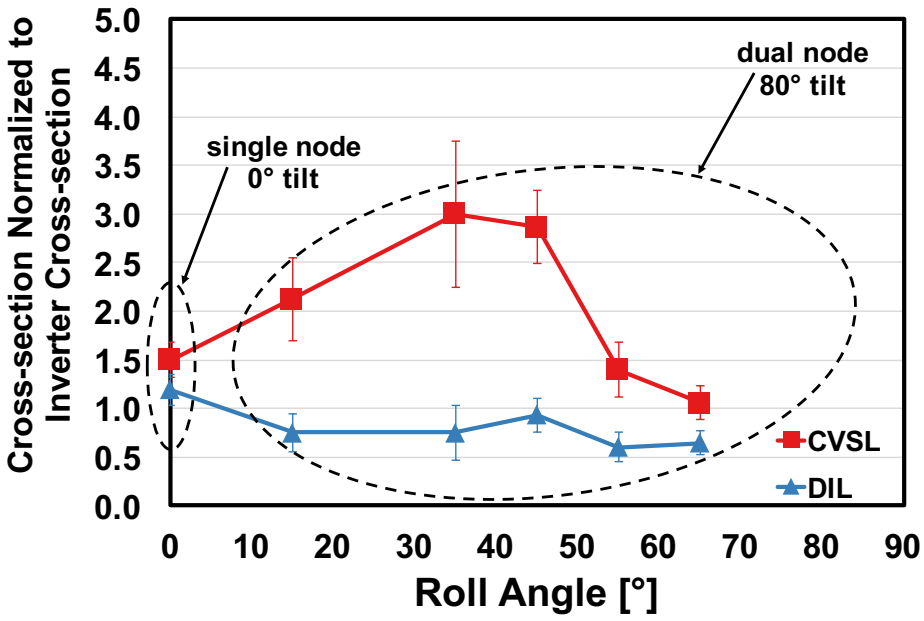


Figure 32: CVSL and DIL heavy-ion irradiation results using 16 MeV/u Si ions (LET @ 0° = 4.6 MeV·cm^2/mg). Cross-section is calculated per gate. At normal incidence both the CVSL and DIL chains are close to 1, meaning that their cross sections are similar to a standard inverter chain. The data at normal incidence are believed to have originated from the CMOS logic at the end of the CVSL and DIL chains. At 80° tilt and 15° to 45° roll, the CVSL cross section begins to increase with respect to a standard inverter chain while the DIL chain remains flat. The increased cross section over the standard inverter is attributed to the CVSL chain exhibiting dual node sensitivity. The DIL chain does not have dual-node sensitivity.

Fig. 32 shows the heavy-ion cross section, as calculated from the distributions in Fig. 33, for each target structure. A cross section per gate was first calculated by dividing the total error count for each target by the fluence and the number of known single-node sensitive gates. The CVSL chain has 11 single-node sensitive gates, DIL has 8, and the CMOS inverter chain has 22. The cross-section ratio, shown in Fig. 32, was calculated by dividing the CVSL and DIL cross section by the CMOS inverter

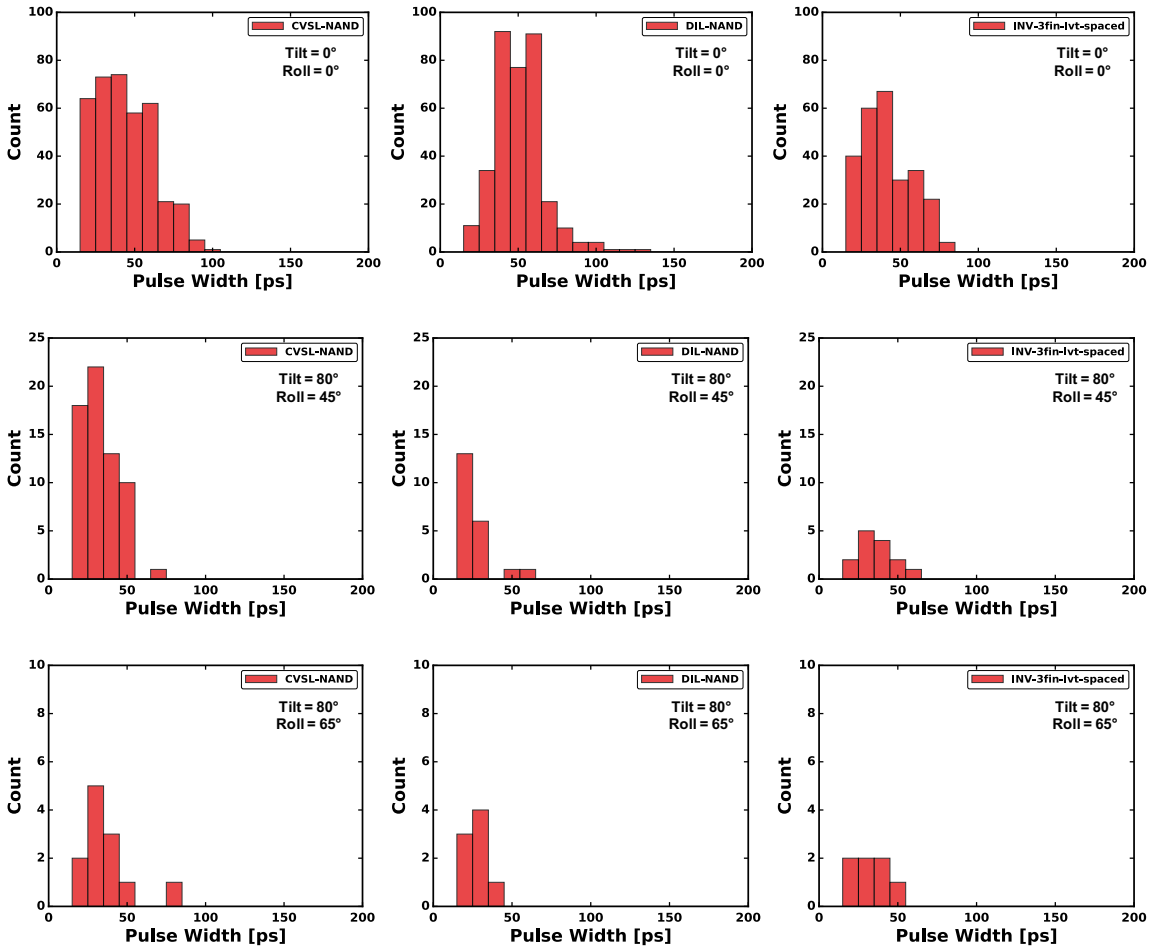


Figure 33: CVSL, DIL and inverter heavy-ion distributions using 16 MeV/u Si ions (LET @ 0° = 4.6 MeV·cm^2/mg).The greatest number of events was measured at 0° roll and 0° tilt. As the tilt increases to 80° and the roll angle increases, the total number of events generally decreases. However, the CVSL gate exhibits a particularly higher sensitivity compared to the DIL and CMOS gates at 80° till and 45° roll. This increased sensitivity is due to dual-node sensitivity in the CVSL gate that is not exhibited in the DIL gate.

cross section.

Data from all chains were measured simultaneously thus exposing all chains to the exact same experimental conditions (i.e. temperature, voltage, fluence, etc.). The chains were irradiated at normal incidence and at tilt angle of 80° across roll angles of 15°, 35°, 45°, 55° and 65°. The normal incidence irradiation was performed to evaluate the single-node sensitivity of each gate, and the 80° tilt irradiation was performed to evaluate the dual-node sensitivity of each gate. The arrows imposed on the physical layouts in Fig. 30 correspond to a 45° roll orientation, showing the worst-case dual-node strike targeted during irradiation. The cross section for the CVSL is expected to peak around 45° roll since the ions will have the longest path through the two nodes at this roll angle.

At normal incidence both the CVSL and DIL chains are close to 1, meaning that their cross sections are the same as a standard inverter chain. It is assumed based on these data and simulations that the majority of the measured SETs at normal incidence are from the CMOS logic used at the end of each DIL/CVSL chain and not from within the DIL/CVSL chains themselves. As the irradiation moves from normal incidence to 80° tilt and 15° to 65° roll, the ions are capable of passing through multiple nodes as shown in Fig. 30. At this high tilt angle, the CVSL chain increases in cross section with respect to the inverter chain, while the DIL chain stays relatively constant. These data, along with the supporting simulations in figs. 28 and 29, support the conclusion that the increase in cross section observed in the CVSL chain is due to the contribution of dual-node-induced SETs generated within the CVSL gates themselves which are in addition to SETs generated in the CMOS logic at the end of the chains. The relatively flat trend of the DIL gate over angle along

with the supporting simulations in figs. 28 and 29, support the conclusion that the DIL gates are not sensitive to dual-node strikes, and that all of the SETs measured from the DIL target are due to the CMOS logic at the end of the chains.

Broader Application

Robust Synchronous System Integration

In a synchronous system consisting of combinational logic interspersed among clocked storage elements, errors may occur due to both single-event upsets (SEU) in the storage elements and SETs in the combinational logic. To protect a synchronous system against SEU, flip-flops (FF) based on DICE storage latches have been shown to be very effective against single-node strikes; however, they are still vulnerable to dual-node strikes and clock errors [28, 29]. Several different variations of the DICE FF have been developed, such as the fully-differential DICE topology [6]. It has been shown that a synchronous data transfer system (i.e. no combinational logic) utilizing the fully-differential DICE FF is not susceptible to SETs which can be generated in the transparent stages of the DICE FF [25]. However, if traditional logic topologies are utilized between the differential DICE FFs, the system becomes vulnerable to SETs. Due to the differential input/output configuration of the DIL topology, it is able to naturally integrate with a differential DICE flip-flop, shown in fig. 34, to form a synchronous system that is robust to both SETs and SEUs. The DIL topology enhances the use of the fully-differential DICE FF by providing a combinational logic structure that can be integrated alongside the fully-differential DICE FF without inducing an SET sensitivity. Due to its compatibility with DICE FFs, DIL is a

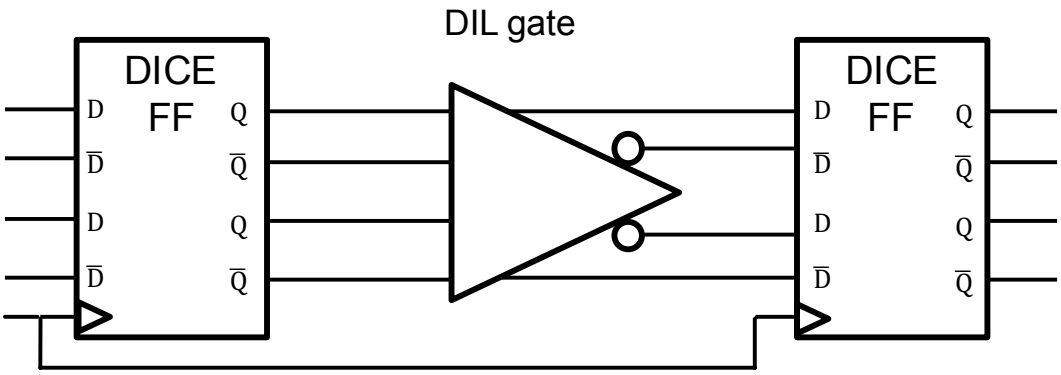


Figure 34: Example schematic showing how DIL and Differential DICE naturally integrate together.

valuable addition to existing RHBD libraries that already have a DICE design.

Power consumption is of utmost concern in modern IC designs. A highly common technique to reduce both static and dynamic power is voltage scaling. As the supply voltage is decreased, the dynamic power goes down proportional to the square of the voltage while also reducing the leakage power. The tradeoff in this case is reduced speed and noise margins. In order to circumvent the effect of the reduced speed while still maintaining low power operation, ICs can be partitioned into voltage islands,see Fig. 35, where each voltage island is operated at the lowest voltage that still allows it to meet timing requirements. Logic signals that traverse from one voltage island to another must have their voltage level translated using a voltage level shifter in order to prevent static current flow that can arise when a low voltage gate cannot fully turn on a high voltage gate. This research has investigated the radiation vulnerabilities that arise when utilizing voltage island partitioning; however, there are numerous low power techniques, as described in Chap. II, that may present their own unique radiation vulnerabilities. This chapter will first analyze the effect of voltage level shifters on both the production and propagation of SETs, and it will conclude with

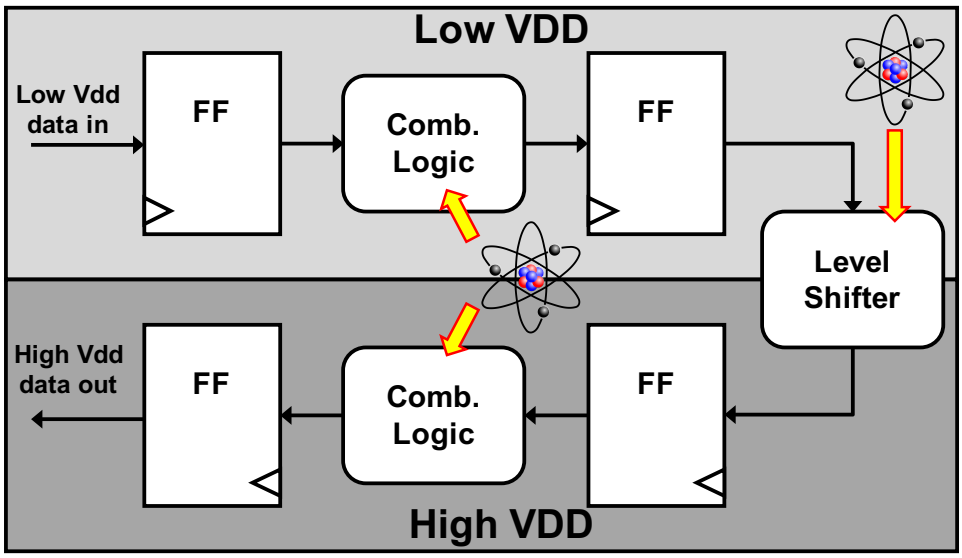


Figure 35: Simplified diagram of a voltage-island-partitioned IC.

an analysis of SETs and their mitigation in low voltage domains.

Voltage Level Shifters in Voltage Partitioned ICs

When utilizing voltage island partitioning, logic signals that traverse from one voltage island to another must have their voltage level translated using a voltage level shifter in order to prevent static current flow that can arise when a low voltage gate cannot fully turn ON a high voltage gate. In this way, level shifters act as gateways of information between different voltage islands, thus making them critical components to investigate for a rad-hard system. Very little research has been published on the design of radiation hardened level shifters, and no actual broadbeam radiation data has been published on the sensitivity of level shifters. Since level shifters operate between two different voltage domains, they may exhibit unique single event vulnerabilities that are not present in other combinational logic.

The most basic level shifter topology consists of a cross-coupled PMOS pair driven

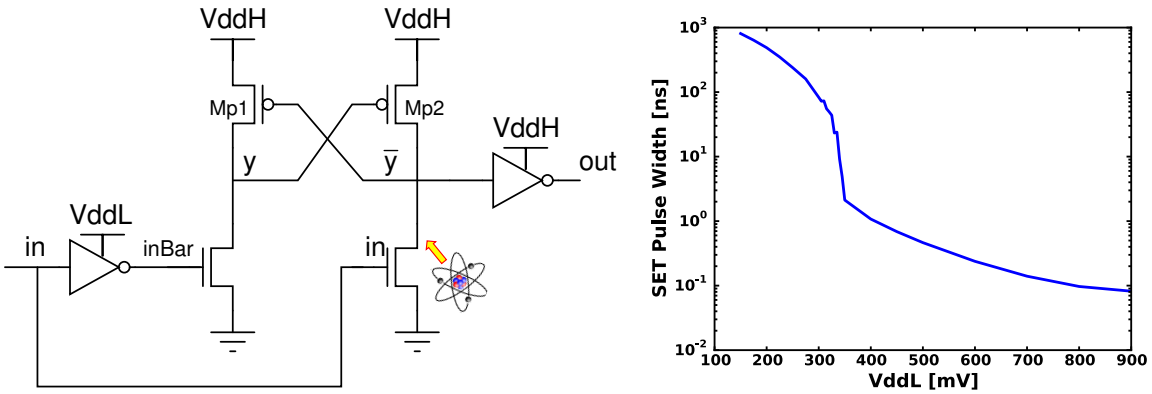
by a differential NMOS logic tree, as shown Fig. 36a. The data driving the NMOS pair originates in the low voltage domain, VddL, and may either come from previous combinational logic or a storage element. The cross-coupled PMOS pair is driven by the weakly-driven NMOS pair, but produces an output that is in the high voltage domain, VddH, due to the assistance of the cross-coupled feedback.

Several variations of the basic level shifter have been designed to improve performance parameters such as switching threshold, delay and power, but few have analyzed the radiation vulnerabilities of the various topologies, especially across a range of voltage domains. In [30], several energy efficient level shifters are proposed and thoroughly analyzed electrically, but the authors do not address single events. One paper does investigate single event effects in level shifters by calculating the critical charge for two non-hardened level shifters and one hardened level shifter at a single voltage [31]. My research expands the single-event sensitivity of level shifters by using a state-of-the-art SEE model to investigate SET duration across a range of low voltage domains as opposed to a calculating a single critical charge value at a single voltage.

The basic level shifter shown in Fig. 36a was designed in the 32nm SOI PDK. SPICE simulations show that the design is functional for a low voltage range of 350 mV to 900 mV while the high voltage domain is at 900 mV, which is nominal for the technology. The RHBD3 SEE model developed by Kauppila was used to investigate various failure modes across the full range of voltages in the low voltage domain. The simulation results from strikes to the OFF NMOS are shown in Fig. 36b. As the voltage in the low voltage domain decreases, the SET duration increases rapidly (notice the log scale for pulse width). This rapid increase is due to the fact that the

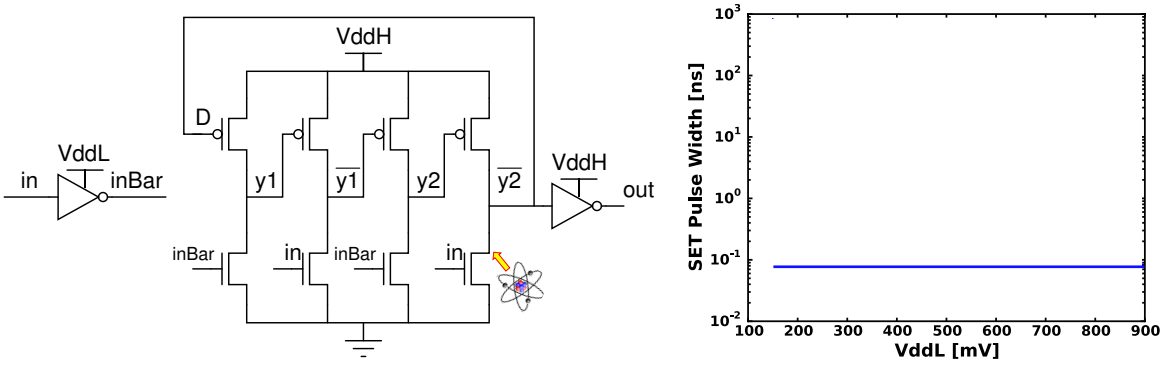
restoring current for the strike essentially comes from the weakly driven ON NMOS through the PMOS feedback. Given this sensitivity, the DIL hardening technique was applied so that the feedback dependence between the struck node and the restoring node would be interrupted.

In order to create a RHBD level shifter, DIL was applied to the traditional level shifter, as shown in Fig. 37a. This is a similar topology to the one proposed by Palakurthi *et al.* in [31], in which they proposed incorporating an entire DICE latch in place of the PMOS half latch. The design that proposed here is simpler and does not require having a full DICE latch, only a PMOS half latch. Similar simulations to Fig. 36b were performed with the hardened level shifter, and the results are shown in Fig. 37b. The interlocked feedback takes away the voltage sensitivity of the SET duration; however, a short SET is still produced at the out put for some strikes due to the design being single-ended.



(a) (b)

Figure 36: (a)Schematic of a basic level shifter topology. The data driving the NMOS pair originates in the low voltage domain, VddL. The cross-coupled PMOS pair is driven by the NMOS pair, but produces an output that is in the high voltage domain, VddH. (b) SET duration as a function of voltage for the low voltage domain when the OFF NMOS is struck with an LET of 60 MeV·cm^2/mg.



(a) (b)

Figure 37: (a) Schematic of a basic level shifter topology hardened via interlock feedback in the PMOS half latch. (b) SET duration as a function of voltage for the low voltage domain when the OFF NMOS is struck with an LET of 60 MeV·cm^2/mg.

CHAPTER V

CONCLUSION

As design choices within a single technology become ever more complex with each new generation and power consumption constraints push operating voltages lower, this research provides guidance into efficient characterization and mitigation of single-event-transients in advanced technologies. This research provided significant advancements in the design of a 16nm/14nm bulk finFET technology characterization vehicle (TCV) and test infrastructure. The incorporation of variable-voltage, heterogeneous target structures and parallel Vernier Delay Line (VDL) measurement circuits were among two of the most critical design changes. Compared to previous approaches, the new TCV design is approximately 13X more efficient resulting in a significant savings in beam time costs. A vast amount of SET data was measured and analyzed at both the 32nm SOI and 16nm/14nm bulk finFET technology node across a variety of logic types, design variants, operating conditions and environmental conditions. These data provide the core base for enabling the development of accurate single-event models and effective mitigation strategies.

This research also experimentally showed that as supply voltage decreases towards near-threshold voltages, SET duration and electrical delay scale in a similar manner. Although similar in trend, SET duration and electrical delay were shown to be linked to supply voltage through different physical processes. The implication of these trends is reassuring for the use of filter-based hardening techniques at near-threshold voltages. Additionally, data showed an increase in the sensitive area of logic gates as

supply voltage decreases. Due to the increase in logic gate sensitive area at reduced supply voltages, SET filters designed for nominal supply voltage operations will not be as effective at reduced supply voltages. In order to overcome this issue, filters need to either be designed with extra margin at nominal voltage or designed with a topology whose electrical delay has a stronger voltage dependency than SET duration.

Lastly, a technology-agnostic RHBD logic topology, Dual Interlocked Logic (DIL), was developed and shown to be resilient to SET propagation even for dual-node strikes. The topology was validated at the 16nm/14nm bulk finFET generation node using both simulation and silicon hardware analyses. Similar to cascode voltage switch logic (CVSL) in form, DIL offers increased SET resiliency while still maintaining the fast characteristic switching times of modern CVSL circuits utilized in both ground-based and space-deployed applications. Compared to TMR-based SET hardening approaches, DIL offers a beneficial tradeoff in area, power and portability. Additionally, the dual-differential input/output configuration of DIL also gives it the unique ability to naturally integrate alongside differential DICE flip-flops to create a single-node-robust synchronous digital system capable of implementing any arbitrary digital function.

Appendix A

ADVANCES IN SINGLE EVENT TRANSIENT TEST CHARACTERIZATION VEHICLES

Single-event transient characterization in advanced technologies is critical to the enablement of robust single-event mitigation schemes, compact-modeling and error-rate calculations. A test characterization vehicle (TCV) is an integrated circuit which enables technology characterization by providing the physical circuitry needed to generate and measure single-event transients. In order to extract data from the TCV, there must be an infrastructure in place to distribute all of the power and data signals to and from the chip. This chapter will give an overview of TCV design along with the associated errors for measuring digital single-event transients. A detailed description will be given of the advancements in Vanderbilt's autonomous SET measurement TCV topology as it progressed from the 32nm node to the 16nm/14nm node. Lastly, advancements in the test infrastructure from the 32nm node to the 16nm/14nm node will be detailed.

Overview of TCV Designs

A single-event transient TCV is typically divided into two parts. The first part is referred to as the target circuity because its primary purpose is ion interaction and SET formation. The target circuity consists of large blocks of logic gates where each block is typically of a single type of logic. Each TCV can have multiple target

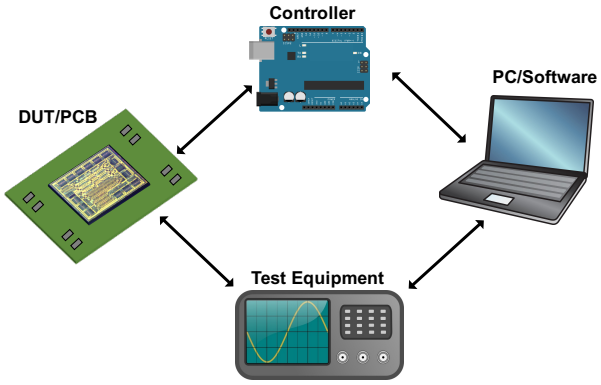


Figure 38: Generic TCV test infrastructure showing the communication channels involved in a typical setup.

circuitry blocks which are routed to either a common or sometimes multiple on-chip measurement circuits. Several topologies of on-chip measurement circuitry have been used, and they can be divided into those that only count the number of SETs generated and those that both count the number of SETs and measure their temporal duration. Vanderbilt has implemented on-chip SET duration measurement circuits in both 32nm and 16nm/14nm technologies. This research aided in the advancement of Vanderbilt's temporal measurement technique as it transitioned from the 32nm node to the 16nm/14nm node.

32nm SOI SET TCV

The measurement method used at the 32nm node is a pulse width measurement technique that was first developed by Nicoladis *et al.* in [32] and later improved upon by Narasimham *et al.* and Loveless *et al.* [33, 34]. The initial design was done by Narasimham *et al.* in [33]. The major difference between the measurement circuits of Narasimham and Loveless is that Loveless included a variable trigger delay which allowed for the characterization of error within the measurement circuit. In Fig. 39

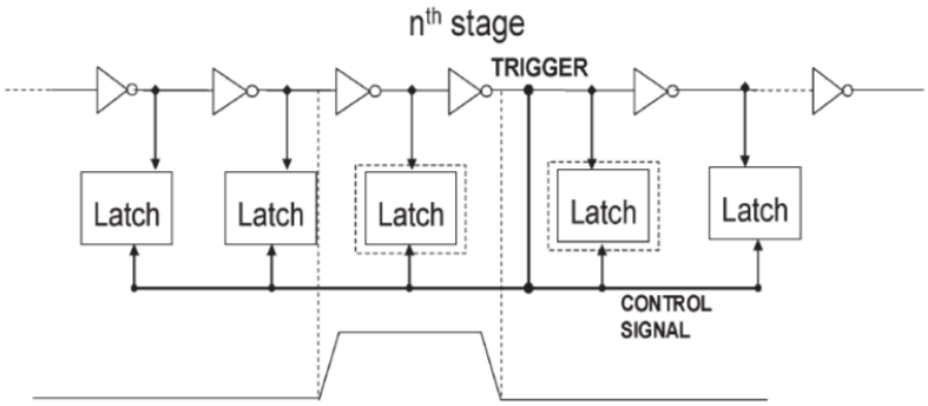


Figure 39: Basic time-to-digital-converter (TDC) schematic. This topology was the basis for the some of the first on-chip SET duration measurement circuits. The pulse width is digitized by capturing the output of a chain of delay cells while the SET is propagating along the chain. The propagation delay of each cell can be used to convert the digitized pulse width back to time. [33]

the basic schematic for the autonomous pulse capture circuit is shown.

Previous pulse capture circuits used a similar latching method as the one shown in Fig. 39; however they all used an external trigger to send a flag back to the chip in order for the pulse to be captured. Narasimham designed the pulse capture circuit to create its own self-triggered flag so that an external trigger was not necessary. This is extremely useful for heavy-ion testing in which case the timing of ion interaction with the target is impossible to know (as opposed to laser testing for example). Fig. 40 shows more detail on the function of the self-trigger. The output of the nth stage is constantly monitored. When an SET propagates through the nth stage, a trigger is formed after some delay which then sends a hold signal through a series of buffers to all the latches. If the first latch has recovered to its initial state once the SET is captured then the SET pulse width has been fully captured and the pulse width can be known to within the accuracy of the measurement circuit. However, if the SET is captured before the first latch has recovered to its initial state then the SET pulse

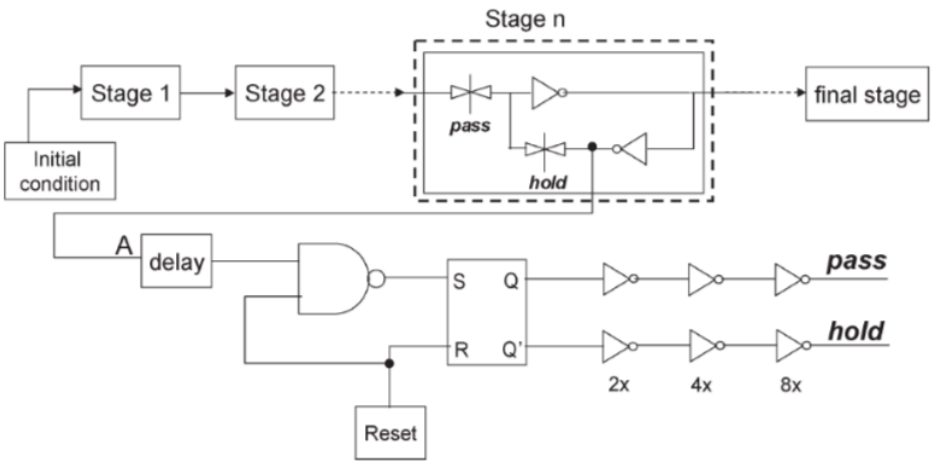


Figure 40: On-chip capture circuit first proposed by Narasimham *et al.*. [33]. This circuit was designed for use in a heavy-ion broadbeam environment by adding a self-trigger.

width cannot be fully known since it is possible that the SET was much longer than what was captured. The reason for the delay in the trigger is that the SET needs enough time to fully propagate into the pulse capture circuit.

The target circuitry, designed by Dr. Kauppila, consists of 16 different logic blocks. Most of the targets are inverter arrays with various PDK device types and layout configurations. Each chip also contains targets that are calibration structures to aid in the extraction and quantification of measurement error. Each inverter array target consists of short chains of serially connected inverters, 8-24 per chain, with the input of all of the chains connected in parallel, and the output of the chains combined using a balanced OR-gate tree. All 16 logic blocks are routed to a 16 channel analog multiplexer which allows only one target to be enabled at any given time in order to identify in which logic block the SET occurred. Selecting one target block at a time is inefficient compared to monitoring all logic blocks simultaneously.

Several advancements were incorporated in the target logic portion of this chip.

The first improvement was using short logic chains combined in parallel as opposed to one long continuous chain. SET target circuitry was traditionally organized as long chains of logic gates in order that the overall cross section of the target could be maximized. This method was expected to give a fairly accurate look at the SETs generated in a given technology. However, in 2007, Ferlet-Cavrois *et al.* observed and explained that SETs could broaden as they propagate through a chain of logic gates. This effect is called propagation-induced pulse broadening (PIPB), and it is a cumulative effect in that it is worse for long chains than it is for short ones [35]. PIPB can occur for reasons. One is that if the inverters in a chain have asymmetric drives and loads. The second reason PIPB can occur is due to MOS VT hysteresis [21]. This newly discovered effect shed doubt on the validity of previously gathered SET data that used long logic chains. It is also possible that an SET is attenuated as it propagates if it is not as long as the intrinsic rise and fall time of the logic gate [21]. In order to diminish the PIPB effect as much as possible in the 32nm chips, the target circuitry was laid out in short chains of inverters (8-12 per chain) with the input of each chain connected together and the outputs routed through the distribution network. These short chains of logic gates help to reduce the effect of PIPB on the generated SETs.

The second improvement was balancing the propagation network between the target logic and the measurement circuit. Since the target circuitry was laid out in short chains, an extensive distribution network had to be designed to bring the output of each chain of inverters to a single node in order that an SET generated in any chain could be measured. Fig. 41 shows the schematic of the distribution network which logically ORs the outputs of each chain of inverters together. There are few

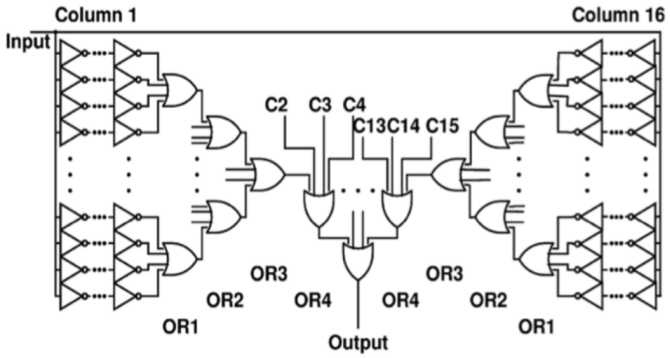


Figure 41: Schematic for the balanced OR network first used in the 32nm TCV. It is balanced because the output of OR1 in any column is laid out such that it sees the exact same RC load. The same is also true for all of the other OR gates. This balancing helps to reduce pulse skew due spatial variations.

ways in which the distribution network can contribute errors to the measurement of SETs generated in the target circuitry. The distribution network inherently gives rise to RC loading on the target circuitry. Anytime there is an RC load then there is the possibility of RC filtering. The distribution network acts as a low pass filter on the output of the target circuitry. When really short pulses (SETs) go through this filter it is possible that they will be attenuated to a shorter pulse or be completely diminished. This effect cannot be eliminated as long as a there is a distribution network. However, in order to not introduce more error, the distribution network was designed such that every inverter chain in a target has the same RC load attached to its output. This eliminates any spatial dependency due to RC attenuation since SETs from one chain are not filtered more than SETs from another chain.

The SET capture circuit also introduces error into the SET measurement. As discussed above, PIPB can alter the SET as it propagates through the target circuitry. The same is also true for the SET capture circuit. As the SET propagates into the pulse capture circuit it will experience broadening. This broadening alters the pulse

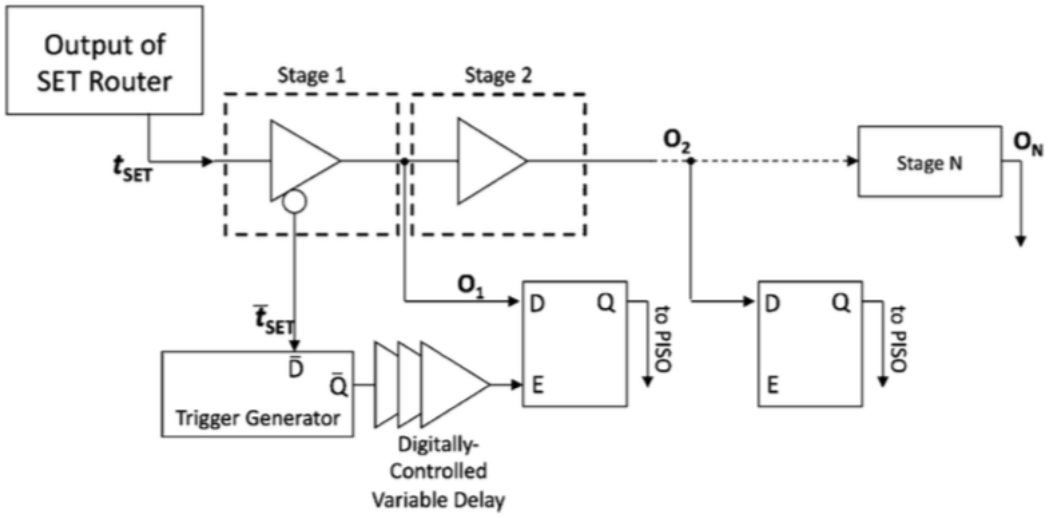


Figure 42: Enhanced version of the on-chip capture circuit first proposed Loveless *et al.*. [34]. A digitally-controlled variable trigger was added in order to extract skew due to the propagation of the SET in the capture circuit.

width and causes the capture circuit to incorrectly measure the generated SET. In order to quantify this error, the delay trigger of the measurement circuit was designed with a selectable delay [34]. By making this delay a variable delay, as shown in Fig. 42, the SET is able to be captured in different segments of the pulse capture circuit. This variable delay allows error introduced by the SET propagating deep into the measurement circuit to be quantified, as shown in Fig. 43.

Proper calibration of TCVs is for critical measuring reliable data. For calibration, a built-in-self-test (BIST) using a pulse generator was also included on the 32nm TCV. Sending in pulses on the order of tens of picoseconds is practically impossible to do off-chip due to parasitic capacitance, inductance and resistance. However, with an on-chip pulse generator this is possible. The 32nm TCV was designed with on on-chip fast pulse generator that can produce pulses between 100 ps and 750 ps. The pulse-generator produces a pulse that is injected at the input of the target

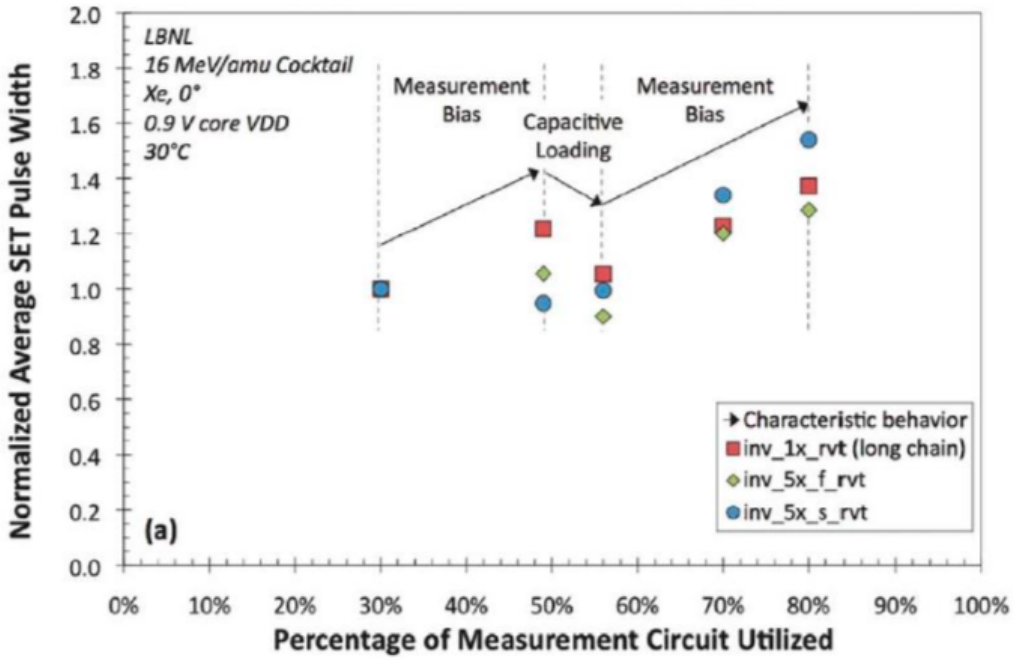


Figure 43: Impact of propagation skew on the average SET pulse width.

circuitry. The injected pulse is captured by the on-chip measurement circuit, and the measured duration is compared to the duration of the injected pulses. This capability allows for functional electrical verification as well as the quantification of measurement uncertainty.

In summary, the 32nm TCV incorporated many improvements over previous designs including short logic chains, a balanced OR network, on-chip pulse generator and a variable delay for the pulse capture circuit. Although much improved, the 32nm TCV did have some limitations. One limitation is that only one type of logic could be measured at each time. This is highly inefficient since it essentially multiplies the test matrix by a factor equal to the number of logic types. The other limitation is with the pulse measurement circuit. Although, the 32nm pulse measurement circuit included many advancements, the traditional TDC topology that it is based on is inferior

to other TDC topologies such as the Vernier Delay Line (VDL) TDC in terms of resolution and propagation induced skew. The limitations above were targeted as advancements during the design of the 16nm/14nm TCV.

16nm/14nm bulk FinFET TCV

J.S. Kauppila, J.A. Maharrey, R.C. Harrington, T.D. Haeffner, P. Nsengiyumva, D.R. Ball, A.L. Sternberg, E.X. Zhang, B.L. Bhuva and L.W. Massengill. "Exploiting parallelism and heterogeneity in a radiation effects test vehicle for efficient single-event characterization of nanoscale circuits," *IEEE Transactions on Nuclear Science*, Vol. 65, no. 1, pp.486-494, Jan. 2018. [36]

The bulk FinFET TCV, designed and fabricated for this work, was developed with an emphasis on testing multiple combinational logic cells and flip-flop shift registers over bias, angle of incidence, and heavy-ion linear energy transfer (LET) values. The TCV was constrained to a chip size of 1 mm^2 and 22-23 I/O pads per side for data signals, power, and ground. To achieve the capability of irradiating the TCV with high angles of incidence, up to 85° tilt from normal incidence, the chip was further constrained by limiting I/O pad placement to only the top and right side of the TCV to allow for high angle testing from the left and bottom side of the die, avoiding shadowing from bond pads and bond wires, which resulted in a final design with only 45 I/O pads on the die. Additional constraints on sample availability and testing resources required the TCV to be designed with the goal of efficient utilization of

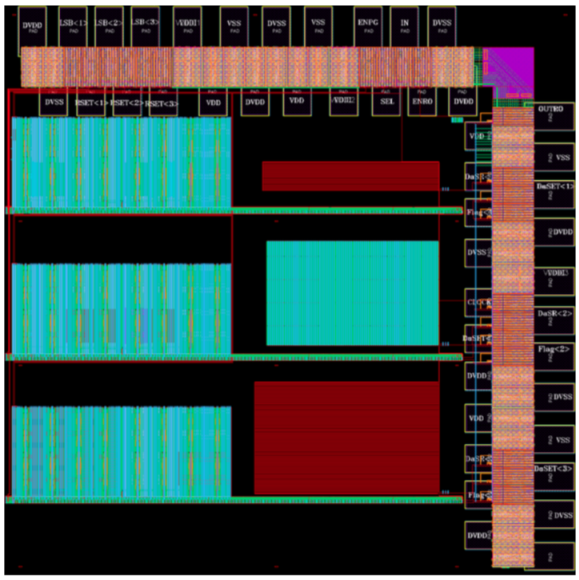


Figure 44: Physical layout of the 16nm/14nm TCV. I/O pad were only included on 2 sides in order to allow grazing angle strikes on the non-bonded sides.

beam resources, which was a significant driver for the architecture-level design process. These design constraints led to the development of a novel heterogeneous SET target design and the use of parallelization, where each target is connected to a measurement circuit that operates simultaneously and independently. The bulk FinFET TCV was fabricated in a commercial process at the 16nm/14nm node.

A top-level layout floorplan view of the TCV is shown in Fig. 44. The TCV design includes three combinational logic SET targets, three flip-flop shift register designs, and a ring oscillator for calibration of SET pulse-width measurement circuits and parasitics. The SET target circuits utilize a novel heterogeneous logic cell topology with one measurement circuit per target. Additionally, the SET targets were developed to operate with a variable supply voltage for the combinational logic and a constant supply voltage for the SET propagation network and measurement circuit, which provides the capability of multiple bias characterization of SETs in the combinational logic while maintaining a single calibration point for the SET

propagation and measurement circuits. The heterogeneous logic in the target design and parallel operation of the SET measurement circuits provide an anticipated 12X beam utilization improvement compared to similar TCV test campaigns that utilized multiplexed SET targets and one measurement circuit [34, 18, 37]. The addition of the shift registers, which can be tested and measured in parallel with the SET targets, provides an increased test efficiency for the TCV of 13X; while shift registers are traditionally tested in parallel, they are often implemented on a separate chip or in a separate test domain [38]. Table 6 provides a list of the combinational logic variants, design parameters, and cell counts included across the three SET targets. In addition to the combinational logic cells in the SET targets, three flip-flop variants are tested in the shift registers, which cover an unhardened design and two variants of radiation hardened by design (RHBD) approaches.

SET Target and Propagation Network Overview

Previous SET target and measurement circuit implementations have included a single target for each of the combinational logic cells to be characterized and a method to propagate the SET to the target output, either using a single long chain of logic or multiple short chains and an OR-gate network. Each target is tested one at a time, where the target output is directly connected, or multiple target outputs may be multiplexed and connected, to one or more SET measurement circuits [34, 18, 37]. However, the chip area constraint of this TCV prevented the use of multiple full targets for each combinational logic type. Therefore, a new heterogeneous or mixed logic SET target design has been developed. Additionally, the specifications for characterizing the technology required SET testing of the

Table 6: Description of target logic included on the 16nm/14nm TCV. The 6 fin devices were physically designed with 2 fingers having 3 fins each.

Logic Cell	**# Fins**	**Threshold Voltage**	**Spacing**	**# Cells**	**Supply Voltage**
inverter	3	low	min	17,408	0.45 to 0.80 V
inverter	6	low	min	13,312,	0.45 to 0.80 V
inverter	3	regular	4X	11,264	0.45 to 0.80 V
inverter	3	low	4X	11,264	0.45 to 0.80 V
level shifter	n/a	regular	min	1,536	0.45 to 0.80 V
NAND	3	low	min	13,312	0.45 to 0.80 V
NOR-NAND	n/a	low	min	13,312	0.45 to 0.80 V
NAND-NOR	n/a	low	min	13,312	0.45 to 0.80 V
DIL NAND	n/a	regular	min	8,704	0.45 to 0.80 V
CVSL NAND	n/a	regular	min	17,408	0.45 to 0.80 V
NAND	3	regular	min	13,312	0.45 to 0.80 V
inverter	6	low	4X	10,240	0.45 to 0.80 V

combinational logic cells at VDD voltages from 0.45V to 0.8V. This TCV includes a methodology to provide a variable VDD supply to the combinational logic chains in the target. However, to minimize supply voltage induced skew during propagation of the SET to the measurement circuit, the OR-gate based propagation network and the SET measurement circuit have been designed to always operate at the nominal VDD voltage of 0.8V, minimizing skew and eliminating recalibration at each of the tested variable VDD values.

The architecture of the combinational logic SET targets builds upon the methods

presented in [34] and [18], which utilize many short chains of combinational logic cells to minimize propagation induced skew [15],[22], where the outputs of the short chains are combined to a single target output using an OR-gate network. New target design methodologies, developed in this work, provide the capability to utilize a heterogeneous mix of logic chains in one target with traceability to the logic type in which the SET originated. This new method is a top-level architectural change compared to the work of [34] and [18]. Additionally, the separation of the supply voltage of the combinational logic chains from the OR-gate propagation network and the measurement circuit provides a new capability, which required topology changes in the short logic chains and a top-level architecture change to the SET target design.

Heterogeneous Combinational Logic Target Design

The SET target design in this work contains sixteen columns of combinational logic chains. Each column contains 128 short chains of combinational logic cells whose outputs are combined using an OR-gate network, which connects the short chains into a combined output for each of the columns, as illustrated by Column 1 with the output C1 in Fig. 45. In this design, neighboring columns have been designed to contain identical combinational logic types. As shown in Fig. 45, the neighboring column outputs, C1 and C2, are combined with OR gates to create a single output for the column pair, C1 OR C2. The output of each column pair is connected to a resettable DICE-based latch, which flips from 0 to 1 if a SET as short as 15 ps appears at the output of the column pair, denoted as C12Flag in Fig. 45. The DICE-based latch transitions from 0 (reset) to 1 (VDD) when a high logic state input appears at the enable input (EN). In this design, the SET signal is applied to the enable input

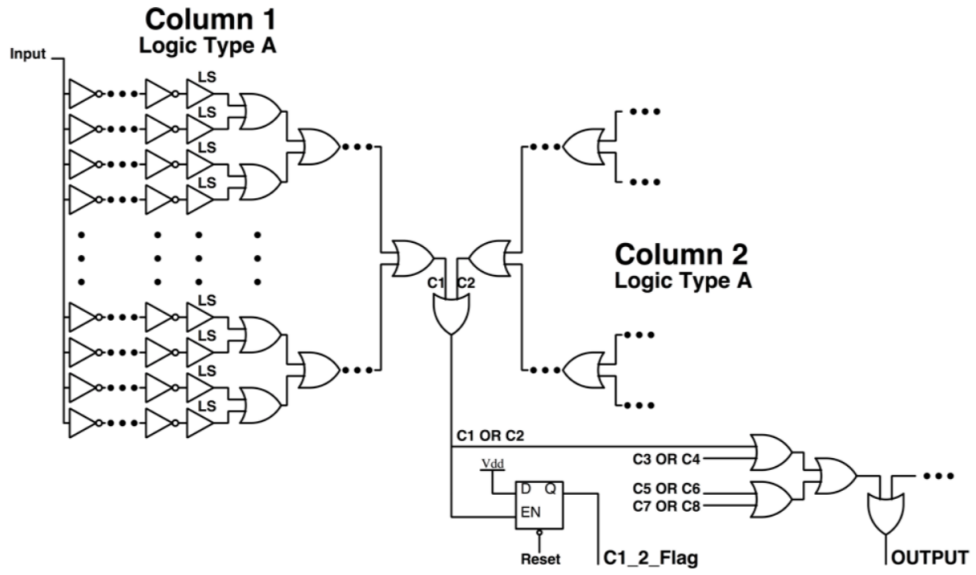


Figure 45: Propagation network for the 16nm/14nm TCV. Level shifters were inserted at the end of the logic chains. A DICE latch was inserted to flag which logic structure the SET originated in.

allowing the data input (D), which is tied to a logic high signal (VDD), to pass to the output (Q). The eight latch outputs in the full target are included as an 8-bit header in the serially output digital word, which also contains the digitized SET pulse width measurement. This 8-bit header serves as a tag address to identify the column pair from which the SET originated and propagated to the pulse-width measurement circuit. The development of this novel column tagging methodology enabled the use of heterogeneous combinational logic cell chains across different column pair sets, thus utilizing heterogeneity within the target design to gain parallelism. The column pair outputs are also combined with an OR-gate network to generate a single target output, as shown in Fig. 45.

To ensure significant statistics across all of the logic variants during each heavy-ion exposure, this TCV implementation included sets of four columns in the target that utilized the same combinational logic chain cells, resulting in a total of 12 logic cell

types characterized across the three targets on the TCV. The SET origination flags were set by pairing columns, maintaining the 8-bit header as previously described. Theoretically, this heterogeneous SET target design methodology can utilize different logic chain types in each column, where the output of each column would be connected to a latch to track the SET origination point. However, the ability to efficiently gather significant statistics across all logic variants during testing should be considered.

If two or more simultaneous SETs occur within one target, but different logic types, the output word would contain multiple column flags set to 1. In the event of multiple column flags equal to 1 or all column flags equal to 0, a case that could occur if the SET is generated in the OR-gate propagation network downstream from the column-pair combination or within the SET measurement circuit input, the resulting output from the measurement circuit will be stored and labeled as invalid. The data is considered invalid because the specific origin of the SET pulse, that is the originating column pair, cannot be determined. The invalid data outputs are tracked to ensure they do not have a statistically significant impact on the measured results.

Variable Supply Voltage Combinational Logic Chains

The short combinational logic chains utilized in the SET target are connected to a variable supply voltage and include a voltage level shifter between the short chain output and the OR-gate propagation network, which is enabled by breaking the VDD supply rail and N-well between the combinational logic chain and level shifter. This topology change required the addition of well contacts dedicated to the variable supply voltage chain, in addition to the well contact for the nominal supply voltage, which is connected to the level shifter. The introduction of the level shifter circuit between

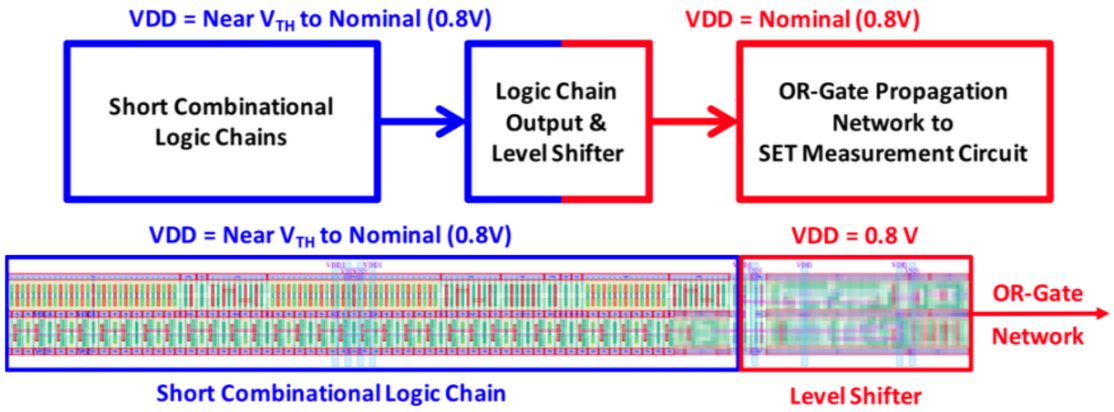


Figure 46: Simplified representation of the separate voltage domains implemented in the target. The logic chains operate in an independent variable voltage domain, while the rest of the TCV operates at nominal voltage. A voltage level shifter was inserted to transition the logic signal from the low voltage domain to the high voltage domain.

the short chains and the propagation network is also noted by the buffer circuit symbol with the label LS in Fig. 45. A notional diagram and annotated layout of a combinational logic chain and level shifter, with the voltage partitions highlighted, is shown in Fig. 46. As previously noted, the OR-gate propagation network and the on-chip measurement circuit run at the nominal supply voltage to minimize the need for re-calibration at each of the tested supply voltages.

Autonomous SET Measurement Circuit Design

The autonomous SET pulse-width measurement circuit on this TCV was implemented using the Vernier Delay Line (VDL) topology similar to the design presented in [37, 38, 39]. The measurement circuit on this TCV is capable of capturing pulse widths as short as 15 ps with a 10 ps per bin resolution. The maximum measurable pulse width is approximately 2.3 ns. A schematic of the VDL measurement circuit implemented on this TCV is shown in Fig. 47.

As presented in [37, 38, 39], the arrival of the SET pulse produces two, delayed,

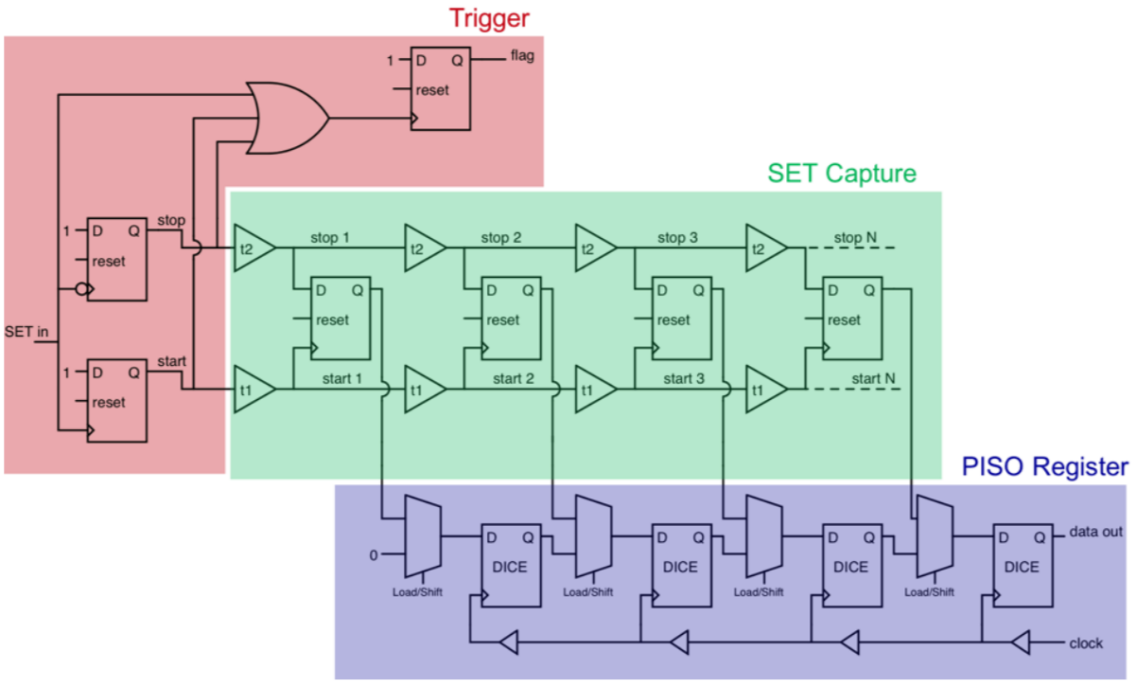


Figure 47: Schematic diagram of the Vernier Delay Line (VDL) implemented on the 16nm/14nm TCV.

rising-edge signals. The rising edge of the SET pulse produces the start signal, and the falling edge of the SET pulse produces the stop signal. The SET pulse width is encoded in the initial delay between start and stop signals. The signals propagate through two delay chains, where the per stage delay is for the start signal (t1) is larger than the delay for the stop signal (t2). For this design, the t1 delay is twice that of the t2 delay. The stop signal, corresponding to the falling edge of the SET pulse, propagates through the chain with less per-stage delay and advances on the start signal by (t1 - t2) per stage with respect to the edge on chain t1. The number of stages required for the stop signal to surpass the start signal provides the digital measurement of the SET pulse width with a precision of (t1 − t2). The enhanced resolution of the VDL approach, which is not directly limited by combinational gate delay, provides the capability to measure very short pulse widths [37, 15]. If very fine

resolution measurements are needed, the logic cells for t1 and t2 may be designed to have a variable delay (e.g. current-starved inverters).

A few pitfalls lurk in the proper design of a VDL. For the start and stop trigger flip flops, it is critical that they have identical clk-to-Q delays, otherwise measurement skew can be introduced. The skew introduced by this difference will show up as a constant addition or subtraction from the true pulse width. The flip-flops used in SET capture portion of the VDL, see Fig. 47, may also introduce skew. For the data in the SET capture flip flops to change, the stop signal must surpass the start signal by at least the setup time of the flip flops. If the setup time is much less than the VDL resolution, (t1 - t2), the effect may be masked and not cause any offset in the data. However, this is not the case if the setup time is commensurate with or greater than the VDL resolution, (t1 - t2). For this case, the setup time will be added to the true pulse width. If the setup time for each flip-flop is the same, which is a good assumption given their proximity to each other, the addition will be constant. With proper calibration, such as on-chip pulse injection, constant offsets can easily be extracted out of the final data.

When a transient pulse arrives at the measurement circuit, the trigger circuit signals the external controller that a transient is being measured. The external controller then signals the on-chip measurement circuit to serially shift out the digital tags for the column pairs and the contents of the DICE-based PISO shift register. The digital representation of the pulse width is a string of 0s followed by all 1s and the pulse width corresponds to the bin where the 0 to 1 transition occurs. The output word is inherently resistant to SEU within the digitized pulse width measurement, because an SEU will appear as a bubble in the code, unless it occurs at the 0 to 1

transition. This is a significant improvement over on-chip measurement techniques that capture the pulse with a series of alternating 1s and 0s or even a pulse captured as all 1s in the output word [37, 33]. The 8-bit digital word from the heterogeneous target architecture, which provides traceability to the logic from which the SET originated, is appended to the front of the digital word representing the measured pulse width.

Each of the three measurement circuits on the TCV have independent control I/O and reset signals, allowing for parallel operation of each target and measurement circuit. The parallelization of the measurement circuits along with the heterogeneous target structure significantly reduces test time compared with previous implementations that utilized a multiplexing of targets to a single measurement circuit [34, 18, 40].

Erroneous Data Detection in TCV

Since single-events may occur anywhere on the TCV and not just in the target circuity, erroneous data must be able to be identified. In order for an SET from the target circuitry to be counted as real, three protocols must be met. First, one and only one of the 8 bits from the target flags must be set to 1. If none are set to 1, the SET did not originate within the target logic. If more than one bit is set to 1, either two SETs were produced in separate target blocks or one of the flip flops used for column tagging was upset. In either case, the data is flagged as erroneous. It is also possible that the trigger circuitry could be upset. The OR gate in Fig. 47 was added in order to identify upsets in the trigger circuitry. An upset anywhere in the trigger circuitry will produce an external flag. The external controller will then read out all of the data and reset the TCV. If the data stored in the SET capture is all 0's or if the 8-bit target word is all 0's, then the flag is marked as erroneous. An SET in the

delay cells of the VDL will not produce erroneous data. If one of the flip flops in the SET capture circuit or PISO register is upset before an SET arrives, then it will be overwritten once an SET is measured. If the SEU occurs after an SET is captured, but before the data has been read out, the error will show up as a bubble in the output stream, unless it occurs at the transition from the data being all 0's to all 1's. There are two known types of errors that may occur which are not accounted for. If an SET occurs in the clock circuitry of the PISO register while data is being shifted out, it will at worst cause an extra 0 to be added into the data stream which adds 1 bin to the pulse width. The other type of error that may occur is when an SET is generated in one of the OR gates of the target circuitry before the column flagging flip flop. An SET from these OR gates is indistinguishable from an SET originated in the target logic chains. This type of error is minimized by having a much larger cross section for the logic chains than OR network.

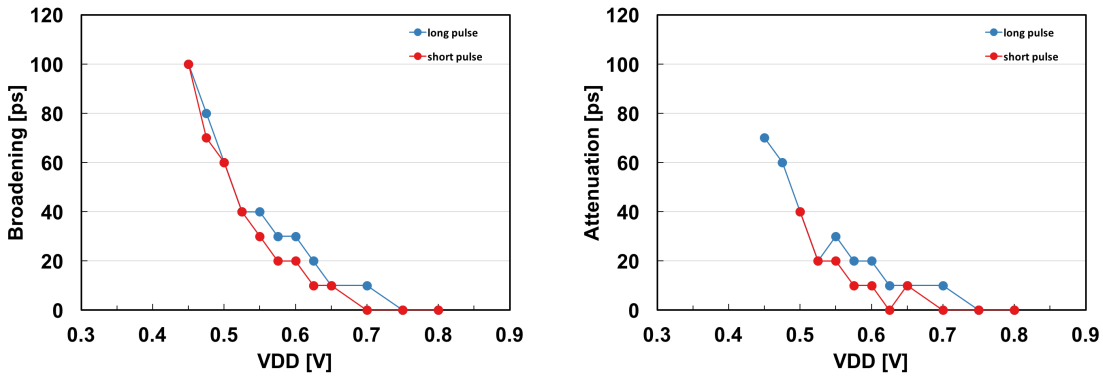
Calibration Methods

While the SET target and measurement topology on the TCV provides a new variable-supply voltage SET testing capability that does not require recalibration of the measurement circuit at each VDD, the propagation characteristics of the logic chains and the voltage level shifter at the output of each short chain introduce potential sources of skew. Circuit simulations indicated a broadening skew through the level shifter for logic chain supply voltages below 0.6 V. Previous work has shown that broadening or attenuation can occur when an SET propagates down a logic chain [21] To characterize this skew, an on-chip fast pulse generator, operating at nominal supply voltage and capable of producing a selectable 120ps or 280ps pulse, was

connected to one short chain input on each of the SET targets on the TCV. The on-chip pulse generator provides the capability to characterize the induced skew over bias during electrical functionality tests in the lab because the pulse width at the input of the combinational logic chain is known. Fig. 48 shows the measured characterization of the broadening skew (due to level shifter) and attenuation skew (due to logic chain) over bias. Fig. 49 shows the effect of the broadening and attenuation at three supply voltages on experimental data distributions. Figs. 49a and 49b show the data as measured, without the broadening and attenuation extracted. Figs. 49c and 49d show the results of one extraction method. Since the broadening is likely due to the level shifter and the level shifter is at the end of the logic chain, it provides a constant addition to the measured pulse width. To extract the broadening from the measured data, the full amount of broadening is simply subtracted from all SETs. The attenuation is a little more complex to account for. The attenuation is likely a cumulative effect along the entire logic chain. Each cell in the logic chain attenuates the pulse by a small amount. The simplest method for extracting the attenuation from the measured data is to add half of the amount of attenuation to every SET. Half was chosen since it is the average amount of attenuation that will be experienced by an SET that is randomly generated somewhere in the chain. SETs at the beginning of the chain will experience the full amount of attenuation whereas SETs at the end of the logic chain will experience little to no attenuation.

Test Infrastructure

The design of the heavy-ion test printed circuit board (PCB) was heavily influenced by the desire to characterize the 16nm/14nm bulk FinFET technology



(a) (b)

Figure 48: Measured skew across bias from the TCV using an on-chip pulse generator. The broadening is attributed to the level shifter at the end of the logic chain. The attenuation occurs along the logic chain. These data were collected by injecting a pulse into a 3 fin, lvt inverter with minimum spacing.

up to high angles of incidence during testing. As seen in Fig. 50, the device under test (DUT) was placed close to the corner of the board and free from any obstructions. Board components, such as decoupling capacitors on power lines, level shifters, and cable connections, were placed in a manner that provided a clear beam path, corresponding to the clear paths on the TCV, which allowed for a high tilt angle of incidence from normal to 85° and coverage of roll angles, from perpendicular to the fins (0°) to parallel to the fins (90°). Additionally, to achieve high tilt angle of incidence testing, the DUT was packaged with the TCV chip on gold spacers elevated above the edge of the package cavity, as shown in Fig. 51, and the bond wires extended from only two sides of the DUT. The DUT was oriented on the PCB so that the unobstructed edges of the PCB and the TCV aligned, shown in Fig. 50 as the top and left edges of the PCB.

Previous similar SET and SEU measurement setups utilized a field-programmable-gate array (FPGA) to control the measurement circuits during irradiation [34, 18,

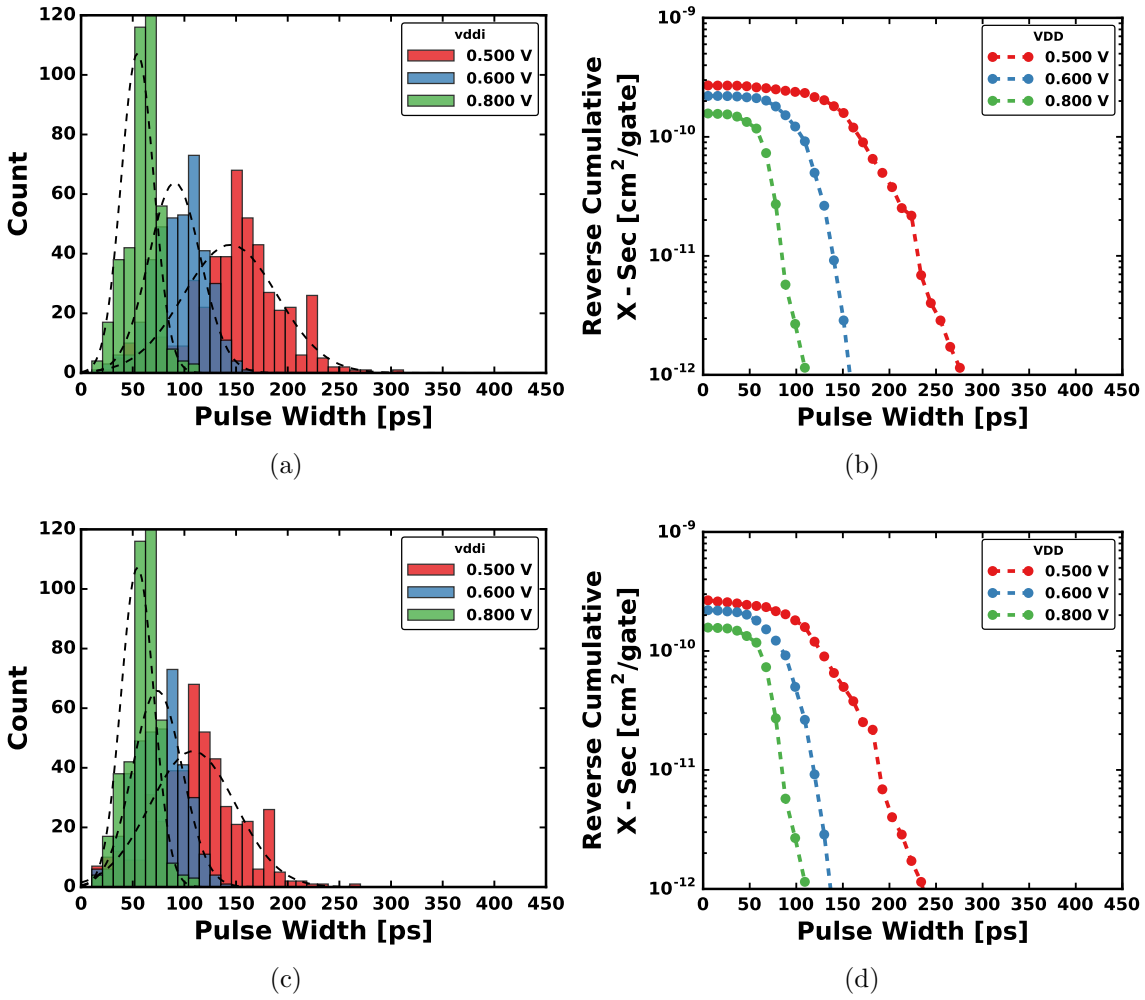


Figure 49: SET data showing impact of measurement skew. Parts (a) and (b) show experimental data as measured. Parts (c) and (d) show the same data with an attempt to extract the skew due to broadening and attenuation.

16, 41]. The FPGA test infrastructure required multiple cables, including long ribbon cables, to connect the DUT board to the FPGA controller. These cables were notoriously noisy and prone to open/shorts at the connectors. The FPGA controller also had its own cables to connect to the control computer. In effort to reduce test setup complexity and increase in-test efficiency, a microcontroller was placed on the test PCB, out of the beam path on the right edge. Placing the microcontroller on board with the DUT eliminated the faulty and cumbersome ribbon

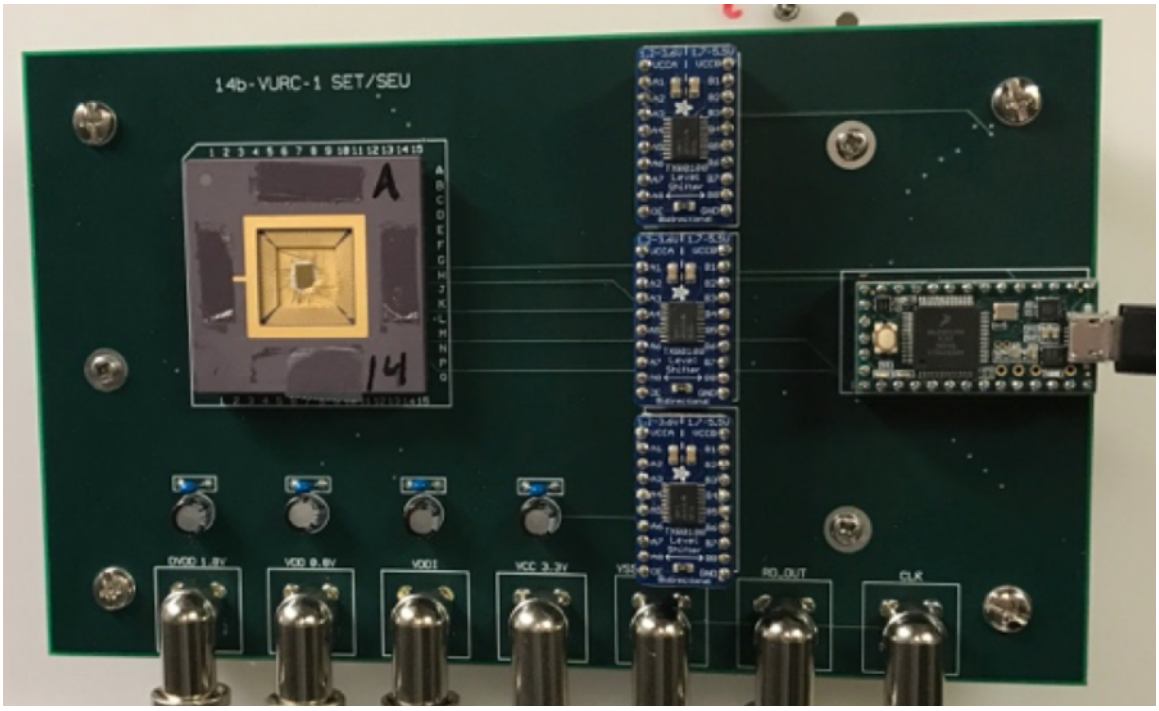


Figure 50: Printed circuit board (PCB) for the 16nm/14nm TCV. The TCV was mounted in the upper left hand corner in order to have unobstructed access to the TCV at high tilt angles. The microcontroller was mounted directly to the PCB in order to eliminate cable clutter and ensure a more reliable connection.

cables and reduced cabling required between the PCB and the control computer outside of the test chamber to a single USB cable. The microcontroller provides an economical interface to communicate with the DUT and the control computer. Microcontrollers are typically easy to code and debug, include lots of built-in functions for communication and data control, and are low cost. In this work, a Teensy 3.2 USB development board with a 72MHz 32-bit ARM processor, 33 digital I/O and micro-USB capability was utilized for these tests. Using the microcontroller and one USB data cable from the PCB reduced the test control software complexity, on-site setup time, and the time required to debug issues during testing.

The microcontroller also provided the capability to pre-process the raw data from the serial digital streams in real-time, in addition to sending the raw digital bit streams

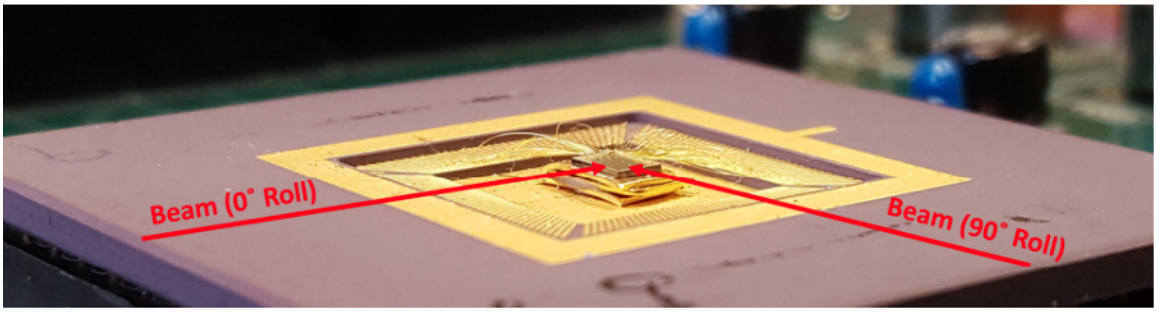


Figure 51: Several of the TCVs were mounted on gold spacers in order to elevate it above the surface of the ceramic package. Grazing angle irradiation was possible since the TCV was elevated above the package and only bonded on two sides.

over USB. This allowed for the plotting of real-time data for test monitoring and informed decision making with respect to the test matrix. Real-time visualization on the test computer was performed by having pre-written visualization code for analyzing the pre-processed data coming from the microcontroller. Fig. 52 shows a snapshot of the type of real-time data analysis and visualization, using Python code on the control computer, that can be performed during active beam tests. The same code utilized in real-time data processing and visualization was also the basis for the data analysis and visualization in post-processing of the raw output bit streams.

The measured data is stored in a structured data format that contains the relevant information about the test: the DUT identifier (chipID), the date and time of the test, ion-beam settings, electrical calibration data, the raw data output, the test voltage, and the target identification information. Fig. 53 shows an example data output for one SET measurement. Utilizing a structured data format provides a means of simplifying the data analysis, the ability to search for specific event types, and the capability to archive the test data in a readable format.

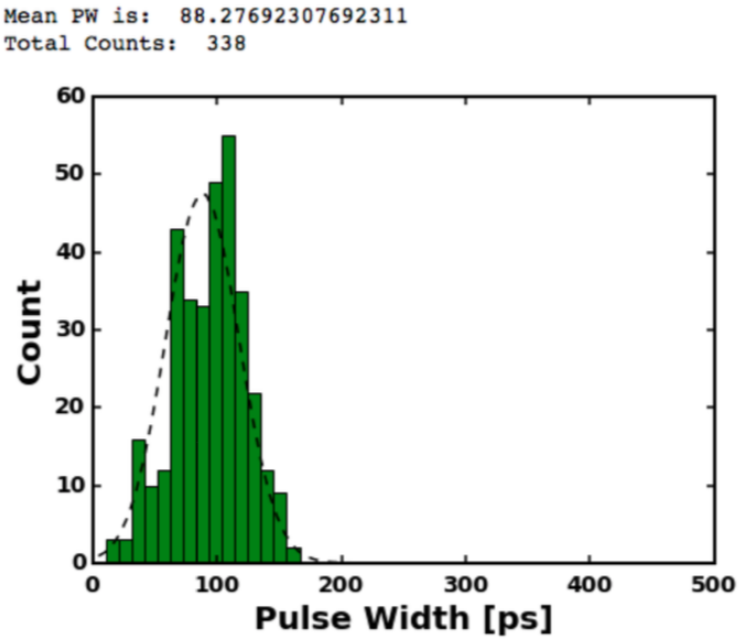


Figure 52: Example of the near-real-time data visualization possible during test.

bins	13
chipID	A14
data	00000000000001111111111111...
dateBegin	Dec 6 15:00:48 PST 2016
dateEnd	Dec 6 15:29:02 PST 2016
device	00000100
dvdd	1.800 V
energy	10 MeV/u
fluence	5e8
ion	O
pw	135.2
resolution	10.4
roFreq	3.75 MHz
roll	0
runNum	100
target	SET2
targetID	7
targetName	NOR-NAND-lvt
targetNum	13312
tilt	0
vdd	0.800 V
vddi	0.650 V

Figure 53: Each SET was recorded in a structured data format that included all of the pertinent experimental information.

Appendix B

14nm BULK FINFET AND 32nm SOI SET CHARACTERIZATION

My research primarily focuses on the characterization of SETs from two technologies: 32nm planar SOI and 14nm bulk finFET. Test chips for the autonomous capture of SETs have been designed and tested in both of these technologies. Both test chips have been tested extensively using heavy-ion broadbeam. This chapter serves as an overview of the data collected, similar to what may be in a data workshop. Further analysis of the 32nm SOI data was the subject of my Master's thesis [40] and further analysis of the 16nm/14nm data will be presented in chapters III and IV.

32nm SOI

Single-event transients are a dominant contributor in the soft-error response of digital CMOS integrated circuits (ICs) [42, 43, 4]. Consequently, it is important to know both the SET pulse width and cross section as they are critical parameters in radiation-robust circuit design. In this section, the analysis of SET pulse width data gathered from the heavy-ion irradiation of 32nm silicon-on-insulator (SOI) technology is discussed. It is now commonly known that single-LET beam exposure produces a distribution of pulse widths and that using the worst case pulse width often leads to an overestimation of the sensitivity of a circuit. This work shows with experimental data that the distribution of pulse widths from inverter chains at a given LET is significantly impacted by the choice of standard Process Design Kit (PDK) MOS variants and layout variations such as threshold voltage and body

contact. While inverters may or may not provide the longest SETs, they allow the most straightforward comparison for the device variants in that they minimize the circuit aspects (for example logic states and numbers of inputs). Several different PDK MOS variants and layout variations were used in the design of the test structures. Results are shown for several of the devices across a variety of experimental conditions such as variations in LET, angular incidence, and bias.

Experimental Conditions 32nm SOI

The devices under test are inverter arrays with various PDK device types and layout configurations. Each inverter array consists of short chains of serially connected inverters, each chain consisting of between 8 and 24 inverters with the inputs of all of the chains connected in parallel, and the output of the chains combined using a balanced-load OR-gate tree. The short chain length helps control pulse broadening, while the parallel connection provides a large total cross section for the target. The SETs generated in the inverter arrays are propagated to an on-chip autonomous pulse width measurement circuit. The pulse width measurement circuit consists of a standard time-to-digital converter which digitizes the pulse width in terms of the propagation delay of two inverters. The minimum measurable pulse width for this design is 23 ps with a binning resolution of 16 ps. Table 7 details the 32nm devices that will be summarized in this chapter. Three of the reported inverter arrays contain minimum-sized (1X) NMOS devices and scaled PMOS devices (designated as RVT, MVT, and UVT). These three arrays differ only in device threshold voltage. One of the inverter arrays contain devices that have an increased device width of 3X the minimum width devices. All of the inverters are floating body. Further details of the

Table 7: Description of target logic on 32nm SOI TCV.

Ref	**Circuit**	**PMOS W/L [nm]**	**NMOS W/L [nm]**	**Gates per Chain**	**Total Gates**
RVT	Regular Vt	214/40	104/40	24	24576
MVT	Mid Vt	214/40	104/40	24	24576
UVT	Ultrahigh Vt	214/40	104/40	24	24576
3XS	3X Low Vt Single Finger	642/40	312/40	8	8192

inverter arrays and measurement circuit may be found in previous papers [34, 18, 40].

All of the data was gathered using the same experimental conditions. Test chips were irradiated in a heavy-ion broadbeam environment using the 88" cyclotron at Lawrence Berkeley National Laboratory (LBNL) with the 10 MeV/u cocktail. Unless otherwise stated, all tests were performed using the Xe ion which has an LET of 59 MeV·cm^2/mg at normal (0°) incidence. Unless otherwise stated, all tests were done at nominal operating voltage of 0.9 V. The bin width for the autonomous measurement circuit was calibrated by measuring the frequency of an on-chip ring oscillator that consists of an equivalent number of stages as the measurement circuit. Additional calibration was performed using an on-chip pulse generator to send pulses of known widths to the measurement circuit. The minimum detectable pulse of the autonomous SET measurement circuit is 23 ps with a resolution of 16 ps per bin. The minimum detectable pulse corresponds to the shortest pulse that will propagate from the target and still be at least half a bin of resolution when it reaches the trigger of the measurement circuit. The 23-39 ps bin was split based on whether an event only triggered the measurement circuit or whether it was captured in the first stage of the measurement circuit. Events that triggered but were not captured in the first stage

of the measurement circuit are counted in a 23-31 ps bin. Events that both triggered and were captured in the first stage of the measurement circuit are counted in the 31-39 ps bin. The quantization error of the SET measurement circuit is less than one bin of resolution.

Results

Seen in Fig. 54 is a typical distribution from this work for 32nm SET pulse widths generated in a heavy-ion environment. This particular distribution is for a 1x minimum size, high VT, floating-body inverter. A large number of pulses captured were at the minimum measurement capability of the autonomous measurement circuit, between 23 and 31 ps. The longest captured pulse was between 90 and 107 ps. This accumulation of pulses at the lower end of the measurement capability was also seen in [34] and is due to RC attenuation as the pulse propagates through the series of logic from the output of the target chain to the input of the measurement circuit and is worse for shorter pulses than for longer ones. The 23-31 ps bin in Fig. 54 represents an SET that was long enough to trigger the measurement circuit but not long enough to be latched. The 31-39 ps bin represents the shortest SET pulse width capable of being latched by the measurement circuit.

Converting a count distribution to a cumulative distribution has been used in previous work, and it can be a very useful way to visualize relevant information from one or several count distributions in a single plot [44, 10]. In a typical cumulative distribution, each y-value corresponds to a value on the x-axis or less; however, in a reverse cumulative distribution, each y-value corresponds to a value on the x-axis or greater. In [44], by Benedetto *et al.*, the SET measurement technique inherently

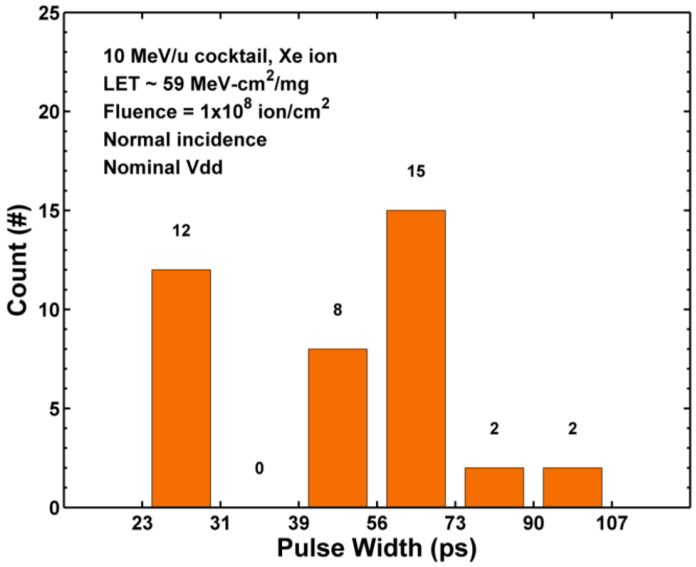


Figure 54: SET pulse distribution for a 1X minimum size, high Vt, floating-body inverter in 32nm SOI collected from a heavy-ion broadbeam environment [18].

gave rise to a reverse cumulative distribution. Ferlet-Cavrois *et al.*, in [10], showed how plotting the reverse cumulative distribution of collected charge can be useful for comparing several devices at different technology nodes. In this work, the reverse cumulative distribution is extracted from a count distribution of experimental pulse widths and is used to compare several different devices within the same technology.

Effect of Device Variants

It is often the case that the heavy-ion induced SET response of a particular technology is represented with data collected from elementary devices [10]. While this is often a good first look a technology's SET response, it is not representative of the complete SET response of a technology due to the effect that PDK-standard MOS variants and layout variations such as threshold voltage, body contact, and oxide thickness can have on the SET distributions. In [40] it was shown that, within a single technology, both the cross section and pulse width cover a broad range of

values due to PDK-standard MOS variants and layout techniques. A summary of the results presented in [18, 40, 16] across variations in threshold voltage, supply voltage and LET will be shown below.

Threshold Voltage

Shown in Fig. 55 are the results of irradiating the UVT, MVT, and RVT targets from Table 7 with the heavy-ion Xe. These three targets were designed with identical geometries, and vary only in their threshold voltage. The threshold voltage of these devices increases in order from RVT to MVT to UVT. Thus, the UVT target has the highest threshold voltage and lowest drive current, while the RVT target has the lowest threshold voltage and the highest drive current. The data show that as the threshold voltage increases, longer SETs are more likely to occur. This behavior is expected since, all other variables being equal, as drive current increases the SET pulse width decreases due to the devices ability to more quickly evacuate the collected charge and return to its normal operating state. The observed trend of the cross section decreasing with decreased threshold voltage is a result of the decrease in SET pulse width. The SET measurement circuit has a minimum measurable pulse width of 23 ps, thus if a target produces relatively more SETs below 23 ps then a decrease in cross section is expected.

LET Variation

Shown in Fig. 56 are the results of irradiating the 3XS target using seven different ions at normal incidence. SETs were measured at an LET as low as 4 MeV$\cdot$cm^2/mg, and SET pulse widths up to 183 ps were observed. For higher LETs, it is observed

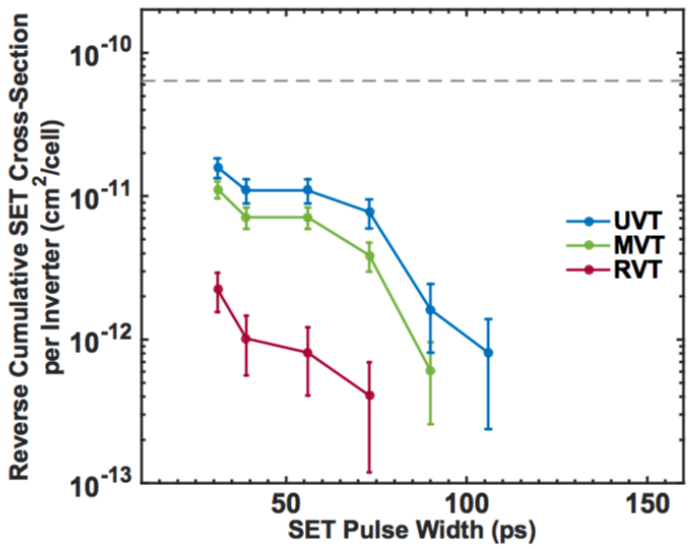


Figure 55: Cross section versus pulse width characterized across multiple threshold voltages for devices with identical geometries. The irradiation was performed at 0.9 V, normal incidence, and with an LET of 59 MeV·cm^2/mg. The dashed line corresponds to the average combined body area of the NMOS and PMOS [16].

that a reasonable estimate for the cross section per inverter is the average of the NMOS and PMOS body (i.e. gate) areas, as indicated by the dashed line in Fig. 56. The average is used since only one transistor is sensitive in an inverter for a static input condition, and in a chain of inverters an equal number of NMOS and PMOS transistors will be sensitive.

Bias Variation

Devices were irradiated at normal incidence across bias. Shown in Fig. 57 are the SET responses of the 3XS and UVT targets at biases of 0.7, 0.8, 0.9 and 1.0 V (0.9V is nominal for this technology). Significantly longer SETs are produced under reduced bias, as expected, since the restoring current decreases with decreased bias. As the supply voltage is reduced and the SET duration increases, more of the SET distribution is captured by the measurement circuit. This is evident in the cross

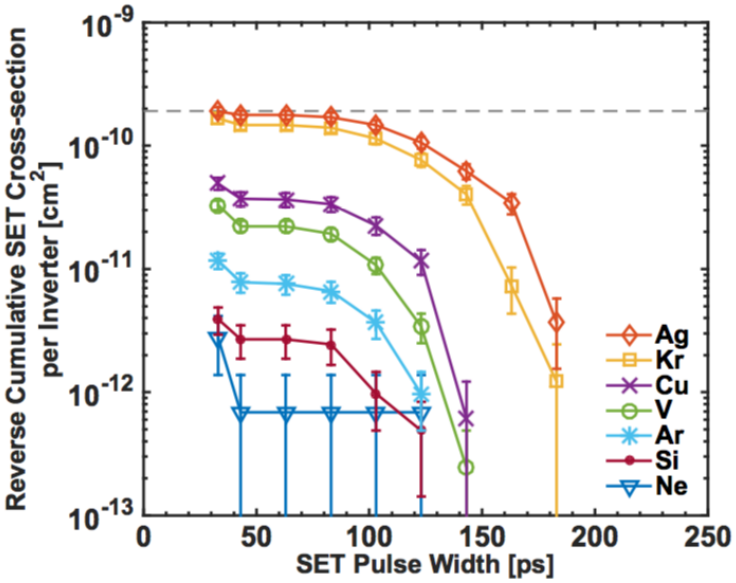


Figure 56: Cross section versus pulse width characterized across multiple LET values for the 3XS device at normal incidence. The dashed line corresponds to the average combined body area of the NMOS and PMOS [16].

section saturating at the average NMOS and PMOS body area for the for both devices for supply voltages of 0.7 V and 0.8 V.

Angular Variation

Irradiations at various angles of incidence were performed using the Cu ion (which has a normal incident LET of 21 MeV·cm^2/mg). The results from the 3XS device across angle are shown in Fig. 58. The orientation of the beam with the device is such that a tilt of 90° and a roll of 0° corresponds to a strike along the width of the device (i.e. parallel to the gate). Generally, both the number and length of SETs were observed to increase as the tilt angle increased. This is likely due to an increased path length of the ion through the sensitive volume (i.e. body area).

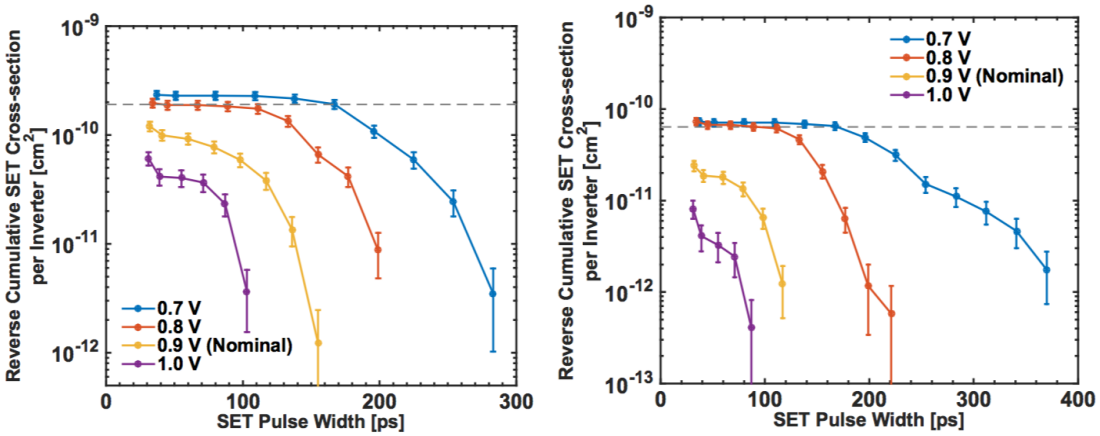


Figure 57: Cross section versus pulse width characterized across multiple biases for (a) the 3XS inverter and (b) the UVT inverter. The dashed line corresponds to the average body area of the NMOS and PMOS. These data were collected at normal incidence using the Kr ion, which has an LET of 30 MeV·cm^2/mg [16].

14nm Bulk FinFET

An SET TCV was designed in Global Foundries 14nm bulk finFET technology. The chip consists of various SET structures comprised of serially connected logic gates. There are five inverter chains with variations in fin number, threshold voltage and inverter-to-inverter spacing. There are two ARM level shifter chains, one with a 0 input and the other with a 1 input. There is one NAND/NOR chain which supplies the post-SET restoring current through a pair of parallel transistors. The NAND gate is restored through a pair of PMOS transistors and the NOR through a pair of NMOS. Conversely, there is one NOR/NAND chain which supplies the post-SET restoring current through a pair of stacked devices, PMOS for the NOR gate and NMOS for the NAND gate. There are two custom-designed logic gates, one CVSL NAND chain and one RHBD NAND chain, which uses the DIL topology, a novel aspect of this work. All of the aforementioned chains, except for the CVSL and DIL ones, use ARM level shifters at the output so that the chains operate on an isolated, variable

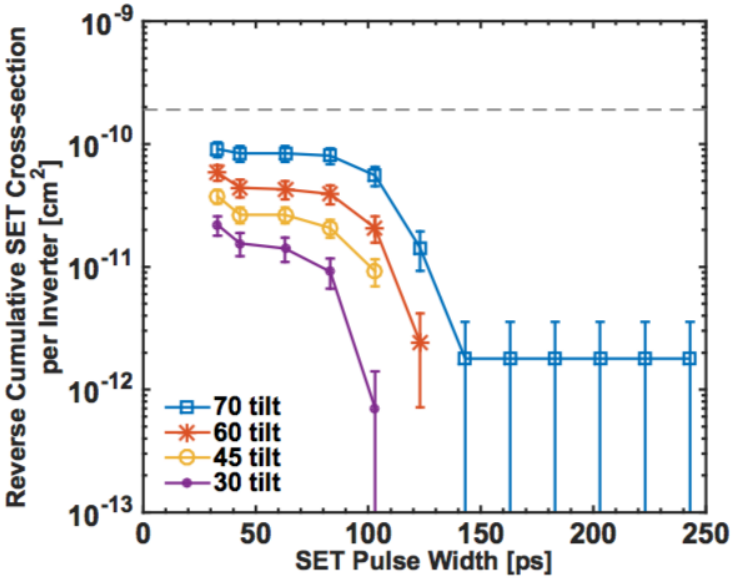


Figure 58: Cross section versus pulse width characterized across multiple angles of incidence for the 3XS device using the Cu ion (normal incidence LET = 21 MeV·cm^2/mg). The roll angle was such that the beam traversed the width of each device. For a tilt of 70 degrees, one SET was measured at 245 ps and no transients were measured between 125 ps and 245 ps.

voltage. The incorporation of level shifters is also a novel aspect of this chip in that it allows the target chains to operate at a reduced supply while the propagation and measurement circuitry stay at nominal voltage, thus eliminating the need to calibrate the measurement circuit at different voltage. Additionally, this setup more closely mimics real systems that use voltage scaling to reduce power consumption. Appendix A provides exhaustive detail on the design of the 16nm/14nm TCV.

Extensive heavy-ion testing across voltage, angle and LET has been performed using the 16nm/14nm SET TCV. Fig. 59 shows an exemplar SET distribution collected from a 3 fin LVT inverter chain operating at at 0.8 V for an LET of 21 MeV·cm^2/mg.

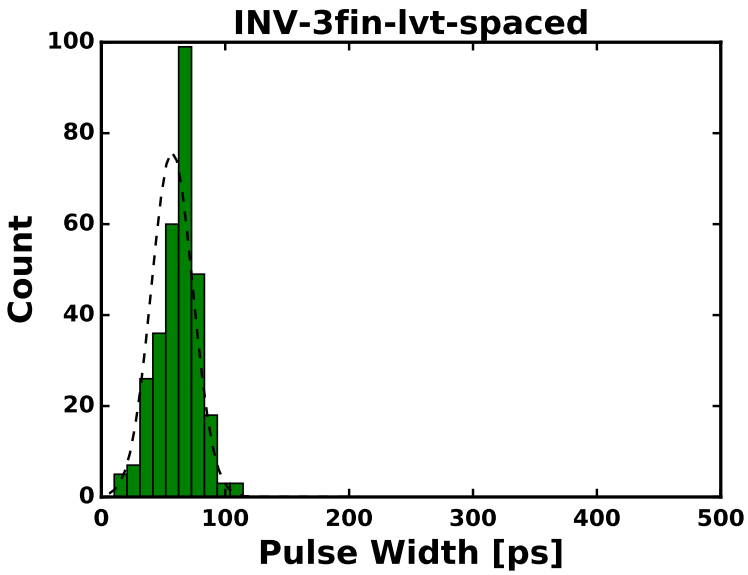


Figure 59: Exemplar SET distribution obtained from 16nm/14nm SET test chip. This particular data was collected from a 3 fin LVT inverter chain operating at at 0.8 V for an LET of 21 MeV·cm^2/mg.

16nm/14nm Library SET Characterization

Library SET characterization is an important aspect of model development and error rate predictions. It is impractical to test every variety of logic gate available in a single PDK, thus it is important to wisely select a subset of gates that allow for the SET sensitivity analysis of single design parameters. The 16nm/14nm TCV includes many different logic topologies as discussed above that allow the isolation of several pertinent design parameters. This section will present heavy-ion SET data due to design variations in fin count, threshold voltage, logic type, cell spacing and whether the restoring current is sourced from stacked or parallel devices. Additionally, the impact of operating/environmental conditions such as supply voltage, tilt angle, roll angle and LET will be shown. Device sizes will be given in terms of poly pitch and fin pitch as laid out in the ITRS roadmap. The poly pitch for the 16nm/14nm generation is 70 nm and the fin pitch is 42 nm [1].

Standard Inverter

Fig. 60 shows the distribution and cross section for a 3 fin lvt inverter with 2X spacing operating at 0.8 V. Fig. 60a shows a tightly clustered distribution of SET duration across LET; however, the maximum SET duration does increase slightly as LET increases. Fig. 60b shows the cumulative cross section over LET, and the increase in maximum SET duration is clearly evident. The dashed line in Fig. 60b corresponds to the drawn active area, two poly pitches by three fin pitches, of one PMOS or NMOS transistor in the inverter since only one transistor is sensitive in any given inverter. As LET increases to 60 MeV·cm^2/mg, the cross section increases to over twice the drawn active area. The traditional metric of using the drain area as a rough estimate for sensitive area is obviously no longer valid as the device is capable of collecting charge from regions outside of the drawn active area.

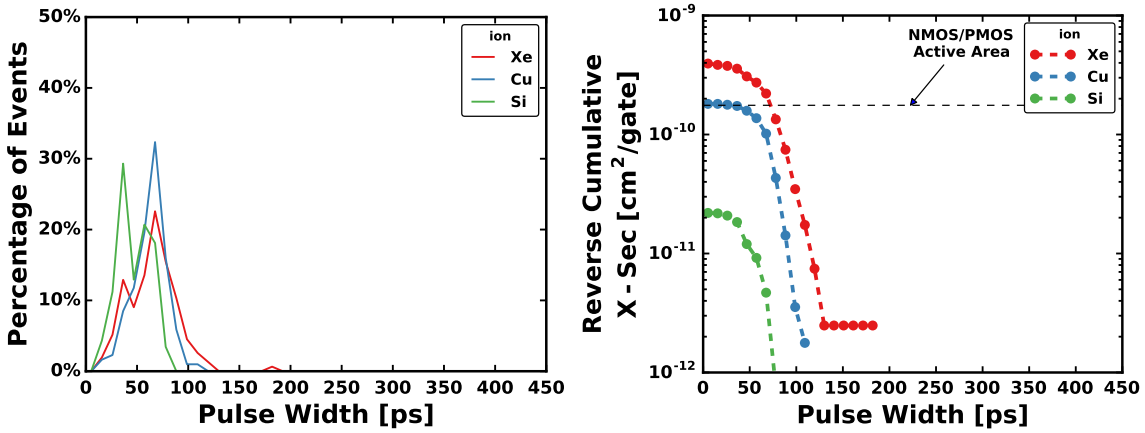


Figure 60: Measured SET distribution and cross section as a function of LET for a 3 fin lvt inverter with 2X spacing operating at 0.8 V. The LET for Xe, Cu and Si is 60, 21 and 6 MeV·cm^2/mg respectively.

Standard NAND

Fig. 61 shows the distribution and cross section for a 2-input NAND gate operating at 0.8 V. The PMOS devices have a total active area of three poly pitches by two fin pitches and the NMOS devices have a total active area of three poly pitches by three fin pitches. Both inputs of the NAND gates are tied together thus the input is either 00 or 11. In this configuration the NAND gates behave as inverters, with half the gates having an input of 00 and the other half with 11. For the NAND gate, the cross section increases with LET as expected, but, unlike the inverter, the measured cross section does not exceed the drawn active area by much. This is most likely due to the fact that the NAND gate has a higher restoring current and thus produces short duration SETs. The measured cross section is only for SETs with duration $>$ 15 ps. There are likely many SETs being produced below the measurement threshold. This is an important aspect of a majority of the data collected on the 16nm/14nm TCV. There is a trend that cross section and SET duration typically increase in the same direction.

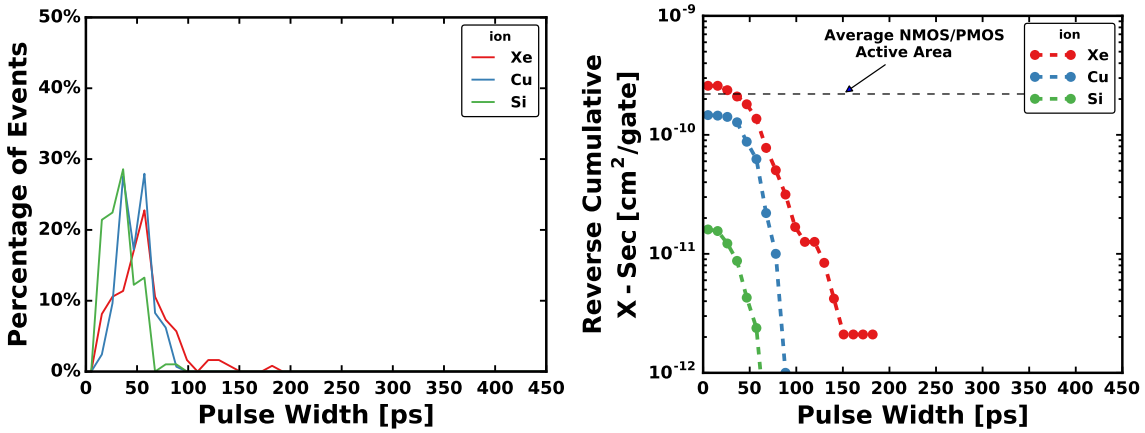


Figure 61: Measured SET distribution and cross section as a function of LET for a NAND gate operating at 0.8 V. The LET for Xe, Cu and Si is 60, 21 and 6 MeV$\cdot$cm^2/mg respectively.

Fin Count

The impact of drive strength differences due to device width, or fin count in the case of finFETs, on SET distributions has brought about various conclusions. The impact is highly dependent on technology, especially whether it is a bulk or SOI technology. SET results from increased transistor width in a 32nm SOI inverter were presented in [40]. Those results showed that a larger inverter produced a larger measured cross section and longer measured SETs. Further analysis showed that the smaller inverter produced shorter measured SETs due to increased pulse attenuation along the chain compared to the larger inverter. The attenuation was also attributed to large decrease in cross section that was measured for the small inverter compared to the large inverter. It was concluded that in SOI it was likely that increasing the drive strength via device width would lead to shorter SET pulses, but it would also result in an increased SET cross section since the sensitive area is tied to the SOI body area. The impact of increased drive strength in a planar bulk technology was examined by Glorieux *et al.* in [15]. It was shown that increasing the drive strength via device size led to a slight reduction in cross section for low LET and a slight increase in cross section at high LET. The decrease at low LET is likely due to an increased critical charge. The increase at high LET was attributed to a larger sensitive area. It is important to note that the increase in cross section at high LET was small compared to the increase in drive strength. For a 12X increase in drive strength, the cross section increase was under 2x. Fig. 62 shows the results for an increase in fin count from three to six for inverters in the 16nm/14nm bulk finFET technology. Results are given at three different supply voltages (0.5, 0.65 and 0.8 V) and two LETs (6 and 59 $\text{MeV}\cdot\text{cm}^2/\text{mg}$). The results show a significant difference in

both cross section and SET duration across bias and LET. The six fin inverter has a consistently lower cross section and shorter pulses than the three fin inverter. This is a different result than presented in either [40] or [15]. The shorter pulse widths produced by the six fin inverter are intuitively explained via restoring current. A higher restoring current will recover the output node after a single event faster than a lower restoring current. The restoring current of the six fin inverter is always higher than the three fin inverter. It is interesting to note that the restoring current of both gates has the same voltage dependency, and thus the difference in cross section is observed across all supply voltages. One possible explanation for the lower cross section of the six fin inverter at both low and high LET is that it is producing more SETs that are below the minimum measurable pulse width of the capture circuit, thus the measured cross section appears lower. However, if the minimum measurable pulse width was the sole reason for the decreased cross section, the difference would diminish at low supply voltages and high LET where a majority of the SETs are well above the minimum. However, even at at supply voltage of 0.5 V and an LET of 59 MeV$\cdot$cm^2/mg, the difference still exists which suggests that there is a real reduction in SET cross section as the drive strength increases via fin count. These data suggest that increasing the drive strength via fin count is a viable hardening technique for combinatorial circuits in advanced technologies.

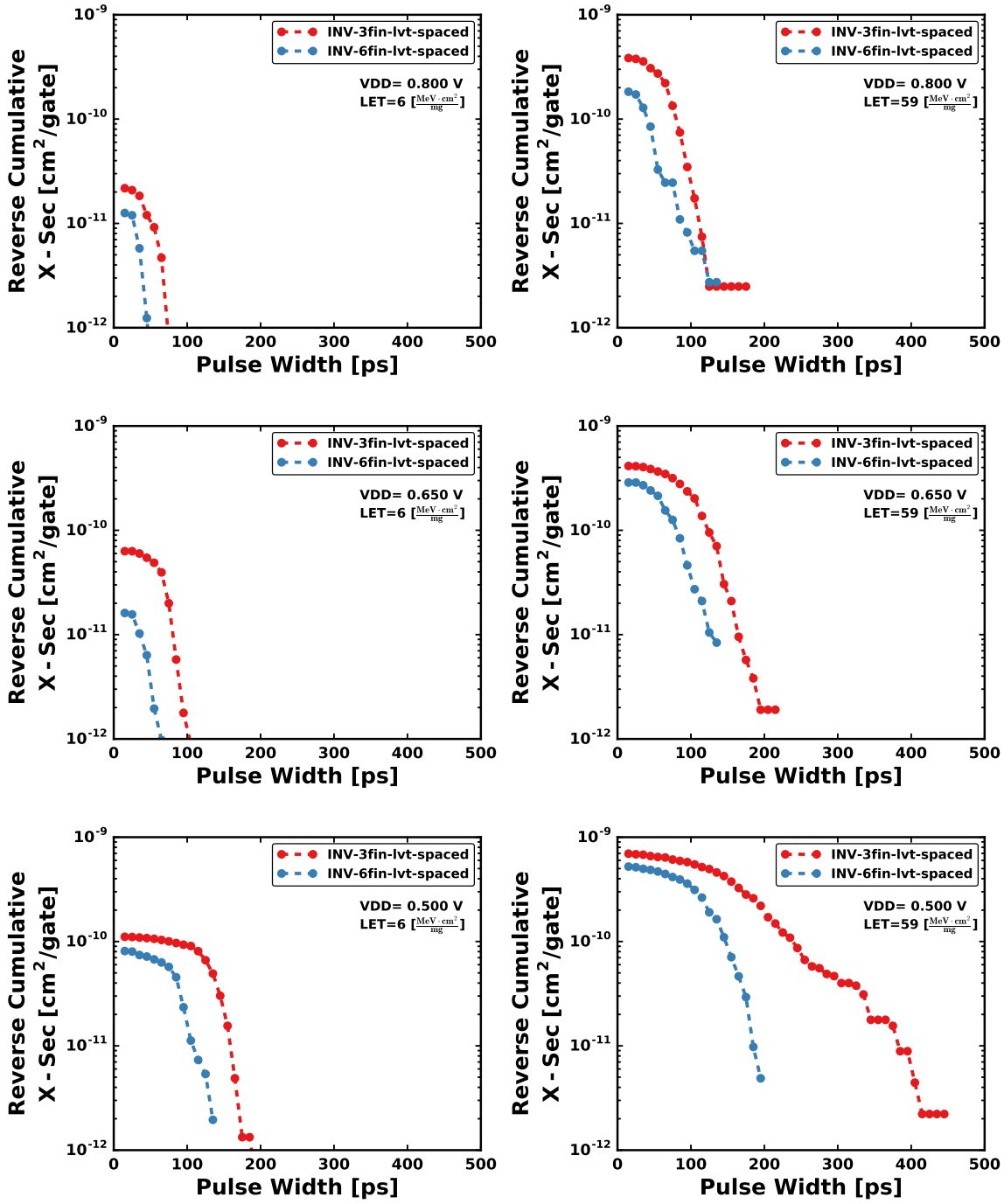


Figure 62: Characterization of fin count on the SET sensitivity in 16nm/14nm bulk finFET logic gates. These data were measured from the normally incident broadbeam irradiation of a three fin, low Vt inverter and a six fin, low Vt inverter. The 2X spaced versions of the gates were chose for comparison as to reduce the influence of charge sharing. The six fin inverter has a consistently lower cross section and shorter duration SETs across both supply voltage and LET.

Threshold Voltage

In most advanced technologies, there are several levels of threshold voltage that a designer can choose for any logic gate. Since the threshold voltage is such a tunable design parameter, it is vital to evaluate the impact it has on SET sensitivity. The 16nm/14nm TCV included inverter and NAND chains with two levels of threshold voltage, low and regular, where regular is higher than low. The inverter SET cross section measured at three supply voltages and at low and high LETs is shown in Fig. 63. It is important to note that the only difference between the two logic gates is threshold voltage. They both have the exact same number of gates, dimensions, etc. Fig. 63 shows that the SET cross section and duration are essentially identical at nominal supply voltage of 0.8 V. At nominal supply voltage the two inverters have very similar restoring currents, and since they both have identical physical dimensions, it is intuitive that their SET sensitivity is similar. As supply voltage decreases, the restoring currents of the inverters begin to diverge since they have different threshold voltages. The decrease in restoring current of both inverters is evidenced in the data by higher cross sections and longer SETs. The effect of higher threshold voltage (i.e. lower restoring current) is evidenced in the more rapid increase in SET duration with decreased supply voltage of the regular Vt inverter compared to the low Vt inverter. Unlike changing restoring current via fin count, changing restoring current via threshold voltage does not seem to affect the total SET cross section.

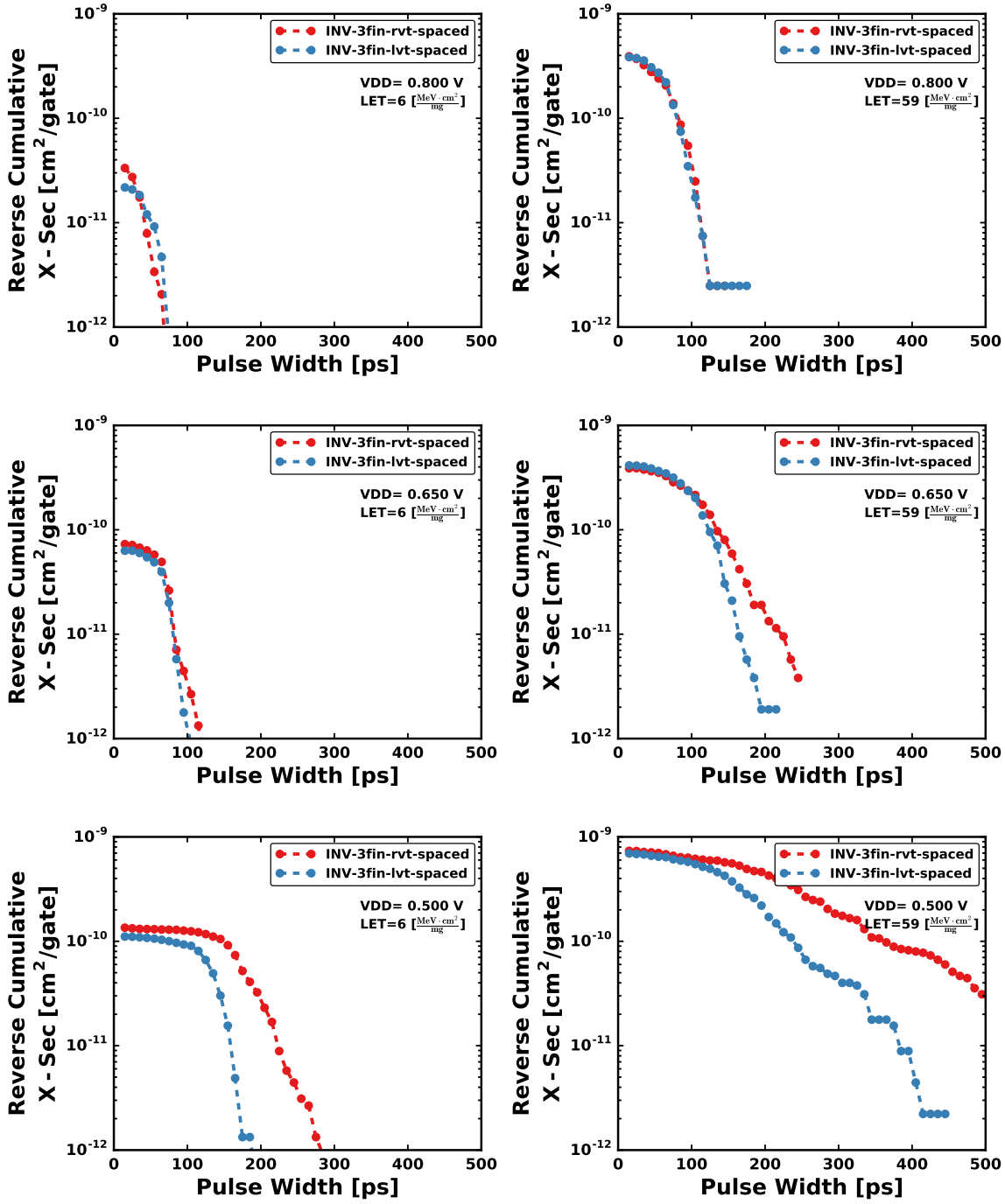


Figure 63: Characterization of threshold on the SET sensitivity in 16nm/14nm bulk finFET logic gates. These data were measured from the normally incident broadbeam irradiation of a three fin, low Vt (lvt) inverter and a three fin, regular Vt (rvt) inverter. Regular threshold voltage is higher than low threshold voltage. The 2X spaced versions of the gates were chose for comparison as to reduce the influence of charge sharing. At nominal supply voltage, the two threshold voltages exhibit similar SET sensitivities; however, as supply voltage decreases, the regular Vt inverter produces much longer duration SETs than the low Vt inverter.

Gate Spacing

In order to investigate charge sharing phenomena, two identical inverter chains with different gate to gate spacings were included on the 16nm/14nm TCV. Both inverters were three fin low Vt designs, with one have a spacing of 168 nm and the other having a spacing of 336 nm. One of the main mechanisms affecting SETs due to charge sharing is pulse quenching [45, 46]. Pulse quenching occurs when multiple nodes collect charge, and the SET from the originating node is truncated by collection at a node in the original SET's propagation path. It was shown [46] that decreased gate spacing, from 1.3 µm to 0.75 µm, and a shared n-well greatly increased pulse quenching. For the 16nm/14nm TCV, each inverter chain was laid out with a common n-well and the inverter chains only had a difference of 168 nm. Fig 64 shows the SET cross section for three different supply voltages and at low and high LET. At low LET and high supply voltage, there is very little difference between the two chains. However, as LET increases and supply voltage decreases the two chains begin to exhibit a difference in SET sensitivity. Because of the shared n-well and relatively small difference in spacing it is likely that both inverter chains are subject to charge sharing and pulse quenching, just to varying degrees. For comparison, the same data are shown for two six fin low Vt inverters in Fig. 65. The six fin chains have the same spacing difference as the three fin chains. Similar to the three fin inverters, the SET sensitivity difference between the two spacings in Fig. 65 appears to increase with decreased supply voltage and increased LET; however, the six fin inverters seem to be less sensitive to spacing differences than the three fin inverters.

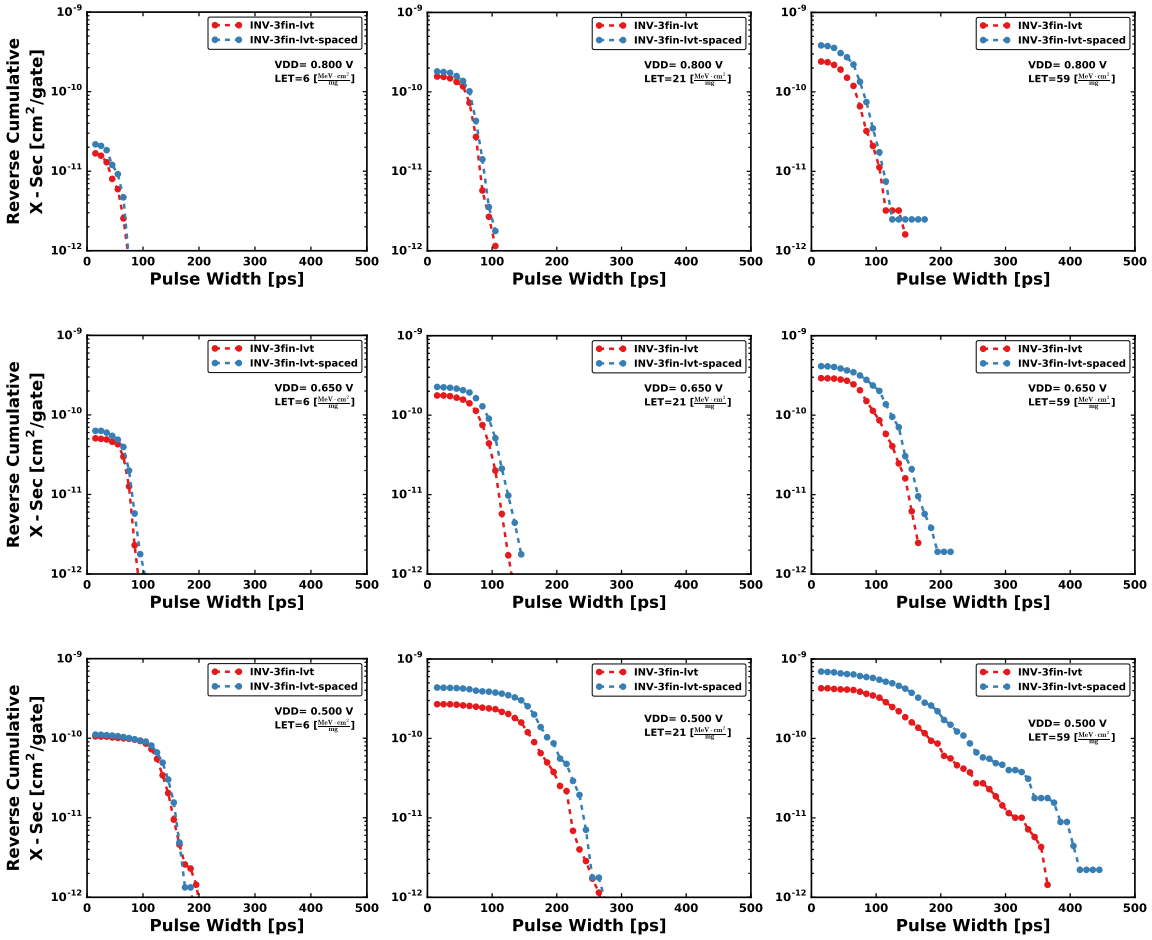


Figure 64: Characterization of gate spacing on the SET sensitivity in 16nm/14nm bulk finFET logic gates. These data were measured from the normally incident broadbeam irradiation of a three fin, low Vt inverter with 168 nm gate-to-gate spacing and a three fin, low Vt inverter with 336 nm gate-to-gate spacing (INV-3fin-lvt-spaced). At nominal supply voltage and low LET, the two spacing variations exhibit similar SET sensitivities. As supply voltage decreases and LET increases, the inverter chain with minimal spacing exhibits lower cross section and shorter SET duration compared to the inverter chain with increased spacing. This is likely due to increased charge sharing among the minimally spaced chain causing increased pulse quenching.

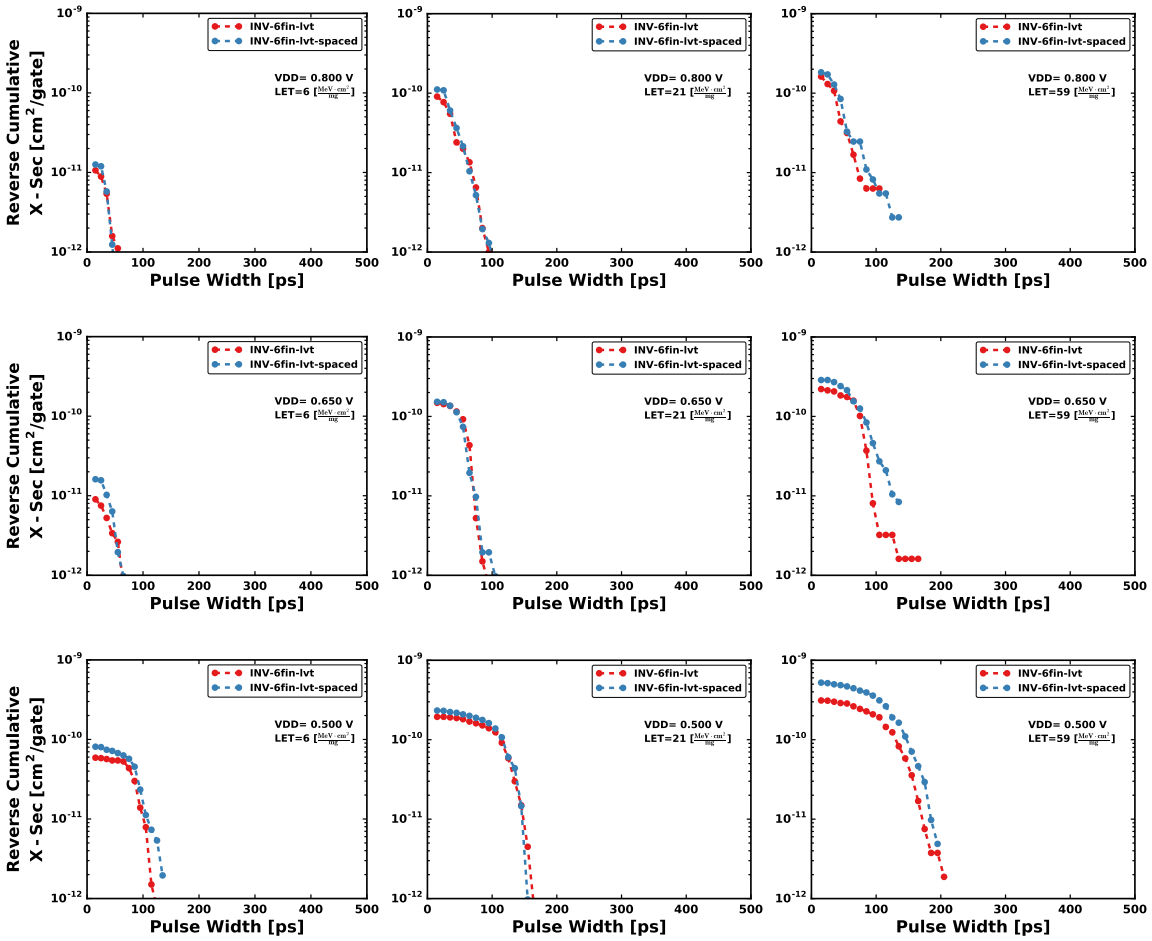


Figure 65: Characterization of gate spacing on the SET sensitivity in 16nm/14nm bulk finFET logic gates. These data were measured from the normally incident broadbeam irradiation of a six fin, low Vt inverter with 168 nm gate-to-gate spacing and a six fin, low Vt inverter with 336 nm gate-to-gate spacing (INV-6fin-lvt-spaced). At nominal supply voltage and low LET, the two spacing variations exhibit similar SET sensitivities. As supply voltage decreases and LET increases, the inverter chain with minimal spacing exhibits lower cross section and shorter SET duration compared to the inverter chain with increased spacing. This is likely due to increased charge sharing among the minimally spaced chain causing increased pulse quenching.

Conclusions

A vast amount of heavy-ion induced SET data has been collected in both 32nm SOI planar and 16nm/14nm bulk finFET technologies. The impact of design choices such as threshold voltage, logic type, device width and gate spacing were evaluated along with variations in supply voltage and LET. For 32nm SOI, the sensitive area is shown to be limited to the body area of the device, while in 16nm/14nm bulk the sensitive area is not confined to either the fin or the drawn active area. The 16nm/14nm data reveal that drive strength variation is one of the dominant factors influencing SET duration, whether it is due to changes in threshold voltage, fin count or supply voltage. A more thorough analysis of the influence of supply voltage is presented in Chap. III.

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