SINGLE-EVENT CHARGE COLLECTION AND UPSET IN 65-NM AND 40-NM DUAL- AND TRIPLE-WELL BULK CMOS SRAMS

By

Indranil Chatterjee

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Approved by:

Professor Bharat L. Bhuva

Professor Ronald D. Schrimpf

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CHAPTER I

INTRODUCTION

1.1 Single Event Effects: A Brief Overview

Since the discovery of May and Woods [1], considerable effort was spent by the semiconductor community to deal with the problem of errors from alpha particles emanating from packaging, metallization and other materials. Similar efforts were made to study the soft error mechanisms arising from protons, neutrons and heavy ions impinging on semiconductor devices. Single-Event Effects (SEE) in microelectronic devices results from highly energetic particles impinging on sensitive regions in a semiconductor device. These particles (e.g., protons, neutrons, alpha particles, or other heavy ions) are present in the natural space environment and they may also be a significant reliability issue for terrestrial applications. Depending on several factors, the particle strike may cause no observable effect, a transient disruption of circuit operation (Single Event Transient, SET), a change of logic state (Single Event Upset, SEU), or even permanent damage (Single Event Gate Rupture, SEGR & Single Event Burnout) to the device or integrated circuit (IC) [2].

There are two primary methods by which ionizing radiation releases charge in a semiconductor device: direct ionization by the incident particle itself and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device. Both mechanisms can lead to integrated circuit malfunction.

Direct Ionization: When an energetic nuclear particle strikes a semiconductor material, it loses its energy through Rutherford scattering (Coulombic interactions) with the semiconductor lattice structure. The energy creates electron-hole pairs. When all of its energy is lost, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's range. Direct ionization is

the primary charge deposition mechanism for upsets caused by heavy ions (Heavy Ion: Ion with atomic number greater than or equal to two i.e., particles other than protons, electrons, neutrons, or pions).

Indirect Ionization: As a high-energy proton or neutron enters the semiconductor, it may undergo a collision with a target nucleus. Possible reactions include: 1) elastic collisions that produce Si recoils; 2) the emission of alpha or gamma particles and the recoil of a daughter nucleus (e.g., Si emits alpha-particle and a recoiling Mg nucleus); and 3) spallation reactions, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. The secondary particles, thus generated, deposit charge along the path they traverse by direct ionization, thereby resulting in an upset.

Ions can also lose energy by non-ionizing energy loss (NIEL) where the ion has elastic or inelastic collisions with the atoms of the material. This work focuses only on direct ionization processes. In case of ionizing energy loss, the particle slows down inside the semiconductor through predominantly Compton interactions with the nuclei of the crystalline structure and transfers energy to the lattice and leaves an ionization trail of free electron-hole pairs, as shown in Fig. 1.

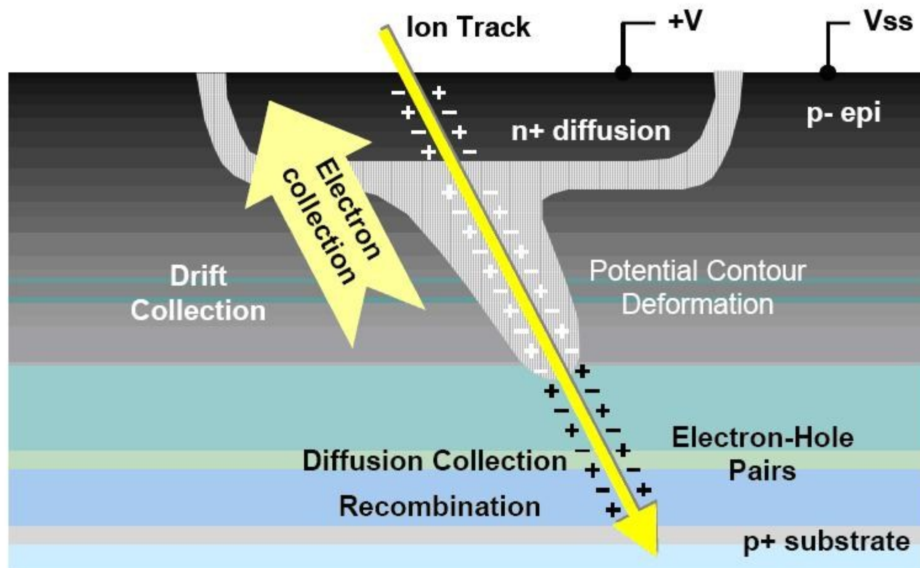


Fig. 1: An illustration showing the generation of electron hole pairs caused by a single event ion strike [3](**R. Baumann,** ***IEEE NSREC Short Course*****, 2005)**

Within an integrated circuit, these excess carriers may come under the influence of an electric field, leading to current transients across device junctions and voltage transients on the circuit nodes. These current and voltage transients may cause loss of data stored in storage cells, such as latches or SRAM cells, resulting in single-event soft errors. These errors are called soft errors because the functionality of the storage cell is not affected. At the next clock cycle (or at the next write cycle at that address in SRAM), the cells accept new data and function normally without any permanent damage.

Direct ionization energy transfer can be quantified by calculating the linear energy transfer (LET) value. LET is defined as the energy loss per unit path length of the particle, typically given in units of MeV-cm^2/mg after dividing by the density of the target material. Using the LET of the ion, the average energy needed to create an electron-hole pair (EHP) for the material, and the density of the material a calculation of charge deposited per unit length can be done. As a reference, in silicon an ion with an LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm [12]. Traditionally heavy ions and alpha particles (heavier nuclei) have been responsible for causing SEE in circuits. However, with technology scaling, particles like muons etc. are also causing substantial effect in devices. In modern electronics the single-event soft error rate (SER) is expected to be higher than the combined failure rate due to device degradation issues, during the lifetime of a product [3]. SRAM cell topology and layout significantly affect the SRAM SER. The inherent feedback in the cell topology amplifies and strengthens the transient effects of the particle strike. SRAM cell layouts are designed to be as small as possible (both to increase density and to increase the frequency of operation). This approach results in decreased critical charge due to reduced transistor currents and nodal capacitances as compared to conventional logic gate designs. On the other hand, decreased cell layout footprint decreases the cell cross-section, resulting in decreased SER. Along with traditional methods of charge collections, new mechanisms such as parasitic bipolar charge injection, Multiple Cell Upsets (MCUs) and multiple-node charge collection have also resulted in a significant increase in the Soft Error Rate (SER) of circuits [4].

Various techniques have been proposed to mitigate the effects of soft errors in electronic circuits, namely error correcting codes [5], Guard Rings [6], Silicon-on-Insulator (SOI) technology [7], DICE latches [8], etc. Triple-well technology (described below) has a lot of electrical advantages compared to dual-well technology. However, the single-event response of such devices is not without ambiguity. While some published literature has reported cases of single-event hardening using triple-well structures, others have reported the opposite. In this work, the underlying mechanisms of the single event response have been studied to understand in detail the response of triple-well devices to ionizing radiation.

1.2 Triple Well Technology

The aggressive scaling of CMOS technologies has enabled the realization of monolithic systems that integrate high-speed digital circuits with high performance analog circuits [9], [10], and thereby the integration of wireless RF circuitries as well. In such mixed-mode systems, substrate noise coupling has been identified as a major problem [11], [12], [13]. This paved the way for the use of triple-well technology in CMOS manufacturing process. The triple-well technology comprises a buried n-well layer that isolates the p-well from the p-substrate.

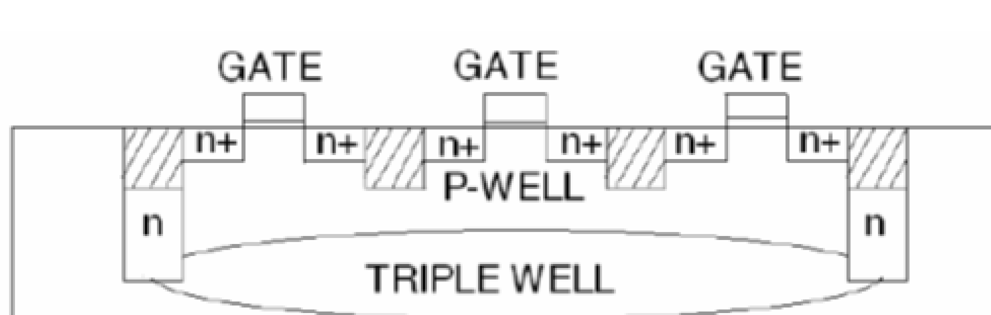


Fig. 2: Triple Well NMOS transistors

Triple-well technology is widely used in SRAM cells to improve the isolation of transistors from the substrate [14]. It has several other electrical advantages compared to a twin (dual)-well technology.

For analog circuits, triple well is used for reducing noise and cross-talk. In digital CMOS circuits, triple well technology enables low threshold voltage NMOS transistors to improve the frequency of operation. It may also be used to reduce power locally by modifying the threshold voltage using well bias. A modification of the triple-well technology, described as “merged triple-well’ technology, reduces CMOS latchup susceptibility [15]-[16]. However, the implantation of the deep n-well causes damage (interstitials, vacancies, amorphous clusters, and amorphous layers) to the silicon lattice, as shown in [17] which increases the leakage current by a considerable margin. The damage produced is dependent on the dose of the dopants and at higher doses, the damage production rate increases to the extent of initiating amorphization of silicon. The threshold voltage of a triple-well NMOS device, similarly, increases first with increasing implant dose, and then decreases due to amorphization of the silicon. The main advantage of triple-well technology is that it allows circuits to be independent of the substrate bias condition. This is an advantage for noise isolation, mixed signal and dynamic threshold MOSFET applications. Additionally, allowing independent biasing of the substrate allows for biasing of the channel region in the isolated region, and providing a different back-bias condition, or dynamic threshold MOS (DTMOS) devices [18].

1.3 Single Event Response of Triple Well Devices: Literature Review

There have been conflicting reports about the single event performance of triple-well devices. One of the earliest references that discuss the influence of triple-well structures on the radiation response of devices was by Burnett et al. The paper showed that the use of a triple-well technology resulted in a reduction in the alpha-particle-induced soft error rate (SER) in 0.5-µm BiCMOS technology [19]. A 4Mb SRAM was fabricated in a triple well, and also in a p-well/p-substrate with a p+ buried layer. A standard BiCMOS process exhibited ~7X higher SER than a standard CMOS process. The authors attributed this difference to the p-well/n-substrate junction under the array for the CMOS process. The presence of the p+ buried layer or a deep n-well in a BiCMOS process was observed to reduce the charge collection [20]. The best results were obtained using a triple-well structure that reduces SER by ~600%. Roche et al.

showed that triple wells brought about a 40% decrease in alpha-particle-induced SER for SRAMs fabricated in a 130 nm technology and a 25% decrease in a 90 nm technology [21]. It was observed that triple-well structures reduce the SER sensitivity as the electrons generated deep inside the substrate are more efficiently collected by the extended n buried zone and then better evacuated through n-well ties. Similar observations were made by Kishimoto *et al.,* Noda *et al.,* and Sato *et al.* [22]-[23]. In 0.25µm technology, a shallow triple well and 4T SRAM cell with stacked capacitor were used to improve the soft error rate by 3.5X compared to a conventional SRAM cell [24]. In this 0.25 µm process, Sato *et al.* demonstrated an increase of storage node capacitance from 8fC to 25fC by using a stacked-type capacitor with a two-layer polysilicon. Alpha and neutron irradiation was performed on the 64K × 36 bit SRAM. It was observed that the increased storage capacitance prevented the particle-generated charge from overwhelming the stored data, thereby exponentially improving the soft error immunity. It was hypothesized in this paper that a shallow triple-well structure reduces the possibility for charge to be generated because of the shallow depth of the p-type well through which the ion strike passes. The effect of the deep n-well was used along with the effect of increased storage node capacitance to obtain low soft error rate (SER).

While some of the published literature reports that the use of triple-well structures is beneficial to reducing error rates, many report the opposite. Puchner et al. found that using a triple-well increases the Failure-in-Time (FIT) rate for heavy ions in a 90 nm CMOS technology [25]. In this case, a triple-well scheme has been implemented on an 18-Mb fast synchronous SRAM by using a high energy implant to evaluate its impact on the alpha-particle-induced accelerated soft error rate. It was observed that because of the collection of holes in the p-well of the triple-well structure, the well gets de-biased. The excess holes can be removed by recombination with minority carriers or through the well contacts. The recombination rate is much lower than the generation rate of the free carriers by the particle hit and thus results in greater charge collection by the transistors, which increases the overall error rates by as much as 3x. Later in this thesis we will observe how charge confinement in the p-well will affect the single event

response of triple-well structures on a positive note. Roy et al. showed that the use of a triple-well technology results in greater transient pulse-widths in 90 nm inverter circuits [26]. They detailed the charge collection mechanisms in a 90 nm triple-well inverter circuit and it was observed that primarily because of the p-well de-bias, the pulse-widths were larger compared to dual-well structures. Combinational-logic circuits fabricated in a 65 nm technology showed a similar trend [27]. Mostly, these results were obtained using separated transistors so that only a single transistor collected charge due to an ion hit. Because of these apparently conflicting results for triple-well structures, it is important to understand the single-event response of triple-well transistors more thoroughly over a wide range of particle LETs.

1.4 Charge-Sharing at advanced technology nodes

With greater packing density at advanced technology nodes, multiple node charge collection becomes important. Black et al. showed that at 65 nm SRAM cells can recover from upset because of well collapse source injection mechanism arising from charge-sharing at high LETs [28]. Ahlbin et al. showed that for 90 nm and 130 nm technologies, single event transient pulse-widths in combinational logic may decrease for irradiation with particles that have high LETs [29]. Seifert et al. demonstrated reinforcing charge collection between nMOS transistors using dummy gates [30]. While Black et al. focused on charge-sharing between nMOS and pMOS transistors in SRAM cells, Ahlbin et al. and Seifert et al. described multiple node charge collection between similar transistors in combinational and sequential circuit elements. Thus the charge collection mechanisms in a triple-well structure are bound to be affected by charge sharing between adjacent transistors. This work focuses on the effects of multiple node charge collection between nMOS transistors in triple-well SRAMs.

1.5 Overview of the work

In this work, a detailed analysis of the single-event response of dual-well and triple-well structures is reported over a wide range of particle LETs. Simulations were performed over a wide range

of deposited charge to observe the effects of charge-sharing in these structures. From these simulations, it was observed that triple-well technologies are more vulnerable than dual-well technologies for particles with low LET values, whereas for particles with moderate and high LET values, dual-well designs are more vulnerable. Chapter II details the 3D TCAD simulation setup used to understand the mechanisms of charge collection while Chapter III reports the underlying mechanisms of charge collection in dual- and triple-well structures. It was found that charge confinement and multiple node charge collection triggers the "Single Event Upset Reversal" in triple-well structures that lowers the soft error rate compared to dual-well structures at high LETs. Alpha, neutron and heavy-ion tests were carried out on SRAM designs built in both dual-well and triple-well technologies at 65 nm and 40 nm technology nodes in order to verify the simulation results obtained. Results for heavy-ion exposure are reported in Chapter IV. Chapter V briefly discusses the effects of various process parameters on the single-event upset reversal mechanism. The calibration of a 40 nm commercial NMOS and PMOS transistor is described in Appendix A and the Structure Editor and Sdevice scripts used in the simulations are included in Appendix B.

CHAPTER II

3-D TCAD SIMULATIONS

2.1 Simulation Setup

Simulations are used to analyze the single-event performance of dual- and triple-well NMOSFETs. Simulation results in the form of electrostatic potential and carrier concentration plots are used to explain the physical mechanisms of charge collection in triple-well devices. The device structures simulated using 3D TCAD are described in this chapter. Two NMOSFETs are constructed in 3-D TCAD in dual and triple well technology to simulate single event upsets caused by ion strikes on or near the drain of the NMOSFETs. The drains of the NMOSFETs are loaded with PMOSFETs and connected to simulate an SRAM cell, so that circuit effects on the behavior of the devices can be obtained. The aspect ratio of the PMOSFET simulated by means of a compact model is detailed in this chapter. Also, the parameters of the ion strikes are mentioned.

2.2 TCAD Structure

Synopsys® Sentaurus Structure Editor is used to create the 3-D NMOS transistors in order to study the single event effects on these devices. The devices belong to the 45 nm technology nodes. Figs. 3(a) and 3(b) show the 2D cross-sections of the dual- and triple-well NMOS transistors respectively while Fig. 4 shows a 1-D cut showing the doping concentration along a vertical cutline taken through the source of the dual- and triple-well NMOSFETs. On a p-substrate having a constant doping of 1×10^{16} cm^{-3}, a buried n-well is made having a Gaussian doping profile. The p-well enclosed by the n-well has a Gaussian doping profile that peaks at 1×10^{18} cm^{-3}. The doping and dimensions for the dual-well NMOS system were obtained after iterative simulations in order to match the commercial 45nm PDK. The n-well doping was adjusted so that the net doping at the surface where the NMOS device was built remained the same

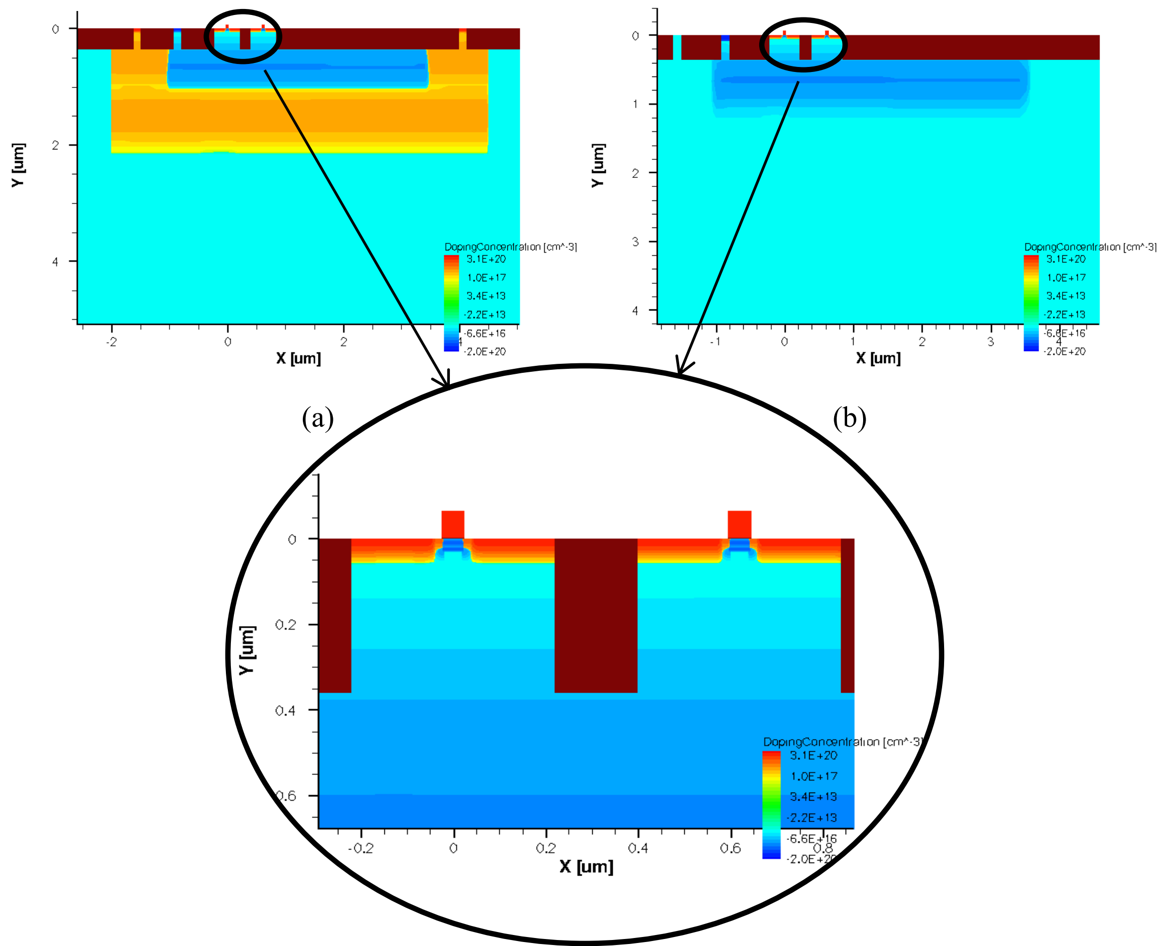


Fig.3: 2D cross-section of the (a) Triple-well and (b) Dual-well 40 nm NMOSFETs

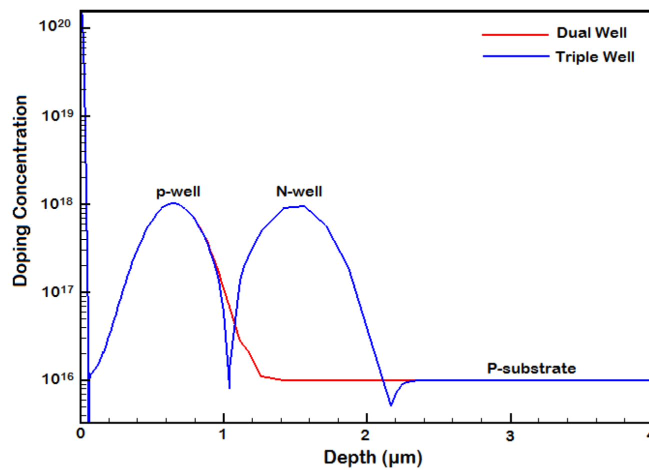


Fig. 4: 1-D slice showing the doping concentration along a vertical cutline taken through the source of the dual- and triple-well NMOSFETs

for both the dual- and triple-well systems. The TCAD transistors were calibrated to match the DC and AC electrical characteristics of the Process Design Kit (PDK). The DC characteristics curves are shown in Figs. 5 and 6.

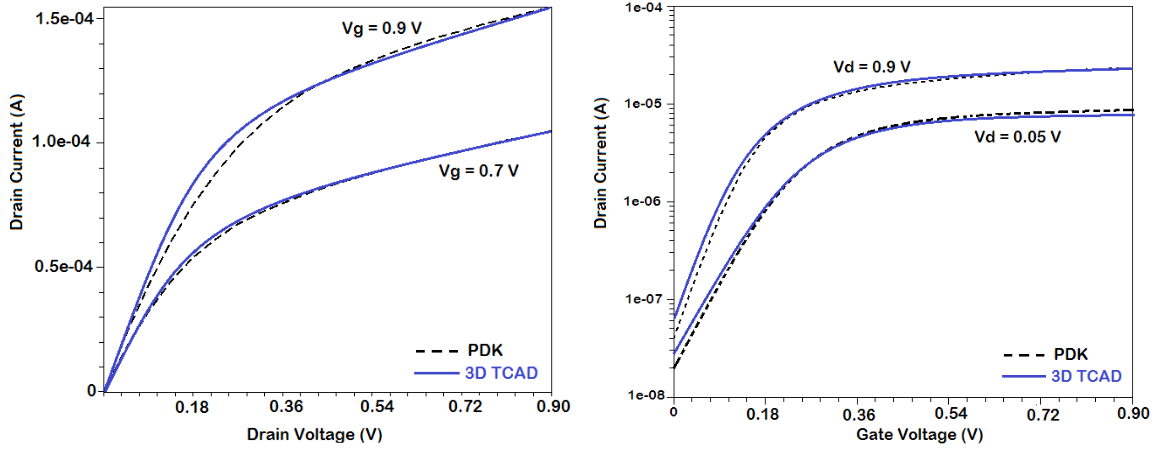


Fig. 5: I_D-V_D and I_D-V_G curves a dual-well/triple-well NMOSFET. The dashed lines are from the PDK while the solid lines are of the calibrated devices.

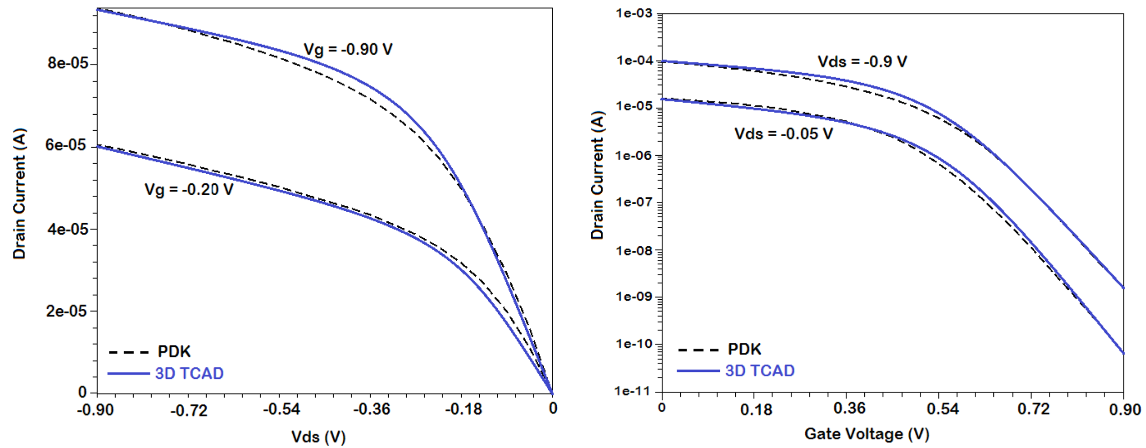


Fig. 6: I_D-V_D and I_D-V_G curves a PMOSFET. The solid lines are from the PDK while the dashed lines are of the calibrated devices.

The simulation shows a close match with the PDK curves. The threshold voltage and the drive current are very similar in both cases. The block of silicon used for the simulations was 10 μm × 10 μm × 10 μm.

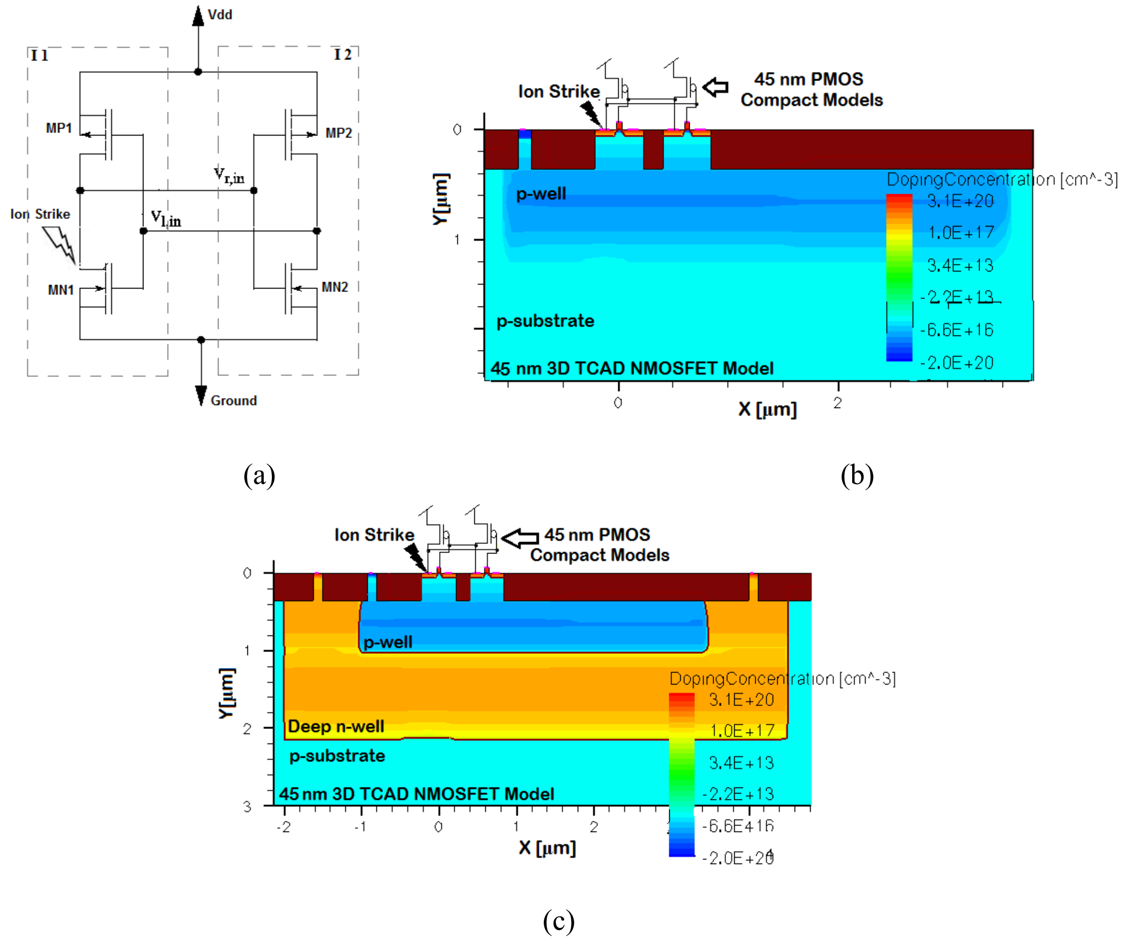


Fig. 7: Simulation setup (a) Circuit Schematic, 2D cut of a (b) dual well and (c) triple-well NMOSFETs of an SRAM circuit in 3D TCAD and PMOSFETs in Compact Models.

2.3 Mixed Mode Simulation setup

The TCAD NMOS transistors described in the previous section are connected to PMOS devices. A calibrated BSIM3 compact model of the PMOS transistor is used. The simulations are carried out on a SRAM cell thus formed. The mixed mode simulations are performed to obtain the effect of an active load on the struck node, and to observe the circuit effects on the voltage and current at the struck node.

2.4 Heavy Ion Simulations

The charge deposited by the incident ions was modeled using a Gaussian radial profile with characteristic 1/e radius of 50 nm, and a Gaussian temporal profile with a characteristic time of 2 ps. It

may be noted that a Gaussian radial profile is not the best estimate for a single-event ion track profile [31], [32]. It has been observed that a realistic ion track may which conforms to the Kobetich and Katz (KK) theory [33], has a greater charge density in the track core compared to the Gaussian profile, often used in TCAD simulations. It was observed that the actual ion-track profile resembled more of an exponential function, rather than a Gaussian approximation. However, simulations carried out with both Gaussian and a realistic ion-track structure showed saturation in SET pulse widths for 90 nm inverters [32]. In the simulations carried out in this paper, the Gaussian ion-track has been used in conjunction with SRH and Auger recombination mechanisms that would provide a realistic trend from the simulations in terms of charge density in the track. Additionally, the total charge deposited is the same with both Gaussian and realistic tracks, corresponding to the incident particle LET. In this work, the charge deposited by the incident ion is important as that would determine whether the "single-event upset reversal" would trigger or not and the ion track profile would not influence the underlying mechanisms described here.

The circuit was simulated in an initial state with the output of inverter I1 HIGH and that for I2 LOW, which results from transistors MN1 and MP2 being in the OFF state and transistors MP1 and MN2 being in the ON state. The ion was incident on (or near) the drain region of transistor MN1, as shown in Fig. 7(a).

2.5 Summary

The device structure and the setup used for the simulation of single event effects in dual-well and triple-well devices are described in this chapter. The following chapters describe the result of simulating ion strikes on the devices described here. The mechanisms of charge collection in these devices are developed based on the results obtained from the simulations.

CHAPTER III

MECHANISMS BEHIND THE SINGLE EVENT RESPONSE OF DUAL- AND TRIPLE-WELL SRAM CELLS

In this chapter, an SRAM cell is simulated and the drain of the OFF NMOSFET is struck with ions. Ion strikes of different LET values are considered. The p-well contacts of the dual-well and triple-well devices are of comparable sizes. The upset pulses at drain of an NMOSFET built in a triple well are compared with those in a dual well. The single-event upset voltage and current pulses are shown here.

3.1 Heavy Ion Simulations

Ion strikes that deposit a maximum initial charge density lower than the background doping of the substrate are classified here as low-LET ion strikes. Fig. 8 shows the acceptor and donor concentrations and the free carrier densities before and 10 ps after the peak of the carrier generation occurs for an ion strike of LET 1 and 35 MeVcm^2/ mg.

It can be seen that the charge density deposited by an ion strike of LET = 1 MeVcm^2/ mg at the peak of the Gaussian temporal profile (time t = 1 ns) hardly surpasses the background doping, while that deposited by an ion having LET = 35 MeV-cm^2/mg deposits a charge density two orders of magnitude greater than the background doping density at the peak of the Gaussian temporal profile (time t = 1 ns. The difference in the physics of these two cases shall be explained in the following section.

The upset pulse width depends on the LET of the ion. The following section shows the voltage and current characteristics of dual- and triple-well NMOS drains when struck by ions having different energies. First the simulated results for normal incidence are presented for LETs of 5, 10, 20 and 30 MeV-cm^2/mg, followed by angled hits. Angular strikes have been simulated for LETs of 5, 15 and 25 MeV-cm^2/mg for 30° and 60° angle of incidence. Further simulations for very high LETs (> 40 MeV-

cm^2/mg) are presented. The physics behind the single event response of dual- and triple-well SRAM cells are discussed in the following section.

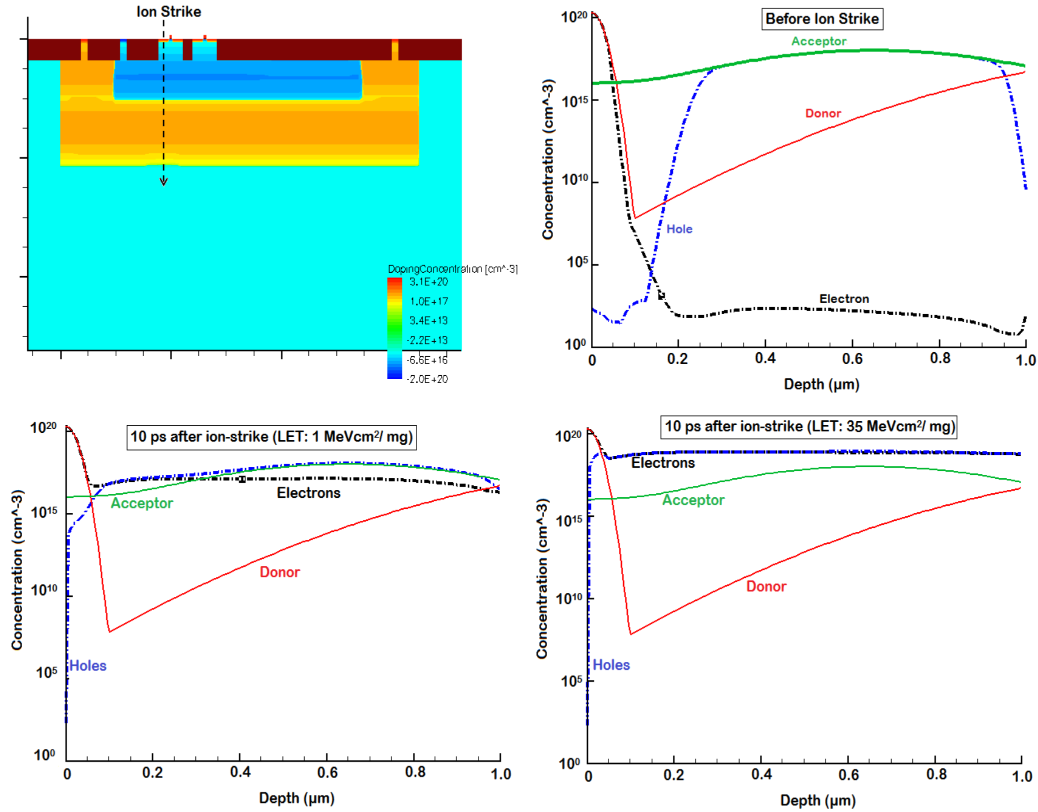


Fig. 8: (a) Cross section of a triple-well NMOSFETs. The dotted arrow shows the location of the ion strike. Doping density and carrier concentrations in p-well (b) prior to ion strike, (c) 10 ps after an ion strike of LET = 1 MeV-cm^2/mg, and (d) 10 ps after an ion strike of LET = 35 MeV-cm^2/mg.

3.2 Mechanisms behind the Single Event Response

In this section, the fundamental mechanisms of charge collection in dual- and triple-well structures are described. The simulation results obtained in the previous chapter are discussed in detail and the physical mechanisms behind the results are investigated. We discover a new phenomenon described as the **SINGLE EVENT UPSET REVERSAL MECHANISM**, which explains the single event response of triple-well structures at moderate to high LETs.

3.3 Overview of the Charge Collection Mechanisms

The differences in mechanisms related to charge collection and removal in both the technologies are discussed below. The mechanisms have been discussed in detail in [26]. In this section, it is necessary to recapitulate the mechanisms.

The major difference between dual-well and triple-well technologies arises due to the presence of deep n-well structure in triple-well devices. The differences in collected charge for these technologies is affected by the amount of charge collected by a p-well, amount of charge injected by a source region, presence or absence of parasitic bipolar transistors, and the charge removal through p-well contact. Each of these mechanisms is briefly discussed for both technologies below. Fig 9 shows a summary of the charge collection mechanism in triple-well technology.

A) Charge Collection in the p-well

In dual-well technology, when a strike occurs, the electrons generated in the p-well are collected by the source and drain of the NMOSFET. The holes are removed from the well by the p-well contact. The majority of the holes generated by the strike get distributed over the well and the substrate. Thus, there is just a slight increase in the p-well potential. In the case of a triple well technology, the electrons generated in the p-well due to the ion strike are collected by the n-well. The electric field in the p-well/n-well depletion region confines the holes to the p-well. This causes a large potential increase in the well, which is much greater than the p-well potential rise in dual-well.

B) Electron Injection from the Source

The sources of NMOSFETs in both the technologies are tied to the ground potential. The large potential perturbation in the p-well in a triple-well technology due to an ion hit, forward biases the p-well—source junction of the NMOSFET. Thus the electric field at this junction injects electrons from the source of the NMOSFET into the p-well. In the dual well, the source–p-well junction is not forward biased as the p-

well-potential perturbation is small, resulting in very little electron injection into the p-well from the NMOSFET source region.

C) Parasitic Bipolar Action

In a triple-well device, the electrons that are injected into the p-well, need to find an n-doped region to go into. This is provided by two n-doped regions, the drain of the NMOSFET and the n-well. Thus here are two parasitic bipolar paths in this technology. One is the source--p-well--n-well path and the second is the source--p-well—drain path. Both of these parasitic transistors play a role in charge collection and the resultant voltage perturbations. These parasitic bipolar transistors are absent in dual-well technologies due to smaller well-potential perturbations.

D) Charge Removal through p-well Contact

For a triple-well technology, the n-well--p-well junction is reverse-biased and this allows electrons to drift into the n-well region. As long as the charges are not completely removed from the p-well, it stays at a higher potential, thereby forward biasing the source–p-well junction causing more electrons to be injected into the p-well and collected by the drain. Thus, the key point for faster recovery of the system lies in the faster removal of holes from the p-well, which is thus dependent on the size and location of the p-well contact.

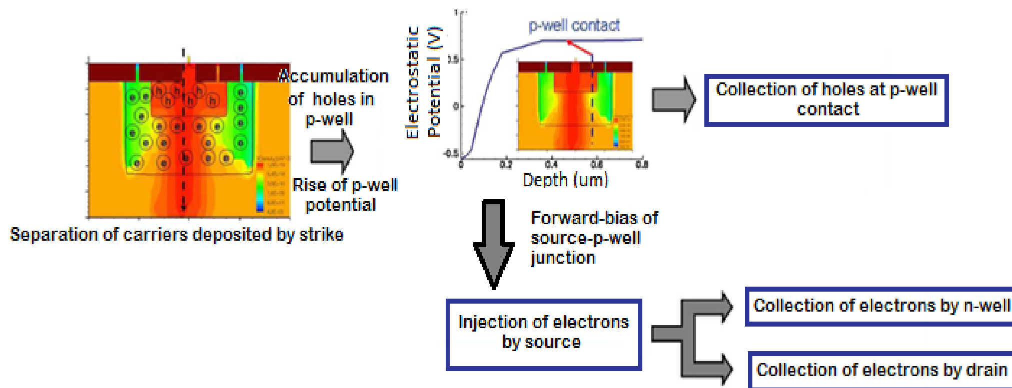
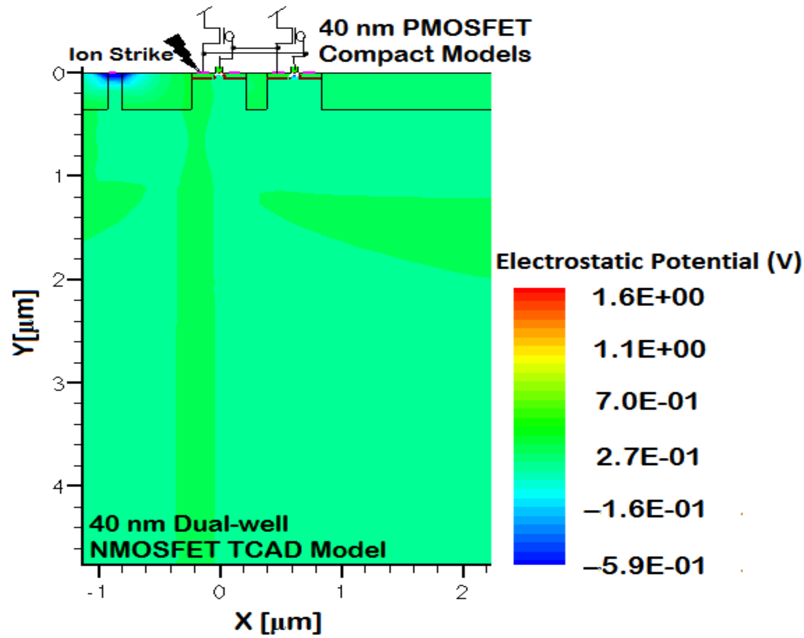


Fig. 9: Overview of the physical mechanisms responsible for charge collection in triple-well NMOSFETs. [26]

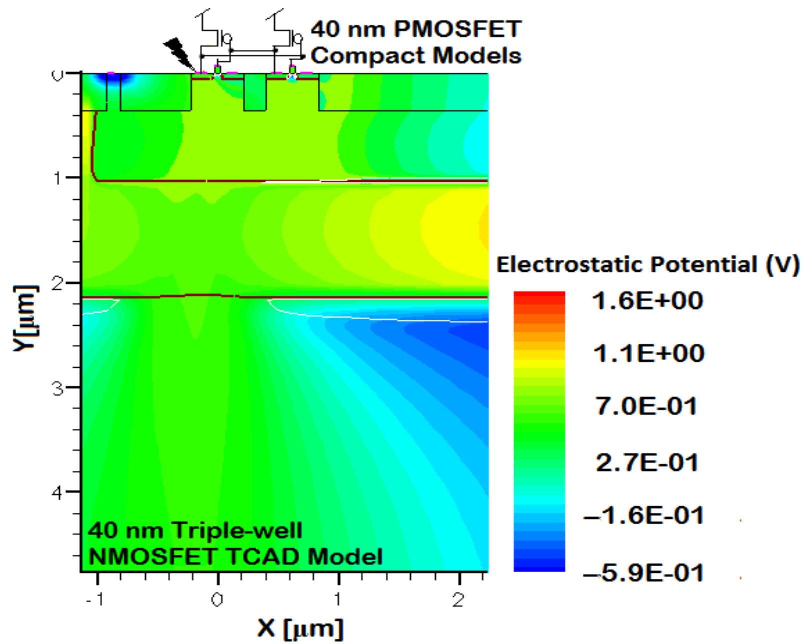
3.4 Charge confinement in triple-well structures

Soft error rates for SRAMs depend on the critical charge of the circuit and the amount of charge collected by sensitive circuit nodes. The collected charge depends on the charge generation and transport processes. In a triple-well structure, the deep n-well–p-well junction is reverse-biased. This causes the electrons to drift into the n-well, leaving the holes behind in the p-well. In a dual-well technology, the holes spread throughout the p-substrate, while in a triple-well technology, majority of the holes are confined within the p-well. This may be termed as "charge confinement". Thus, the electrostatic potential perturbation in the p-well of a p-substrate dual-well technology is less than that in the p-well of a triple-well technology (Fig. 10).

The parasitic bipolar effect is reduced in the dual-well technology, decreasing the collected charge. Also, charge confinement in the triple-well structure may lead to a higher number of multiple-cell errors within a single p-well [4]. This is why dual-well technology is sometimes considered to be superior to triple-well technology from a soft-error point of view. As shown in Fig. 10, the change in substrate potential under the NMOS transistors is much less in the dual-well technology than in the p-well of the triple-well technology for high LET ion strikes. The charge confinement in the well affects other OFF transistors in the same well. When the ion hit occurs, the nMOS transistor (MN1) is OFF and when it collects charge, the output of inverter I1 goes from HIGH to LOW. This turns the nMOS transistor (MN2) in the opposite inverter (I2) OFF and the pMOS transistor (MP2) ON. The output of the inverter I2 goes from LOW to HIGH and the OFF nMOS transistor (MN2) collects the residual charge in the p-well of the triple-well system. As MN2 collects charge, it turns ON and the output of the inverter I2 goes from HIGH to LOW and subsequently the feedback mechanism inherent in the SRAM cell changes the output of the inverter I1 from LOW to HIGH. Thus the original state of the cell is restored. The entire process is shown schematically in Fig. 11. We term this phenomenon "Single Event Upset Reversal" which is similar to the "Pulse Quenching" mechanism observed in combinational logic, also known as "Reinforcing Charge Collection" [30].



(a) Dual Well at High LET



(b) Triple Well at High LET

Fig. 10: Potential in the p-well in the (a) dual-well and (b) triple-well device 50 picoseconds after being struck with a particle of LET of 20 MeV-cm^2/mg. The potential of the p-well is higher in the triple-well device than in the dual-well device.

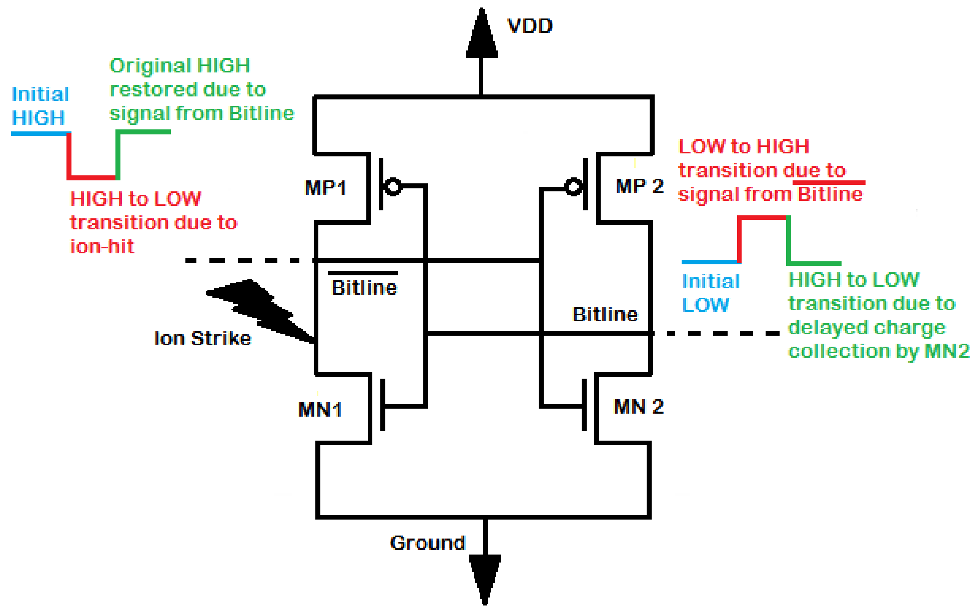


Fig. 11: A schematic of a standard SRAM cell illustrating the upset reversal mechanism observed in a triple-well SRAM cell.

Figs. 12-15 show the drain voltage perturbations of both nMOS transistors (MN1 and MN2) after an ion hit. For a low-LET particle hit (5MeV-cm^2/mg, in this case), both the dual-well nMOS transistors upset, but the triple-well transistor shows the signs of a delayed charge collection (Fig. 12). This effect is more pronounced in Fig. 13. In the triple-well system, the second nMOS transistor (MN2) tries to recover due to residual charge collection, but there is not enough charge available for the drain voltage to recover fully to its original value. On the other hand, for a high-LET particle strike (typically above 15 MeV-cm^2/mg), the amount of charge available for the second triple-well NMOS transistor (MN2) to collect is sufficient to reverse the upset. Fig. 14 shows this effect where the drain of the transistor MN1 was struck with an ion of LET 20 MeV-cm^2/mg. Here, the drain voltage of MN2 fully recovers to its original state. The mechanism described above is actually two upsets in sequence happening within an SRAM cell. Fig. 13 shows the drain voltages for an ion hit of LET 35 MeV-cm^2/mg. It shows that the system recovery time now increases to a few nanoseconds.

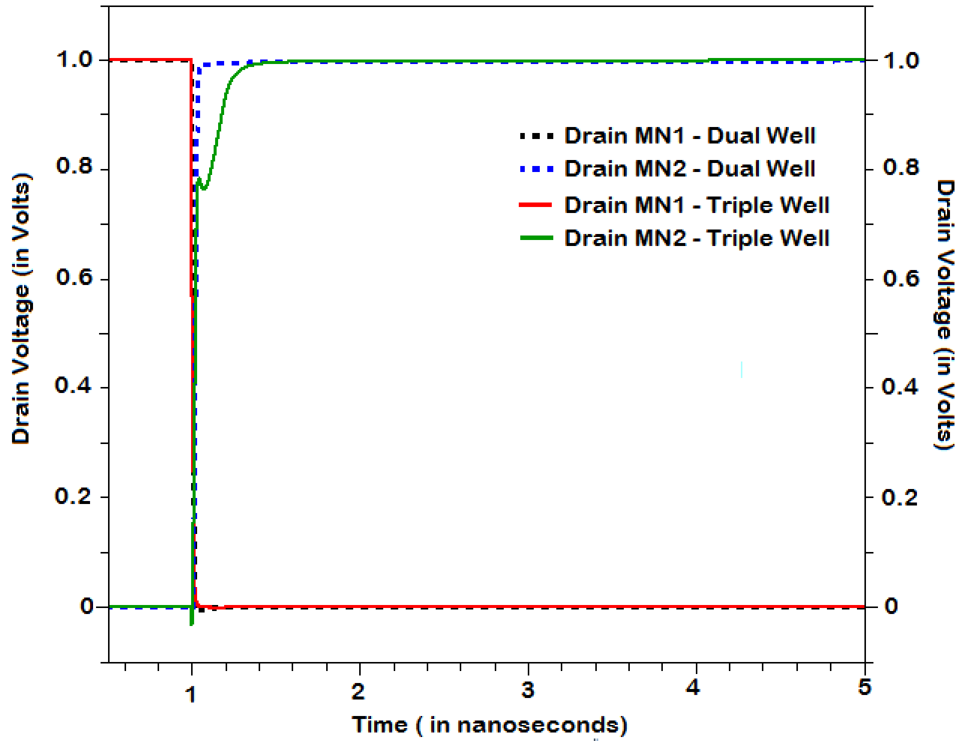


Fig. 12: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 5 MeV-cm^2/mg

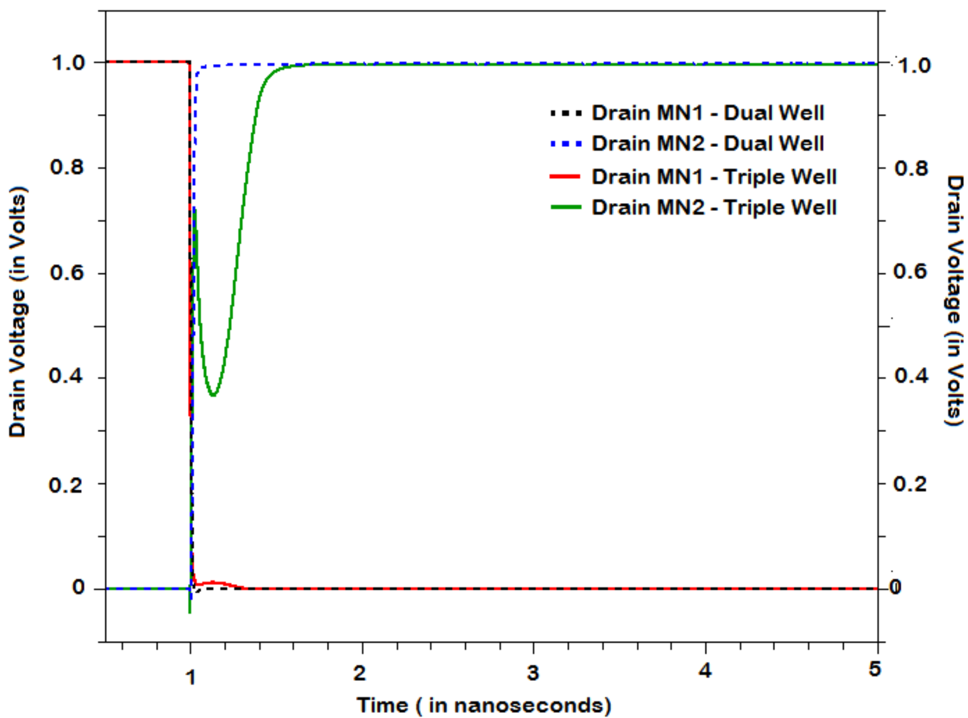


Fig. 13: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 10 MeV-cm^2/mg

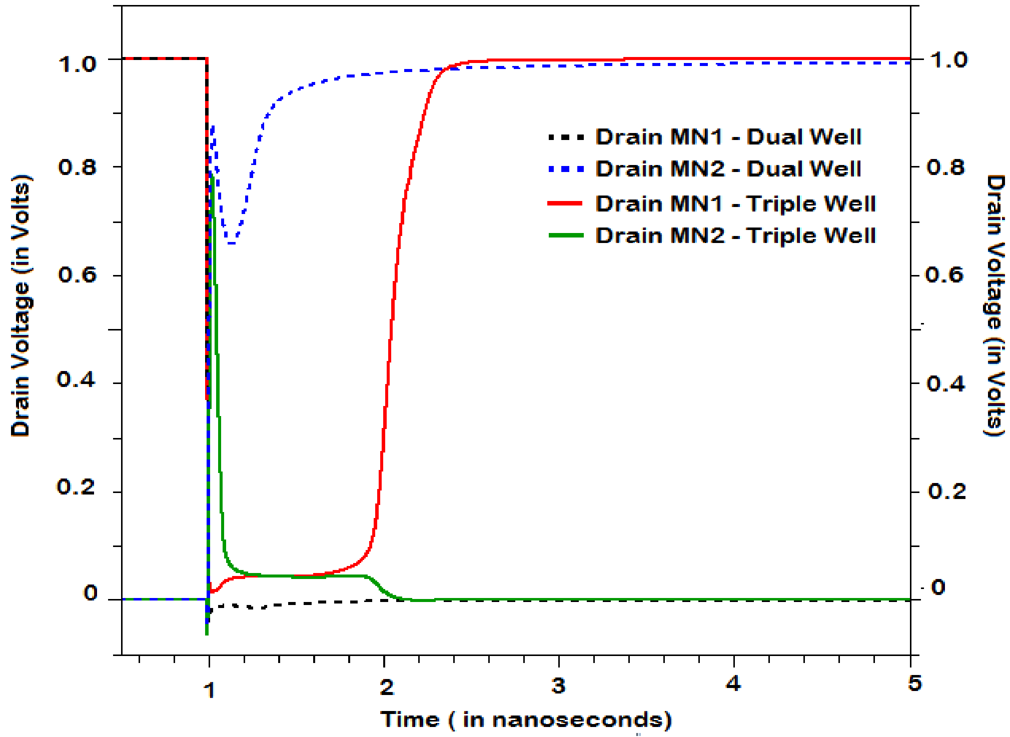


Fig. 14: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 20 MeV-cm^2/mg

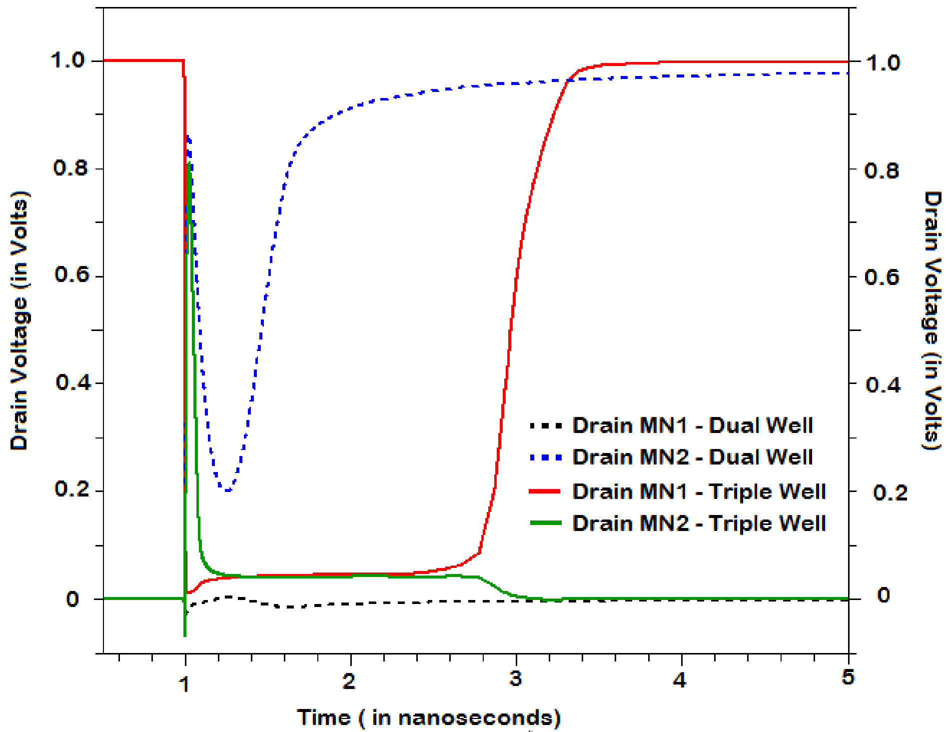


Fig. 15: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 35 MeV-cm^2/mg

Although the dual-well system shows signs of delayed of charge collection, there is never enough charge in the system to trigger the upset reversal mechanism.

Figs. 16 and 17 show the carrier concentration in the p-well of a dual- and triple-well system for a particle strike of LET 25 MeV-cm^2/mg. The concentration of the holes in the p-well determines whether the p-well is de-biased. Thus, as long as there are excess carriers in the system, the OFF transistors can collect charge. In the dual well, the hole concentration of the well 1.1 ns after the ion-strike is similar to the pre-strike condition, while in the triple well, enough charge is left in the system for the OFF nMOS transistor to collect and turn ON.

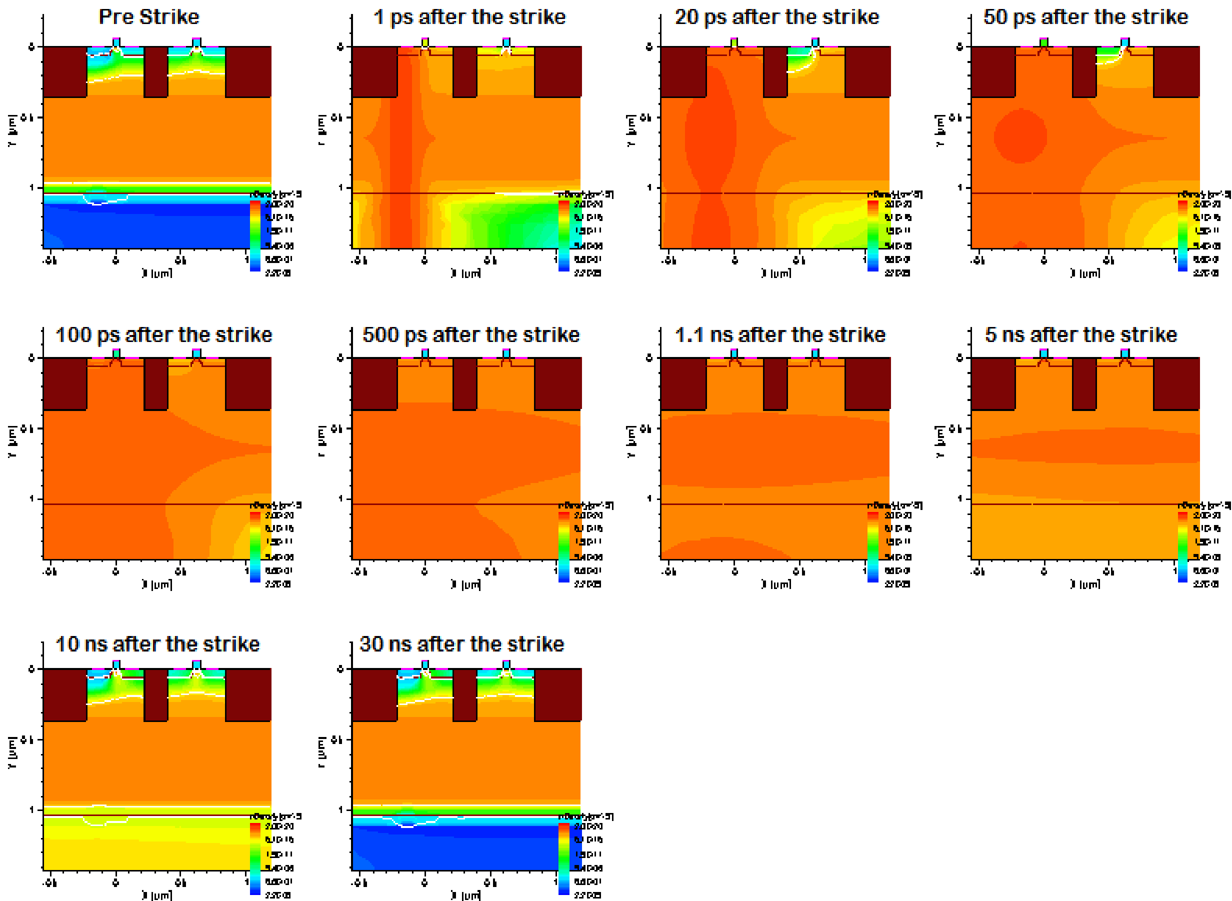


Fig. 16: Carrier (Hole) concentration in the p-well of the triple-well SRAM cell at various time instants after the drain of transistor MN1 is hit with an ion of LET: 25MeV-cm^2/mg.

In the dual-well system, 5 ns after the strike, almost all of the deposited charge has moved out of the system while in the triple-well, the well is still de-biased. Charge collection by the second NMOS transistor is less in dual-well SRAM cells.

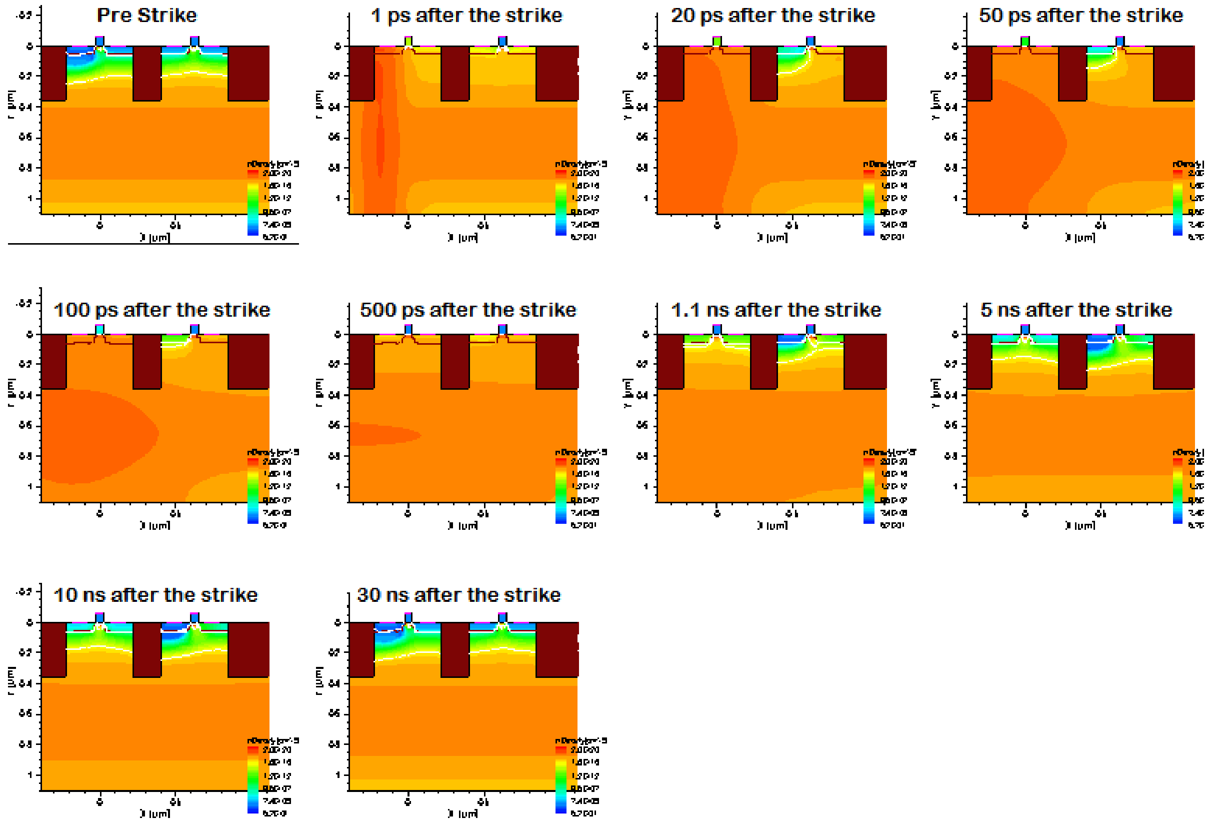


Fig. 17: Carrier (Hole) concentration in the p-well of the dual-well SRAM cell at various time instants after the drain of transistor MN1 is hit with an ion of LET: 25MeV-cm^2/mg.

Fig. 18 shows the current pulse and the charge collected by NMOSFET MN2 in both the dual- and triple-well systems for an ion-strike of LET = 20 MeV-cm^2/mg. As a result of this delayed multiple node charge collection, the SRAM cell restores back to its original state, thereby nullifying the effects of the ion-strike. This phenomenon may decrease the overall soft error rates for SRAM cells at high LETs in a triple-well process.

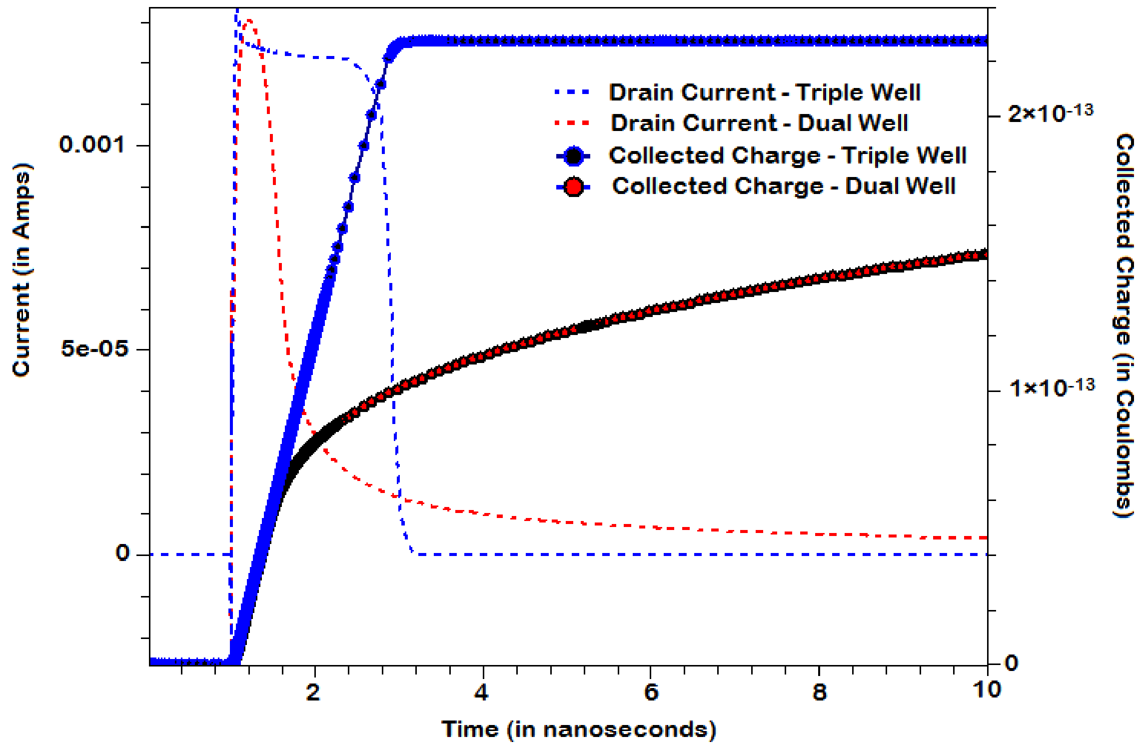


Fig. 18: Current pulse and charge collected by the second NMOS transistor (MN2) in a dual- and triple-well SRAM cell after the drain of the NMOSFET MN1 is struck with an ion of LET 20 MeV-cm^2/mg.

3.5 Very High LET Particle Strike

The simulations were extended for very high LETs (>40 MeV-cm^2/mg) for both dual- and triple-well structures. It was seen in Fig. 15 that the second transistor in the dual-well system showed effects of delayed charge collection. For higher LETs, the dual-well systems show more pronounced effects of multiple node charge collection, but the system never recovers, unlike triple-wells. Figs. 19-22 show the drain voltages of the SRAM cell on being struck with ions of LETs 45, 55, 65 and 75 MeV-cm^2/mg. It is observed that the cell recovery time increases with increasing LET for triple-well structures. Delayed charge collection is observable in dual-well structures as well, but the SRAM cells never recover to their original states.

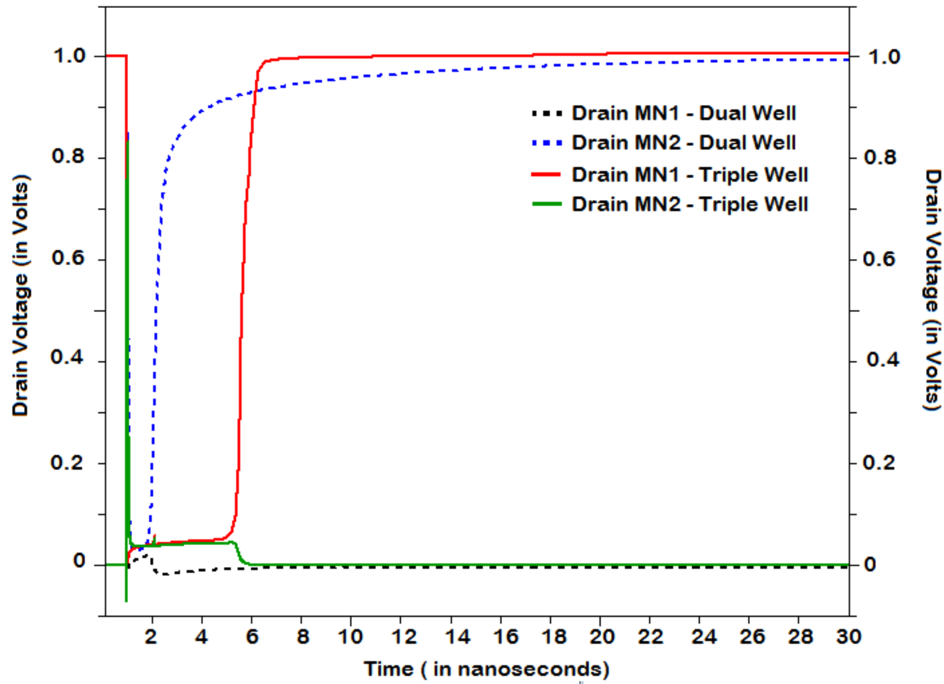


Fig. 19: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 45 MeV-cm^2/mg

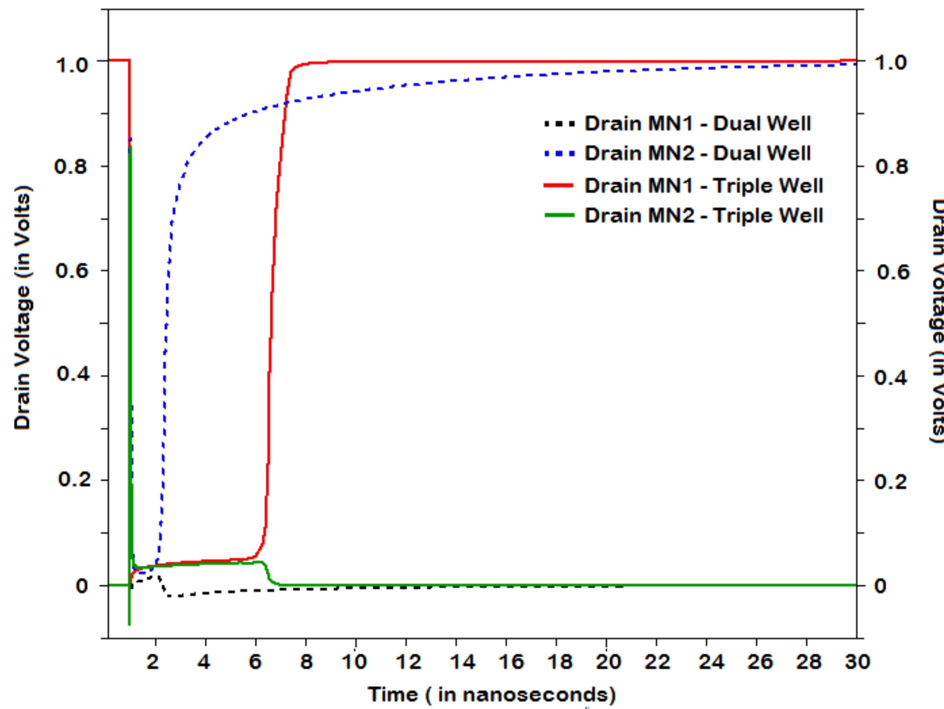


Fig. 20: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 55 MeV-cm^2/mg

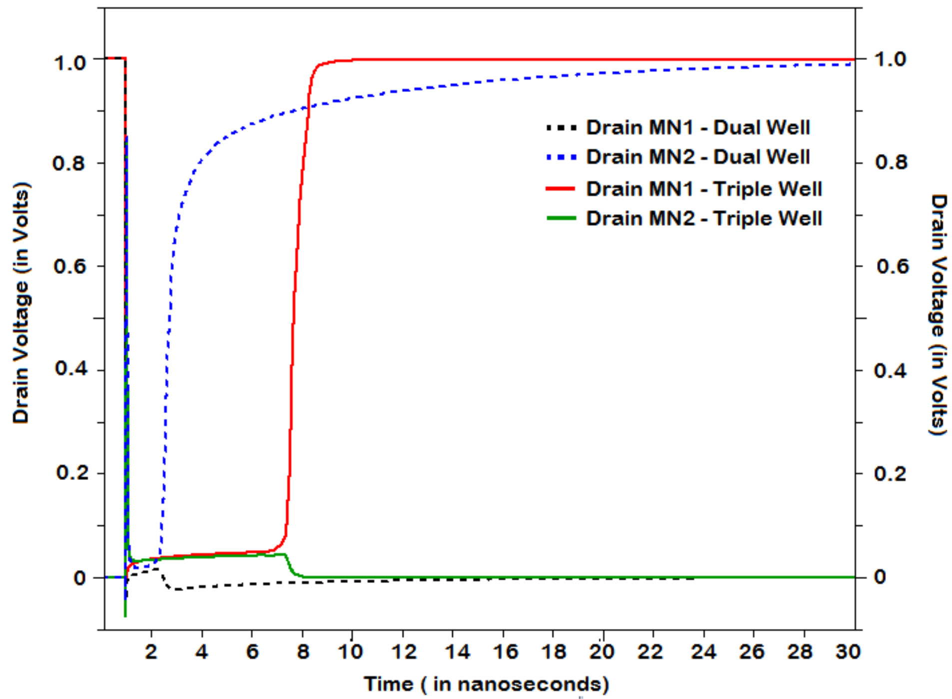


Fig. 21: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 65 MeV-cm^2/mg

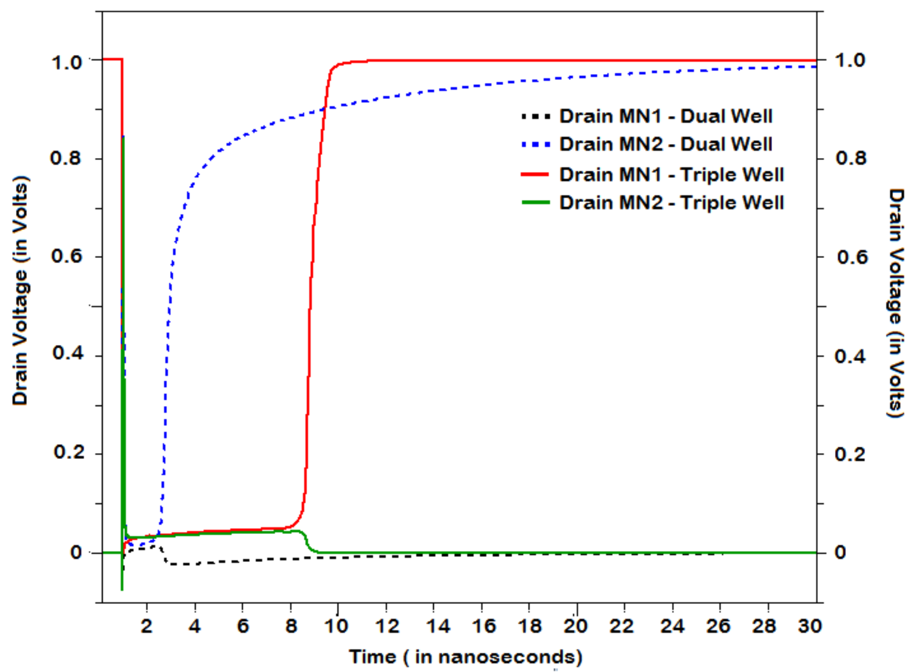


Fig. 22: Drain Voltage in both dual-well and triple-well NMOSFETs devices when the drain of NMOSFET MN1 is struck with an ion of LET 75 MeV-cm^2/mg

3.6 Angular Incidence

The previous section dealt with ion strikes at normal incidence. In this section, we explore ion strikes occurring at certain angles. Two angles of incidence (30° and 60°) are discussed for three different LETs (10, 25 and 35 MeV-cm^2/mg.). Two SRAM cells were simulated using TCAD in an ALL-1 pattern. The 2D cross-section of the structure is shown in Fig. 23.

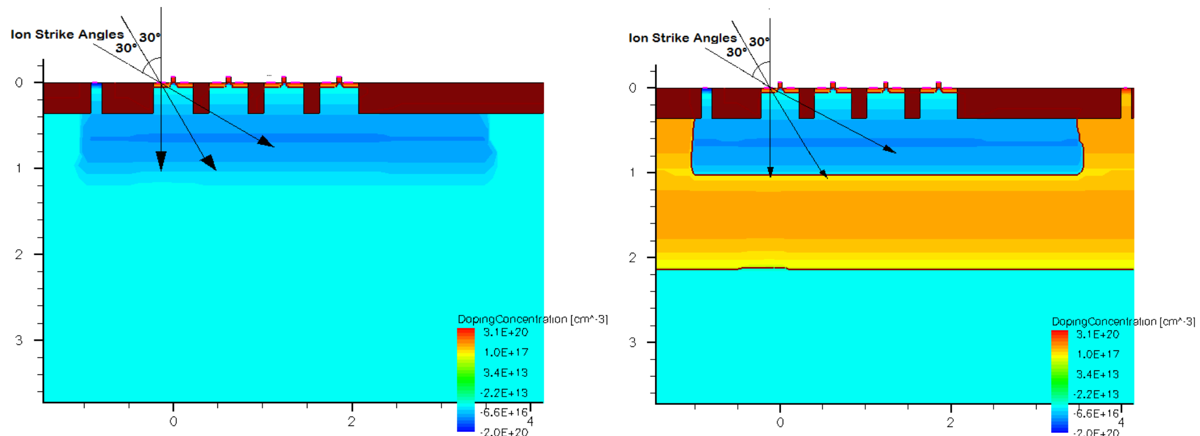
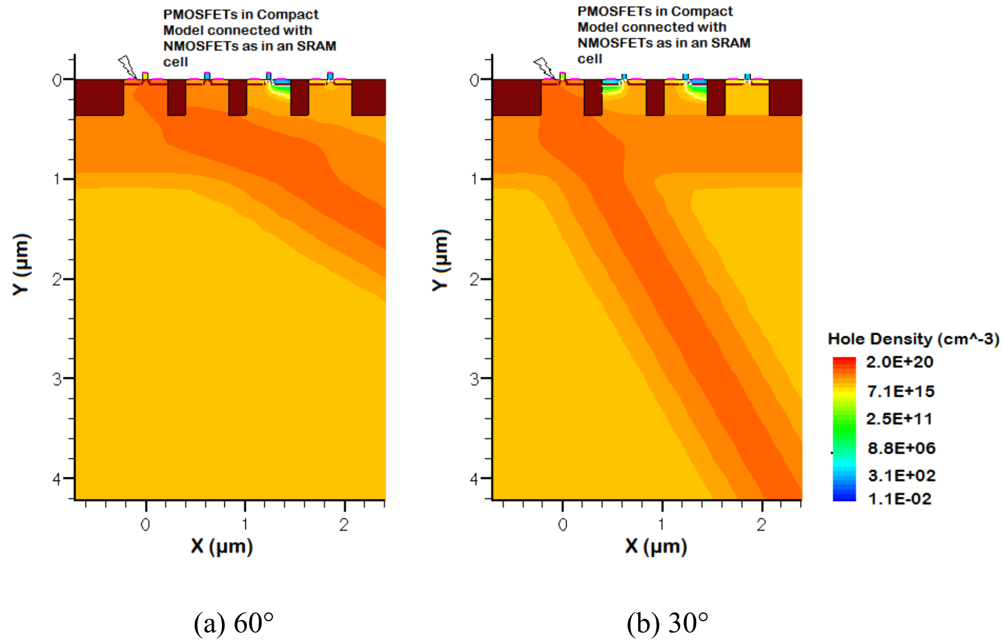


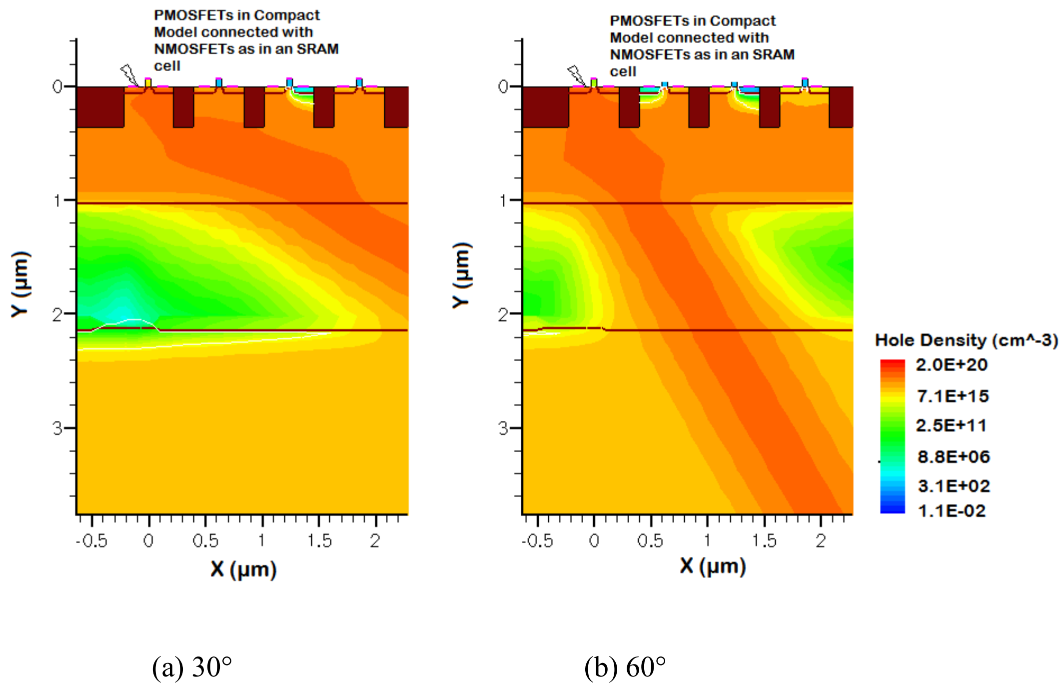
Fig. 23: 2D cross-section of the dual- and triple-well NMOSFETs belonging to two different SRAM cells.

It is observed that strikes at 30° or 60° angle of incidence create a larger charge cloud compared to that of normal incidence. This is shown in Figs. 24 and 25. Thus, greater numbers of SRAM cells are affected by the charge cloud. Because of the charge confinement in triple-well systems, the charge cloud impacts transistors much more severely than it does in dual-well systems. The voltage characteristics of the NMOS transistors of both the SRAM cells are shown in Figs. 26-28 for 30° angle of incidence. It is seen that for low LET (5 MeV-cm^2/mg) for 30° angle of incidence, both the SRAM cells upset in case of the dual-well system while one of the triple-well SRAM cell (the one hit) upsets. However, for moderate to high LETs (15 MeV-cm^2/mg and 35 MeV-cm^2/mg), the struck SRAM cell recovers its original state because of the single event upset reversal mechanism. However, the second cell still upsets whereas in triple-well systems, both the SRAM cells recover.



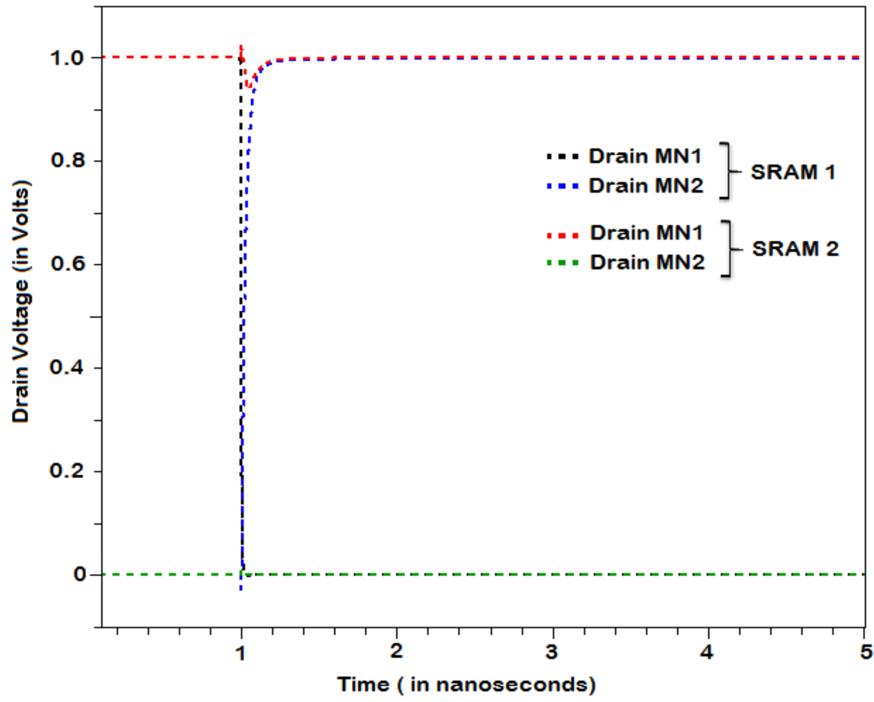
(a) 60° (b) 30°

Fig. 24: Charge cloud in the p-well of a dual-well SRAM cell for a) 60° and b) 30° angle of incidence 50 ps after the ion-hit. It is seen that the charge cloud for the 60° angle of incidence is larger compared to that for the 30° angle of incidence.

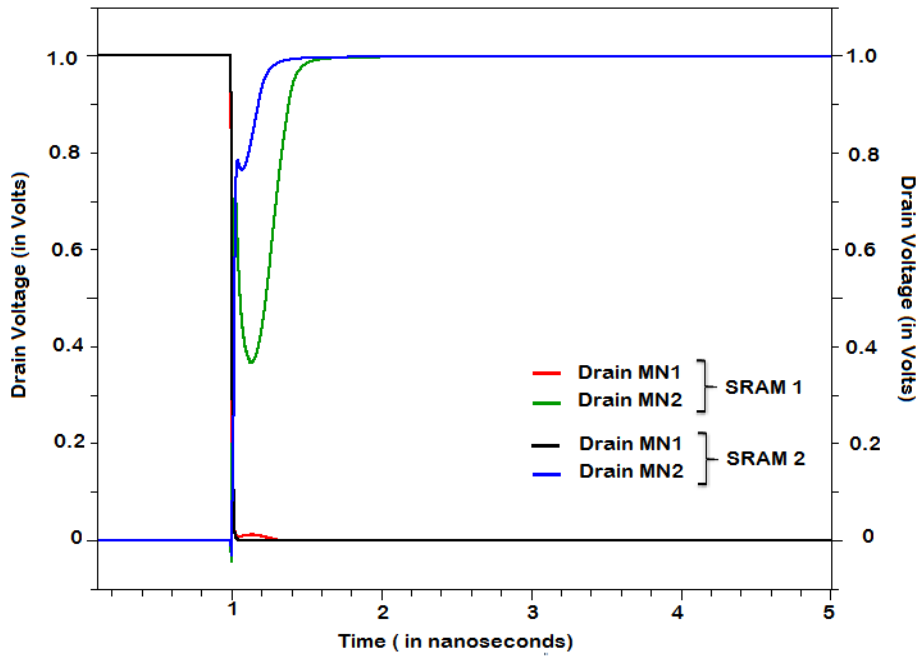


(a) 30° (b) 60°

Fig. 25: Charge cloud in the p-well of a dual-well SRAM cell for a) 60° and b) 30° angle of incidence 50 ps after the ion-hit. It is seen that the charge cloud affects the SRAM cells in the same well more for the 30° angle of incidence.

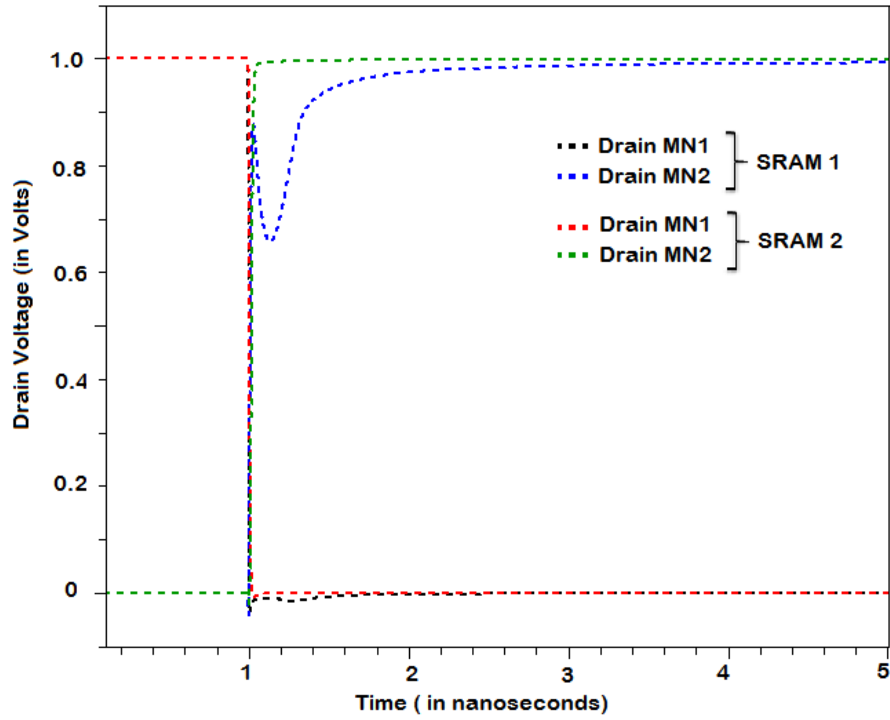


(a) Dual-well: SRAM 1 upsets, SRAM 2 does not

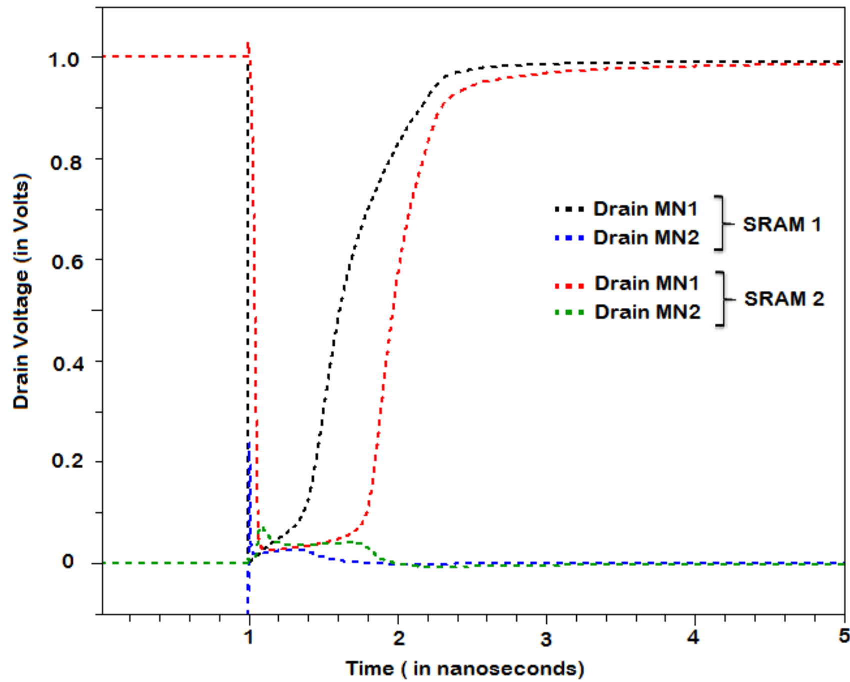


(b) Triple-well: Both SRAMs upset

Fig. 26: Drain Voltage in both dual-well NMOSFETs when the drain of NMOSFET MN1 of SRAM 1 is struck with an ion of LET 5 MeV-cm^2/mg at an angle of 30°

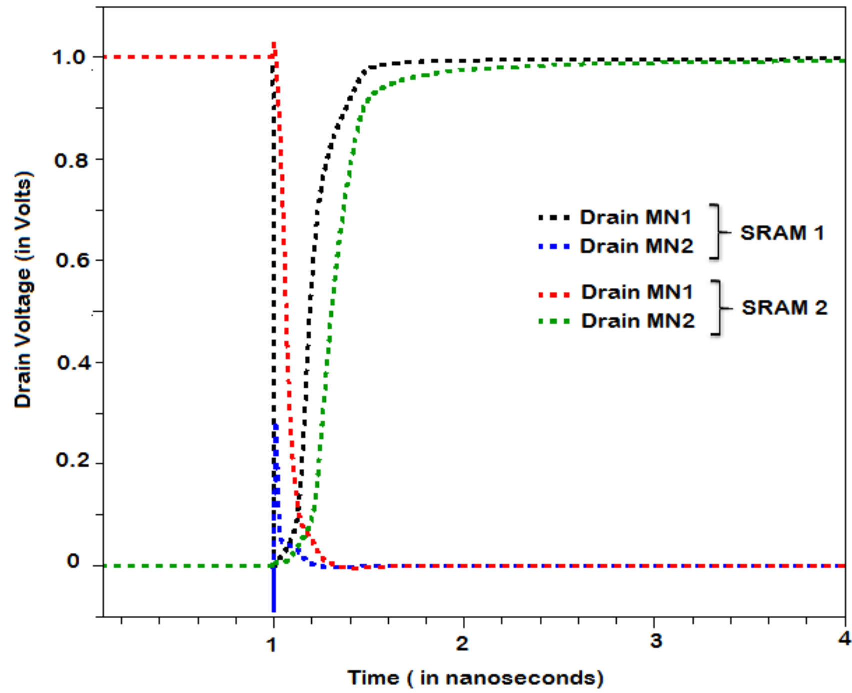


(a) Dual-well: Both cells upset

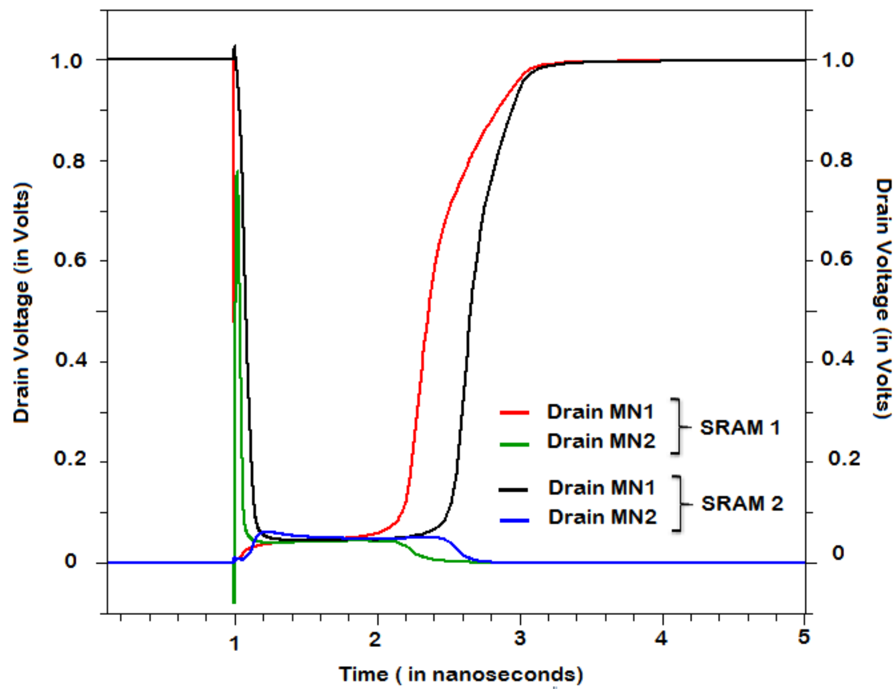


(b) Triple-well: SRAM 1 recovers

Fig. 27: Drain Voltage in both dual-well NMOSFETs when the drain of NMOSFET MN1 of SRAM 1 is struck with an ion of LET 15 MeV-cm^2/mg at an angle of 30°



(a) Dual-well: SRAM 1 recovers



(b) Triple-well: Both cells recover

Fig. 28: Drain Voltage in both dual-well NMOSFETs when the drain of NMOSFET MN1 of SRAM 1 is struck with an ion of LET 35 MeV-cm^2/mg at an angle of 30°

For 60° angle of incidence, the effects of multiple node charge collection are even more predominant. While for low and moderate LETs, the trend was similar to as shown in Figs. 24-25, for high LET ion strikes (30 MeV-cm^2/mg), both the SRAM cells in the dual-well system upset.

3.7 Summary

This chapter dealt with the simulation results of heavy ion irradiation on dual- and triple-well SRAM cells over a wide range of particle LETs. Simulations were done for normal and angular incidence. It was observed that nMOS transistors in a triple-well usually collect more charge during a single event strike than those in a dual-well due to charge confinement within the well. For high LET values, however, charge collection at more than one node in a triple-well technology may restore the original state of the SRAM cells in the vicinity of the strike. Thus, for high-LET particles (typically above 15 MeV-cm^2/mg), the triple-well SRAMs do not always upset. We describe this phenomenon as "single-event upset reversal". This phenomenon decreases the soft-error rate in certain circumstances, particularly those dominated by ions with high LET values. Dual-well nMOS transistors collect less charge for low LET strikes and thus typically have a lower error rate for environments in which low LET particles dominate.

For angled strikes, it was seen that for moderate and high LETs, the single event upset reversal was observed in dual-well NMOSFETs as well. However, the effect was much more pronounced in case of triple-well structures. In the following chapter, the experimental results for alpha, neutron and heavy ion irradiation on 40 nm dual- and triple-well SRAM cells are discussed as a verification of the theory developed in this chapter.

CHAPTER IV

ALPHA, NEUTRON AND HEAVY ION IRRADIATION

4MB SRAM chips were fabricated using two different process technologies. The design and layouts were similar, with the only difference being that one chip was fabricated in a dual-well CMOS process and the other in a triple-well process technology. The chips were subjected to alpha-particle, neutron, and heavy-ion irradiations. The thickness of the back-end-of-line overlayers at this technology node is approximately 10 µm.

4.1 Alpha-Particle Irradiation

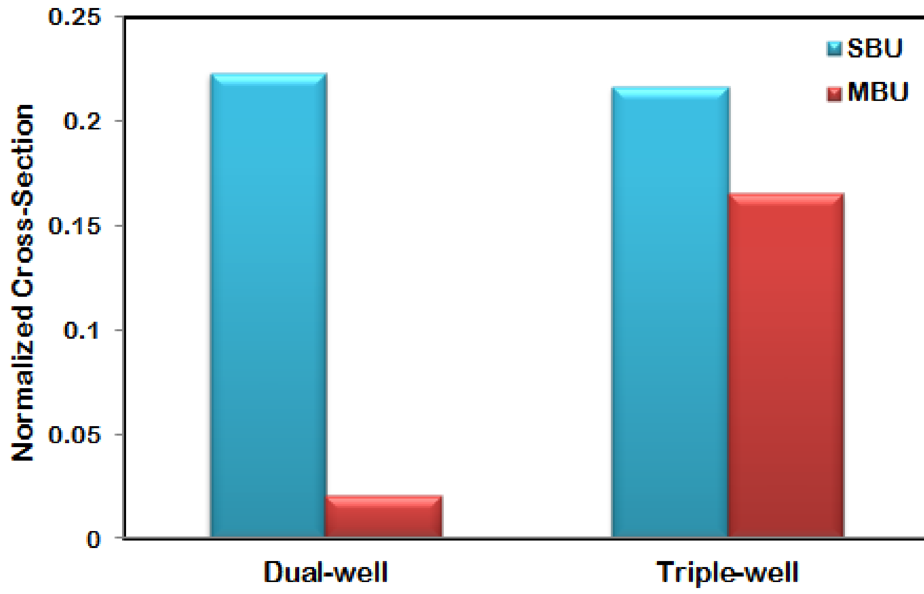
4.1.1 Experimental Setup

Alpha-particle soft error testing was conducted using Americium-241at Vanderbilt University. The source was deposited as a liquid on a thin foil and allowed to dry. The source spot size was 20 mm in diameter and the deposited activity level was 300 nCi. The flux measured at the surface of the source was 6.4×10^{6} $hr^{-1}cm^{-2}$. All parts were opened to expose the die face and the ^{241}Am source was mounted at a distance of 15 mm above the SRAM. The test procedure was compliant with the JEDEC SER test standard labeled JESD89A [34]. The tests were carried out for the Checkerboard, ALL-0 and ALL-1 patterns.

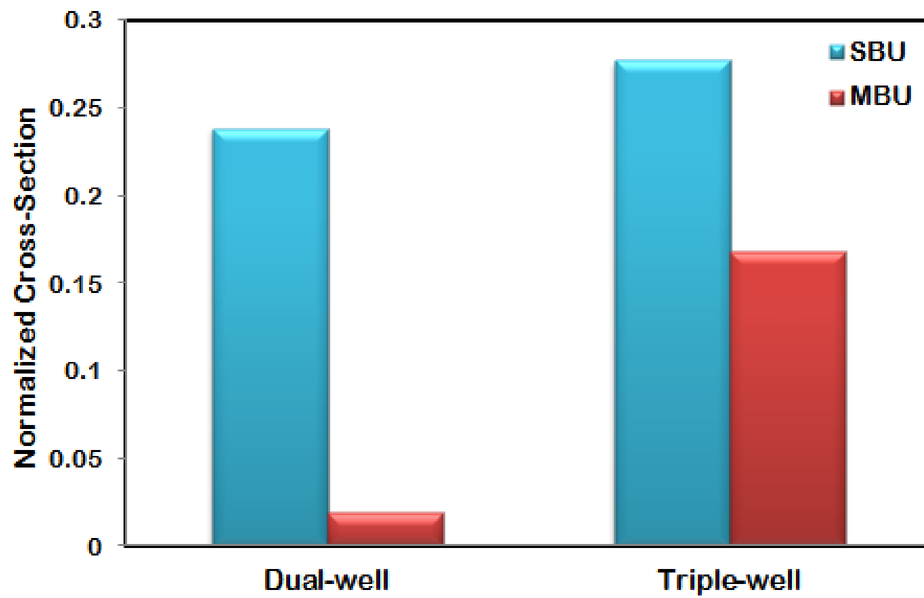
4.1.2 Results

The simulation results for low-LET ion strikes indicated that dual-well transistors collect less charge and are less vulnerable to upsets. The experimental results from alpha irradiation showed a similar trend. Fig. 30 shows the Single Bit Upsets (SBUs) and Multiple Bit Upsets (MBUs) observed in the dual-

and triple-well systems on alpha particle irradiation while Fig. 31 shows the location of errors with respect to the well-taps.

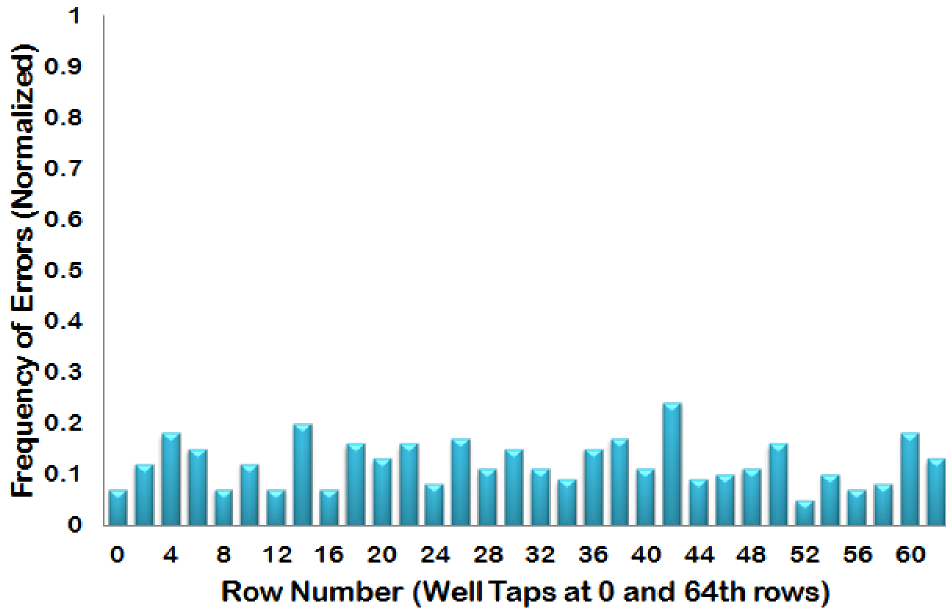


(a) Checkerboard Pattern

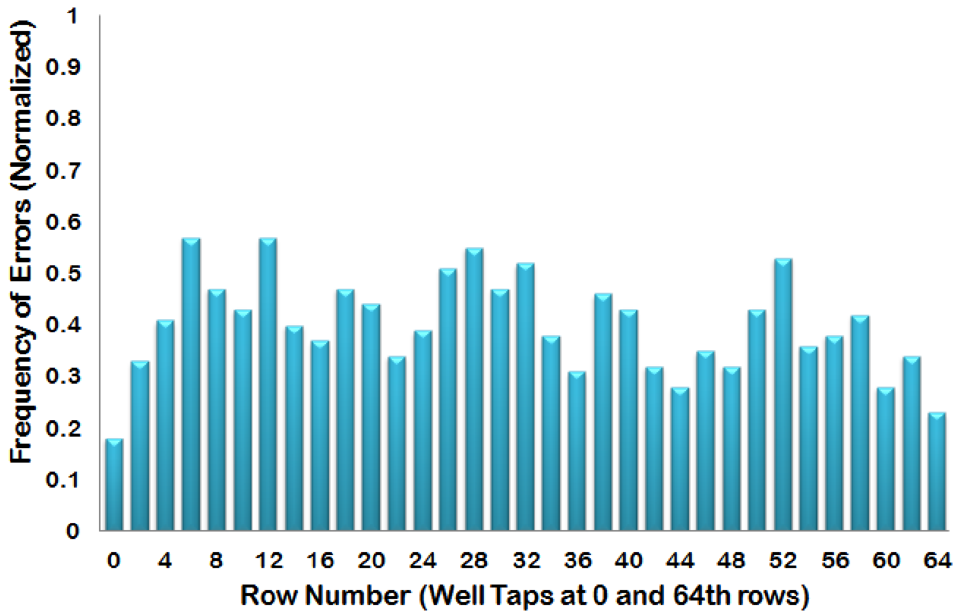


(b) ALL-0 Pattern / ALL-1 Pattern

Fig. 29: SBU and MBU in the dual- and triple-well SRAM cells after being irradiation with alpha particles



(a) Dual-well



(b) Triple-well

Fig. 30: Frequency of errors with respect to location for alpha particle irradiation for (a) dual-well and (b) triple well SRAM cells for checkerboard pattern.

It is seen that the number of errors is much less in dual-well systems compared to triple-well structures. The concentration of errors does not vary a lot with respect to the location. However, near the

well taps, the triple-well cells records the least number of errors as the charges are quickly removed from the system. Alpha particle energy deposition is in the same range as low-LET ions. The results show that dual-well SRAM cells perform better compared to the triple-well systems for low energy deposition. This is similar to the simulation results for low LET ions.

4.2 Neutron Irradiation

4.2.1 Experimental Setup

SRAM circuits fabricated in dual-well and triple-well 65-nm technologies were irradiated with high-energy neutrons at the Weapon Neutron Research test facility, Los Alamos Neutron Science Center (LANSCE). This neutron energy spectrum, shown in Fig. 31, closely resembles the sea-level neutron spectrum for energies from 10 to 500 MeV. The exposure was carried out at room temperature and with a

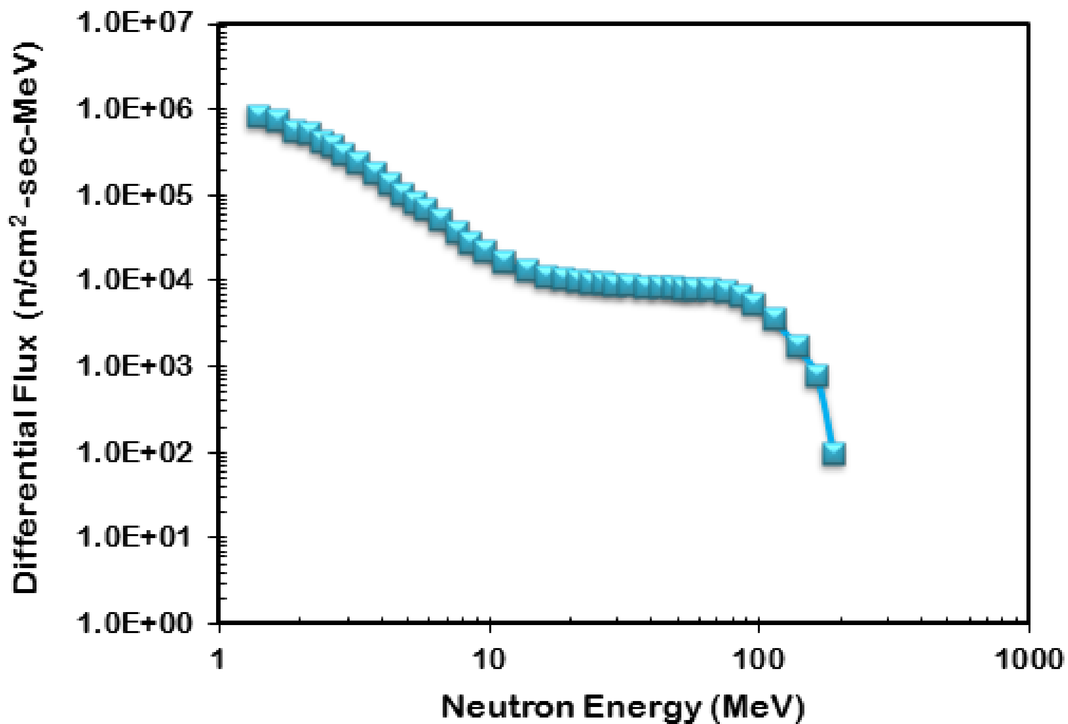


Fig 31: Energy spectrum of the LANSCE neutron beam. This spectrum closely resembles the energy spectrum of terrestrial neutrons.

checkerboard pattern over a wide range of supply voltages and temperature. The range of LETs of the secondary particles generated by the neutrons is 2-12 MeVcm^2/mg, as shown in Fig. 32.

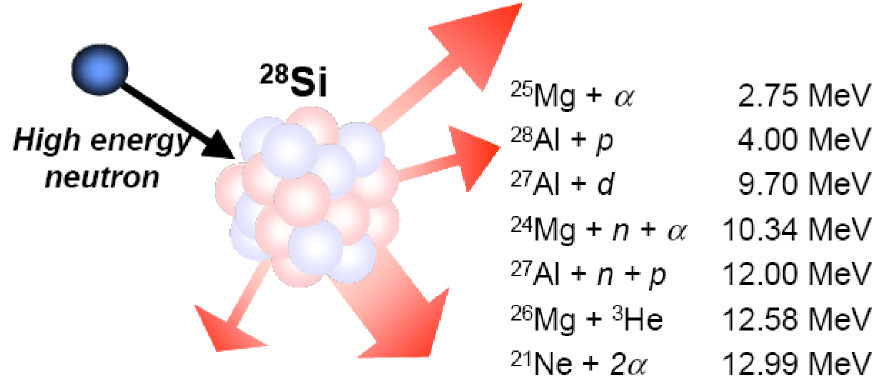


Fig. 32: Secondary particles generated when a high energy neutron interacts with silicon

The experimental conditions are listed in the following table.

TABLE I: EXPERIMENTAL SETUP FOR NEUTRON IRRADIATION TESTS

Test Conditions	Voltage (in Volts)	Temperature (in °C)	
1	1.2	35	
2	1.1	35	Voltage Dependence Test
3	1.3	35	

4.2.2 Experimental Results

The results show that for triple-well technology, the error rates are much higher compared to dual-well technology, as shown in Fig. 33 below. In highly scaled technologies, multiple-cell upsets contribute significantly to the total error rate due to charge-sharing between adjacent transistors. The number of multiple-bit upsets was also higher in case of triple-well SRAM cells.

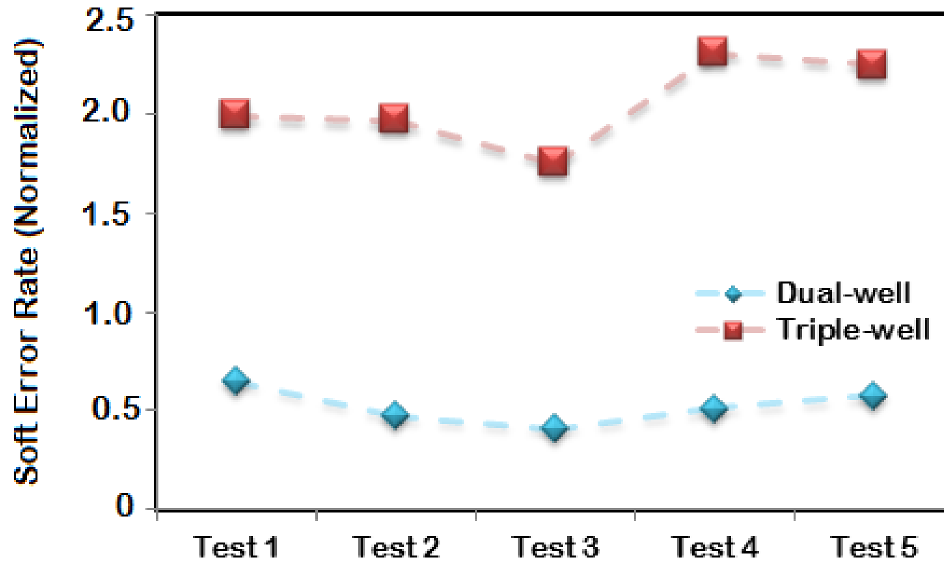


Fig. 33: Soft error rate in 65 nm dual- and triple-well SRAM cells after being irradiated with high energy neutrons

4.3 Heavy Ion Irradiation

4.3.1: Experimental Setup

Heavy-ion tests were performed over a wide range of LETs at Lawrence Berkley National Laboratory (LBNL) at V_{DD} = 1.2 V with the SRAMs in either a checkerboard or an ALL-0 pattern. The design and layout for the dual- and triple-well structures were similar and both were fabricated in a commercial 40 nm bulk CMOS process. The total thickness of the back-end-of-line overlayers at this technology node is approximately 10 µm. A 16 MeV/nucleon cocktail was used for the tests. The tests were carried out with four heavy ions (N, Ar, Cu and Kr) at normal incidence, 60° N-S (along bitlines) and 60° W-E (along wordlines). The range of particle LETs used was 1–30 MeV-cm^2/mg. Table I lists the ion beams, the corresponding energy, LET values and the ranges.

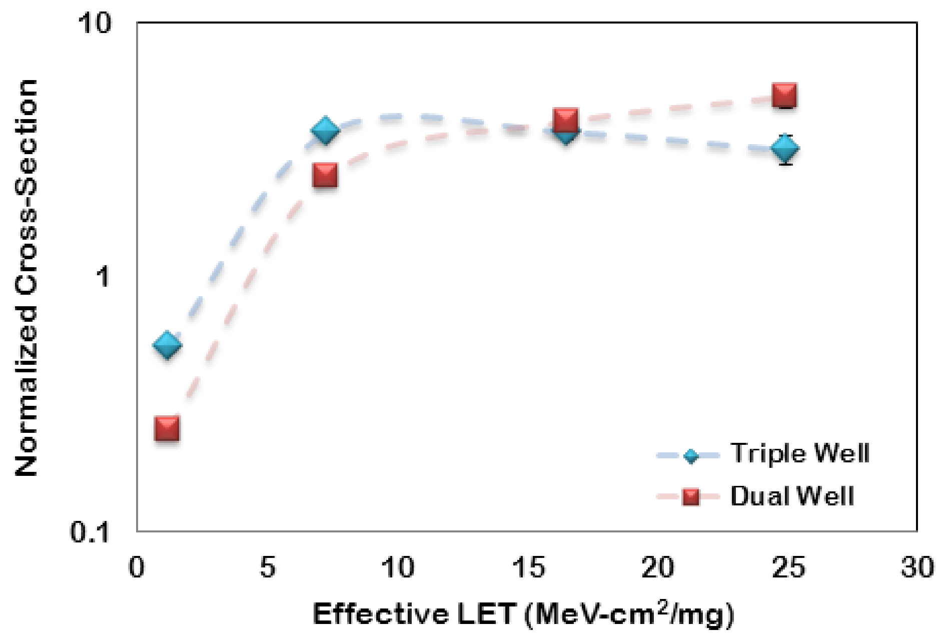
TABLE II

16 MEV/NUCLEON COCKTAIL COMPONENTS

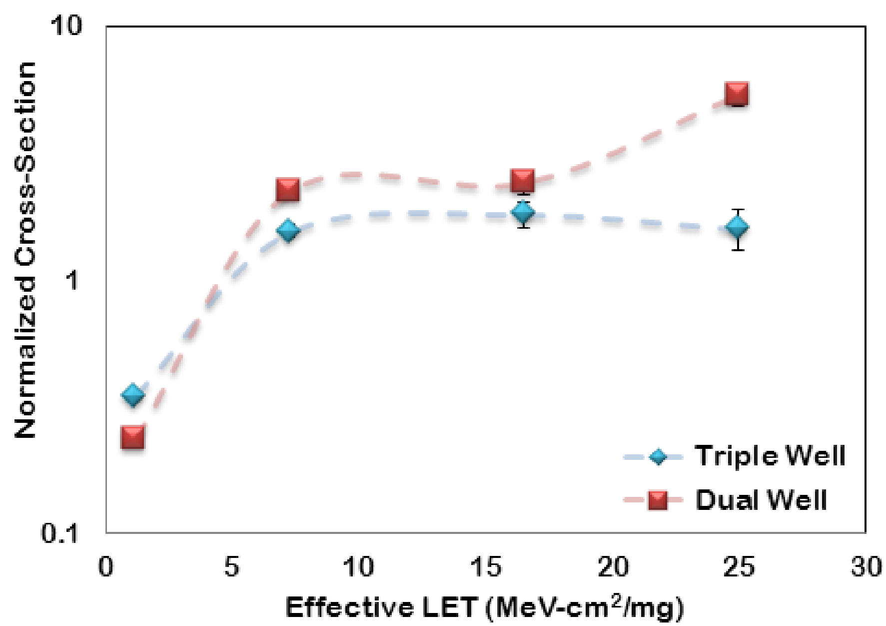
Ion	**Energy (MeV)**	**LET ($MeV/mg/cm^2$)**	**$Range_{Bragg}$ (µm)**	**$Range_{final}$ (µm)**
$^{14}N^{+5}$	234	1.16	505	508
$^{40}Ar^{+14}$	642	8.34	243	256
$^{63}Cu^{+22}$	1007	16.53	169	190
$^{78}Kr^{+27}$	1226	24.98	142	163

4.3.2: Experimental Results: Normal Incidence

The test results for normal incidence are shown in Fig 34. The data in the figure are normalized with a single factor for effective presentation. Based on the number of events measured, the error bars for these data are less than 10% of the mean value across all LETs. For particles with low LET, the triple-well structures have a greater soft-error cross-section. As the LET of the incident particles increases, the dual-well designs become more vulnerable compared to the triple-well designs. For SRAMs built in advanced-technology nodes, multiple-bit upsets (MBUs) are predominant [10]. Figs. 35 and 36 show the single-bit upset (SBU) and MBU cross-sections for dual- and triple-well SRAM cells at low and high LETs. For low-LET particle strikes, the MBU cross section is higher for triple-well structures compared to dual-well structures, whereas for particles with higher LETs, MBUs increase significantly in dual-well designs. Both SBU and MBU events are lower for triple-well devices compared to dual-well devices for high-LET particle strikes.

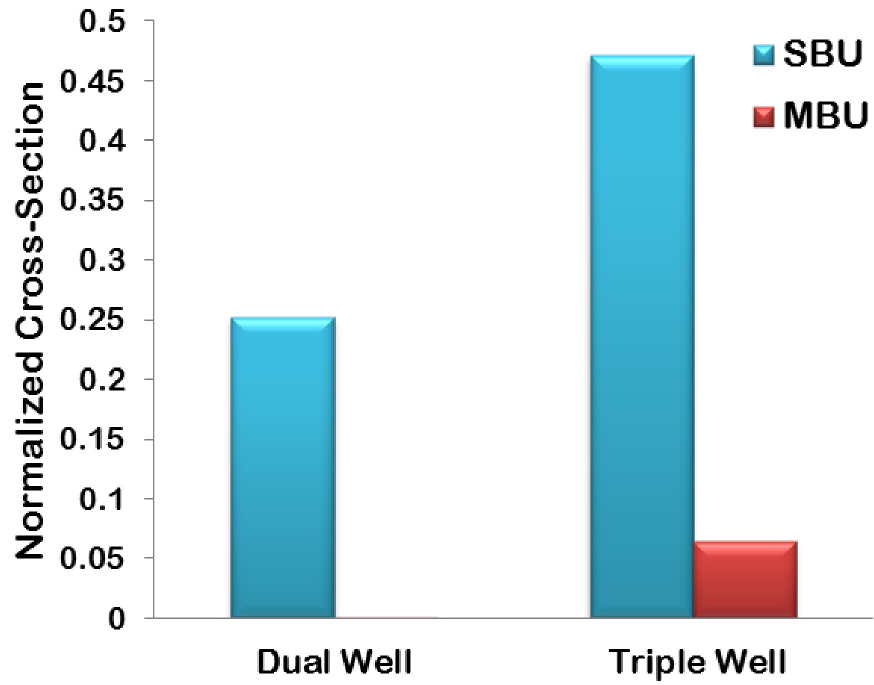


(a)

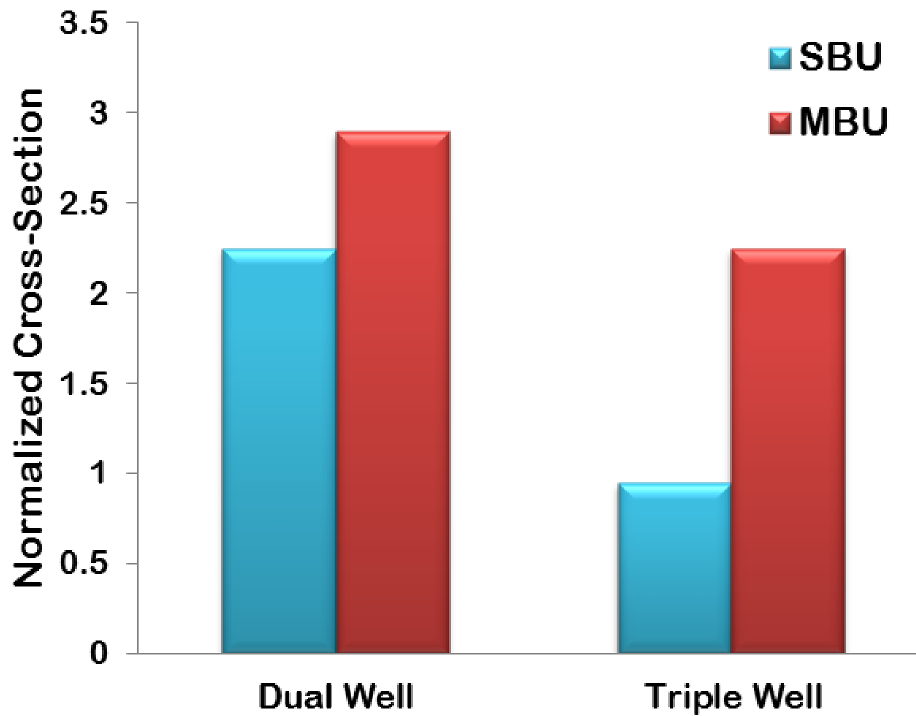


(b)

Fig 34: Normalized cross section vs. LET for dual-well and triple-well devices for normal incidence irradiation with a (a) checkerboard pattern and (b) ALL-0 pattern.

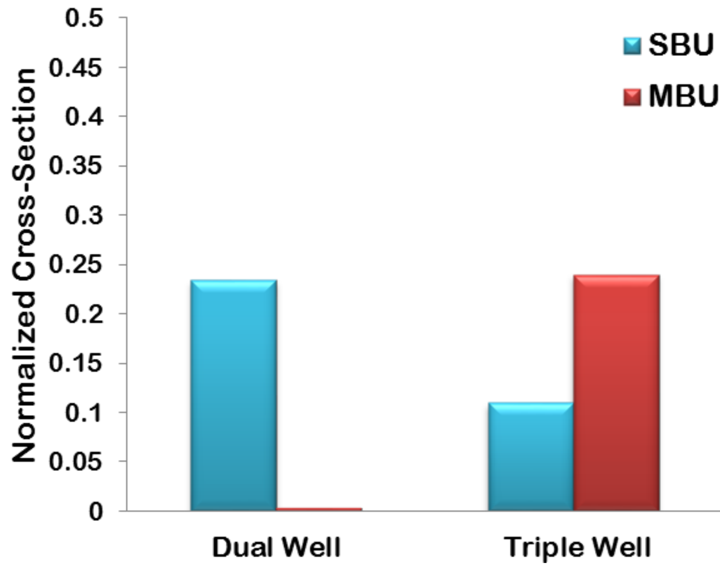


(a) LET = N ion: 1.16 MeV-cm^2/mg

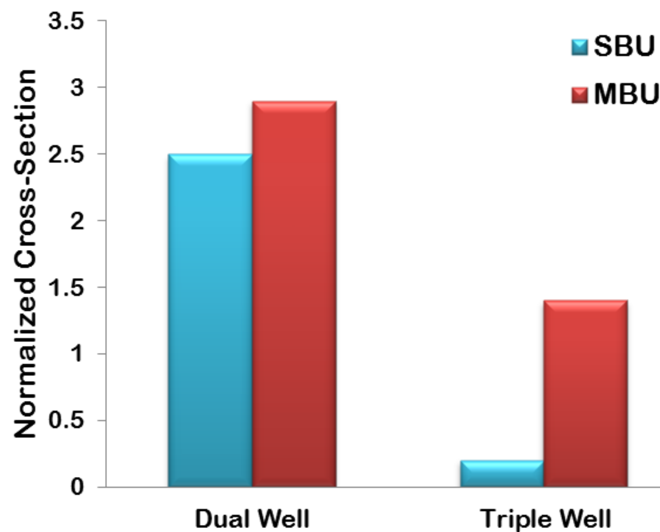


(b) LET = Kr ion: 24.98 MeV-cm^2/mg

Fig.35: a) SBU and MBU for normal strikes for (a) low LET and (b) high LET for the checkerboard pattern.



(a) LET = N ion: 1.16 MeV-cm^2/mg



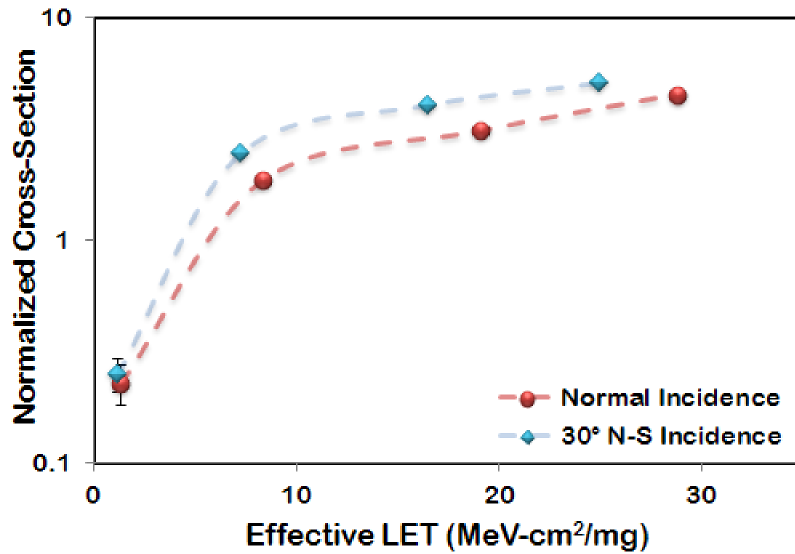
(b) LET = Kr ion: 24.98 MeV-cm^2/mg

Fig.36: a) SBU and MBU for normal strikes for (a) low LET and (b) high LET for the ALL-0 pattern.

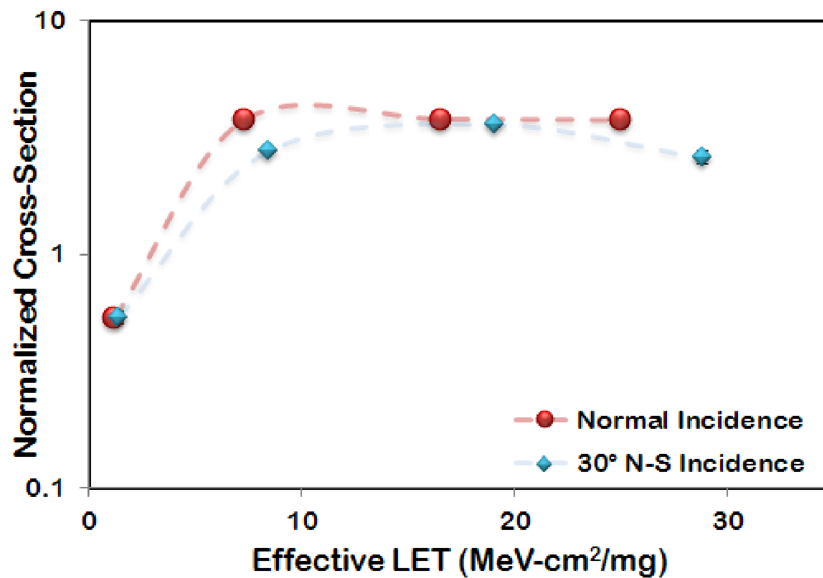
The results show that at low LETs dual-well transistors collect less charge, thus they are less vulnerable to upsets. However, at moderate to high LETs, multiple node charge sharing triggers the single event upset reversal mechanism observed in the previous chapter to lower the overall error rates of the triple-well NMOS transistors.

4.3.3 Experimental Results: Angular Incidence

It was noted in the previous chapter that the single event upset reversal mechanism is more pronounced for angular strikes. Fig. 37 below shows the responses of the dual- and triple-well for angled strikes. This verifies that the mechanism is effective for tilted strikes.

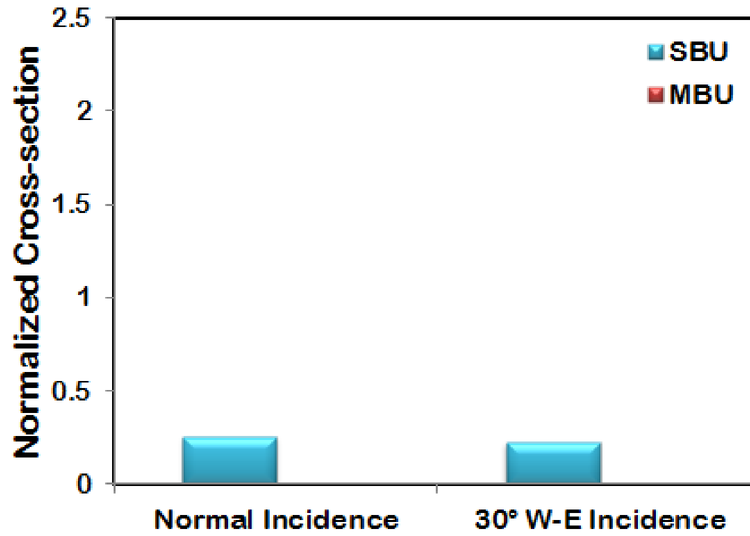


(a) Dual-well SRAM

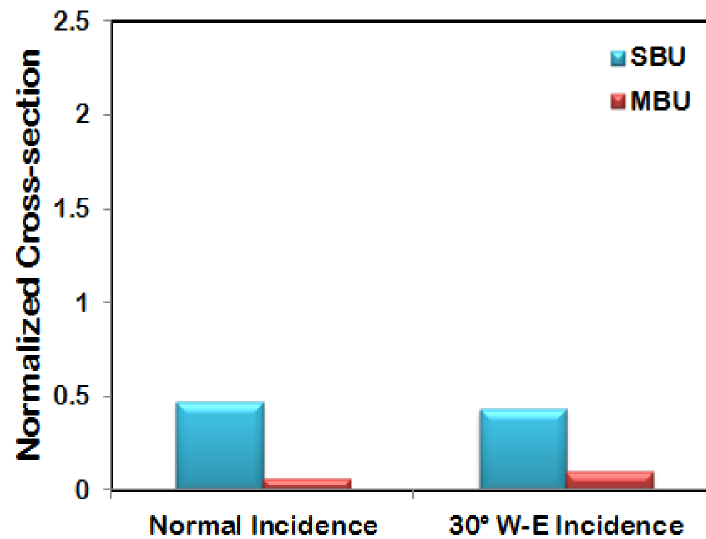


(b) Triple-well SRAM

Fig 37: Normalized cross section vs. Effective LET for a) dual-well and b) triple-well devices for normal and 30°W-E incidence irradiation with a checkerboard pattern.



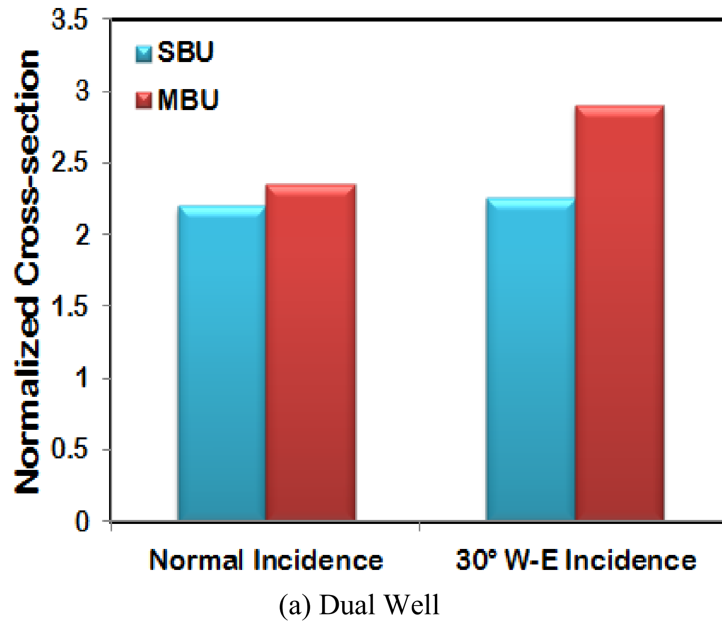
(a) Dual-well



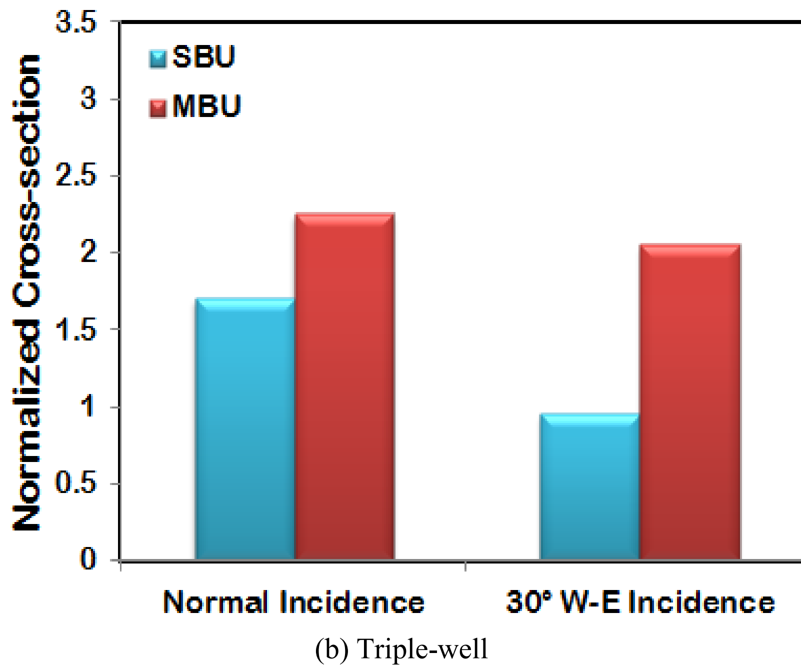
(b) Triple-well

Fig. 38: SBU and MBU for normal and 30°W-E incidence at low LET (N ion: 1.16 MeV-cm^2/mg) for a) dual-well and b) triple-well SRAM cells.

At moderate to high LETs, the soft error rates of the dual-well system increase dramatically, while for triple-well systems the error rate remains fairly constant or decreases compared to normally incident strikes. Similar behavior is observed in the simulations where at moderate or high LETs, both the SRAM cells are restored to their original state because of delayed collection of the confined charge in the p-well. Figs. 38 and 39 show the SBUs and MBUs for the angled ion-hits.



(a) Dual Well



(b) Triple-well

Fig.39: SBU and MBU for normal and 30°W-E incidence at high LET (Kr ion: 24.98 MeV-cm2/mg) for a) dual-well and b) triple-well SRAM cells.

The above results show that at high LETs, for angled strikes, the triple-well structures are more resistant to soft errors compared to dual-well structures. This is in contradiction to the common idea that devices exhibit more errors when exposed to ions impinging at an angle other than normal incidence.

4.3.4 Cluster Size

Maximum cluster size is defined as the product of the maximum number of errors in the horizontal (word-lines) and vertical (bit-lines) directions. Such a number will yield a measure of the spread of error across multiple rows and columns. The cluster size of the MBUs is lower for the triple-

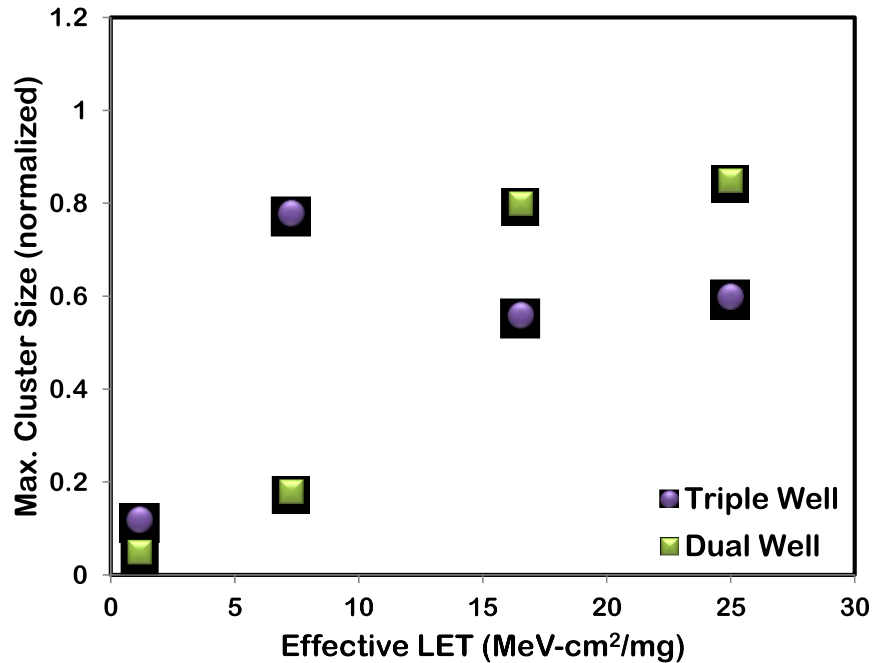


Fig 40: Maximum cluster size of recorded errors (checkerboard pattern) for dual-well and triple-well SRAM cells for normal incidence.

well SRAMs compared to the dual-well SRAMs at high LETs for both angles of incidence. Further, the cluster size decreases for an angular strike from that for a normally incident ion. Fig. 40 shows the maximum cluster size of recorded errors for dual and triple-well structures.

4.3.5 Location of Errors

The theory developed in the previous chapter makes use of the confined charge to reverse the upset in triple-well SRAM cells. Thus, the process is facilitated by not allowing the deposited charge to drain off the system faster than the electrical signal propagation time. Thus it should be more dominant in areas farther away from well taps. Figs. 41 and 42 show the total number of errors (normalized) vs. cell

location. In this case, as well, the data are normalized with a single factor. The n-wells run in the vertical direction and the well taps are placed every 64 rows. Word-lines run in the horizontal direction and bit-lines in the vertical direction.

Two distinct patterns are observed, one for low LET particles and the other for high LET particles. For the dual-well technology, for low LET particles (Ar ion: LET = 8.34 MeV-cm^2/mg), the concentration of errors farthest from the well taps is up to 82% higher than the average number of errors. However, it is around 90% lower than the average closer to the well taps, but the variation with location is much less for the triple-well technology (Fig. 42). A similar trend was observed by Gasiot et al. [4]. However, a higher number of errors are observed in the triple-well SRAM cells because of the charge confinement which has been explained in the following section. For high LET particles (Kr ion: LET = 24.98 MeV-cm^2/mg), however, the triple-well cells show fewer errors far away from the well tap (~27% of the average number of errors) compared to the dual-well structures (~76% of the average number of errors)(Fig. 43). This is because near the well taps, the charges are quickly removed. This does not create an environment favorable for the upset-reversal mechanism. In areas farther away, charge confinement favors the upset-reversal mechanism, and thus some of the cells flip twice, thereby reducing the number of errors. The pattern is schematically shown in the figure below.

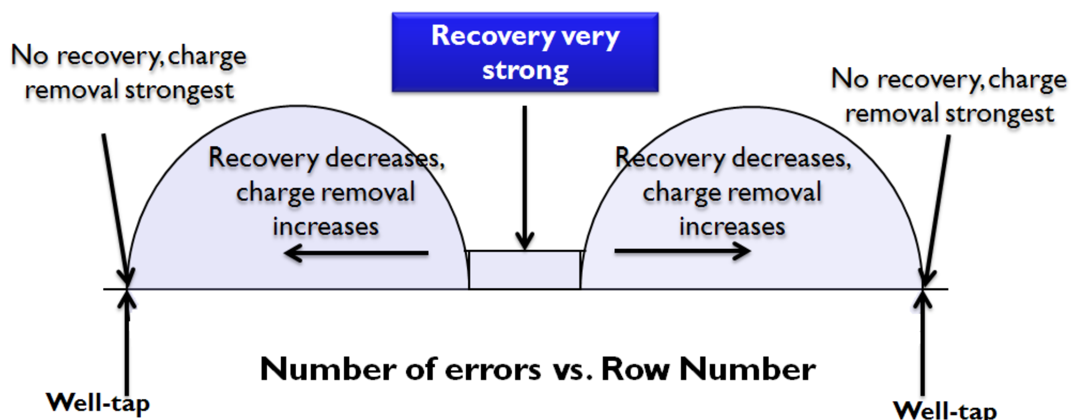
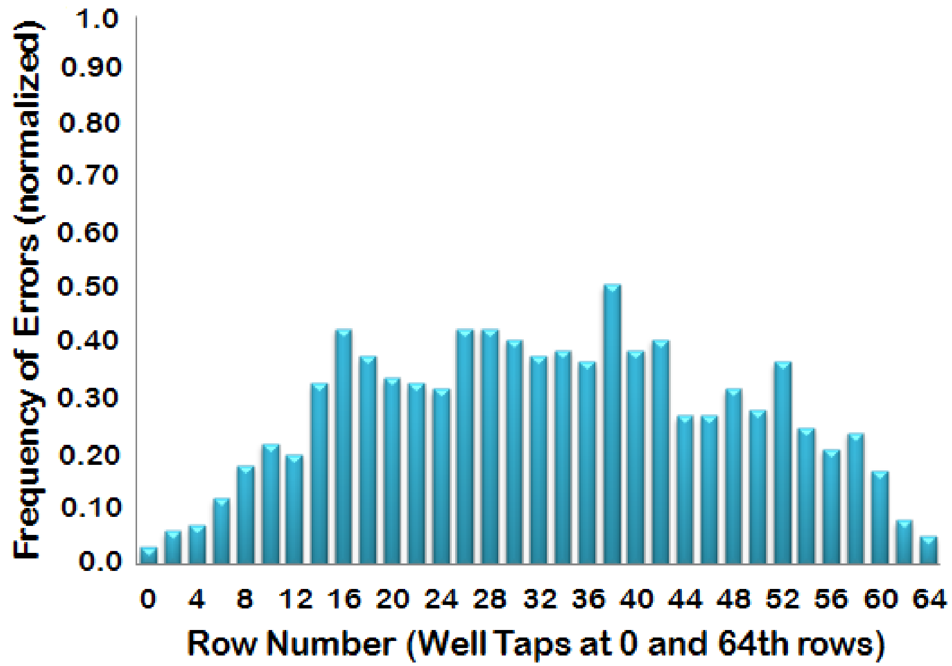
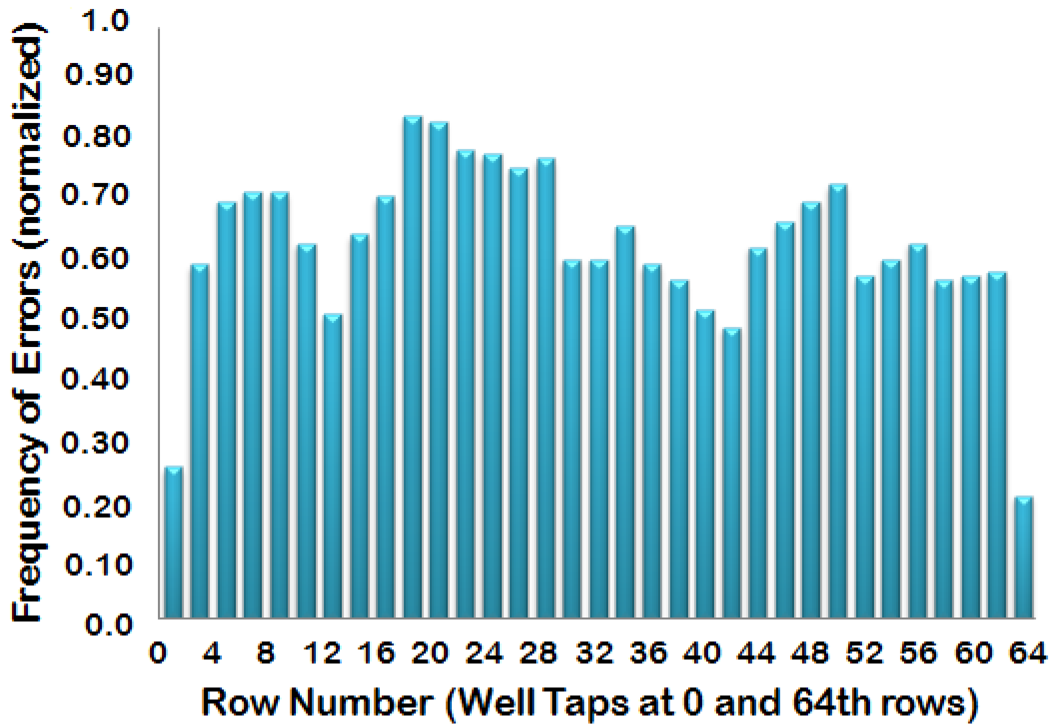


Fig. 41: Schematic showing the frequency of errors vs. well tap in the SRAM cell

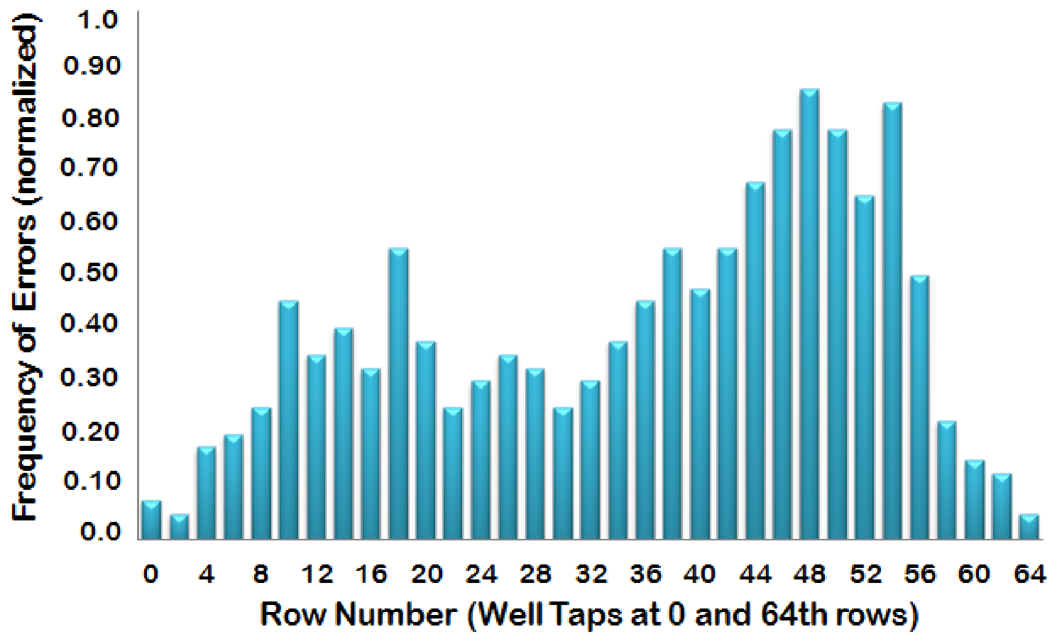


(a) Dual Well

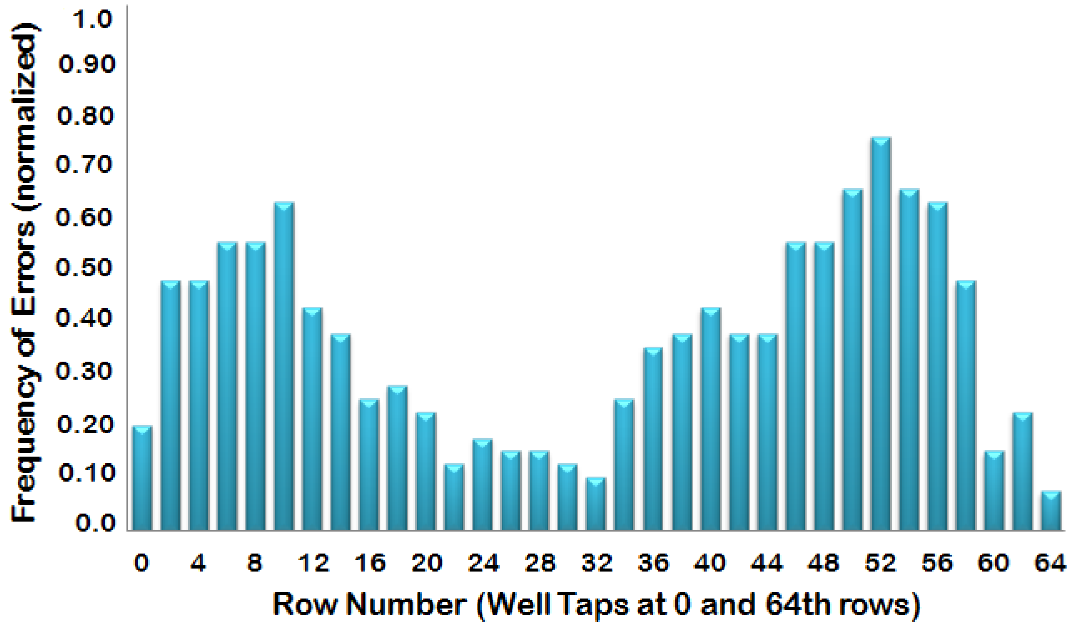


(b) Triple Well

Fig. 42: Frequency of errors with respect to location for Ar ion (LET: 8.34 MeV-cm^2/mg) for (a) dual-well and (b) triple well SRAM cells for checkerboard pattern.



(a) Dual Well



(b) Triple Well

Fig. 43: Frequency of errors with respect to location for Kr ion (LET: 24.98 MeV-cm^2/mg) for (a) dual-well and (b) triple well SRAM cells for checkerboard pattern.

CHAPTER V

GENERAL DISCUSSION

In SRAMs, multiple cells are associated with a single well. If enough charge is collected by transistors in the vicinity of the strike to flip the state of a cell twice, no upset will be observed in those cells. For cells distant from the struck node or near the well taps, however, this effect may not occur because the amount of confined charge is lower. Thus, for high-LET particles, there is a greater probability that cells close to the strike will revert back to their original state, with no upset occurring. The reversal effect will not, however, be observed for low LETs. In dual-well technologies, this effect does not occur in nMOS transistors because the collected charge is spread over the entire substrate as there is no deep n-well to confine the charges.

It is usually believed that angular ion strikes are more problematic for any device from the soft error point of view. In this work, it has been shown that that this may not always be the case especially for triple well structures at advanced technology nodes. Because of charge confinement in triple-well structures, reinforcing charge collection mechanism is predominant that decreases the soft error rates for SRAM cells. In dual-well structures, the deposited charge from the ion strike spreads over the entire substrate. Thus the probability of the reinforcing charge collection mechanism to trigger is considerably lower, and the soft error rates are higher.

Previous work done on triple-well technology used close spacing of well taps to drain the charge out the system quickly [5]. However, for high LET ion strikes, in order to drain the charge off the system efficiently, the well taps need to be placed much more frequently. Placing

a large number of well taps has a penalty on space. An alternative is to benefit from multiple node charge collection phenomenon occurring in advanced technology nodes to reduce the upset. The location of the well taps needs to be optimized so that there is a balance between the two approaches which reduce the overall error rates of the memory. The single event upset reversal mechanism is dependent on well engineering in triple-well nMOS transistors. The propensity of charge collection is determined by various factors such as the depth and doping of the p-well. If the well is made deeper, then the upset-reversal mechanism will be less effective. Similarly, if the doping concentration of the well is comparable to the confined charge, then the upset-reversal mechanism will not be observed. This mechanism will be effective in all technology nodes that exhibit significant multiple-node charge collection (also known as charge-sharing). Previous works have shown this effect in 90 nm and 65 nm technologies [7, 8, and 10] as well as in a 32 nm technology [9]. Single-event upset reversal mechanism described in this work may not entirely prevent the occurrence of upsets in memory cells. However, it may lower the error rates in triple-well SRAM cells, thereby increasing the overall radiation tolerance for memory cells in environments dominated by high LET particles.

CHAPTER VI

SUMMARY

NMOS transistors in a triple-well usually collect more charge during a single event strike than those in a dual-well due to charge confinement within the well. For high LET values, however, charge collection at more than one node in a triple-well technology may restore the original state of the SRAM cells in the vicinity of the strike. Thus, for high-LET particles (typically above 15 MeV-cm^2/mg), the triple-well SRAMs do not always upset. We describe this phenomenon as “SINGLE-EVENT UPSET REVERSAL”. This phenomenon decreases the soft-error rate in certain circumstances, particularly those dominated by ions with high LET values. Dual-well nMOS transistors collect less charge for low LET strikes and thus typically have a lower error rate for environments in which low LET particles dominate. Test results for high LET environments show that triple-well SRAM cells are less vulnerable compared to dual-well SRAM cells. Additionally, triple-well SRAM cells show a range of particle LETs beyond which SER is seen to decrease significantly. The device response at the lower end of the LET range is due to the conventional critical charge, while that at the upper end of the LET range is defined by the upset reversal mechanism. SRAMs built in advanced technology nodes also show increased vulnerability to multiple-bit upsets (MBUs) due to charge-sharing between transistors in close proximity. It is generally believed that high LET particles incident at an angle represent the worst-case conditions for single-event tests. This was applicable for older technology generations where logic gate delays were longer compared with charge removal times for a single-event hit. For advanced technology nodes, where logic gate delays are shorter compared with charge-removal times, the reinforcing charge collection mechanism results in lower SER. Thus, for triple-well technology, at high particle LETs, the soft error rate decreases for angled hits. In dual-well systems, the delayed charge collection mechanism is much less predominant, thereby increasing the overall soft error rate for SRAM cells.

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APPENDIX I

CALIBRATION OF NMOS AND PMOS TRANSISTORS WITH 40 NM COMMERCIAL PROCESS DESIGN KIT (PDK)

A.1 Introduction

The evolution of technology computer-aided design (TCAD)--the synergistic combination of process, device and circuit simulation and modeling tools—finds its roots in bipolar technology, starting in the late 1960s, and the challenges of junction isolated, double-and triple-diffused transistors. These devices and technology were the basis of the first integrated circuits; nonetheless, many of the scaling issues and underlying physical effects are integral to IC design, even after four decades of IC development. With these early generations of IC, process variability and parametric yield were an issue—a theme that will reemerge as a controlling factor in future IC technology as well.

Process control issues--both for the intrinsic devices and all the associated parasitics--presented formidable challenges and mandated the development of a range of advanced physical models for process and device simulation. Starting in the late 1960s and into the 1970s, the modeling approaches exploited, were dominantly one- and two-dimensional simulators. While TCAD in these early generations showed exciting promise in addressing the physics-oriented challenges of bipolar technology, the superior scalability and power consumption of MOS technology revolutionized the IC industry. By the mid-1980s, CMOS became the dominant driver for integrated electronics. Nonetheless, these early TCAD developments set the stage for their growth and broad deployment as an essential toolset that has leveraged technology development through the VLSI and ULSI eras which are now the mainstream. [A1 & A2]

A.2 TCAD Hierarchy

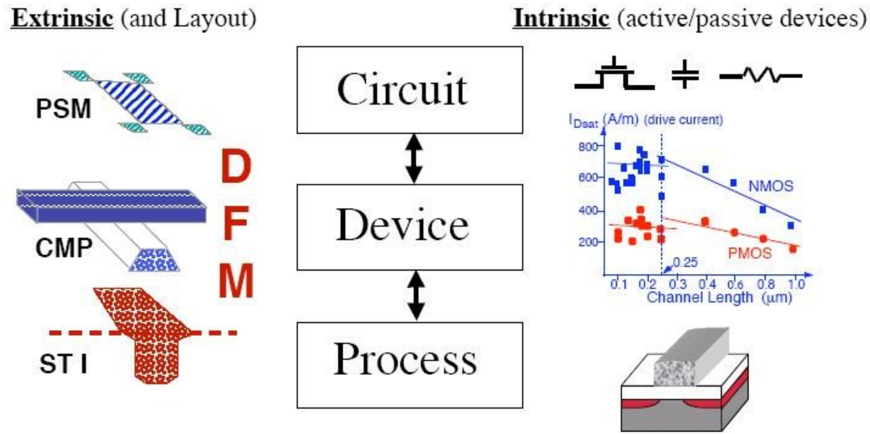


Fig A1: Hierarchy of technology CAD tools building from the process level to circuits. Left side icons show typical manufacturing issues; right side icons reflect MOS scaling results based on TCAD [A1]

A.3 Problem: Calibration of Device Models

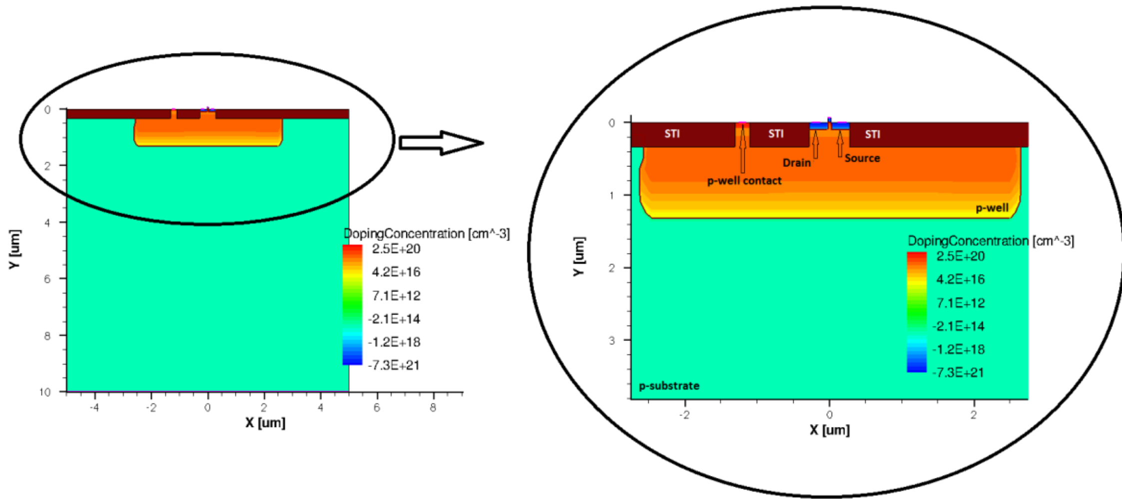
Calibration of devices is quite important as various analyses depend on it. For example, the single-event behavior of a circuit turns out to be a fairly sensitive function of a number of device properties such as its drive strength, drain engineering and threshold voltage levels. Therefore, it is necessary to replicate the device properties with sufficient accuracy in order to lend credibility to the mechanisms. The required input for the calibration task is the geometry and doping profiles of a commercial 40 nm technology. Most of the information used to model the device comes from two sources. For basic structure and isolation geometry, published literature was used. The actual doping profiles were determined using the commercial PDK and the corresponding documentation, through physical intuition. The TCAD simulations for the 3-D electrical models were performed with version of 2009 of the Synopsys TCAD tool suite, primarily with SDE (to define the device geometry and doping) and SDEVICE.

A.4 Approach: Commercial 40 nm Device Cross Sections

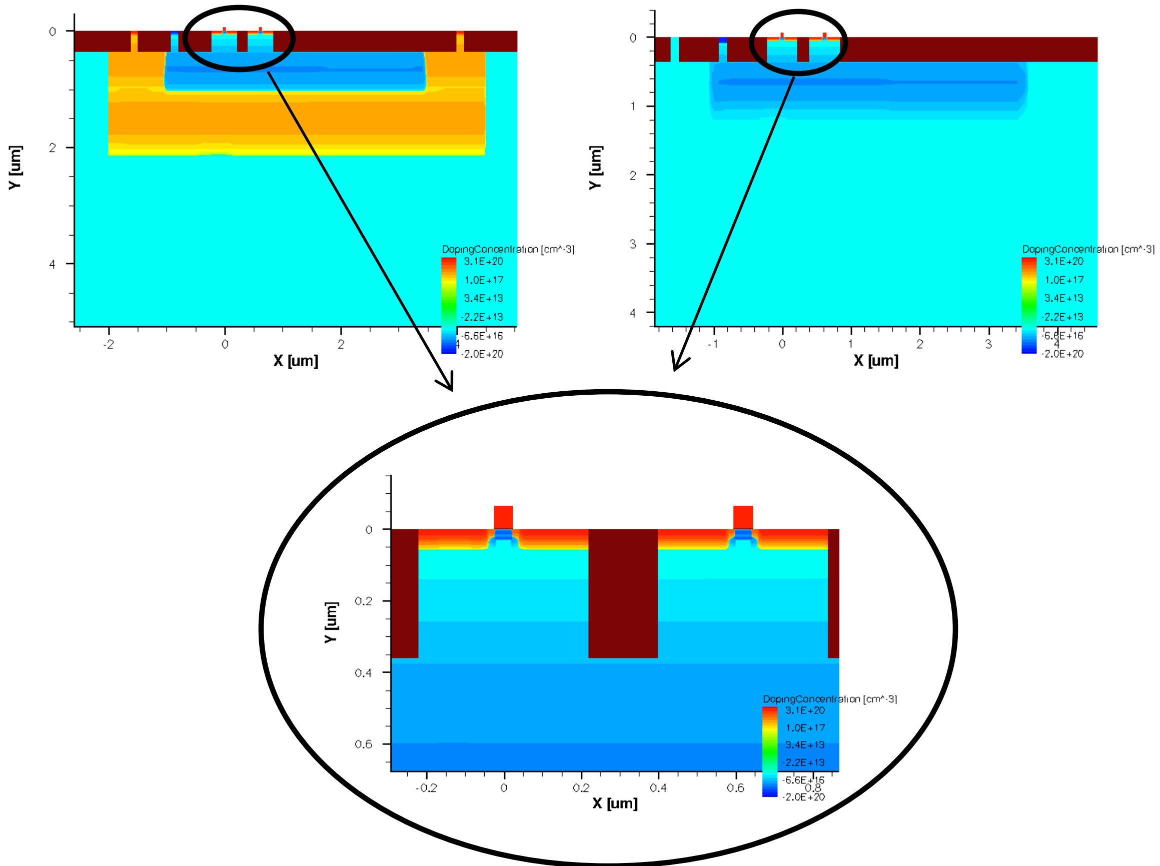
The device geometry and doping profiles are described in this section. Some of the dimensions and profiles for the well and substrate were retained from the ones used in 90 nm CMOS described in [A3]. For the NMOS, the doping in the P-well is Gaussian with the peak around 0.4 μm down from the surface. It was similar for PMOS transistors, but with opposite doping type. There is also a N+ deep implant with the peak of the Gaussian at about 1.25 μm. This is primarily a low resistance path introduced for latchup protection. The shallow trench isolation is about 0.30 μm deep, and is present where source, drain, or well contact diffusions are not defined. An accurate estimate of the gate oxide thickness is necessary to achieve proper calibration. Published literature indicates that this thickness would be physically 1.25 nm. Comparison of various films and the thickness that would result is done using the concept of equivalent oxide thickness (EOT). EOT is given by:

$$\text{EOT} = \frac{\kappa_{SiO2}}{\kappa_x} * \text{tx}$$

Where κ_x is the κ value for the film of interest, tx is the physical thickness of the film of interest and κ_{SiO2} is the κ value of silicon dioxide. By calculation, we obtain the tx is 0.9 nm. However, since gate leakage due to tunneling was not modeled (as this introduced unreasonable computational requirement), the equivalent oxide thickness of 1.05 nm was used. The poly-silicon gate was taken to be 64 nm thick. The NMOS and PMOS device structures are shown below.



(a) 40 nm PMOSFETs



(b) 40 nm dual- and triple-well NMOSFETs

Fig A2: 2D Cross-sections of the TCAD Models

The doping profiles in the channel were ascertained largely through iterative methods during the dc calibration process. The channel implant structure consisted of a threshold implant at the surface, which is used to adjust the device threshold voltage (V_t). Flanking the lightly-doped shallow drain (LDD) extensions on both the source and drain sides are two small regions of doping known as “halo doping”. Electrically, the halo deters short channel effects and DIBL (Drain Induced Barrier Lowering) without introducing unrealistically high capacitances. From a calibration perspective, it provides a control over the subthreshold slope without significantly changing the threshold voltage. There is also a separate subsurface punch-through implant. For the lightly-doped drain extensions (LDD), dimensions and doping levels decide the series resistance of the device, which has a significant effect on the peak drive strength of the device. Once these factors were determined through a prolonged iterative comparison of the device characteristics with the ones in the paper, the effective channel length came to be about 34 nm.

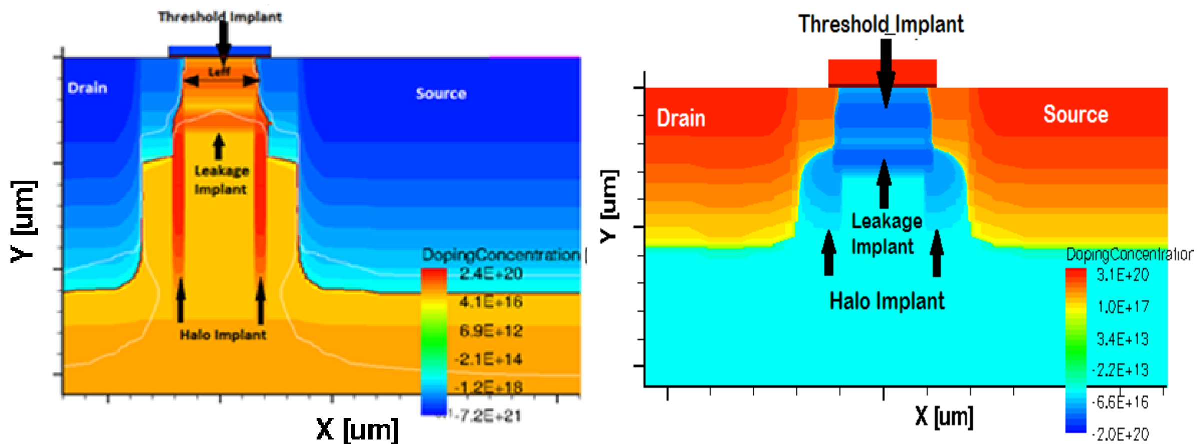
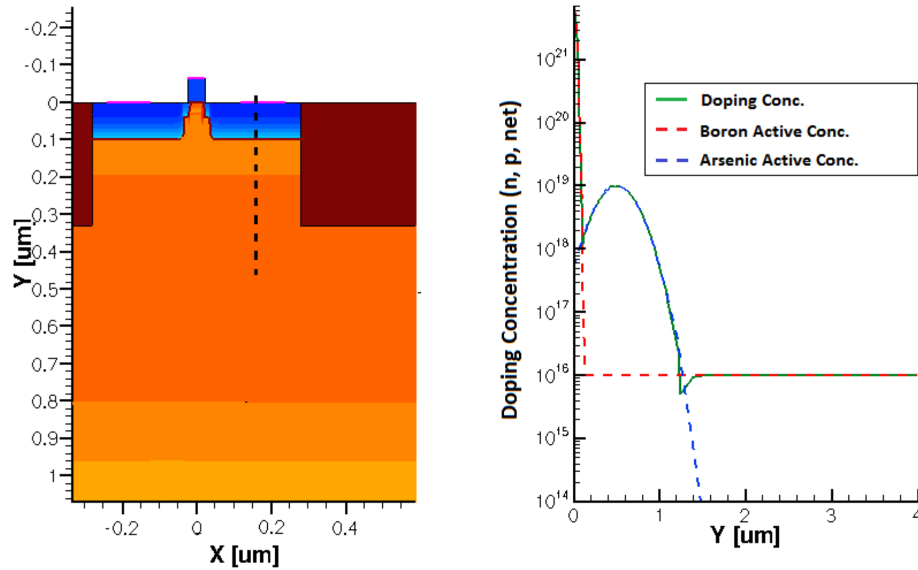


Fig A3: Close-up view of Source, Drain and the various implants of a) PMOSFET and b) NMOSFET

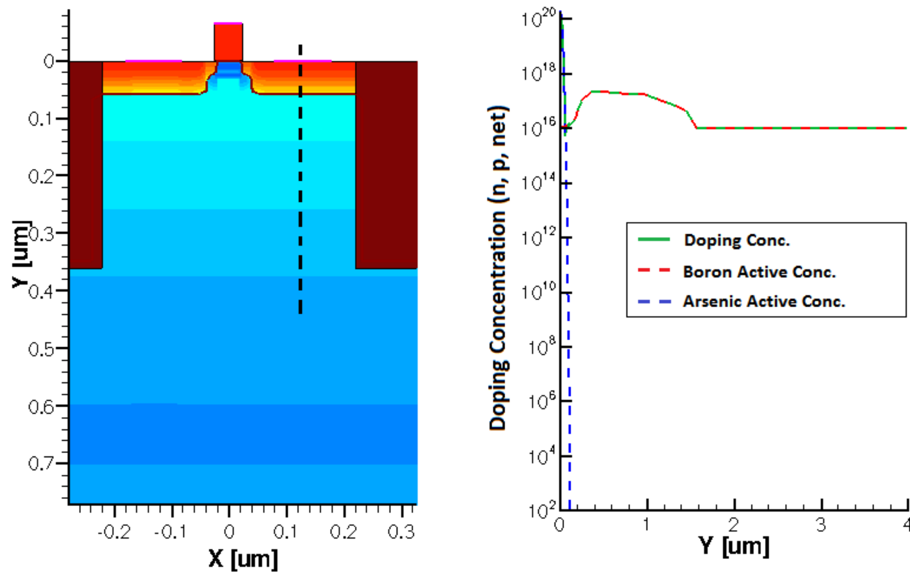
A.5 Doping Profiles of Devices

The doping profiles of the different device models were reached by iterative calibration to match the device characteristics of the PDK. The substrate and well doping profiles were obtained from

earlier calibrated models. It was assumed that similar well and substrate profiles were used for the 45 nm devices.



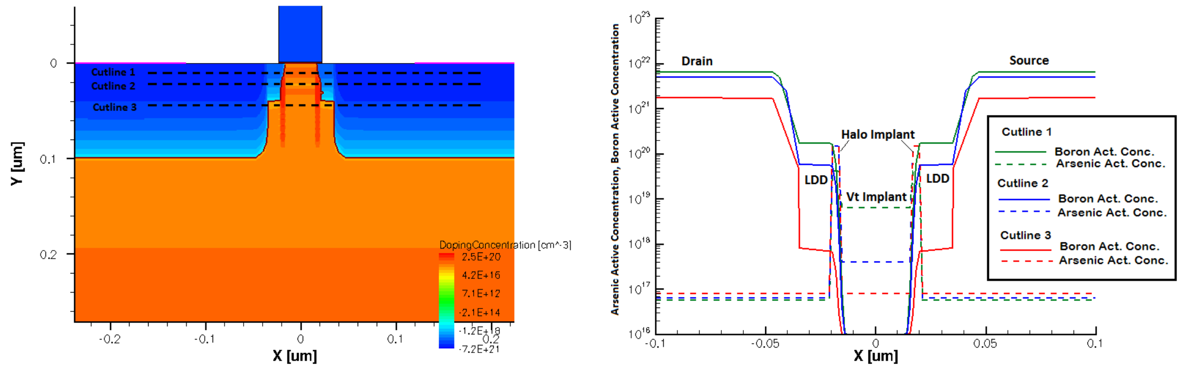
(a) PMOSFET



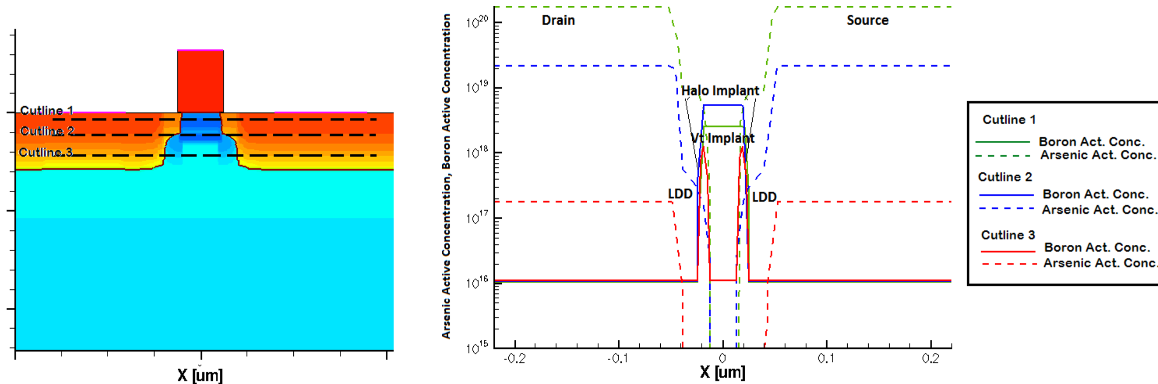
(b) NMOSFET

Fig A4: 1-D doping cuts showing the well and substrate profiles for the PMOS and NMOS devices.

For the fine structure of the channel and LDD doping profiles, we choose a number of cutlines in different locations. These Cutlines will show some representative numbers for a 40 nm PMOS and NMOS.



(a) PMOSFET



(b) NMOSFET

Fig A5: Cutlines 1, 2 & 3. Cutline 1- goes through close to the surface. Cutline 2 goes between the threshold and punch through implant regions. Cutline 3 goes below the punch through implant, and shows only the halo implant spikes

A.6 References

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APPENDIX B

SAMPLE SCRIPT FOR SDE AND SDEVICE

40nm 3D NMOSFET

```
; Setting parameters
; - lateral
(define Ltot 2.5)   ; [um] Lateral extend total
(define Lg 0.05)   ; [um] Drawn Gate length
(define subxmin -3.00); [um] Max. leftside extension in the x-direction
(define subxmax 6.00); [um] Max. rightside extension in the x-direction
(define subzmin -5.00); [um] Max. frontside extension in the z-direction
(define subzmax 5.00); [um] Max. backside extension in the z-direction
(define wn 0.14); [um] width of the nmos device
; Layers
(define Ysub 10)   ; [um] Substrate thickness
(define Tox 0.00107) ; [um] Gate oxide thickness - 1.25nm
(define Ypol -0.064)  ; [um] Poly gate thickness
; Substrate doping level
(define Dop 1e16) ; [1/cm3]
; Derived quantities
(define Xmax (/ Ltot 2.0))
(define Xg   (/ Lg   2.0))

(define Ygox (* Tox -1.0))
;------------------------------------------------------------------------------------------
; Overlap resolution: New replaces Old
```

```
(sdegeo:set-default-boolean "ABA")
;-------------------------------------------------------------------------------------------
; CREATE REGIONS
; SUBSTRATE REGION
(isegeo:create-cuboid (position subxmin 0 subzmin) (position subxmax Ysub subzmax) "Silicon"
"region_1" )
; GATE OXIDE REGION - Main
(isegeo:create-cuboid (position (* Xg -1.0) 0 0) (position Xg Ygox wn) "SiO2" "region_2")
; PolySi GATE - Main
(isegeo:create-cuboid (position (* Xg -1.0) Ygox 0) (position Xg Ypol wn) "PolySi" "region_3")
;------------------------------------------------------------
; ISOLATIONS
; STI REGION - I(from left edge to p-well contact)
(isegeo:create-cuboid (position subxmin 0 subzmin) (position -0.92 0.36 subzmax) "Oxide" "STI1" )
; STI REGION - II (from p-well contact to device)
(isegeo:create-cuboid (position -0.8 0 subzmin) (position -0.22 0.36 subzmax) "Oxide" "STI2" )
; STI REGION - III (contact to edges along z dimension)
(isegeo:create-cuboid (position -0.92 0 1) (position -0.8 0.36 subzmax ) "Oxide" "STI3" )
(isegeo:create-cuboid (position -0.92 0 subzmin) (position -0.8 0.36 -1 ) "Oxide" "STI4" )
; STI REGION (device to edges along z dimension)
(isegeo:create-cuboid (position -0.22 0 subzmin) (position 0.22 0.36 0) "Oxide" "STI5" )
(isegeo:create-cuboid (position -0.22 0 wn) (position 0.22 0.36 subzmax) "Oxide" "STI6" )
; STI REGION - IV ("to the right" of S/D)
(isegeo:create-cuboid (position 0.22 0 subzmin) (position subxmax 0.36 subzmax ) "Oxide" "STI7" )
```

```
; STI REGION - III ("to the right" of S/D)

;(isegeo:create-rectangle (position 0.84 0 0) (position subxmax 0.36 0 ) "Oxide" "STI5" )

; STI REGION - IV ("in front of" of S/D, till the left edge of the gate extension)

;(isegeo:create-rectangle (position 4.12 0 0) (position subxmax 0.36 0) "Oxide" "STI6" )

;-----------------------------------------------------------------------------------------

; DEFINING AND PLACING CONTACTS

; SUBSTRATE CONTACT

(isegeo:define-contact-set "substrate" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

(isegeo:define-3d-contact (find-face-id (position 0 Ysub 0)) "substrate")

; GATE CONTACT

(isegeo:define-contact-set "gate1" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

(isegeo:define-3d-contact (find-face-id (position 0 Ypol 0.07)) "gate")

; DRAIN CONTACT

(isegeo:create-cuboid (position -0.08 0 0.04) (position -0.18 -0.2 0.08) "Metal" "Drainmetal")

(isegeo:define-contact-set "drain_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

(isegeo:define-3d-contact (find-face-id (position -0.13 0 0.05)) "drain_nmos")

(isegeo:delete-region (find-body-id (position -0.13 -0.1 0.05)))

; SOURCE CONTACT

(isegeo:create-cuboid (position 0.08 0 0.04) (position 0.18 -0.2 0.08) "Metal" "Sourcemetal")

(isegeo:define-contact-set "source_nmos" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

(isegeo:define-3d-contact (find-face-id (position 0.13 0 0.05)) "source_nmos")

(isegeo:delete-region (find-body-id (position 0.13 -0.1 0.05)))

; p-WELL CONTACT

(isegeo:create-cuboid (position -0.9 0 -1) (position -0.85 -0.2 1) "Metal" "pwell")

(isegeo:define-contact-set "pwell" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

(isegeo:define-3d-contact (find-face-id (position -0.87 0 0.12)) "pwell")
```

```
(isegeo:delete-region (find-body-id (position -0.87 -0.1 0.12)))

; n-WELL LEFT CONTACT

;(isegeo:create-cuboid (position 4.03 0 -2) (position 4.07 -0.2 2) "Metal" "nwell1")

;(isegeo:define-contact-set "nwell1" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

;(isegeo:define-3d-contact (find-face-id (position 4.04 0 0.12)) "nwell1")

;(isegeo:delete-region (find-body-id (position 4.04 -0.1 0.12)))

; n-WELL RIGHT CONTACT

;(isegeo:create-cuboid (position -1.6 0 -2) (position -1.55 -0.2 2) "Metal" "nwell2")

;(isegeo:define-contact-set "nwell2" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")

;(isegeo:define-3d-contact (find-face-id (position -1.57 0 0.12)) "nwell2")

;(isegeo:delete-region (find-body-id (position -1.57 -0.1 0.12)))

;------------------------------------------------------------------------------------------------

; SET DOPING REGIONS AND PROFILES

; CONSTANT DOPING PROFILES

; SUBSTRATE REGION AND PROFILE

(isedr:define-constant-profile "region_1" "BoronActiveConcentration" Dop )

(isedr:define-constant-profile-region  "region_1" "region_1" "region_1" )

; PolySi GATE REGION AND PROFILE

(isedr:define-constant-profile "region_3" "ArsenicActiveConcentration" 8e20)

(isedr:define-constant-profile-region "region_3" "region_3" "region_3")

;------------------------------------------------------------------------------------------------

; ANALYTICAL DOPING PROFILES

; NWELL PROFILE LEFT

;(isedr:define-refinement-window "nwell1.Profile.Region" "Rectangle" (position -2 0.5 -3) (position -1
0.5 3))
```

```
;(isedr:define-gaussian-profile "nwell1.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1e18 "ValueAtDepth" 5e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwell1.Profile.Place" "nwell1.Profile"
"nwell1.Profile.Region" "Symm" "NoReplace" "Eval")
; NWELL PROFILE RIGHT
;(isedr:define-refinement-window "nwell2.Profile.Region" "Rectangle" (position 3.5 0.5 -3) (position 4.5
0.5 3))
;(isedr:define-gaussian-profile "nwell2.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1e18 "ValueAtDepth" 5e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwell2.Profile.Place" "nwell2.Profile"
"nwell2.Profile.Region" "Symm" "NoReplace" "Eval")
; DEEP NWELL PROFILE
;(isedr:define-refinement-window "nwell3.Profile.Region" "Rectangle" (position -2 1.5 -3) (position 4.5
1.5 3))
;(isedr:define-gaussian-profile "nwell3.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1e18 "ValueAtDepth" 5e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwell5.Profile.Place" "nwell3.Profile"
"nwell3.Profile.Region" "Symm" "NoReplace" "Eval")
; NWELL PROFILE SIDE
;(isedr:define-refinement-window "nwell4.Profile.Region" "Rectangle" (position -2 0.5 -3.0) (position 4
0.5 -1.5))
;(isedr:define-gaussian-profile "nwell4.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1e18 "ValueAtDepth" 5e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwell3.Profile.Place" "nwell4.Profile"
"nwell4.Profile.Region" "Symm" "NoReplace" "Eval")
; NWELL PROFILE SIDE
```

```
;(isedr:define-refinement-window "nwell5.Profile.Region" "Rectangle" (position -2 0.5 1.5) (position 2.5
0.5 3))
;(isedr:define-gaussian-profile "nwell5.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1e18 "ValueAtDepth" 5e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwell4.Profile.Place" "nwell5.Profile"
"nwell5.Profile.Region" "Symm" "NoReplace" "Eval")
; NWELL CONTACT LEFT
;(isedr:define-refinement-window "nwelltap.Profile.Region" "Rectangle" (position 4 0 -2) (position 4.12 0
2))
;(isedr:define-gaussian-profile "nwelltap.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwelltap.Profile.Place" "nwelltap.Profile"
"nwelltap.Profile.Region" "Symm" "NoReplace" "Eval")
; NWELL CONTACT RIGHT
;(isedr:define-refinement-window "nwelltap2.Profile.Region" "Rectangle" (position -1.62 0 -2) (position -
1.5 0 2))
;(isedr:define-gaussian-profile "nwelltap2.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
2e20 "ValueAtDepth" 1e17 "Depth" 0.08 "Gauss" "Factor" 0.0001)
;(isedr:define-analytical-profile-placement "nwelltap2.Profile.Place" "nwelltap2.Profile"
"nwelltap2.Profile.Region" "Symm" "NoReplace" "Eval")
; p-WELL PROFILE OF THE NMOS DEVICE
(isedr:define-refinement-window "pwell.Profile.Region" "Rectangle" (position -1 0.65 -1.5) (position 3.5
0.65 1.5))
(isedr:define-gaussian-profile "pwell.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18
"ValueAtDepth" 1e17 "Depth" 0.35 "Gauss" "Factor" 0.0001)
```

```
(isedr:define-analytical-profile-placement "pwell.Profile.Place" "pwell.Profile" "pwell.Profile.Region"
"Symm" "NoReplace" "Eval")
; p-WELL CONTACT PROFILE (DEGENRATE DOPING FOR p-WELL CONTACT)
(isedr:define-refinement-window "pwelltap.Profile.Region" "Rectangle" (position -0.92 0 -1) (position -
0.8 0 1))
(isedr:define-gaussian-profile "pwelltap.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal"
2e20 "ValueAtDepth" 1e16 "Depth" 0.06 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "pwelltap.Profile.Place" "pwelltap.Profile"
"pwelltap.Profile.Region" "Symm" "NoReplace" "Eval")
;-----------------------------------------------------------------------------------------
; NMOSFET
;-----------------------------------------------------------------------------------------
; SOURCE
(isedr:define-refinement-window "source.Profile.Region" "Rectangle" (position 0.045 0 0) (position 0.28
0 wn))
(isedr:define-gaussian-profile "source.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
2e20 "ValueAtDepth" 1e18 "Depth" 0.04 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.Place" "source.Profile" "source.Profile.Region"
"Symm" "NoReplace" "Eval")
; SOURCE HALO
(isedr:define-refinement-window "HSimplant.Profile.Region" "Rectangle" (position 0.016 0.06 0)
(position 0.020 0.06 wn))
(isedr:define-gaussian-profile "HSimplant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal"
2e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HSimplant.Profile.Place" "HSimplant.Profile"
"HSimplant.Profile.Region" "Symm" "NoReplace" "Eval")
```

```
; LDD - SOURCE
(isedr:define-refinement-window "sourceldd.Profile.Region" "Rectangle" (position 0.020 0.0 0) (position
0.045 0 wn))
(isedr:define-gaussian-profile "sourceldd.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1.05e19 "ValueAtDepth" 6e17 "Depth" 0.025 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "sourceldd.Profile.Place" "sourceldd.Profile"
"sourceldd.Profile.Region" "Symm" "NoReplace" "Eval")
; DRAIN
(isedr:define-refinement-window "drain.Profile.Region" "Rectangle" (position -0.045 0 0) (position -0.28
0 wn))
(isedr:define-gaussian-profile "drain.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e20
"ValueAtDepth" 1e18 "Depth" 0.04 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.Place" "drain.Profile" "drain.Profile.Region"
"Symm" "NoReplace" "Eval")
; DRAIN HALO
(isedr:define-refinement-window "HDimplant.Profile.Region" "Rectangle" (position -0.016 0.06 0)
(position -0.020 0.06 wn))
(isedr:define-gaussian-profile "HDimplant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal"
2e18 "ValueAtDepth" 1e17 "Depth" 0.03 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "HDimplant.Profile.Place" "HDimplant.Profile"
"HDimplant.Profile.Region" "Symm" "NoReplace" "Eval")
; LDD - DRAIN
(isedr:define-refinement-window "drainldd.Profile.Region" "Rectangle" (position -0.020 0.0 0) (position -
0.045 0 wn))
(isedr:define-gaussian-profile "drainldd.Profile" "ArsenicActiveConcentration" "PeakPos" 0 "PeakVal"
1.05e19 "ValueAtDepth" 6e17 "Depth" 0.025 "Gauss" "Factor" 0.1)
```

```
(isedr:define-analytical-profile-placement "drainldd.Profile.Place" "drainldd.Profile"
"drainldd.Profile.Region" "Symm" "NoReplace" "Eval")
; Vt IMPLANT
(isedr:define-refinement-window "implant.Profile.Region" "Rectangle" (position -0.020 0.01 0) (position
0.020 0.01 wn))
(isedr:define-gaussian-profile "implant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal"
6.4e18 "ValueAtDepth" 3.2e17 "Depth" 0.01 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "implant.Profile.Place" "implant.Profile"
"implant.Profile.Region" "Symm" "NoReplace" "Eval")
; IMPLANT TO MITIGATE LEAKAGE (BELOW Vt IMPLANT)
(isedr:define-refinement-window "limplant.Profile.Region" "Rectangle" (position -0.020 0.03 0) (position
0.020 0.03 wn))
(isedr:define-gaussian-profile "limplant.Profile" "BoronActiveConcentration" "PeakPos" 0 "PeakVal"
9e18 "ValueAtDepth" 3e17 "Depth" 0.005 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.Place" "limplant.Profile"
"limplant.Profile.Region" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------------------------------------------------------------------
; DEFINE MESHING REGIONS AND MAX-MIN MESH SPACINGS
; UPPER SUBSTRATE REGION
(isedr:define-refinement-size "region_1" 0.5 0.5 0.5 0.4 0.4 0.4)
(isedr:define-refinement-window "region_1" "Cuboid" (position subxmin 0.1 subzmin) (position subxmax
2 subzmax))
(isedr:define-refinement-function "region_1" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "region_1" "region_1" "region_1" )
; UPPER SUBSTRATE REGION- I
;(isedr:define-refinement-size "uppersub" 0.1 0.1 0.1 0.05 0.05 0.05)
```

```
;(isedr:define-refinement-window "uppersub" "Cuboid" (position -0.5 0.1 -0.25) (position 0.5 1 0.5))
;(isedr:define-refinement-function "uppersub" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "uppersub" "uppersub" "uppersub" )
; UPPER SUBSTRATE REGION- I
;(isedr:define-refinement-size "uppersub2" 0.1 0.1 0.1 0.05 0.05 0.05)
;(isedr:define-refinement-window "uppersub2" "Cuboid" (position 0.5 0.2 0) (position 1.3 1 0))
;(isedr:define-refinement-function "uppersub2" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "uppersub2" "uppersub2" "uppersub2" )
; LOWER SUBSTRATE REGION
(isedr:define-refinement-size "region_12"  0.5 0.5 0.5 0.5 0.5 0.5)
(isedr:define-refinement-window "region_12" "Cuboid" (position subxmin 2 subzmin) (position subxmax
Ysub subzmax))
(isedr:define-refinement-function "region_12" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "region_12" "region_12" "region_12" )
;NMOS 1
;-----------------------------------------------------------------------------------------------------------
; CHANNEL REGION
(isedr:define-refinement-size "R.Channel" 0.005 0.005 0.005 0.005 0.005 0.01)
(isedr:define-refinement-window "R.Channel" "Cuboid" (position (* Xg -1.0) 0 0) (position Xg 0.05 wn))
(isedr:define-refinement-function "R.Channel" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "R.Channel" "R.Channel" "R.Channel")
; SOURCE/DRAIN REGION
(isedr:define-refinement-size "sourcedrain" 0.01 0.01 0.01 0.01 0.01 0.01)
(isedr:define-refinement-window "sourcedrain" "Cuboid" (position -0.24 0 0) (position 0.24 0.1 wn))
(isedr:define-refinement-function "sourcedrain" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "sourcedrain" "sourcedrain" "sourcedrain")
```

```
; Vt & LEAKAGE IMPLANT REGIONS
(isedr:define-refinement-size "implant" 0.01 0.01 0.01 0.01 0.01 0.01)
(isedr:define-refinement-window "implant" "Cuboid" (position -0.025 0 0) (position 0.025 0.07 wn))
(isedr:define-refinement-function "implant" "DopingConcentration" "MaxTransDiff" 0.1)
(isedr:define-refinement-placement "implant" "implant" "implant" )
; n-WELL CONTACT REGION I
;(isedr:define-refinement-size "ntap1" 0.1 0.1 0.1 0.1 0.1 0.1)
;(isedr:define-refinement-window "ntap1" "Cuboid" (position 4.03 0 -2) (position 4.07 0.1 2))
;(isedr:define-refinement-function "ntap1" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "ntap1" "ntap1" "ntap1" )
; n-WELL CONTACT REGION II
;(isedr:define-refinement-size "ntap3" 0.1 0.1 0.1 0.1 0.1 0.1)
;(isedr:define-refinement-window "ntap3" "Cuboid" (position -1.6 0 -2) (position -1.55 0.1 2))
;(isedr:define-refinement-function "ntap3" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "ntap3" "ntap3" "ntap3" )
; p-WELL CONTACT REGION-I
;(isedr:define-refinement-size "ptap1" 0.1 0.1 0.1 0.1 0.1 0.1)
;(isedr:define-refinement-window "ptap1" "Cuboid" (position -0.9 0 -1) (position -0.85 0.1 1))
;(isedr:define-refinement-function "ptap1" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "ptap1" "ptap1" "ptap1" )
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc" 0.1 0.02 0 0.1 0.02 0)
;(isedr:define-refinement-window "npjunc" "Rectangle" (position -1 0.8 0) (position 3.5 1.0 0))
;(isedr:define-refinement-function "npjunc" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc" "npjunc" "npjunc" )
```

```
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc1" 0.01 0.02 0 0.02 0.02 0)
;(isedr:define-refinement-window "npjunc1" "Rectangle" (position -2.05 0.35 0) (position -1.95 2.0 0))
;(isedr:define-refinement-function "npjunc1" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc1" "npjunc1" "npjunc1" )
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc2" 0.1 0.02 0 0.1 0.02 0)
;(isedr:define-refinement-window "npjunc2" "Rectangle" (position -2 2.2 0) (position 4.5 2.4 0))
;(isedr:define-refinement-function "npjunc2" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc2" "npjunc2" "npjunc2" )
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc3" 0.02 0.1 0 0.02 0.1 0)
;(isedr:define-refinement-window "npjunc3" "Rectangle" (position 4.5 0.35 0) (position 4.7 2.0 0))
;(isedr:define-refinement-function "npjunc3" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc3" "npjunc3" "npjunc3" )
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc4" 0.05 0.05 0 0.05 0.05 0)
;(isedr:define-refinement-window "npjunc4" "Rectangle" (position -1.1 0.36 0) (position -0.9 1.05 0))
;(isedr:define-refinement-function "npjunc4" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc4" "npjunc4" "npjunc4" )
; NWELL-PWELL JUNCTION
;(isedr:define-refinement-size "npjunc5" 0.05 0.05 0 0.05 0.05 0)
;(isedr:define-refinement-window "npjunc5" "Rectangle" (position 3.4 0.36 0) (position 3.55 1.05 0))
;(isedr:define-refinement-function "npjunc5" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "npjunc5" "npjunc5" "npjunc5" )
; ION  TRACK
```

```
;(isedr:define-refinement-size "itrack" 0.01 0.01 0.01 0.005 0.5 0.005)
;(isedr:define-refinement-window "itrack" "Cuboid" (position -0.10 0 0) (position -0.16 Ysub 0))
;(isedr:define-refinement-function "itrack" "DopingConcentration" "MaxTransDiff" 0.1)
;(isedr:define-refinement-placement "itrack" "itrack" "itrack" )
(isedr:write-cmd-file "40nm_DW")
(sde:save-model "40nm_DW")
;---------------------------- THE END -------------------------------------------------------
```

Sample Script for Single Event Simulation

```
#--------------------------------------------------------------------------------
#Striking the Drain of NMOS 1 to see the effects - 40nm DW Shared Well - LET 40
#Multiple Cells in the same well
#--------------------------------------------------------------------------------
Device NMOS {
Electrode {
  { Name="source_nmos1"   Voltage=0.0 }
  { Name="source_nmos2"   Voltage=0.0 }
  { Name="drain_nmos1"    Voltage=1.0 }
  { Name="drain_nmos2"    Voltage=0.0 }
  { Name="gate1"          Voltage=0.0 }
  { Name="gate2"          Voltage=1.0 }
  { Name="pwell"          Voltage=0.0 }
 {  Name="substrate"   Voltage=0.0}
}
File {
```

```
# input files:
	Grid    = "40nm_WODN_close_msh.grd"
	Doping  = "40nm_WODN_close_msh.dat"
	Load    = "40nm_WODN_close_bias_des.sav"
}
Physics {
 Mobility( PhuMob ( Arsenic ) HighFieldsat Enormal )
 Fermi
 EffectiveIntrinsicDensity( OldSlotboom )
 Recombination ( SRH Auger )
 HeavyIon (
		PicoCoulomb
		Direction=(0,1,0)
		Location=(-0.18,0,0)
		Length=7
		Time=1e-9
		LET_f=0.40
		wt_hi=0.05
		Gaussian
		)
}
}

File {
Plot="40_WODN_close_let40.dat"
Current="40_WODN_close_let40.plt"
```

```
Output="40_WODN_close_let40.log"
SPICEPath = "."
 }
System {
NMOS nmos ("gate1"=n2 "drain_nmos1"=n1 "source_nmos1"=ng "pwell"=ng "gate2"=n1
"drain_nmos2"=n2 "source_nmos2"=ng)
        rvt_pfet_40nm  MP1    (n1 n2 n4 n4)
                                {w = 0.140e-6 l = 0.04e-6
                                 pd = 0.22e-6 ps =0.22e-6
                                 ad = 1.12e-14 as = 1.12e-14
                               nrd = 0.01 nrs =0.01
                        }

      rvt_pfet_40nm  MP2    (n2 n1 n4 n4)
                             {w = 0.140e-6 l = 0.04e-6
                              pd = 0.22e-6 ps =0.22e-6
                              ad = 1.12e-14 as = 1.12e-14
                               nrd = 0.01 nrs =0.01
                        }

Vsource_pset v2 (n4 0) {dc = 1.0}
Vsource_pset v4 (ng 0) {dc = 0}
Initialize (n1 = 1.0)
Initialize (n2 = 0.0)
#Vsource_pset v5 (bl 0) {dc = 1.2}
#Vsource_pset v6 (blb 0) {dc = 0}
```

```
#Vsource_pset v7 (wl 0) {dc = 1.2}
}
Plot {
  eDensity  hDensity  eCurrent  hCurrent
  Potential  SpaceCharge  ElectricField
  eMobility  hMobility  eVelocity  hVelocity
  Doping  DonorConcentration   AcceptorConcentration
  ConductionBandEnergy ValenceBandEnergy
  AugerRecombination
  HeavyIonChargeDensity
  eQuasiFermiPotential
  hQuasiFermiPotential
}

Math {
   NoAutomaticCircuitContact
   WallClock
   Extrapolate
   Derivatives
   Newdiscretization
   RecBoxIntegr
   Method=ILS
   RelErrControl
   Spice_gmin=1e-15
   Iterations=20
   notdamped=100
```

```
}
# Initial Solution build-up
Solve {
Coupled (iterations=100) {Circuit}
Coupled (iterations=100) {Poisson}
Coupled (iterations=100) {Poisson Circuit
Coupled (iterations=100) {Poisson Circuit Contact}
Coupled (iterations=100) {Poisson Hole Contact Circuit}
Coupled (iterations=100) {Poisson Electron Hole Contact Circuit}
NewCurrentFile="CMOS"
Transient (
 InitialTime=0 FinalTime=0.95e-9 InitialStep=1e-11 MaxStep=1e-10
 Increment=1.2)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit}
Plot (FilePrefix="Pre_strike_let40" Time=(0.85e-9) NoOverwrite)
}
Transient (
 InitialTime=0.95e-9 FinalTime=2.1e-9 InitialStep=1e-13 MaxStep=1e-12
 Increment=1.2)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit}
Plot      (FilePrefix="PS1_let40"      Time=(1.001e-9;1.01e-9;1.02e-9;1.05e-9;1.1e-9;1.3e-9;1.5e-9)
NoOverwrite)
}
Transient (
```

```
 InitialTime=2.1e-9 FinalTime=50e-9 InitialStep=1e-12 MaxStep=1e-10
 Increment=1.3)
{
Coupled {nmos.poisson nmos.electron nmos.hole nmos.contact circuit }
Plot (FilePrefix="PS2_let40" Time=(2.1e-9;5e-9;7e-9;10e-9;15e-9;20e-9;25e-9) NoOverwrite)
}
}
```