CHARACTERIZATION OF THE MECHANISMS AFFECTING SINGLE-EVENT TRANSIENTS IN SUB-100 NM TECHNOLOGIES

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DEDICATION

This dissertation is dedicated to my grandfather, Frank R. Ahlbin Sr., who was the first engineer I ever knew. He provided me guidance and encouragement on my path to becoming an electrical engineer.

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LIST OF ACRONYMS

ASET.....Analog Single Event Transient

BJT.....Bipolar Junction Transistor

CME.....Coronal Mass Ejection

CMOS .....Complementary Metal Oxide Semiconductor

DD.....Displacement Damage

DICE Latch.....Dual Interlocked Cell

DPSET.....Double-Pulse-Single-Event Transient

DRAM .....Dynamic Random Access Memory

DSET.....Digital Single Event Transient

DUT .....Device Under Test

EHP .....Electron-Hole Pair

GCR .....Galactic Cosmic Ray

IC.....Integrated Circuit

LET .....Linear Energy Transfer

MBU .....Multiple Bit Upset

RHBD .....Radiation Hardened By Design

SCR.....Solar Cosmic Rays

SE.....Single Event

SEB .....Single Event Burnout

SEE .....Single Event Effect

SEGR .....Single Event Gate Rupture

SEL ....Single Event Latchup

SET ....Single Event Transient

SEU...Single Event Upset

SOHO...Solar and Heliospheric Observatory

STI..Shallow Trench Isolation

TCAD..Technology Computer-Aided Design

TCR...Terrestial Cosmic Rays

TID...Total Ionizing Dose

TMR...Triple Modular Redundancy

TPA..Two-Photon Absorption

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CHAPTER I

INTRODUCTION

Single-event effects (SEE) have been a growing concern for the space, military, and commercial electronic sectors since the 1970's [Do03]. These concerns have increased as circuit error data is collected on modern-day integrated circuits (ICs) showing an increased susceptibility to SEE as feature sizes decrease and frequencies increase [Bu01]. A single-event (SE) occurs when a charged particle, such as a heavy-ion, passes through a semiconductor material creating electron-hole pairs (EHPs) along its strike path until it has lost all its energy or left the semiconductor [Ma93]. Sensitive junctions within the material, usually reverse-biased p/n junctions, can collect these extra carriers causing harmful effects based on the circuit topology and the amount of charge collected [Ma93].

Many different types of energetic particles can cause a SE. Four particular types of energetic particles have been shown to cause SEs: alpha particles, neutrons, protons, and heavy-ions [Ma79] [Na08].

One type of effect resulting from a SE is a spurious voltage pulse called a single-event transient (SET) [Ma93]. SETs are a significant reliability concern, as they can compete with legitimate logic signals and corrupt downstream logic and latches. In digital circuits, SETs that propagate unhindered in a circuit can become single-event upsets (SEUs) [Ma93]. A SEU is an alteration in the state of a memory circuit (e. g. a memory call can change from a logic "1" state to a logic "0" state) or when corrupted

data propagates to an output of the circuit -- leading to an observable error. These types of errors are termed “soft errors” as they do not result in a permanent failure (hard error) within the circuit.

As transistor density increases with each new CMOS technology node, the probability of a single ion causing a SET in a circuit or depositing charge on multiple nodes increases [Ba05][Ro07]. Multiple-node charge collection from a single ion strike can render hardened storage cells and SET mitigation techniques (such as guard rings, guard drains, additional well contacts, etc.) ineffective [Ol05, Am06]. Therefore, it is important to understand SET characteristics at each new technology node and resulting impacts on circuit designs.

In a 130 nm bulk CMOS technology, research has shown that charge sharing resulting from heavy-ions incident at high angles (> 60°) can affect the pulse width of a propagating SET [Ah09]. The interaction of the electrical signal propagation and charge sharing through the substrate can cause the SET to shorten -- termed “pulse quenching.” Mixed-mode 3D technology computer aided design (TCAD) simulations at the 90 nm technology node have shown that pulse quenching can occur at normal incidence (0°) for minimally spaced and sized circuits. This result indicates that charge sharing is becoming prevalent in sub-90 nm bulk processes.

At the 65 nm technology node, heavy-ion data (normal and at angle) highlight the prominence of charge sharing and pulse quenching [Ah10]. While at 130 nm, where pulse quenching was observed only for ion strikes at high incident angles, pulse quenching (thus the presence of charge sharing) has been observed to occur in a 65 nm bulk technology for ions at normal incidence. This result is attributed to the increase in

transistor density at 65 nm. Additionally during TCAD simulations and heavy-ion testing, it has been observed that single-ion strikes at high angles can cause double-pulse SETs (DPSETs) on a single electrical path [Ah11].

Through a thorough characterization of different technology nodes (130 nm, 90 nm, and 65 nm) this dissertation notes significant mechanisms that affect the operation of digital circuits. These mechanisms have in several cases nullified the effects of traditional radiation-hardened-by-design (RHBD) techniques, but have also led to the creation of new RHBD techniques designed to consider, and occasionally take advantage of mechanisms such as charge sharing and pulse quenching [At11]. Moreover, by examining charge sharing in multiple technology domains, the specific mechanisms, the interaction of the mechanisms, and the resulting device/circuit responses can be isolated and analyzed as they present themselves through technology scaling. Without thorough analysis at each technology level, predictions of how new CMOS technology nodes will perform in the space environment will be inaccurate.

This dissertation uses both three-dimensional mixed-mode technology-computer-aided design (TCAD) simulations and experimental analysis at the 65 nm, 90 nm, and 130 nm technology nodes to fully characterize the mechanisms that affect SETs in sub-100 nm bulk CMOS technologies. Chapter I introduces the motivation for this work. Chapter II presents background on single-event effects. Within the chapter, single-event effects are identified and explained in context to digital circuits. Chapter III then focuses on the specific single-event effect of SETs and the factors that influence them. In the second part of the chapter, the discussion focuses on common methods of experimental SET measurement and the typical target structures used. Chapter IV discusses the

relationship between the parasitic bipolar and n-well contacts, and how it affects the pulse width of SETs. Chapter V then introduces the mechanism of pulse quenching by using TCAD simulations, heavy-ion data, and laser data, to identify pulse quenching in multiple technology nodes. Additionally the chapter explains in detail how the layout and circuit design can influence pulse quenching. Finally, Chapter VI presents simulation and experimental heavy-ion results that explain a new SET mechanism called DPSETs. Instead of a single ion strike creating a single pulse SET, a single ion strike can result in a DPSET.

The research presented in this dissertation directly impacts the SEE circuit qualification and analysis techniques used in the radiation effects community. Simulations supported by experimental data illustrate how there are new mechanisms in sub-100 nm bulk CMOS that can affect SET pulse widths. These mechanisms can negate traditional RHBD solutions, but also can be used as new RHBD solutions. Designers and researchers can use this work to better analyze SET results, and they can predict how SET pulse width will be affected in future bulk CMOS technologies.

CHAPTER II

FUNDAMENTAL MECHANISMS OF SINGLE-EVENTS

Introduction

Microelectronic circuits are exposed to various radiation environments in space and on earth. The exposure of electronics to radiation can lead to temporary or permanent damage of circuits through effects of ionizing particles such as total-ionizing dose (TID), displacement damage (DD), prompt dose (Dose Rate), and single-event effects (SEE). As predicted in [Ma93] with the scaling of microelectronic circuits and the increase in transistor density with each new technology generation, SEEs have become a dominant failure mechanism affecting the reliability of ICs. Therefore, this discussion will focus on SEEs in microelectronic circuits. Though DD [Sr03], Prompt Dose [Al03], and TID [Ol03] are not discussed in this work, references are included for the interested reader.

As shown in Fig. II-1, Koons *et al.* found that in comparison to electrostatic discharge (ESD) damage, other radiation damage (TID), plasma and micrometeroid impacts, and uncategorized energetic particle effects spacecraft anomaly records attributed over 28% of anomalies to SEEs [Ma02]. Of spacecraft anomalies caused only by radiation, 84% are SEE related as illustrated in Fig. II-2 [Ma02][Ko99].

The remainder of this chapter will focus on how energetic particles interact with a semiconductor device, the physical mechanisms of the interactions, and their effects on circuits.

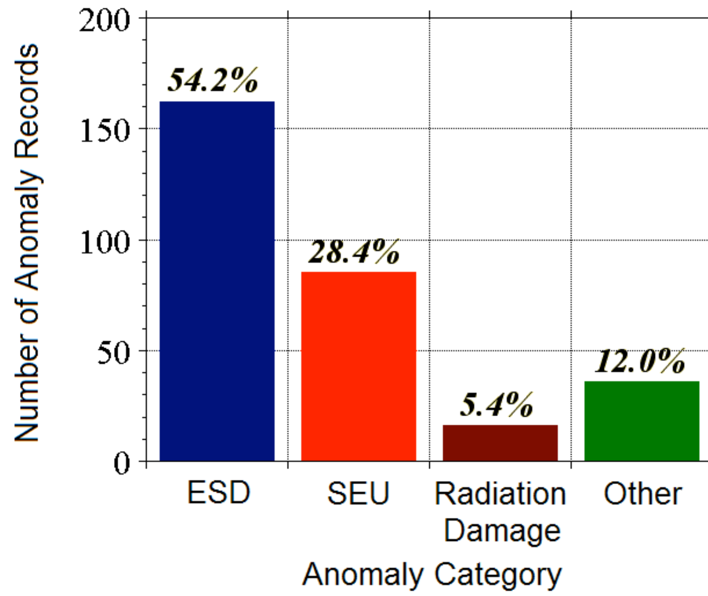

Fig. II-1. Distribution of spacecraft anomaly records versus anomaly type (ESD: electrostatic discharge; SEU: single event upset) [Ma02] (data from [Ko99]).

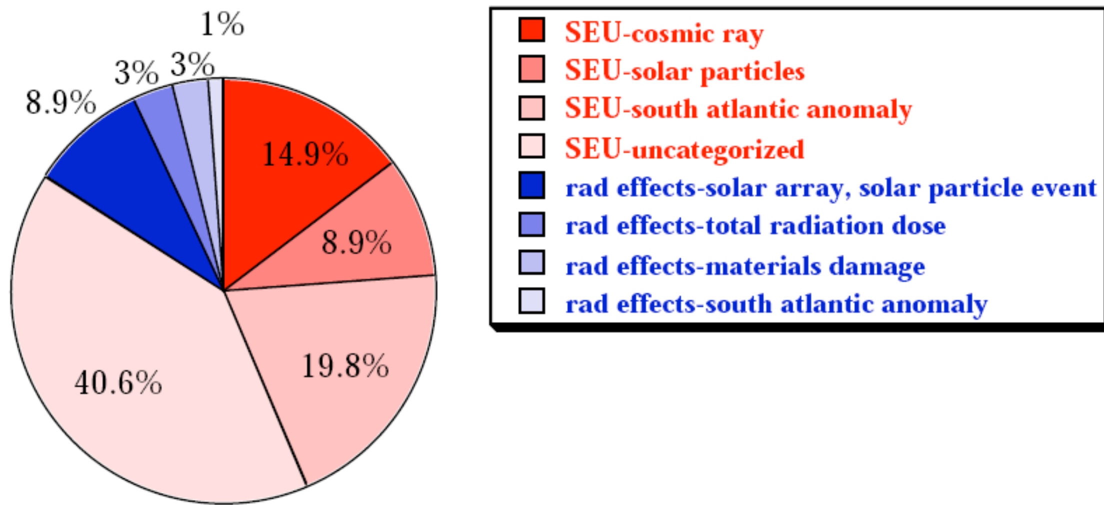

Fig. II-2. Breakdown of SEU and radiation damage anomaly records [Ma02] (data from [Ko99]).

Energetic Particles, Charge Generation, & Charge Collection

For a SE to occur, an energetic particle must interact with a semiconductor device. The primary particles of concern in the space environment are protons, heavy-ions, alpha particles, and electrons. Typically, these particles are a result of cosmic ions, solar flares, products of secondary interactions, or from a natural radiation decay [Ba03].

SEs can also occur within the earth's atmosphere at commercial flight altitudes and even on the ground. For terrestrial electronics, neutrons are the primary radiation effects concern, but particles from device packaging (alphas) along with heavy-ions, protons, electrons, muons, and pions can also be the source of SEs.

When a SE occurs, three things happen: charge generation, charge collection and recombination, and the circuit response. As an energetic particle passes through a semiconductor material, carriers are generated and may directly affect a circuit's operation through coulombic interaction or indirectly through nuclear reactions with the lattice. In direct ionization, electron-hole pairs (EHPs) are created along the particle's strike path until it has lost all its energy or left the semiconductor as shown in Fig. II-3 [Ma93]. For indirect ionization, a collision of particles occurs that results in nuclear reactions that may cause scattering or spallation. The secondary particles then generate charge through coulombic interactions because they have a lower energy than the primary particles. When an energetic particle loses energy, the amount of energy that is lost is referred to as a *linear energy transfer* (LET) value. LET describes the energy loss per unit path length of the particle as normalized by the density of the material and has units

of MeV-cm^2/mg. As a reference, in silicon an ion with an LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm [Do03].

When excess carriers are created by the particle in the material, the carriers must recombine or be collected. Charge can be collected on circuit nodes and cause the circuit to respond incorrectly. One method of charge collection is through drift transport. If charge is within the built-in electric field of a reverse-biased p-n junction, the electric field causes the holes to be swept into the p-region and the electrons into the n-region (drift current), as illustrated in Fig. II-3. Drift transport is a quick process on the order of picoseconds in duration because the carriers are limited only by their saturation velocity.

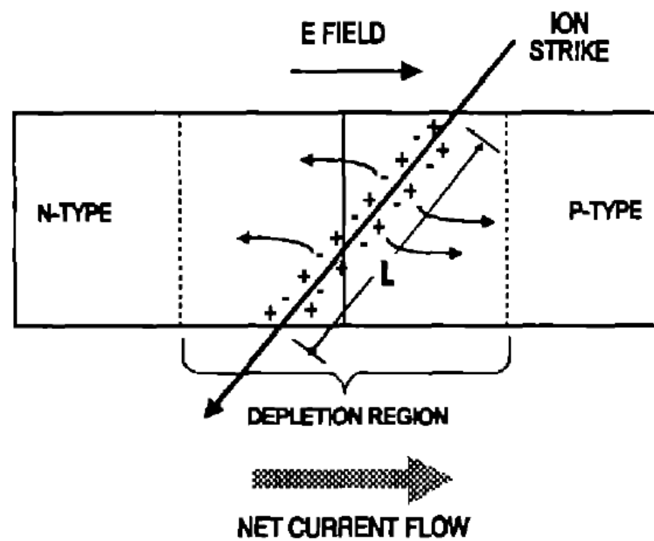

Fig. II-3. Depletion region charge collection via drift transport from an ion strike [Ma93].

A second method responsible for charge collection is diffusion transport. If charge exists outside of the built-in electric field at the junction, but is within a diffusion length of the junction, then it can be collected. Depending on the size of the diffusion length and the spacing of transistors, a single node or multiple nodes near the particle strike may

collect charge. Unlike drift transport, the diffusion process is a very slow process which can take on the order of microseconds depending on the distance. With the carriers surviving longer in the doped regions than those exposed to drift collection, some carriers may recombine – decreasing the amount of electrons and holes that reach the junction. Fig. II-4 illustrates the charge collected through drift and diffusion processes in a reverse-biased n+/p junction [Ba05]. The initial charge collection is due to field-assisted drift, followed by the collection of charge diffused through the substrate.

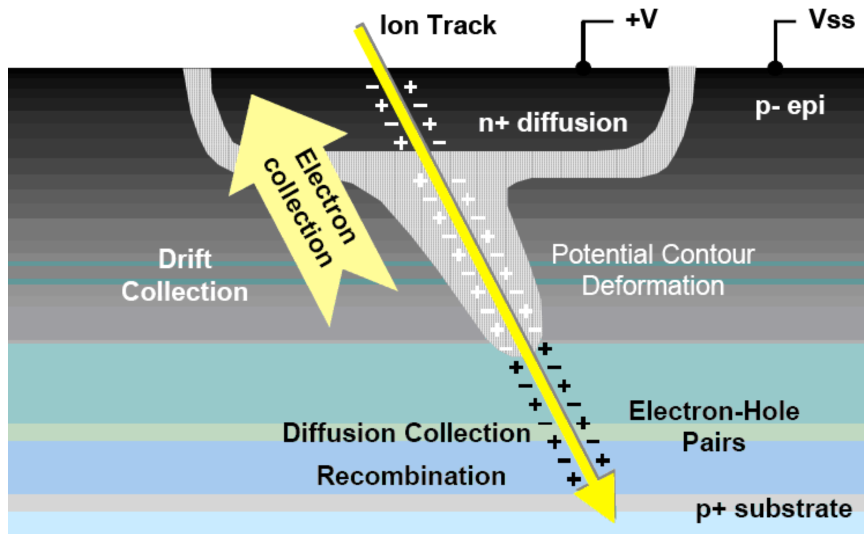

Fig. II-4. Illustration of an ion strike on a reverse-biased n+/p junction [Ba05]

When charge is collected by a semiconductor device, radiation-induced photocurrents are observed at the device terminals. The shape of the current pulse on these terminals is the direct result of the charge collection mechanisms involved. Looking at Fig. II-5 [Me82] the initial spike is due to the quick collection of charge via drift with the tail part of the curve due to the slow collection of charge via diffusion. In deep sub-micron processes, there can be a plateau effect immediately after the initial spike as a result of the circuit load [Da07]. Last, the integral of the current over the total time of the SE is the total charge collected by the circuit node.

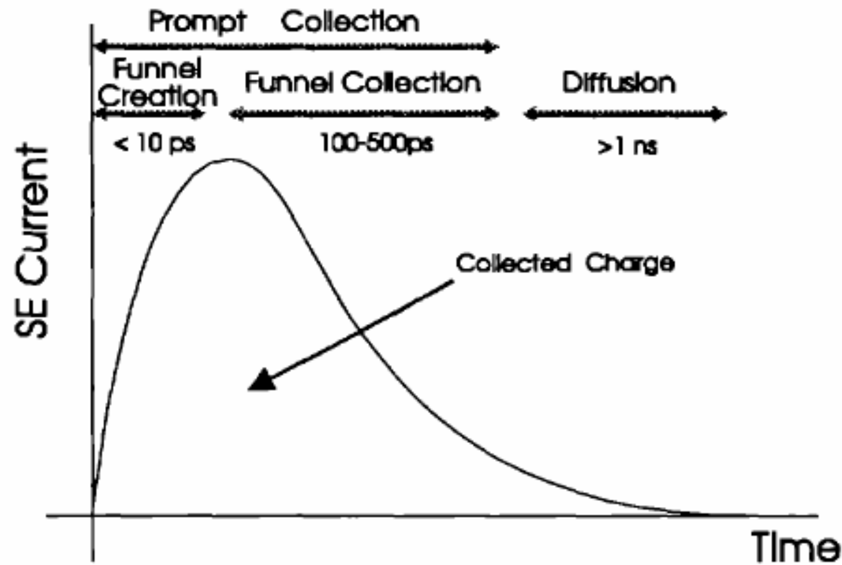

Fig. II-5. Typical shape of the SE current at a junction. The total collected charge corresponds to the area under the curve. [Me82].

The electric field plays an important role in the charge collection of carriers near p-n junctions as noted in the description of charge collection via drift transport. Additional to charge collection via drift transport, early research found the plasma track created by ionizing particles in a semiconductor can distort the surrounding electrostatic potential gradients, creating a field funnel [Hs81]. When the deposited charge is greater than the doping density of the silicon and a plasma track is formed, a path of free carriers exists between the n and p regions. The depletion region is then effectively hidden from the carriers, which are free to move toward (electrons) or away from (holes) the positively-biased n-region. The spreading resistance along the track leads to a voltage drop in the region, which results in the potential initially at the depletion region to spread down the length of the track. Carriers that were outside the depletion region are now susceptible to the electric field and are quickly collected at the junction by a drift mechanism, known as the funneling effect. An illustration of the plasma wire and the mechanism of field-assisted funneling is shown in Fig. II-6 [Ma93].

In devices at the nanometer scale, the radial dimension of the wire in field-assisted funneling may be wide enough to encompass more than one transistor. However, the basic concept remains the same and for the curious reader, recent work at the nanometer scale are referenced [Da07] [Das07].

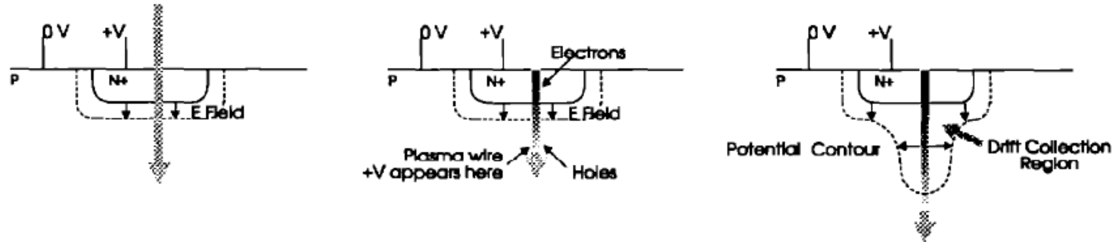

Fig. II-6. Qualitative view of the funnel effect: a) creation of the ion-induced plasma track, b) movement of electrons toward the positive bias, and c) potential drop along the track and redistribution of equipotential lines down the track [Ma93].

Similar to the field-assisted funneling mechanism, an additional charge collection mechanism is called the ion shunt effect [Ha85]. As the name implies, the energetic particle (ion) acts as a shunt (wire) when an ion passes through nearby junctions. The ion acts as a wire connecting the two junctions and conducts current between the junctions – enhancing the charge collected on the node.

Another mechanism that can enhance charge collection from a SE strike is parasitic bipolar junction transistor (BJT) amplification [Do96] [Ke89] [Am06] [Fu85] [Wo93] [Ol05] [Ol07]. A parasitic BJT exists in both pMOS transistors and nMOS transistors between the source-well-drain regions. However, parasitic BJT amplification is usually observed in dual-well pMOS transistors because the n-well resistivity is typically higher than that of the p-well. When an ion strikes, electrons collect in the n-well and reduce the n-well potential (make it more negative). The collapsing of the well potential along with additional carriers present in the well turns on the parasitic BJT with

the drain acting as the collector, the n-well acting as the base, and the source acting as the emitter, as shown in Fig. II-7 [Am06]. In turn, charge flows from the source and is collected by the drain – leading to an increased amount of charge collection at the circuit node.

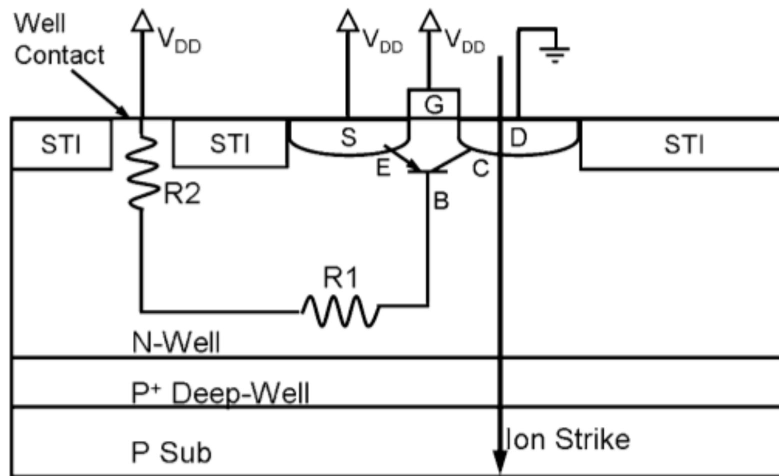

Fig. II-7. Illustration of the horizontal parasitic bipolar junction transistor in a pMOS transistor [Am06].

The final charge collection related mechanism that will be discussed is multiple-node charge collection or as it is more commonly known: charge sharing. With the decreasing of feature sizes and the increasing of transistor densities, free carriers from an ion strike may encompass multiple transistors, allowing charge to be collected through drift and diffusion by these transistors. Fig. II-8, for example, illustrates the relative range of the field-funnel (potential collapse) created by a single-ion strike in a 1 µm CMOS technology and a 90 nm CMOS technology [Da07]. The well collapse encompasses a much larger area in the 90 nm technology than in the 1 µm technology. The collapse causes the well to de-bias (lose its biased potential) and for the parasitic BJT to turn on in

multiple pMOS transistors. These pMOS transistors collect little charge from the original ion strike, but collect the majority of charge from the parasitic bipolar injecting charge from the source of each pMOS transistor. As technology scales, charge sharing has become more prevalent in each new generation of bulk CMOS technology.

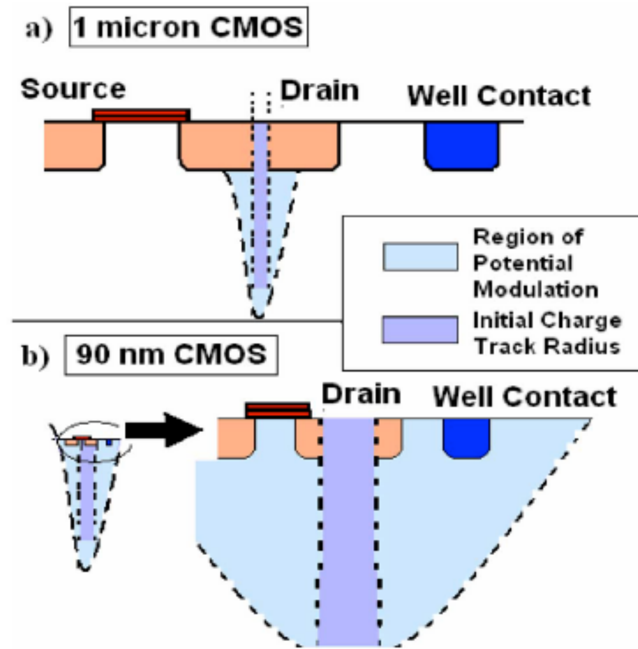

Fig. II-8. Relative range of the "field funnel" in a 1 μm and a 90 nm technology. Top figure (a) shows the "funnel" creating a potential perturbation only on a small portion of the drain. Bottom figure shows a strike with the same radius covering the source, drain and well contact [Da07].

Conclusion

This chapter gives an overview of the mechanisms involved in the interaction of a particle with a semiconductor. Mechanisms for charge generation and charge collection are described that are important to the creation of SETs and SEUs in ICs. The remainder of this work will be focused on factors that cause SETs and that determine the pulse width of SETs.

CHAPTER III

FUNDAMENTALS OF SINGLE-EVENT TRANSIENT GENERATION AND MEASUREMENT

Introduction

Integrated circuit (IC) technology scaling has led to a decrease in minimum transistor-to-transistor spacing and lower operating voltages, which has led to an enhanced sensitivity to ion-induced SETs in combinational logic data paths [Ba05]. An important metric of SETs is the duration of the disturbance at the signal output of a logic gate. This response is determined by the amount of charge collected at the struck node, the rate of charge accumulation at the node, and the rate of charge removal from the node. SETs with very narrow pulse widths (i.e. short transients) tend to be filtered (attenuated) along the data path by the finite response time of subsequent logic gates, while long pulses can propagate unattenuated deep into the logic.

The remainder of this chapter will explain how understanding SET pulse width can be useful in predicting errors. It will then discuss factors that influence SET pulse widths, and the different experimental methods used to measure SET pulse widths. Finally, the influence SET target structures has on the measurement of SET pulse widths will be summarized.

Window of Vulnerability

As introduced in the previous chapter, SETs can be latched by storage devices and be read out as incorrect data (SEU). The pulse width of the SET is a determining factor on whether the SET is latched as an error or not by the storage device. Every storage device or latch has a “window of vulnerability”. The window of vulnerability is the period of time that determines whether the SET is latched or is not latched as shown in Fig. III-1 [Bu93] [Mav02]. A latch’s window of vulnerability is determined by many factors, such as the sampling window and SET shape.

The sampling window is made up of the latch’s setup and hold times. For a latch to latch any signal, the signal must remain the same value for the entire duration of the sampling window. The duration of the sampling window is based on the technology node and the design of the latch, which affects the latching speed of the latch.

If the SET pulse width is longer than the latch’s sampling window, the remaining width of the pulse determines the latch’s window of vulnerability. Thus, the probability of latching an error is then given by the ratio of the window-of-vulnerability period to the clock period. This probability can be further simplified as the ratio of the SET pulse width to the clock period because SET pulse width is directly related to the window of vulnerability.

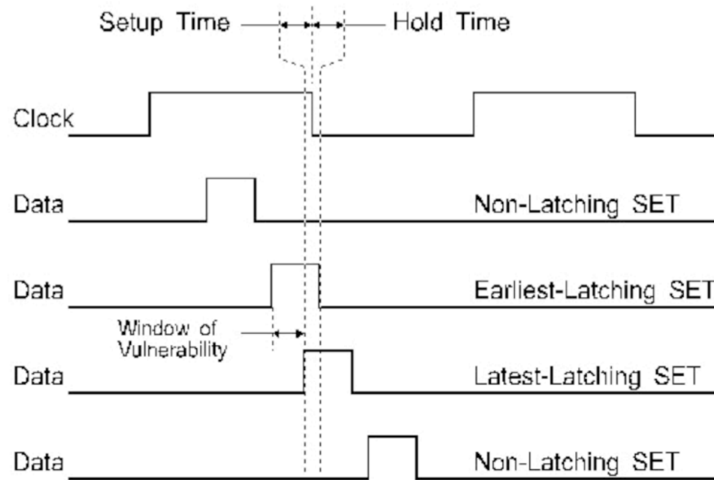

Figure III-1. An illustration showing how a pulse may or may not be latched by a storage [Mav02].

Fig. III-1 illustrates how the window of vulnerability determines whether the SET is latched or not. The example latch captures input data on the falling edge of the clock. In the first case, the SET is not latched because the transient occurs before the falling edge of the clock. In the second and third case, the transients are latched because they appear during a clock falling edge. Their pulse widths are wide enough to fall within the sampling time of the latch. The final case shows another non-latching SET, but this time the SET appeared after the latching event.

Factors that Influence SET Pulse Widths

The temporal charge collection efficiencies at a node struck by an ion determine the pulse characteristics, including the width, of the resulting voltage SET. These temporal mechanisms controlling the SET pulse width include classical drift, diffusion, and the parasitic amplification at that struck node [Ma93]. Additionally, the design of the

circuit influences the SET pulse width through factors such as the nodal capacitance, interconnect resistance, and current drive of other transistors connected to that node [Bu05].

Parasitic Bipolar Junction Transistor (BJT) Amplification

One factor that can significantly affect SET pulse width in sub-100 nm is parasitic bipolar amplification [Amus07]. A parasitic bipolar-junction-transistor structure exists between the source (emitter), the n-well (base), and the drain (collector) in pMOS transistors, shown in Fig. III-2. If this BJT is turned 'on', current is conducted from the MOS source to the drain causing additional charge to be collected on the node of the affected transistors. Therefore, the collected charge from the BJT turn-on and the ion strike can both contribute to the SET pulse width.

Understanding there is a relationship between the parasitic BJT and n-well contact design [Ol07], Amusan *et al.* found that by changing the vertical resistance (R2) of the n-well by varying the n-well contact placement and size, the pulse width of the SET could be affected, as seen in Fig. III-3 [Amus07]. The research in 130 nm and 90 nm bulk CMOS by [Amu07] also stated that the horizontal resistance (R1) could also affect the SET pulse width, but the horizontal resistance was determined by the doping of the n-well. N-wells that had kilo-ohm resistances were easily de-biased and took longer to regain their bias than n-wells with lower resistances.

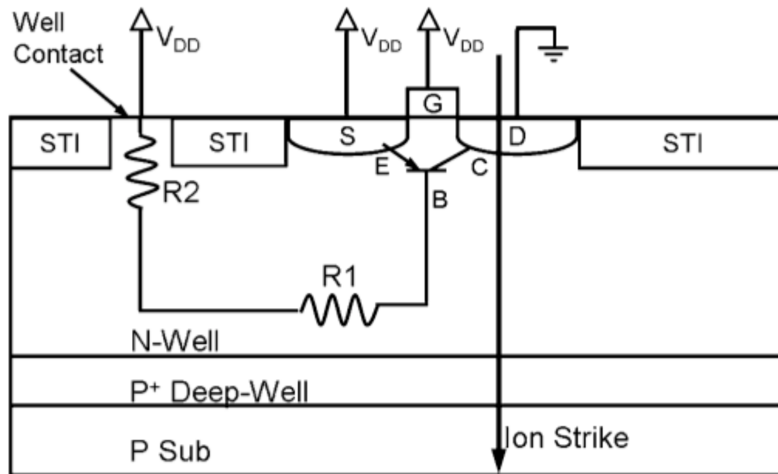

Fig. III-2. Illustration of the horizontal parasitic BJT in a pMOS transistor [Am06].

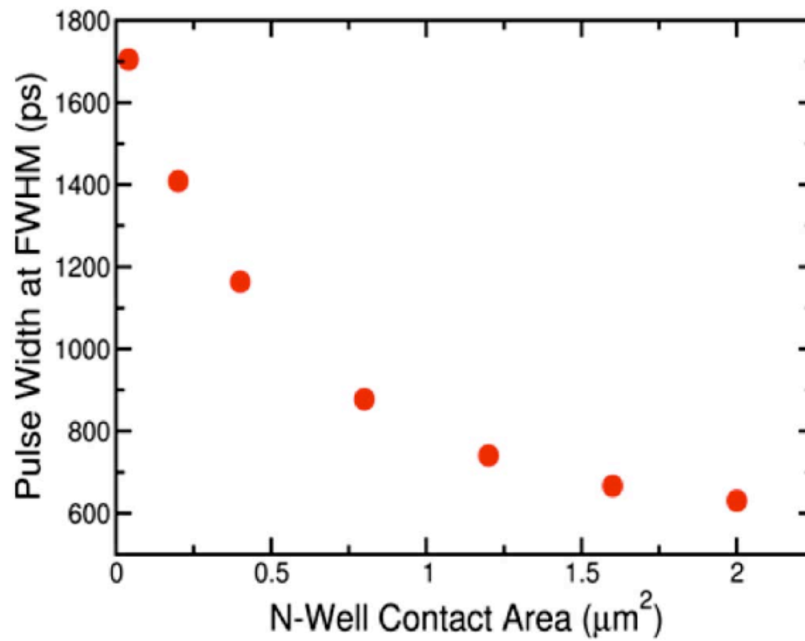

Fig. III-3. FWHM voltage pulse widths for varying n-well contact area from 200 nm x 200 nm to 200 nm x 10 nm. The decrease in the pMOS transistor pulse width (from 1671 to 601 ps) with increased contact area is due to reduced well resistance [Amus07].

Circuit Design

The inherent drive currents and output loads of a circuit are also a key part in determining the pulse width of an SET. CMOS NOR and NOT gates (Fig. III-3) are used to illustrate these concepts. First, consider the drive currents (restoring current) of the transistors. For the case where both inputs are high for the NOR gate, the two nMOS transistors (M3 & M4) in parallel are on and the two pMOS transistors (M1 & M2) in series are 'off'. An ion strike to the drain of M2 will produce a smaller SET than one to the drain of M5 in the inverter with the same size transistor. M3 and M4 restore the voltage to the node as opposed to a single transistor (M6) in the inverter. The greater restoring drive in the NOR reduces the SET pulse width as compared to the inverter.

When the NOR inputs differ, one each of the pMOS transistor and nMOS transistor is 'on', while the other is 'off.' When M1 and M4 are 'off' and M2 and M3 are 'on', the restoring current is half what it is with both inputs 'high' because of the different states of the nMOS transistors. This results in an increased sensitivity of the NOR gate, producing longer SETs than in the previous case. In the opposite case, when M1 and M4 are 'on' and M2 and M3 are 'off', M2 and M3 are equally sensitive to an upset because they both are connected to the output node.

When analyzing the sensitivity of the pMOS transistors, each pMOS transistor is not as equally sensitive when 'off' as the nMOS transistors. With the nMOS transistors in parallel, they both share the 'output' node and the 'ground' node so they have the same loading. However, for the pMOS transistors only M2 is attached to the 'output' node while the other M1 is attached to 'vdd' and M2. Due to this design, M1 has an increased

loading resistance from M2 causing M1 to be less sensitive to ion strikes on its drain while it is ‘off’.

Finally, when comparing the single-event sensitivity of the pMOS transistors to the nMOS transistors while ‘off’, the nFETs are more sensitive. The series pMOS transistors provide a weaker restoring current than the nMOS transistors in parallel because the parallelism of the nMOS transistors provide two separate restoring current paths while the series pMOS transistors provide a single restoring current path to help restore the node after an ion strike.

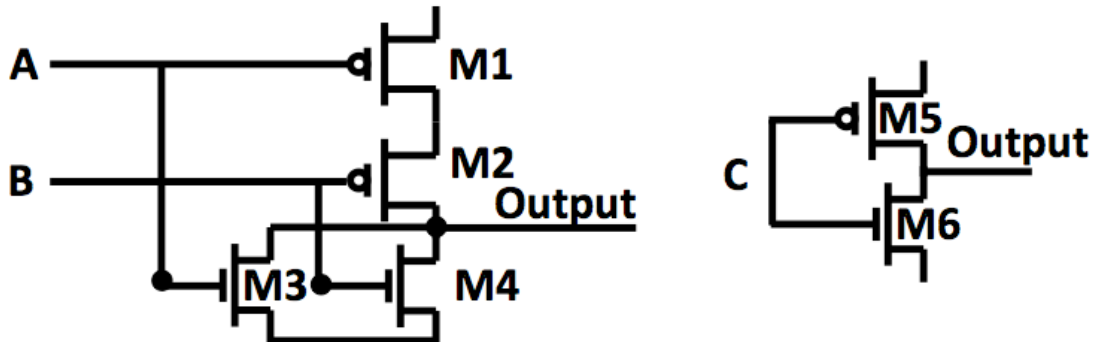

Fig. III-3. Schematic of NOR and NOT gates at the transistor level.

The next factor to consider in circuit sensitivity to ion strikes is output load. Fig. III-4 shows the NOR gate connected to two inverters. The two inverters add capacitance and resistance to the output of the NOR gate. If both inputs to the NOR are ‘low’, then the output voltage is ‘high’. An ion strike to the drain of an nFET will cause a sudden drop in output voltage. Thus, a transient is formed and propagates to the two inverters. However, the additional capacitance and resistance causes the SET to be shorter because of the load on the output. The additional capacitance and resistance requires a larger

amount of drive current to make the NOR gate switch, and this new requirement causes the collected charge to have a reduced effect on the gate.

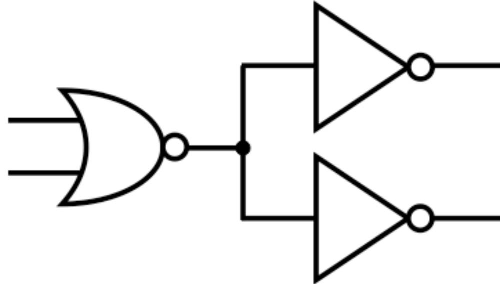

Fig. III-4. Gate level schematic of a NOR gate followed by two inverters.

At sub-100 nm, minimally sized gates, as part of a fan-out design, may not have a significant effect on SET pulse widths [Das07]. The additional capacitance is such that the charging time is short compared to the overall pulse width. However, non-minimum sized gates should provide a significant enough load that will affect SET pulse width [Ha09].

In summary, circuits with large capacitive loads and high restoring currents produce fewer and narrower SETs than circuits with small loads and low restoring currents. A NOR gate has been described showing that transistors in parallel can provide double the restoring current compared to a single transistor to a struck node. Also the sensitivity of different transistors in the NOR gate has been explained. Additionally, gates that increase the amount of resistance and capacitance at the output can reduce the number of SETs. Designers can use these ideas to harden their circuits by increasing the size of transistors in a sensitive circuit, which increases the drive strength, resistance, and

capacitance of the circuit. They can add resistors or capacitors to the outputs of circuits to decrease the sensitivity of the output to generation of SETs.

SET Experimental Characterization

When developing circuit designs in a technology, it is important to know the distribution of SET pulse widths that circuits in the technology will generate in a SE environment. Designers can use the information to predict the error rates for their designs. They can also design hardening schemes that will temporally filter-out certain SET pulse widths to decrease the probability of SEUs occurring [Ea04][Ba06]. To characterize these technologies, many different methods exist for measuring SET pulse widths, but the different methods can be generalized into two categories: off-chip SET measurement and on-chip SET measurement.

Off-chip SET measurement typically involves a string of inverters and pulse laser testing. A device-under-test (DUT) can be laser tested either from the front side by single-photon absorption (SPA) or from the backside by two-photon absorption (TPA) ([Mc02], [Mc03], [St85], [Bo86]); this discussion will only focus on back-side TPA laser testing. For backside laser testing, the DUT is arranged on a platform with the laser striking perpendicular to the DUT backside. Use of the laser, allows a specific region to be hit and a characteristic SET pulse width can be observed from that particular area. Therefore, laser testing can give insight into what regions of a circuit will produce the most severe SETs.

To capture the temporal aspects of SETs, a high-speed oscilloscope that can measure pico-second SET rise and fall times is attached to the output of the DUT. The oscilloscope can be setup where it captures the transient upon detection, or the laser pulse can trigger the oscilloscope. A negative to this type of setup is that the resolution of pulse widths that can be measured is determined by the speed of the oscilloscope. Once the SET is captured, the amount of charge deposited by the laser strike can then be correlated with the captured SET pulse width.

On-chip SET measurement techniques are more varied and can be tested by a pulsed laser or can be tested by a particle accelerator. A particle accelerator can accelerate a variety of ions to high energies and create a realistic SE environment similar to what a circuit in space may experience. For testing, the DUT can be tested in vacuum or in air depending on the testing facilities used. In either case, the DUT is traditionally mounted to a platform that can rotate and tilt so the incident angle of the ion to the DUT can be varied.

To measure SET pulse widths on-chip, researchers have used temporal filtering techniques such as using multiple latches with delayed signal paths (Fig. III-5a) [Ea04]. For a signal to propagate through the temporal latch circuit (Fig. III-5a) and be measured, the signal must have a pulse width wide enough that the built-in delay of the signal path does not stop the signal from appearing at the input of the voter at the same time as the other signal paths. If the multiple inputs of the voter are the same, then the signal propagates through the circuit for measurement. Guard-gate-based techniques have also been used to measure SET pulse widths as shown in Fig. III-5b [Ba06] and operate similarly to the temporal latch technique. There are two signal paths – one with no delay

and one with a variable delay. If the signal is wide enough that the built-in delay of the delayed signal path does not stop it from arriving at the input of the guard gate at the same time as the non-delayed signal path, then the guard gate will change states. The signal will then propagate through the gate.

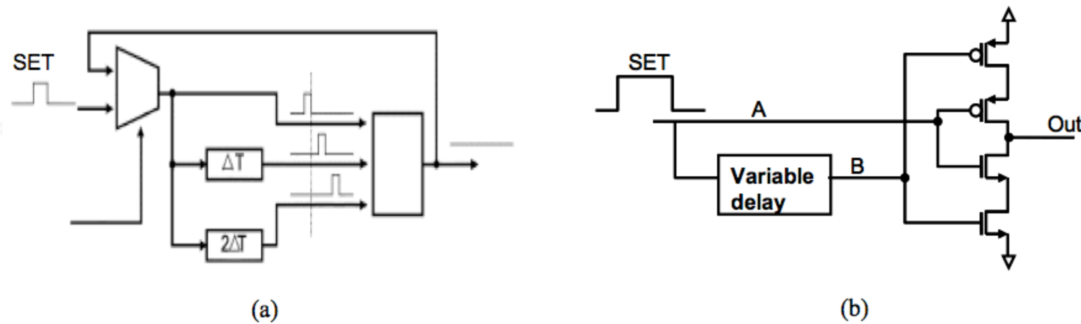

Fig. III-5 (a) Variable temporal latch technique and (b) guard gate based technique for characterizing the width of SET pulses [Ea04] [Ba06].

Another approach to on-chip SET measurement is the autonomous pulse-width measurement technique. Fig. III-6 shows the schematic design of the measurement circuit. This technique measures SET pulse width by latch delays [Na06]. When an SET is generated in the target structure and propagates to the measurement portion of the circuit, the SET passes through latches that switch states. Once an SET pulse has been captured, an attached Field Programmable Gate Array (FPGA) serially reads out the state of each latch in the measurement chain. Software on the FPGA then calculates the number of latches that changed state. Then the pulse width for that SET is calculated by multiplying the number of stages by latch delay.

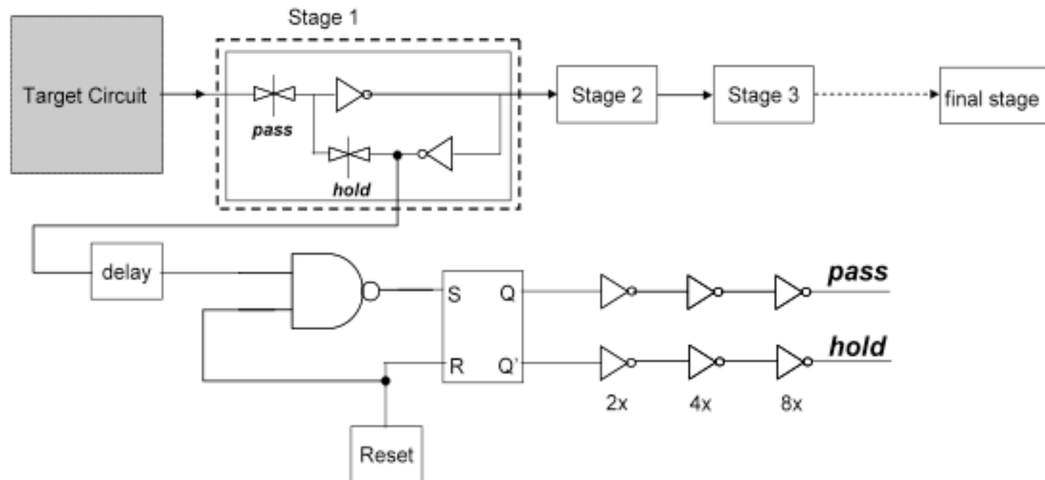

Fig. III-6 Autonomous pulse-width measurement technique [Na06].

Target Structures

This section discusses how target structures can influence the SET measurement results. A common target design is the current-drive matched inverter. The inverter is a simple design that is easily upset by an ion strike. SET pulse widths from an inverter chain can indicate the type of SETs a more complex combinational logic circuit will generate. However, for accurate SET statistics from accelerator testing, it is necessary to create inverter chains that are over 1000 inverters long. In accelerator testing, the ions cannot be precisely aimed towards sensitive parts of the circuit, so a large sensitive area needs to be designed to increase the probability that ions will strike the circuit.

Recently, Ferlet-Cavrois et al. [Fe07] and Massengill & Tuinenga [Ma08] described how transient signals can widen as they propagate through a combinational logic chain. A description of the mechanism behind the pulse broadening effect in inverter chains is given by Massengill [Ma08]. To minimize pulse broadening in target

circuits, designers are using smaller chains OR-ed together to create the cross-section needed for accurate measurement statistics [Ga10].

Additionally, specific inverter layout techniques, such as minimum spacing or separate wells, can distort SET pulse width results. Experimental data has shown how inverters with the same sizing but different layouts can produce different SET pulse width distributions [Ah09]. The mechanisms behind the differences in SET pulse widths between the inverter layouts will be discussed in Chapter V.

Conclusion

This chapter discusses the importance of SET pulse widths and some of the factors that influence the generation of an SET. Transistors that have a parasitic BJT are prone to have longer SET pulse widths than transistors with no parasitic BJT. Circuits with high restoring currents and load capacitance are less sensitive to SET generation. Last, the layout and design of target structures can influence SET pulse width results, which can lead to misinterpreting the data.

CHAPTER IV

EFFECT OF N-WELL CONTACT AREA ON SINGLE-EVENT TRANSIENTS

Introduction

In this chapter, direct experimental evidence is presented that supports previous simulations [Am08] demonstrating the n-well contact area's effect on SETs. Using five inverter chains with a different controlled percentage of the n-well area devoted to ohmic contacts, results show that the inverter chain with minimum-sized n-well contacts spaced 30 μm apart produced the longest and the highest count of SETs. Conversely, the inverter chain with a minimum-contact-width n-well contact strip that spanned the entire n-well, produced the shortest and the lowest count of SETs.

Parasitic BJT's Influence on SET Pulse Widths

As stated in Chapter III, the n-well contact area influences the amount of charge collected by the drain due to parasitic BJT conduction. Fig. IV-1 shows this influence between n-well contact area and charge collection on a drain of a pMOS transistor by plotting the percentage of n-well area contacted versus enhancement factor [Ol07]. The enhancement factor is defined as the amount of charge collected by the drain of a pMOS transistor with the parasitic BJT enabled over the amount of charge collected by the drain with the parasitic BJT disabled.

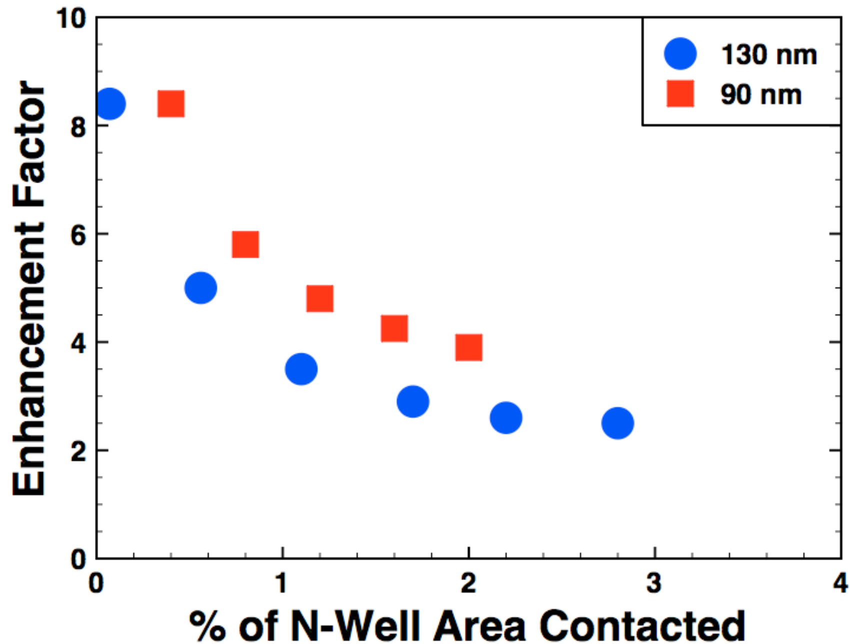

Fig. IV-1. 3D TCAD simulations at an LET of 40 MeV-cm^2/mg illustrating the effect n-well contact area has on parasitic BJT conduction [Ol07].

As the percentage of the n-well area contacted decreases in Fig. IV-1, the amount of parasitic BJT conduction increases [Ol07]. Parasitic BJT conduction increases because the n-well contact controls the vertical resistance of the n-well. As the n-well contact decreases in area, the vertical resistance increases and creates a highly resistive path for electrons to leave the n-well. This condition results in the n-well being easily de-biased by an ion strike and requiring a significant time to restore its bias.

Similar to Fig. IV-1, an inversley proportional relationship exists in Fig. IV-2 between SET pulse width and percentage of the n-well area contacted [Am07]. As the percentage of n-well area contacted decreases, parasitic BJT conduction increases and the drain collects additional charge. The additional charge collection generates a larger collection current at the drain than without parasitic BJT conduction, and the transistor

takes longer to recover. Since the time it takes for the transistor to recover determines the pulse width of the SET, any increase in recovery time results in a longer SET pulse.

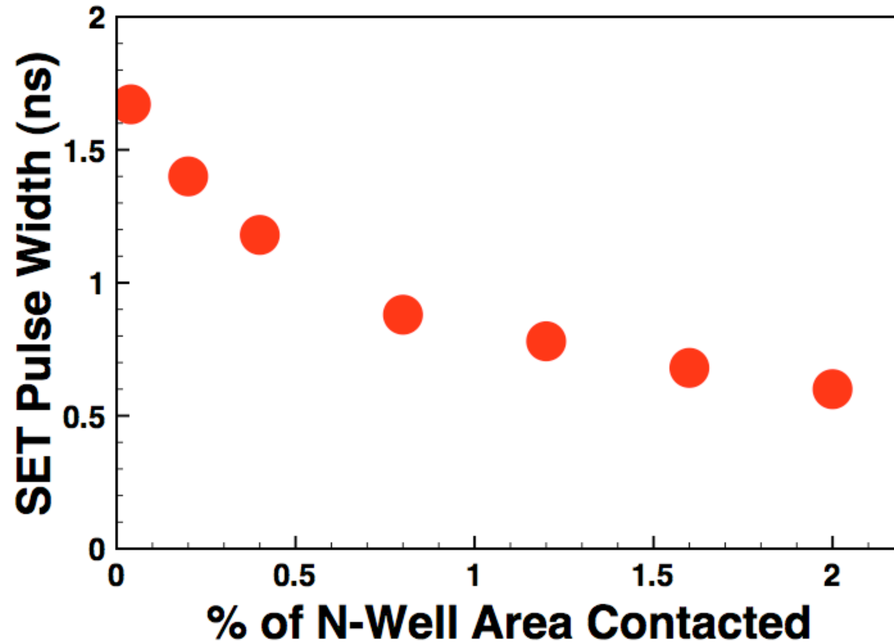

Fig. IV-2. 3D TCAD simulations at an LET of 40 MeV-cm^2/mg illustrating the effect n-well contact area has on SET pulse width [Am07].

Using previously published data, Fig. IV-3 also shows an inversely proportional relationship between the percentage of n-well area contacted and SET pulse width [Ga10]. The figure plots the maximum SET pulse widths measured for 130 nm, 90 nm, and 65 nm dual-well, bulk CMOS technologies. Knowing that an inverseley proportional relationship between the percentage of n-well area contacted and SET pulse width indicates the influence of parasitic BJT conduction, the data suggests parasitic BJT conduction in pMOS transistors determines the maximum SET pulse width in each technology. The data also suggests the design of the n-well contacts may explain the maximum SET pulse width trends observed in the three technology nodes. However, additional variables, such as transistor sizing [Zh04] and pulse quenching [Ah09]

mechanisms exist in those data sets and maybe influencing the SET pulse width data. As a result, those variables need to be minimzed to quantify accurately the effects of n-well contacted area on SET pulse widths.

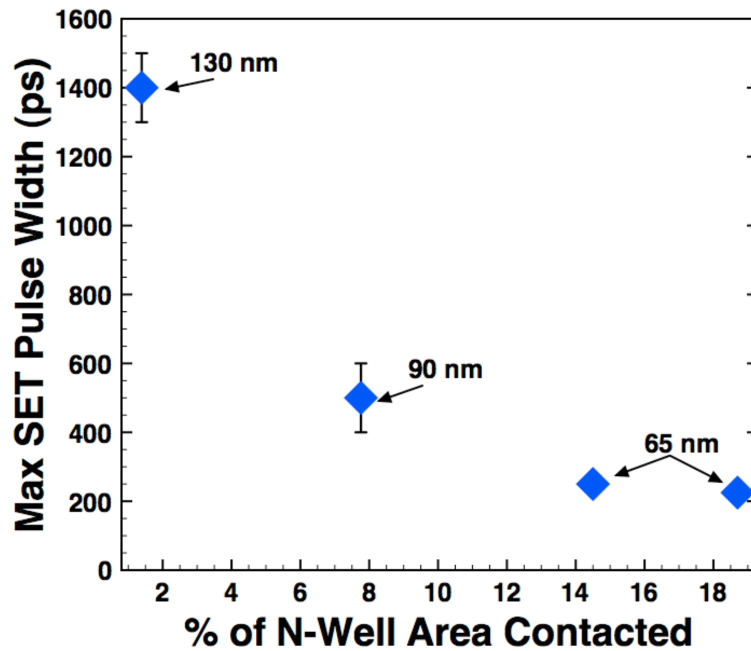

Fig. IV-3. Experimental SET pulse width measurements for 130 nm, 90nm, and 65 nm bulk CMOS technologies at an LET of 58 MeV-cm^2/mg [Ga10].

Design of a Test Circuit to Quantify the Influence the Percentage of N-Well Area Contacted has on SET Characterization

To quantify the impact the percentage of n-well area contacted has on SET pulse width, a test chip containing five inverter chains was designed and fabricated in the TSMC 90 nm dual-well, bulk CMOS process. Each inverter chain was followed by an autonomous pulse-width measurement circuit described in [Na06]. The inverters were designed to be current-matched with a pMOS transistor W/L ratio of 400 nm/100 nm and

an nMOS transistor W/L ratio of 200 nm/100 nm. These target chains were laid out in 10 rows of 100 inverters each and ORed together. So that the SETs measured are minimally affected by pulse broadening [Fe07][Fe08].

To minimize non-n-well contact area effects, most aspects of the target inverter chains were kept constant across the five different designs. Charge sharing was minimized by setting the active area spacing between the inverters at 3 µm. Additionally, each inverter had a minimum-size, 0.26 µm x 0.26 µm, p-well contact and each target chain at the same sized n-well. The differentiating aspect of the designs was the amount of n-well area contacted.

In the first target chain design shown in Fig. IV-4, the n-well was contacted according to the minimum n-well contact and maximum n-well contact spacing as defined by the process design rules. Twelve minimum sized n-well contacts of 0.26 µm x 0.26 µm were placed 30 µm apart in each of the ten n-well chains dedicated to that target design. This is an n-well contact placement design technique commonly used in commercial designs to save space. Since few contacts were used in the design, the contacting scheme covered 0.14% of the n-well area.

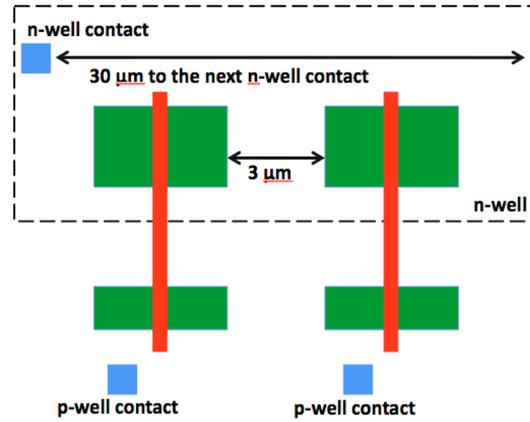

Fig. IV-4. N-well contacting scheme that covers 0.14% of the n-well area (minimum n-well contact design rules). Twelve minimum sized n-well contacts of 0.26 µm x 0.26 µm were placed 30 µm apart in each of the ten n-well chains dedicated to that target design.

The second design, displayed in Fig. IV-5, included n-well contacts covering 0.5% of the n-well area. The same number of n-well contacts was used as the previous design, but each contact size was larger at 0.98 µm x 0.26 µm and spaced 29 µm from each other. Fig. IV-6 shows the third design where each inverter had a minimum-sized n-well contact. In this design 1.2% of the n-well area was covered by contacts. The next design, shown in Fig. IV-7, included n-well contacts covering a total of 5.0% of the n-well area by placing an n-well contact of 1.13 µm x 0.26 µm within each inverter cell. In the final design, Fig. IV-8, a single contact that spans the entire length of the n-well was used – commonly known as a strip n-well contact. The strip contact covered 15.7% of the total n-well area.

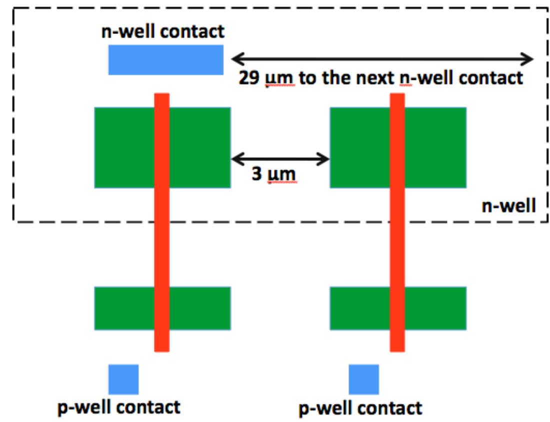

Fig. IV-5. N-well contacting scheme that covers 0.5% of the n-well area. Twelve minimum sized n-well contacts of 0.98 µm x 0.26 µm were designed and spaced 29 µm from each other.

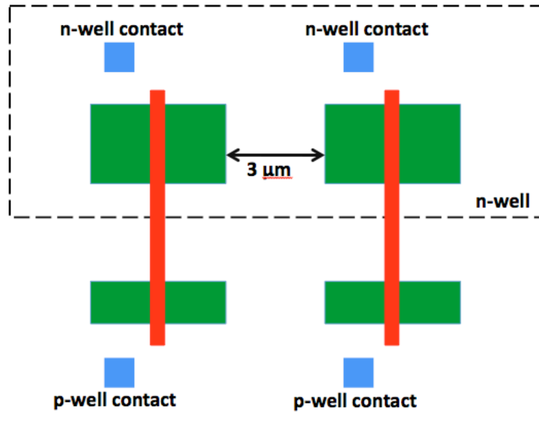

Fig. IV-6. N-well contacting scheme that covers 1.2% of the n-well area because each inverter has a 0.26 µm x 0.26 µm n-well contact.

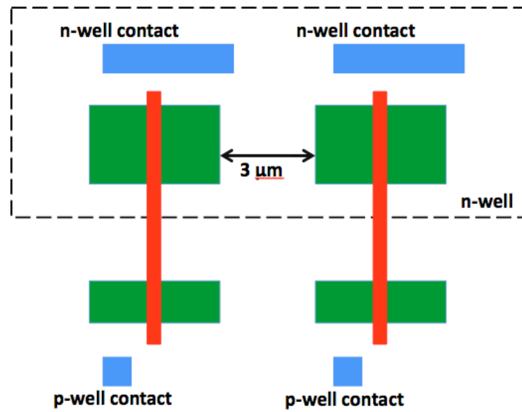

Fig. IV-7. N-well contacting scheme that covers 5.0% of the n-well area. Each inverter has its own 1.13 µm x 0.26 µm n-well contact.

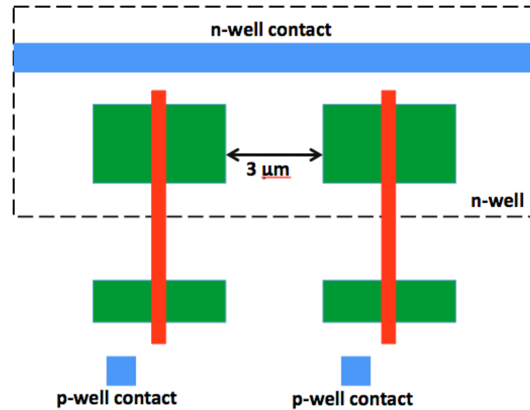

Fig. IV-8. N-well contacting scheme that covers 15.7% of the n-well area because a 0.26 µm wide n-well contact spans the entire length of the n-well.

Experimental Heavy-ion Broadbeam SET Measurements

The circuits were tested at the Lawrence Berkeley National Laboratory with the 10 MeV/nucleon ion cocktail using Ne, Ar, Cu, Kr, and Xe ions at normal incidence. For Xe the circuit was tested to an effective fluence of 1.2 x 10^8 particles/cm^2. Mid-energy ions of Kr and Cu were tested to effective fluences of 5 x 10^7 and 1.5 x 10^8 particles/cm^2 respectively. Last, effective fluences of 3 x 10^8 and 1.2 x 10^9 particles/cm^2 were used for for Ar and Ne.

Figs. IV-9, IV-10, IV-11, IV-12, and IV-13 show the results of the circuits exposed to the different ions. Each circuit is labeled by the percentage of n-well area covered by contacts. The distributions for the lowest n-well contact coverage of 0.14% and 0.5% have the widest distributions of SET pulse widths out of the five circuits, whereas the circuits with 5.0% and 15.7% n-well contact coverage have the narrowest pulse width distributions, as seen in Fig. IV-9. In Figs. IV-10, IV-11, IV-12, IV-13, the SET distributions for 5.0% and 15.7% n-well contact coverage are not easily visible because of the significant amount of events observed for the 0.14% and 0.5% circuits.

The distribution of SET pulse widths is the result of ion strikes occurring at different distances from the sensitive area within an inverter [Fe06]. For the 0.14% and 0.5% circuits, their distributions are the widest because the low percentage of n-well area contacted results in a high vertical resistance [Ol05][Amus07]. The high vertical resistance that exists between the n-well and n-well contact (R2 in Fig. III-2) makes the n-well more susceptible to being de-biased by ion strikes compared to a low vertical resistance. The electrons that are generated in the n-well from the ion strike cannot be collected as quickly by the n-well contacts [Da07]. Unlike the 0.14% and 0.5% circuits, the 5.0% and 15.7% n-well area contacted circuits have a narrower distribution of SET pulse widths because the n-well contacting results in a lower vertical resistance [Ol05][Amus07].

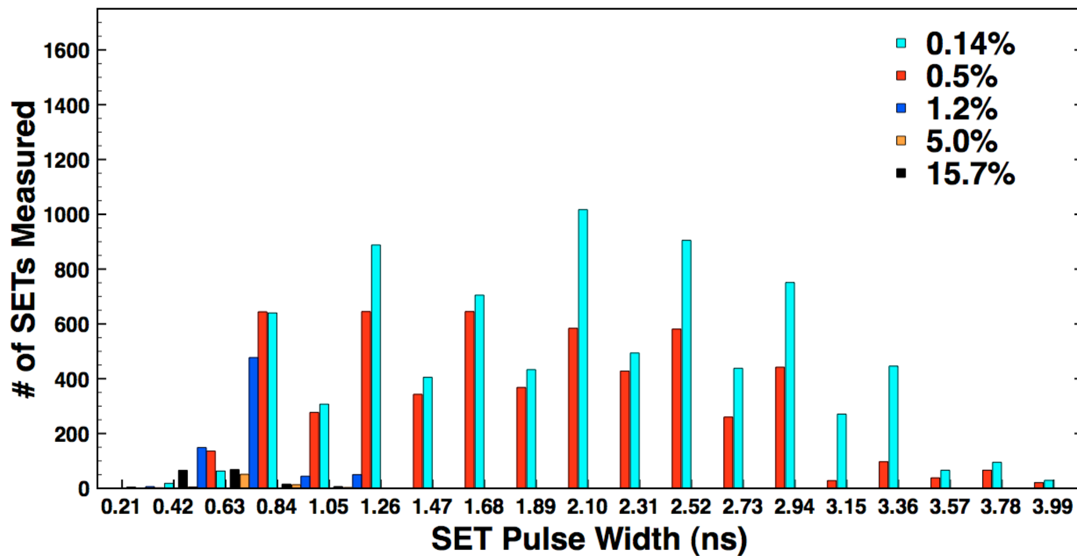

Fig. IV-9. Experimental results for an LET of 58 MeV-cm^2/mg showing the distribution of SET pulse widths for the five different n-well contacting schemes.

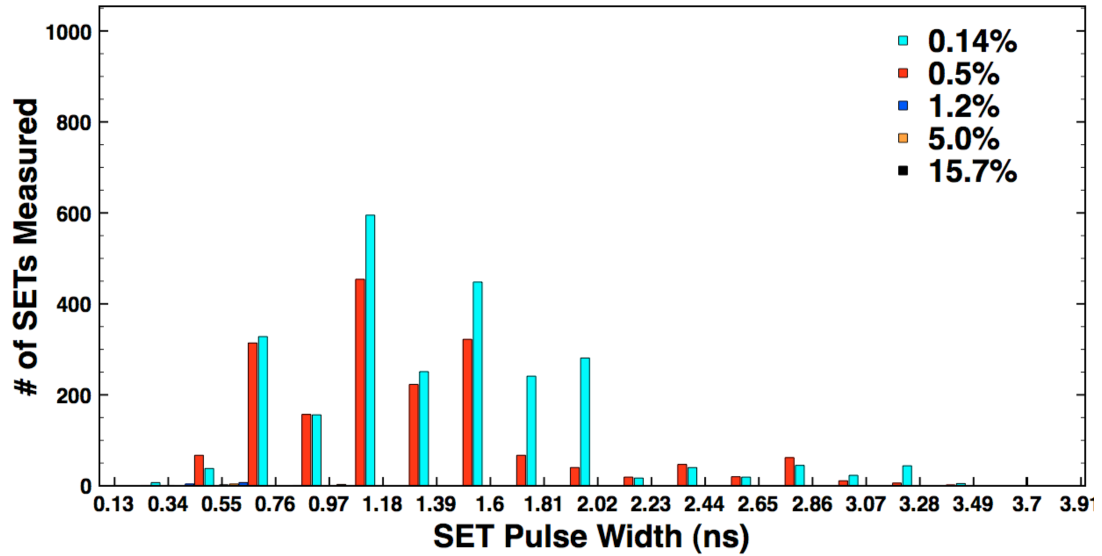

Fig. IV-10. Experimental results for an LET of 30.86 MeV-cm^2/mg showing the distribution of SET pulse widths for the five different n-well contacting schemes.

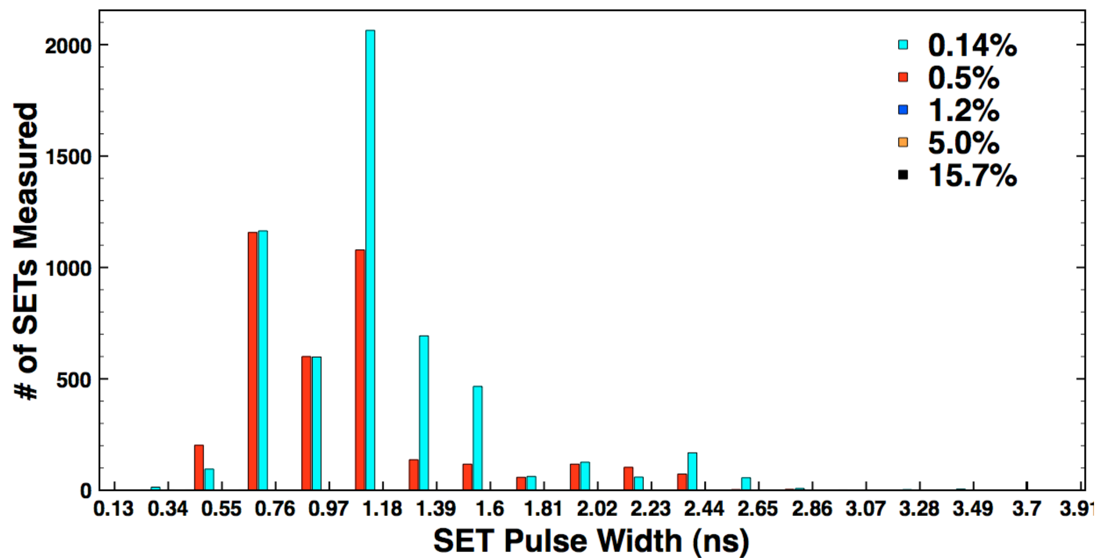

Fig. IV-11. Experimental results for an LET of 21.17 MeV-cm^2/mg showing the distribution of SET pulse widths for the five different n-well contacting schemes.

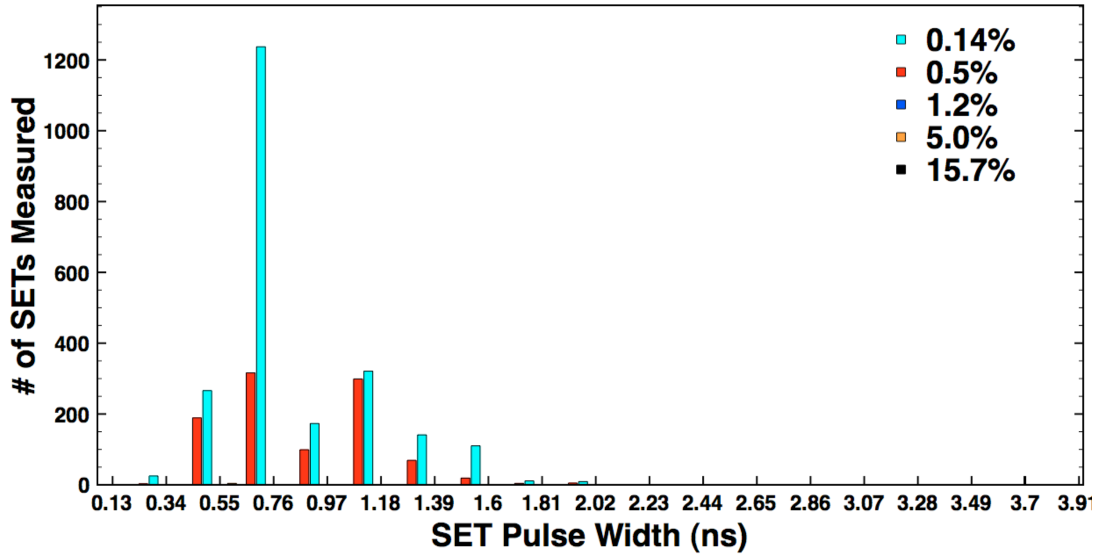

Fig. IV-12. Experimental results for an LET of 9.74 MeV-cm^2/mg showing the distribution of SET pulse widths for the five different n-well contacting schemes.

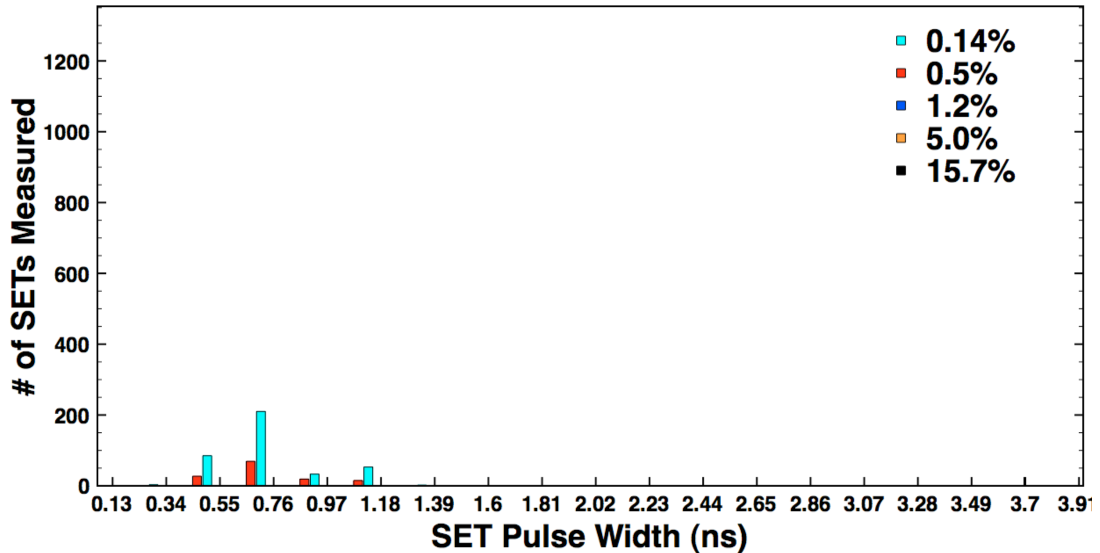

Fig. IV-13. Experimental results for an LET of 3.49 MeV-cm^2/mg showing the distribution of SET pulse widths for the five different n-well contacting schemes.

Using the measured SET pulse widths plotted in Fig. IV-9, the mean SET pulse width (μ) and the standard deviation (σ) are calculated for each circuit, assuming a

Gaussian distribution of pulse widths. These results are plotted in Fig. IV-14. Additionally, the maximum SET pulse widths from Fig. IV-3 and average SET pulse width from [Ga10] are plotted in the same figure.

Similar to Figs. IV-1, IV-2, and IV-3, the results for TSMC 90 nm dual-well, bulk CMOS process exhibit an inverseley proportional relationship between SET pulse width and percentage of n-well area contacted. This inverseley proportional relationship between pulse width and n-well contact area is a result of the parasitic BJT amplification mechanism as observed previously by [Ol07] [Amus08]. Above 2% of n-well area contacted, the SET pulse width data saturates. Pulse width saturation is the result of the lateral resistive path (R1 in Fig. III-2) in the n-well being the dominant resistive path for charge removal instead of the vertical resistive path [Ol07]. The lateral resistance controls the duration for which the parasitic BJT remains ON and the amount of charge collected at the drain node of the hit transistor.

Further than just having similar trends to the TSMC 90 nm data, the 65 nm, 90 nm, and 130 nm data from [Ga10] plotted in Fig. IV-14 have similar magnitudes to the TSMC 90 nm data. For example, the average values for the 130 nm, 90 nm, and 65 nm [Ga10] data would fall within $+1\sigma$ of the TSMC 90 nm data with the best example being a comparison between the 65 nm data and the TSMC 90 nm 15.7% circuits. If the 65 nm data and the 15.7% data were shifted to have the same percentage of n-well area contacted, they would overlap each other. Therefore, the similar trends and magnitudes between all data sets in Fig. IV-14 validate the original conclusion from [Ga10] that the pulse width trends observed from different bulk technologies can be explained by the percentage of the n-well area contacted.

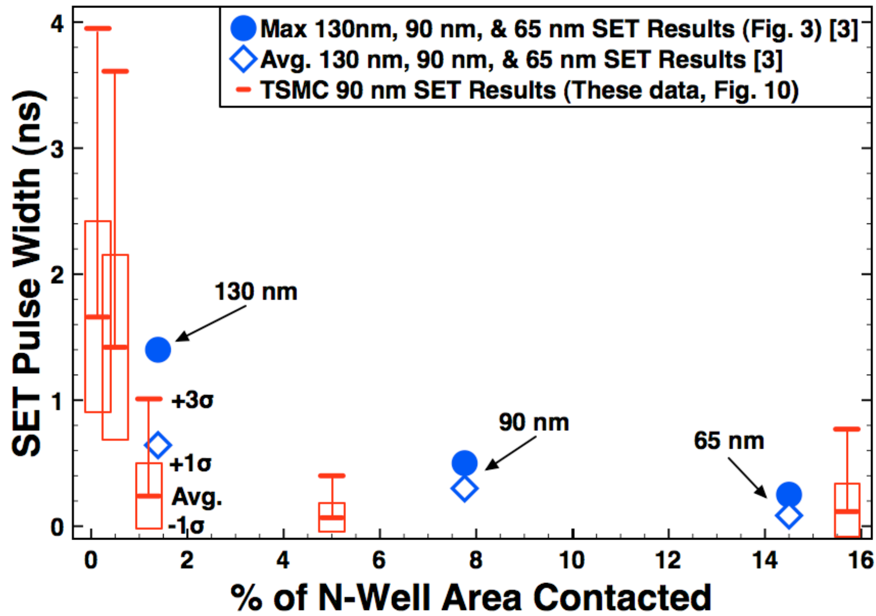

Fig. IV-14. Comparison of TSMC 90 nm SET results to [Ga10] SET results for an LET of 58 MeV-cm^2/mg.

Analysis of the Cross Section Results

Similar to the SET pulse width results where the 0.14% and 0.5% n-well area contacted circuits had the longest SET pulse widths, those two circuits also had the highest cross sections over all LETs, as seen in Fig. IV-15. The cross section calculated in Fig. IV-15 is calculated by defining an upset as any SET longer than 15 ps [Ga10]. As the plot illustrates, there is little difference in the cross sections among the 1.2%, 5%, and 15.7% n-well area contacted circuits – suggesting there is a limit to the effectiveness of n-well contact area at reducing the cross section.

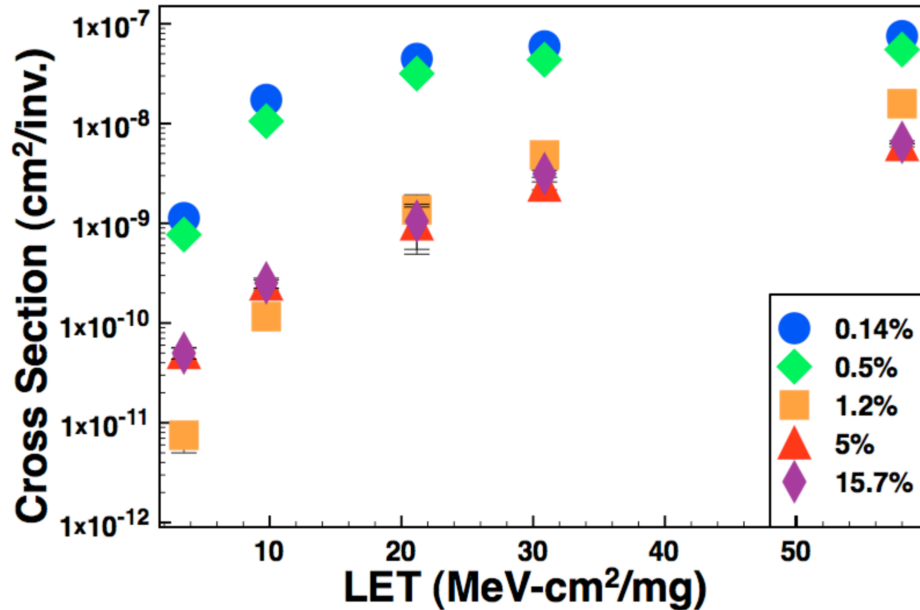

Fig. IV-15. Cross section versus LET for the five different inverter chain test structures.

Further, regardless of transistor design, Fig. IV-15 shows that the percentage of n-well area contacted influences the sensitive area of the inverters. A result that contradicts the traditional theory that cross section of a logic gate is based entirely on the drain regions of the transistors. In this work, the inverters have identical drain regions, but results show vastly different cross sections; indicating there are additional factors (specifically n-well contact area) that influence the logic gate cross section.

The lower percentage of n-well area contacted allows the n-well to be de-biased more often during an ion strike than the other contacting schemes. De-biasing of the well can result in BJT turn-on and the generation of SETs in the inverter chains. Since n-well contacts also serve to dissipate deposited charge, a reduction in the n-well contact area

also increases the probability that deposited charge will be collected by sensitive junctions and not n-well contacts.

Fig. IV-16 illustrates the relationship between cross section and percentage of n-well area contacted at an LET of 58 MeV-cm^2/mg. From the data, there is an obvious inverseley proportional relationship between the cross section and percentage of n-well area contacted, which matches the relationships seen in Figs. IV-1, IV-2, IV-3, and IV-14. This inverseley proportional relationship is a result of parasitic BJT mechanism [Ol07][Amus08][Ahl11]. Therefore, these results suggest that the parasitic BJT is a significant factor in not only determining the pulse width of SETs, but also in determining the sensitive area for a given logic gate.

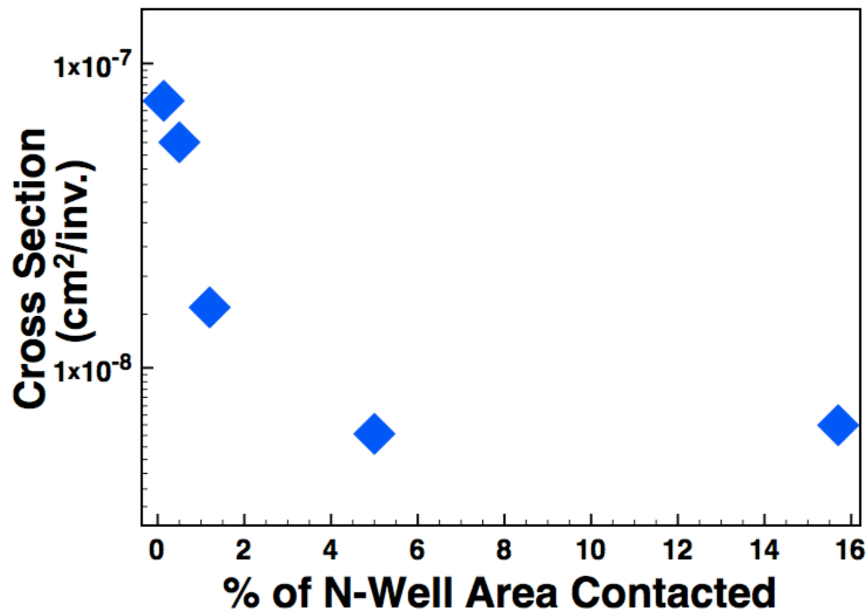

Fig. IV-16. Cross section for the five TSMC 90 nm inverter chain test structures for an LET of 58 MeV-cm^2/mg.

Conclusion

Using five n-well contacting scheme variants for otherwise identical inverter chains, heavy-ion data shows that the percentage of n-well area covered by contacts is a key factor in determining SET pulse widths. These results agree with previous work [Ol07][Amus08] showing a strong relationship between SET pulse width and the percentage of n-well area contacted. Additionally, the data validates that SET pulse widths measured across multiple technologies can be explained by the percentage of n-well area contacted and not by process related changes alone. Thus, the SET pulse width trend for the different technolgies is the result of a design trend in n-well contact area. Designers still need to be aware of pulse broadening and pulse quenching because these mechanisms can significantly affect pulse width measurements regardless of the percentage of n-well area contacted.

In this work, inverseley proportional relationships are observed between SET pulse width and percentage of n-well area contacted and between cross section and percentage of the n-well area contacted. These relationships strongly suggest that parasitic BJT amplification from pMOS transistors influences not only SET pulse width but also cross section. Also, an inverseley proportional relationship between cross section and percentage of n-well area contacted contradicts the traditional theory that the cross section of a logic gate is based entirely on the drain regions of the transistors. Even though all drain regions of the five different test structures are the same, the cross sections for each test structure are vastly different. These results indicate there are now

additional factors (specifically n-well contact area) that can influence the cross section of logic gates.

CHAPTER V

EFFECTS OF CHARGE SHARING ON SINGLE-EVENT TRANSIENTS

Introduction

As the minimum spacing between transistors decreases in each technology node, the probability that charge sharing will occur among multiple nodes increases. Simulation and experimental results from sub-micron process nodes show that charge sharing can affect SET pulse width [Ah09] [Ah10] [Se10] [Ke10] [Ahl10] [Ah11] [At11] [Atk11]. In this chapter, the effects of charge sharing on SETs in 130 nm, 90 nm, and 65 nm bulk CMOS processes will be discussed. The discussion will focus on how layout and circuit design play a critical role in the creation and propagation of SETs, and how designers need to be mindful of both the circuit's layout and electrical characteristics.

Pulse Quenching

At 130 nm and smaller technology nodes, SE simulation and experimental results [Ol05][Am06][Ke07] show that charge sharing between adjacent transistors and signal propagation between adjacent circuits can occur within the same time frame (typically not the case in older technology nodes). Analyses indicate that the concurrency of charge sharing and electrical signal propagation within a circuit can cause downstream SET voltage pulses to be shortened or eliminated – an effect called pulse quenching [Ah09].

Pulse Quenching Between Adjacent Inverters

Fig. V-1 shows a schematic of a three-stage inverter chain. The output nodes of each inverter (Inv1, Inv2, and Inv3) in the figure are designated by Out1, Out2, and Out3, respectively. Assume a LOW input to the chain. Initially, the pMOS transistors associated with Inv1 and Inv3 are ON, the pMOS transistor of Inv2 is OFF, and Out2 is LOW. If an ion strikes the OFF pMOS transistor of Inv2, the logic LOW state at Out2 is driven HIGH by the charge collection and an SET pulse HIGH is generated at Out2. This SET pulse will propagate to Inv3, resulting in a HIGH-to-LOW transition at Out3 and a change of state of the pMOS transistors of Inv3 to OFF. When the pMOS transistor of Inv3 turns OFF, it is then susceptible to charge collection. Charge from the single-event strike on Inv2 can diffuse to Inv3 (through the mechanisms of charge sharing) and be collected by the pMOS transistor of Inv3, driving the state of Out3 HIGH. This LOW-to-HIGH transition at Out3 "resets" the node voltage to the pre-event state, effectively truncating the SET pulse, as shown in Fig. V-2. Thus, there are two factors affecting the dynamic node voltage at Out3. The first is the signal propagation of the SET pulse from Out2; the second is the delayed collection of charge at Out3 due to charge sharing with the struck node of Out2. The propagating SET electrical signal arrives first at Out3, resulting in a HIGH-to-LOW transition; the charge sharing signal arrives second, forcing Out3 back to a HIGH state. The pulse at Out3 is quenched by the delayed charge collection.

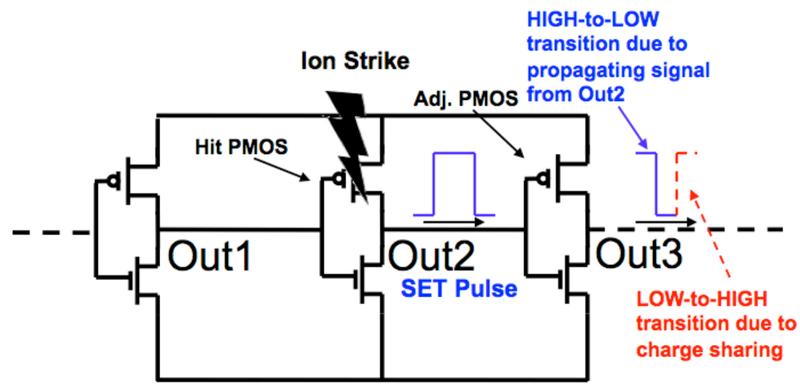

Fig. V-1. A schematic of a chain of three inverters illustrating the change in SET pulse width as it propagates.

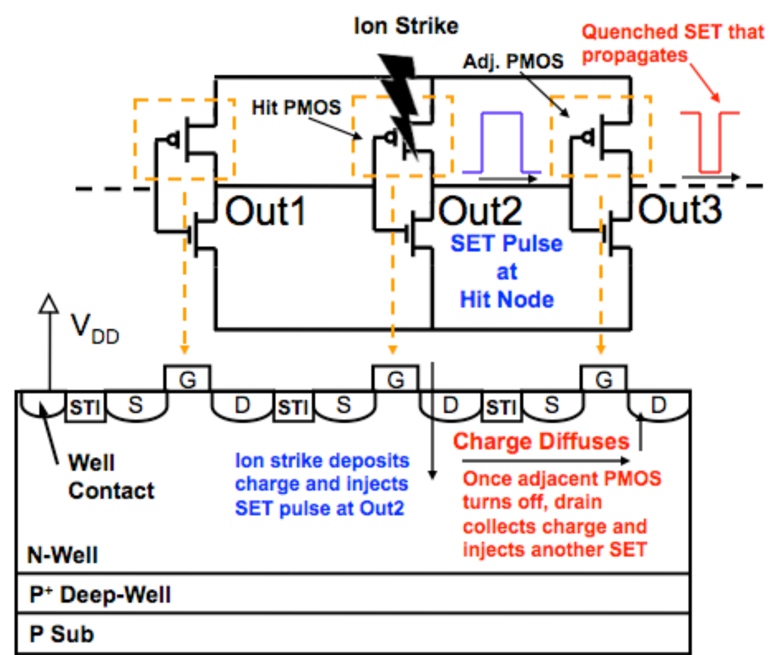

Fig. V-2. Two-dimensional slice of three pMOS transistors depicting the electrical signal and the charge sharing signal caused by an ion strike.

In order for pulse quenching to occur, the technology must be susceptible to charge sharing. So, it could be argued that technologies immune to charge sharing would not exhibit pulse quenching. Also, because some technologies are sensitive to charge sharing only for angled single event strikes [Amu07][Amus07], it could also be argued

that pulse quenching would not be observed in these technologies for normal-incidence ion strikes, but would be observed for angled strikes.

A second requirement for pulse quenching to occur is that the charge collection time constant associated with charge sharing must be on the same order as the gate-to-gate electrical propagation delay of the logic. The charge sharing signal must arrive contemporaneously with the propagating SET electrical signal in order to affect the pulse width.

In addition, while it is expected (and has been demonstrated [Ea04][Ba06][Na06][Na08]) that the SET pulse width at Out2 would increase directly with LET, the quenched pulse width at Out3 instead should depend strongly on the time differential between the arrival of the topside electrical signal and the substrate charge sharing signal, and weakly on the width of the originating SET pulse. Therefore, technologies that exhibit significant charge sharing and possess electrical and charge collection time constants on the same order should exhibit pulse quenching.

Pulse Quenching within an Inverter

Pulse quenching has been explained to occur between inverters in an inverter chain, but it can also occur between the nMOS and pMOS transistors within a single inverter cell. Fig. V-3 shows the steps involved in the charge collection process by both the nMOS and pMOS transistors and the subsequent reduction in the resultant SET. First, the ion strikes the nMOS transistor while it is in the OFF state. The nMOS transistor drain collects charge and perturbs the output node voltage of the inverter. The switch in output node voltage causes the parasitic bipolar within the pMOS transistor to turn-on

and inject charge that is collected by the drain of the pMOS transistor. This collected charge is seen as additional current that enhances the restoring power of the pMOS transistor and helps shorten the SET.

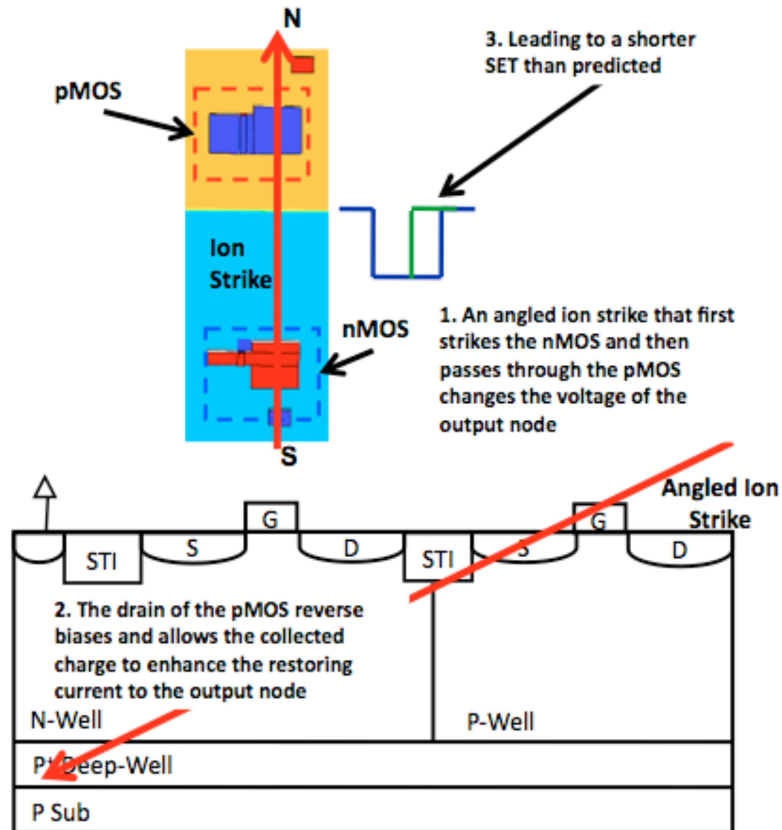

Fig. V-3. Two-dimensional diagram illustrating the multiple transistor charge collection mechanism that leads to a shorter than predicted SET pulse width.

Identification of Pulse Quenching at the 130 nm Technology Node

Effects of Charge Sharing Efficiency on Pulse Quenching

Given that charge sharing is an important contributor to the SET pulse quenching effect, circuits with strong charge sharing should exhibit strong pulse quenching and reduced average SET pulse widths. On the other hand, mitigation of charge sharing should also mitigate pulse quenching. That is, circuits with reduced charge sharing should exhibit longer average SET pulse widths. Thus, charge sharing mitigation (or enhancement) on an otherwise identical circuit would serve as an appropriate test split for pulse quenching experiments.

One technique that has been successful in enhancing charge sharing is testing at a high angle of ion incidence. Nodes that may not share charge at normal incidence of an ion strike are often very sensitive to charge sharing at higher angles of incidence [Am07].

A technique that has been successful in mitigating charge sharing is the use of guard bands [Bl05]. Guard bands serve to reduce the region of influence for charge sharing by serving as a charge sink and by maintaining substrate/well potential. Amusan et al. [Am06] performed 3D TCAD simulations for 130 nm bulk CMOS pMOS transistors to compare the effects of charge sharing on adjacent transistors both with and without guard bands. Fig. V-4 is an example of their results, illustrating the difference in charge collection between the two cases [Amus06]. At ion energies greater than 20 MeV-cm^2/mg, a distinct difference in charge collection between transistors with guard bands and without guard bands can clearly be seen.

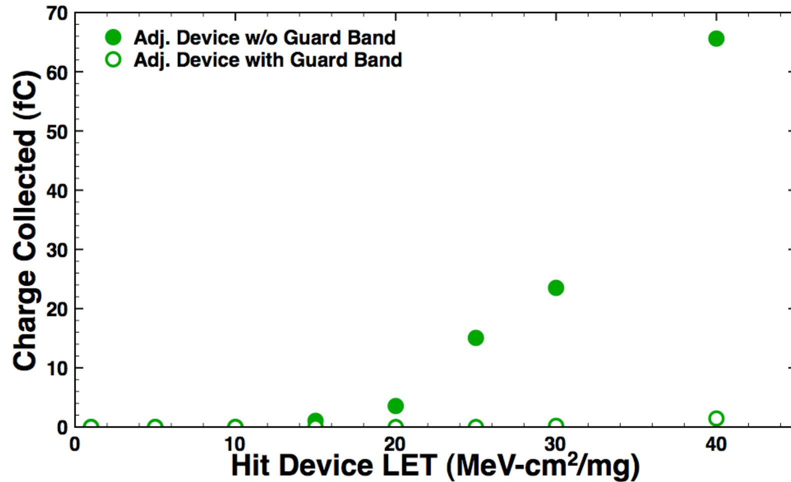

Fig. V-4. Plot comparing charge collected by an adjacent pMOS transistor with/without guard bands (after [Am06]).

Simulation Experiment Correlating Pulse Quenching and Charge Sharing for Multiple Inverters

To understand and verify the presence of the pulse quenching mechanism, an analysis of the 130 nm technology node was carried out using Synopsys 3D mixed-mode (i.e. combination of TCAD finite-element transistor models and SPICE-like admittance-matrix compact models) tools. Each TCAD model contained two pMOS transistors and these transistors were calibrated to match dc and ac electrical characteristics (e.g., I_d-V_d and I_d-V_g curves) based on the IBM CMOS8RF PDK [Am06]. Except for the presence of guard bands, the rest of the circuit/transistor parameters were kept identical. Fig. V-5 shows both TCAD models where the top model contains two pMOS transistors with guard bands while the bottom model does not contain guard bands.

All simulations were carried out with a 9-stage, minimum-sized, matched current-drive inverter chain with the 3D TCAD section representing the pMOS transistors in the 2nd and 3rd stages. The pMOS transistor in the 2nd stage (Out2 from Fig. V-1) represented the hit pMOS transistor while the pMOS transistor in the 3rd stage (Out3 from Fig. V-1)

represented the adjacent PMOS. All simulations used the following physical models: Fermi-Dirac statistics, SRH and Auger recombination, and the Philips mobility model. The incident heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps. In each simulation, the ion strike occurred at 1 ns. Simulations were carried out using the Vanderbilt ACCRE computing cluster [ACCRE].

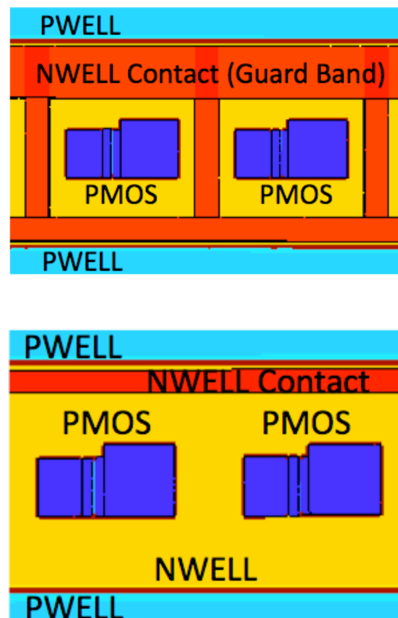

Fig. V-5. Two 3D TCAD models of two 130 nm pMOS transistors with/without guard bands.

These simulation models were each struck with a 30 MeV-cm^2/mg ion at 60° along the n-well longitudinal axis to promote charge sharing conditions among the transistors [Amu07]. Fig. V-6 shows the SET generated from the two pMOS transistors with guard bands. It can be seen that quenching does not occur because the transient at the adjacent node (Out3) is not shorter than the transient at the hit node (Out2). Fig. V-7 shows the SET generated from the two pMOS transistors without guard bands and shows

quenching occurring because the transient at Out3 is shorter than the transient at the Out2. These simulation results directly support the prediction that guard bands would reduce pulse quenching because they reduce charge sharing. Thus, guard bands can be used as an experimental split technique to isolate the quenching effect.

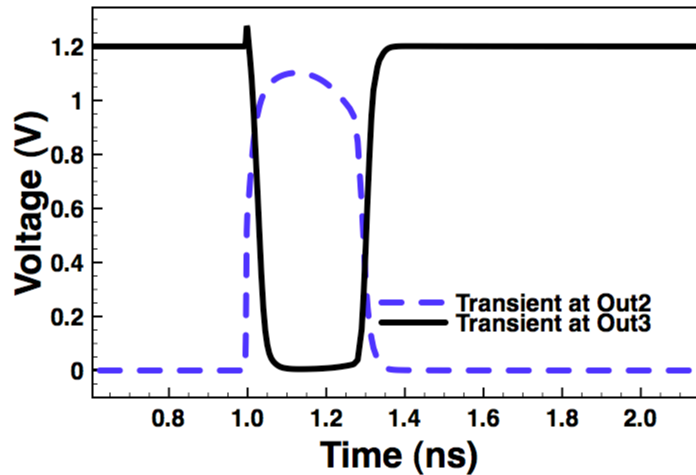

Fig. V-6. Plot showing SET generated from two pMOS transistors with guard bands where quenching does not occur.

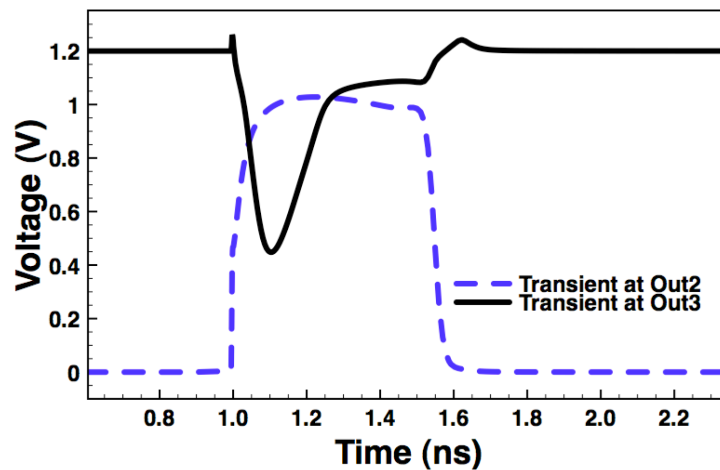

Fig. V-7. Plot showing SET generated from two pMOS transistors without guard bands where quenching does occur.

Simulation Experiment Correlating Pulse Quenching and Charge Sharing *in a Single Inverter*

Using the same technique of charge sharing via angled strikes, pulse quenching was also analyzed between an nMOS transistor and pMOS transistor with and without guard bands as part of a single inverter cell with Synopsys mixed-mode 3D TCAD. Simulations were performed for the 130 nm CMOS technology node with both the pMOS and nMOS transistors of a single inverter being modeled along with an adjacent pMOS transistor, as shown in Fig. V-8 with/without guard bands. The TCAD models were calibrated to the 130 nm IBM CMOS8RF compact models in the process design kit. For each mixed-mode TCAD simulation, the 3D TCAD model of the inverter was the 2nd inverter in a nine-inverter chain with an additional pMOS transistor from the 3rd inverter. The simulated ion strike had a fixed LET of 30 MeV-cm^2/mg, and struck the center of the drain of the nMOS transistor at a 60° angle from south-to-north direction, depicted in Fig. V-8. This allowed the incident particle to hit the nMOS transistor drain and pass under the pMOS transistor.

All simulations used the following physical models: Fermi-Dirac statistics, SRH and Auger recombination, and the Philips mobility model. The incident heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps. In each simulation, the ion strike occurred at 1 ns. Simulations were carried out using the Vanderbilt ACCRE computing cluster [ACCRE].

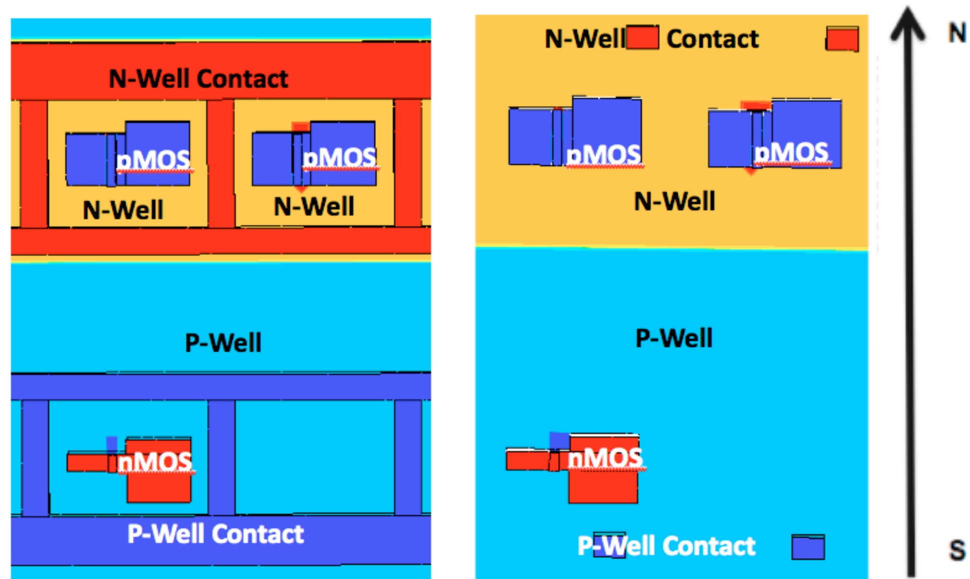

Fig. V-8. TCAD models of 130 nm inverter and adjacent pMOS transistor with and without guard bands.

Using the capabilities of 3D mixed-mode TCAD simulations by monitoring the current and voltage of each transistor within the model, Fig. V-9 shows the drain current plot of the pMOS transistors with and without guard bands. The additional spike in current for the latter condition is caused by the charge collected by the pMOS transistor drain after the strike. A similar spike in current for with-guard-bands condition is not observed because the guard bands serve as a charge sink and help to maintain the substrate/well potential. The additional charge in the without guard band case enhances the restoring current at the output node of the inverter causing the voltage of the output node to quickly return to its original state. The resulting output node voltage of the struck nMOS transistor is shown in Fig. V-10.

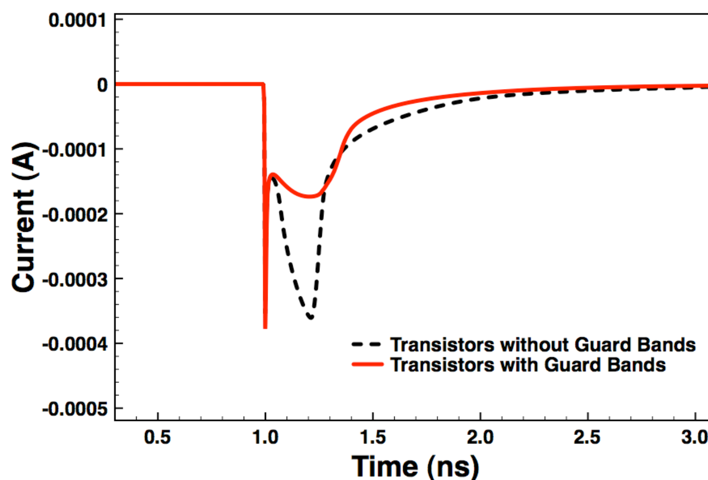

Fig. V-9. Plot showing SET drain current pulses from pMOS transistors with and without guard bands for an ion strike of 30 MeV-cm^2/mg at a 60° angle perpendicular to the n-well.

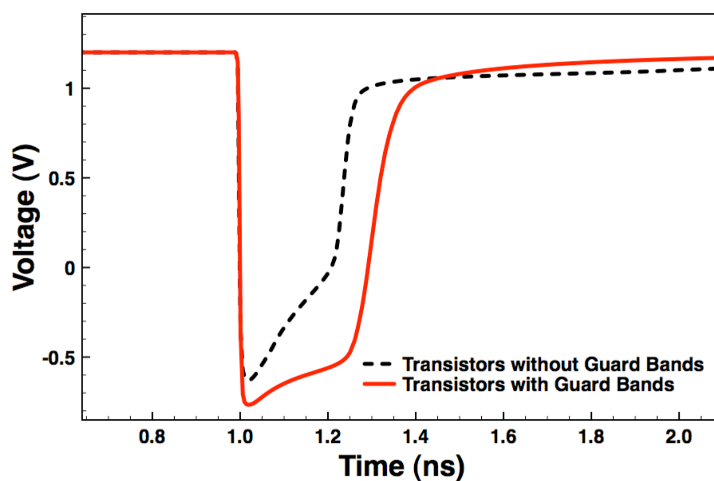

Fig. V-10. Plot showing SET pulse widths from struck nMOS transistors with and without guard bands for an ion strike of 30 MeV-cm^2/mg at a 60° angle perpendicular to the n-well.

Experimental SET Measurements Demonstrating Pulse Quenching

A 130 nm CMOS test chip containing inverters with/without guard bands was designed and fabricated using IBM 8RF CMOS technology. The test chip design was based on the autonomous pulse-width measurement technique described in [Na06] and

contained two variants of otherwise identical target inverter chains. The inverters were designed to be current matched with pMOS transistor W/L of 720 nm x 120 nm and nMOS transistor W/L of 240 nm x 120 nm. These target chains were both laid out in a serpentine arrangement of 4 rows of 25 inverters each. Other than the guard band variant, the layouts were identical, as shown in Fig. V-11 [Nar08]. The ability to simultaneously test both topologies allowed us to directly compare the effects of charge sharing on the observed SET pulse widths.

The circuits were tested at the Lawrence Berkley National Laboratory with 30 MeV-cm^2/mg Krypton and 58 MeV-cm^2/mg Xenon at a 60° angle of incidence. The test fixture was first arranged so that particle penetration was parallel to the n-well – promoting pulse quenching between inverters. Once data was collected, a second set of tests was performed with 30 MeV-cm^2/mg Krypton at a 60° angle of incidence to understand pulse quenching in a single inverter cell. The test fixture was arranged so that particle penetration was from a south-to-north direction (the direction is defined in Fig. V-11). The 60° angle of incidence was intended to promote charge sharing between the nMOS and pMOS transistors within the inverters, creating the conditions necessary for quenched pulses.

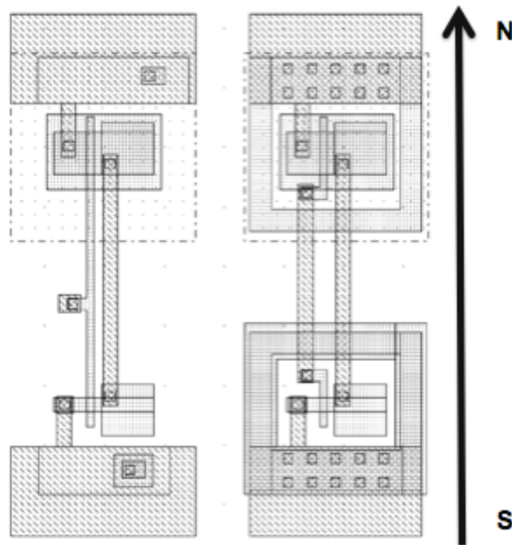

Fig. V-11. Layout of 130 nm inverter without/with guard bands (after [Nar08]).

Heavy-Ion Results Illustrating Pulse Quenching Between Inverters

Measured pulse widths of the two layout variants (guard band versus no guard band) caused by the ions striking south-to-north to the circuit are shown in Fig. V-12. The pulse widths are separated into bins where each SET measured falls within a pulse width range, such as the pulse width bin of 240 ps to 360 ps [Nara08]. An overall disparity in pulse width distributions for the two data sets can be seen. The SET pulse width distribution in blue (thin columns) represents the propagating pulses with minimal charge sharing (because of effective guard banding), this distribution is typical of conventional SET pulses in a 130 nm technology [Nara08]. However, the pulse width distribution shown in red (thick columns), which represents the propagating pulses with considerable charge sharing (due to the lack of guard bands), shows a skew to lower pulse widths as a result of pulse quenching.

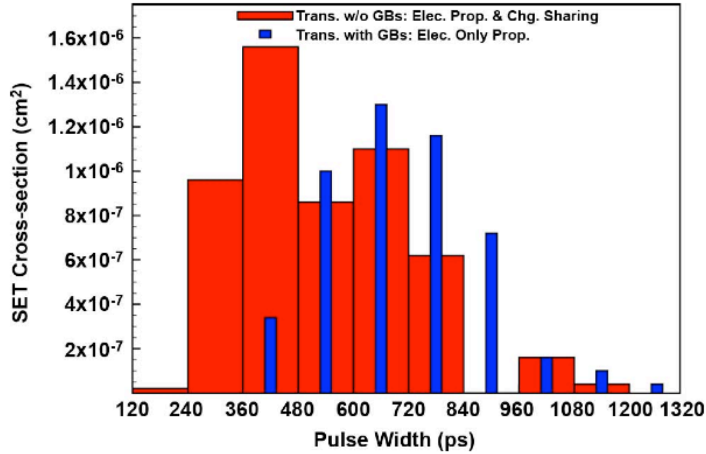

Fig. V-12. Experimental results at 60° and 30 MeV-cm^2/mg ion with 130 nm pulse width measurement circuits.

These results are counter-intuitive to conventional wisdom, as one might expect SET pulse widths without guard bands to be longer than those with guard bands because of sustained diffusion charge collection in the former case and limited charge collection in the latter case [Nar08] – the experimental data shows the opposite. A similar skew in pulse width distributions is observed for the 58 MeV-cm^2/mg Xenon irradiation, as shown in Fig. V-13.

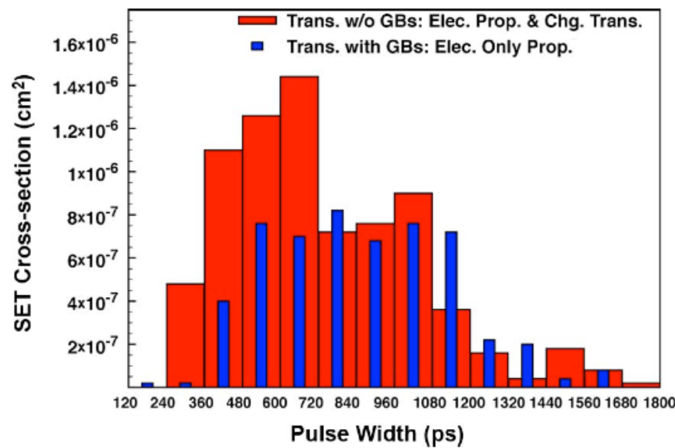

Fig. V-13. Experimental results at 60° and 58 MeV-cm^2/mg ion with 130 nm pulse width measurement circuits.

All of these results are consistent with the pulse quenching effect, as the enhanced charge sharing without guard bands (thick columns) leads to significant pulse quenching, effectively shortening the observed pulse widths. The pulse widths with reduced charge sharing (thin columns) do not exhibit strong pulse quenching and match the expected long-pulse-width distribution of larger technologies.

In Table V-1 the SET pulse width averages for the Krypton and Xenon strikes for each target variant are shown. For each ion, it can be seen that the average SET pulse width for devices without guard bands is smaller than the average SET pulse for devices with guard bands.

Table V-1 – Average SET pulse widths at 60° strike along the well

Ion	**Krypton – 30 MeV-cm^2/mg**	**Xenon – 58 MeV-cm^2/mg**
Avg. SET Pulse Width Guard Bands	**649 ps**	**796 ps**
Avg. SET Pulse Width w/o Guard Bands	**478 ps**	**673 ps**

Heavy-Ion Results Illustrating Pulse Quenching in a Single Inverter

A comparison of SET pulse widths for the transistors with guard bands and without guard bands struck by ions south-to-north to the inverter cell is shown in Fig. V-14. The pulse widths are separated into bins where each SET measured falls within a pulse width range, such as the pulse width bin of 240 ps to 360 ps [Nara08]. For the inverters with guard bands, the pulse width distribution has a median of 620 ps while the pulse width distribution for the inverters without guard bands has a smaller median of

500 ps. The difference between the medians is consistent with the pulse quenching effect and agrees with the 3D TCAD simulations. In both the simulations and experimental data, the transistors without guard bands had shorter SET pulse widths than the transistors with guard bands. Therefore, the experimental data supports the simulations showing that pulse quenching can occur between the nMOS transistor and pMOS transistor in a single inverter cell when an ion strikes an inverter cell in a south-to-north direction.

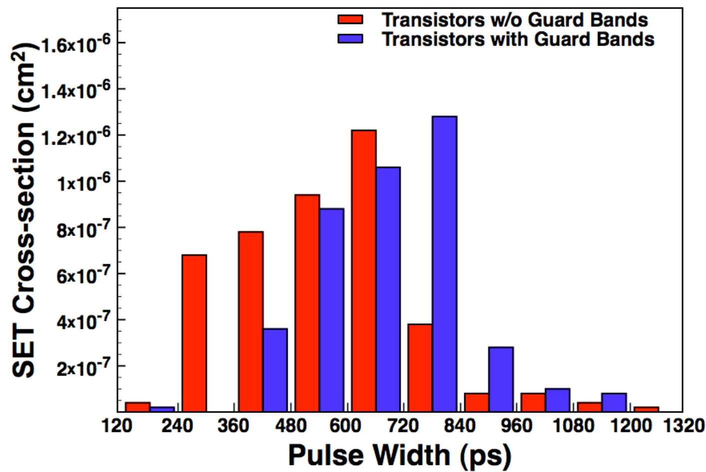

Fig. V-14. Experimental results at 60° and 30 MeV-cm^2/mg Krypton ion with 130 nm pulse width measurement circuits.

Characterization of Pulse Quenching in Sub-100 nm Bulk CMOS

Unlike the 130 nm test circuits described previously, most circuits have transistors spaced closer together. Circuits designed at 130 nm or smaller, may not only be susceptible to pulse quenching for 60° and higher angled heavy-ion strikes, but also maybe susceptible to pulse quenching for normal incidence strikes.

Simulation of Pulse Quenching at 90 nm

To understand and verify the presence of the pulse quenching mechanism at the 90 nm technology node, simulations were carried out using Synopsys 3D mixed-mode tools. Each TCAD model contained two pMOS transistors (Fig. V-15) and these transistors were calibrated to match dc and ac electrical characteristics (e.g., I_d-V_d and I_d-V_g curves) based on the IBM CMOS9SF PDK. Two pMOS transistors were chosen for TCAD modeling because previous work has shown the prevalence of charge sharing among pMOS transistors in this particular technology [Am06]. However, simulations of nMOS and pMOS transistor pulse quenching were not done because pulse quenching between them was shown to be minimal at this technology node [Ahl10]. The remainder of the simulation setup included calibrated compact models for a chain of inverters matching that of the 90 nm experimental test chip.

All simulations were carried out with a 9-stage, minimum-sized, matched current-drive inverter chain with the 3D TCAD section representing the pMOS transistors in the 2nd and 3rd stages. The pMOS transistor in the 2nd stage (Out2 from Fig. V-1) represented the hit pMOS transistor while the pMOS transistor in the 3rd stage (Out3 from Fig. V-1) represented the adjacent pMOS transistor. All simulations used the following physical models: Fermi-Dirac statistics, SRH and Auger recombination, and the Philips mobility model. The incident heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps. In each simulation, the ion strike occurred at 1 ns. Simulations were carried out using the Vanderbilt ACCRE computing cluster [ACCRE].

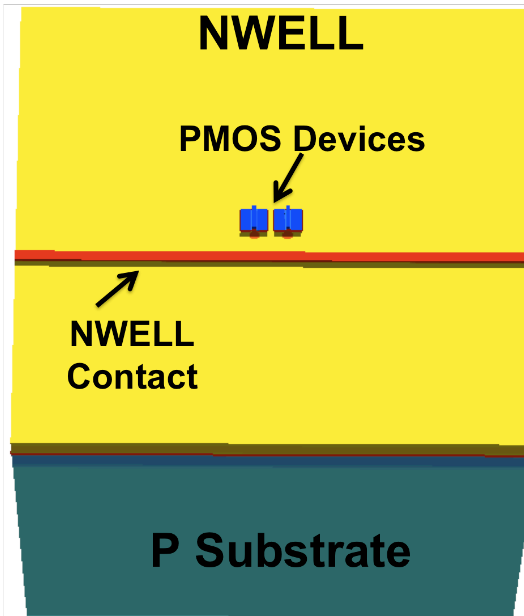

Fig. V-15. 3D TCAD Model of two 90 nm pMOS transistors.

The TCAD simulations of the 90 nm inverter chain show a detailed view of the quenching effect. Fig. V-16 illustrates the initial transient formed by a 40 MeV-cm^2/mg normal incidence ion strike on the hit pMOS transistor along with the transient as it propagates through the subsequent inverter. The initial transient at Out2 shows a measured pulse width of about 750 ps. However, the transient at Out3 (solid line) shows only a pulse width of about 75 ps. This decrease is a result of transient pulse quenching.

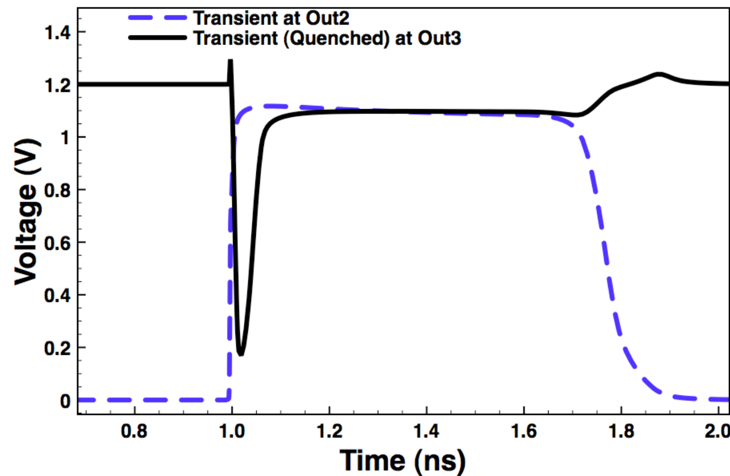

Fig. V-16. Plot showing propagation of initial SET after Out2 and then after Out3.

To insure that the quenched SET was actually caused by delayed charge sharing at Out3, another simulation was performed. This simulation focused on directly observing the time profile of the delayed charge sharing collection at the adjacent pMOS transistor. The same transistors and hit location were used, but in the opposite logic state (hit pMOS transistor ON and adjacent pMOS transistor OFF). For this set up, the charge collected by the hit pMOS transistor (ON) did not result in an SET pulse at Out2 – the resulting SET pulse at Out3 was due to charge sharing only.

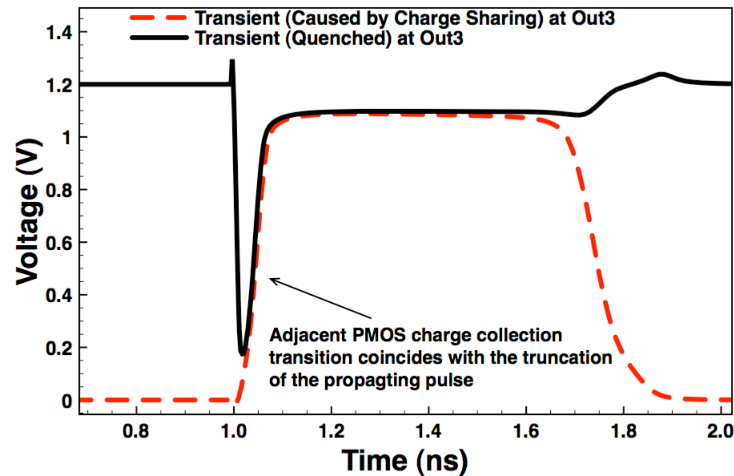

Fig. V-17. Plot showing quenching of transient is the result of the injection of another transient due to charge sharing.

Fig. V-17 shows the results of the second simulation (dotted curve). The figure also plots the quenched pulse from the first simulation. The dotted curve shows the voltage transient induced at the adjacent transistor due to charge sharing. Note that the adjacent charge collection transition coincides with the truncation of the propagating pulse. These SET curves confirm that delayed charge sharing collection at Out3 is the mechanism that quenches the propagating SET.

Simulation of Pulse Quenching at 65 nm

The mixed-mode TCAD simulations at 90 nm illustrated how pulse quenching can occur for normal incidence heavy-ion strikes. To better understand normal incidence induced pulse quenching and to investigate the effects layout has on pulse quenching, 3D TCAD simulations were carried out for two different 65 nm bulk CMOS inverter layouts. These inverters were designed to be current matched with pMOS transistor W/L of 400 nm x 50 nm and nMOS transistor W/L of 200 nm x 50 nm.

The differences between the two inverter chains were the size of the n-well and the spacing. The first inverter design had the inverters in a common n-well and spaced 0.75 μm from gate center to gate center, as shown in Fig.V-18. Additionally, the entire n-well was contacted with a strip contact leading to a total n-well-contact-area-to-well-area percentage of 19%.

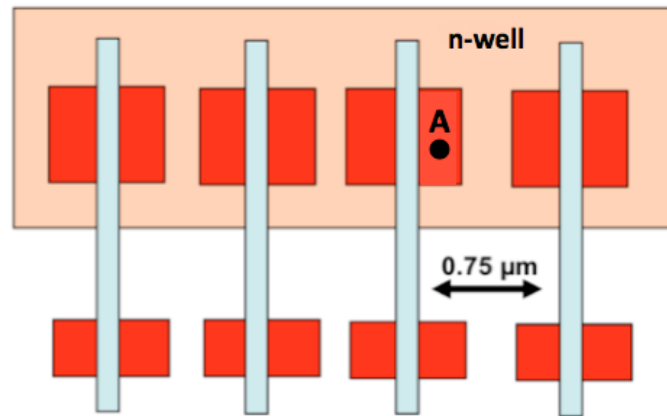

Fig. V-18. Layout of the 65 nm target inverter chain where each row of inverters shares a common n-well (common n-well).

In the second inverter layout, each pMOS transistor was placed in its own separate n-well and spaced 1.3 μm from gate center to gate center, as shown in Fig. V-19. With a p-well between each pMOS transistor and increased spacing, a reduction in pulse quenching and an increase in SET pulse width are expected compared to the common n-well inverter layout. The p-well acts as a doped barrier to charge diffusion, and the increased spacing would reduce the amount of charge that could reach adjacent transistors because more charge could recombine. Each inverter was also designed with its own n-well contact so the total n-well-contact-area-to-well-area percentage was similar to the common n-well design n-well-contact-area-to-well-area percentage. The n-

well contact for each inverter created a total n-well-contact-area-to-well-area percentage of 14%.

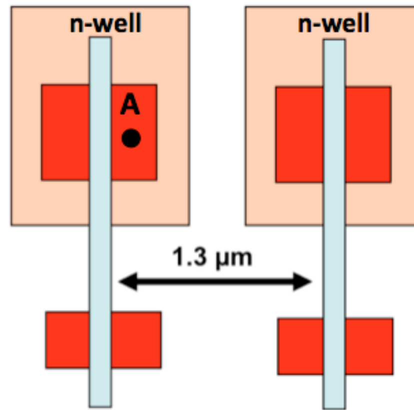

Fig. V-19. Layout of the 65 nm target inverter chain where each inverter has its own separate n-well (separate n-well).

Using Synopsys 3D mixed-mode tools, the two different inverter designs were analyzed for their pulse quenching characteristics. Two different TCAD models were made, with each TCAD model containing five 65 nm pMOS transistors. These transistors were calibrated to match dc and ac electrical characteristics (e.g., I_d-V_d and I_d-V_g curves) based on the IBM CMOS10SF PDK. The models were sized and spaced the same as the 65 nm target structures as seen in Figs. V-20 and V-21. The remainder of the simulation setup included calibrated compact models for a chain of inverters also matching the sizing of the target inverters for the SPICE-based portion of the simulation.

The TCAD models are pictured in Figs. V-20 and V-21. Notice the n-diffusion p-body diodes. The actual nMOS transistors are not modeled in TCAD, and are modeled as compact models because of computing limitations. These diodes represent the drains of the nMOS transistors, matching the active area size and placement to the actual nMOS

transistors. The diodes are electrically biased as if they are nMOS transistors, but they are not electrically connected to the pMOS transistors. They increase the accuracy of the simulation by serving as charge sinks mimicking the actual nMOS transistors in the design. Finally, all simulations were carried out with a 9-stage inverter chain with the 3D TCAD model representing the pMOS transistors in the 2nd through 6th stages.

All the simulations used the following physical models: Fermi-Dirac statistics, SRH and Auger recombination, and the Philips mobility model. The incident heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm, and a Gaussian temporal profile with a characteristic decay time of 2 ps. In each simulation, the ion strike occurred at 1 ns. Simulations were carried out using the Vanderbilt ACCRE computing cluster [ACCRE].

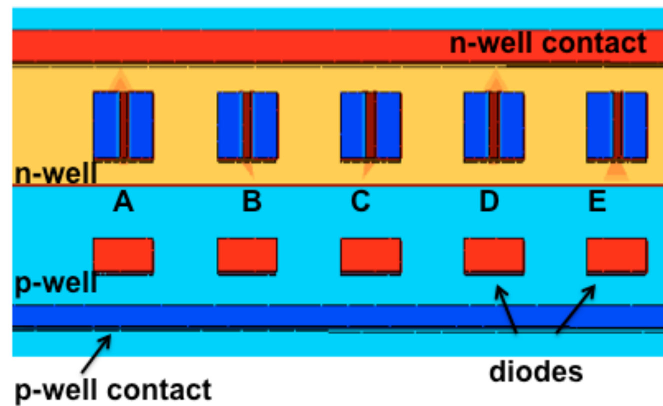

Fig. V-20. TCAD model of 65 nm common n-well inverters with pMOS transistors modeled in TCAD and nMOS transistors as compact models.

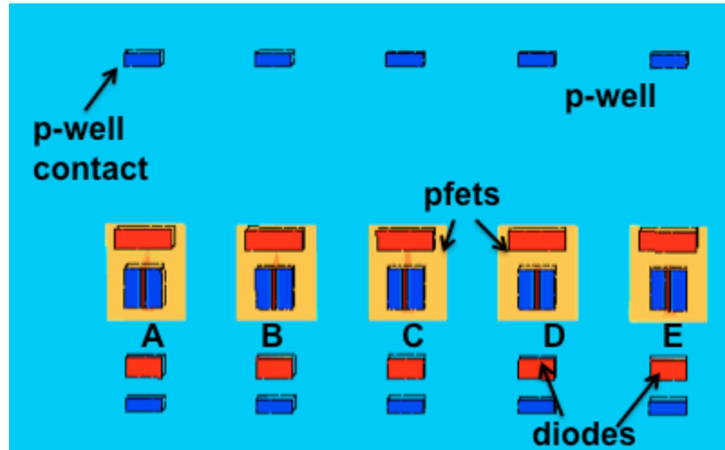

Fig. V-21. TCAD model of 65 nm separate n-well inverters with pMOS transistors modeled in TCAD and nMOS transistors as compact models.

The TCAD simulations of the 65 nm common n-well inverter chain show a detailed view of the quenching effect while simulations of the separate n-well inverter chain do not show pulse quenching. Fig. V-22 illustrates the initial 250 ps transient formed by a 58 MeV-cm^2/mg normal incidence ion strike on the center of the drain for the pMOS transistor at node B along with the transient as it propagates unquenched through the subsequent inverter (node C). However, an ion strike 100 nm away from the center of the drain at node B and closer to the adjacent pMOS transistor causes pulse quenching to occur. The initial transient at node B, Fig. V-23, shows a measured pulse width of about 200 ps. When the transient propagates through node C, the transient is completely quenched.

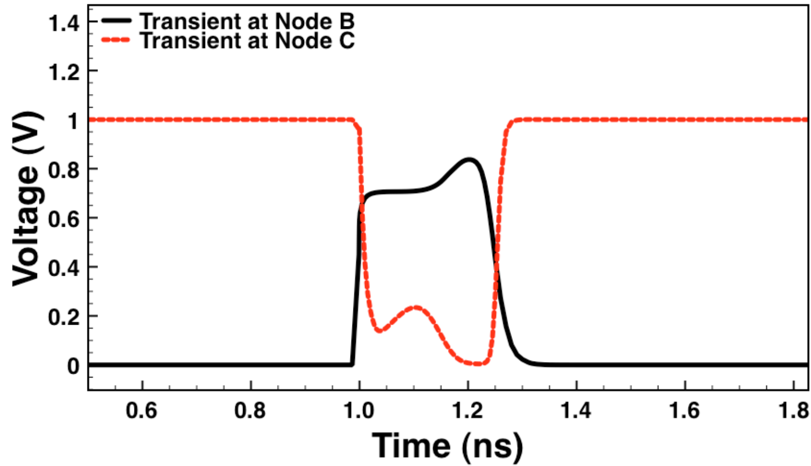

Fig. V-22. Plot showing propagation of initial SET after Node B and then after Node C. The SET is from a normal incidence LET of 58 MeV-cm^2/mg ion strike on the drain-center of the pMOS transistor at Node B in the common n-well circuit.

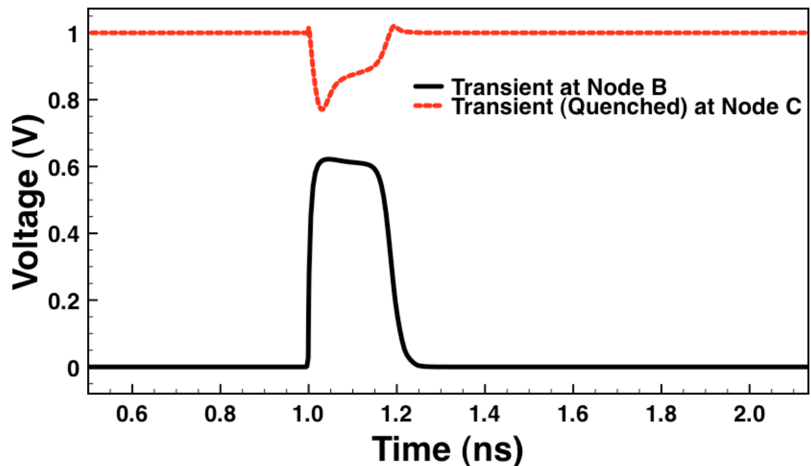

Fig. V-23. Plot showing propagation of initial SET after Node B and then after Node C. The SET is from a normal incidence LET of 58 MeV-cm^2/mg ion strike 100 nm away from the drain-center of the pMOS transistor at Node B in the common n-well circuit.

To insure that the quenched SET was caused by delayed charge sharing at node C, another simulation was performed, shown in Fig. V-24. The same transistors and hit location were used, but the pMOS transistor at node C was replaced with a compact model. The compact model stopped charge sharing from occurring because the transistor

was no longer represented in TCAD – only in SPICE. As expected, at node C, no quenching occurred and the SET propagated through the entire chain with a 250 ps pulse width. Therefore, the simulation proved that quenching occurred at node C.

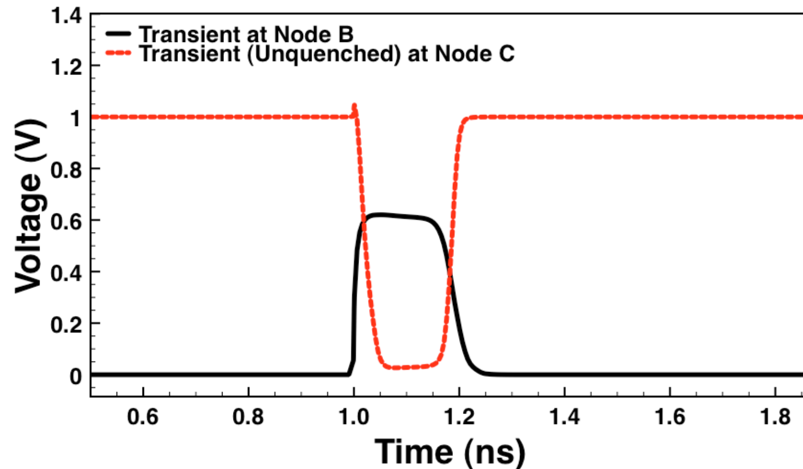

Fig. V-24. Plot showing that by replacing the pMOS transistor at node C with a compact model, the SET is no longer quenched.

As a contrast to the common n-well results, the separate n-well simulations do not show pulse quenching occurring. Figs. V-25 and V-26 are strikes on the center of the drain of the pMOS transistor at node B and 100 nm away from the center of the drain. In both cases, no pulse quenching is observed. An SET with a pulse width of 270 ps is observed for the center drain strike, and an SET with a pulse width of 250 ps is observed for the 100 from the drain-center strike. Therefore, the simulations do show that the separate n-well design does reduce pulse quenching compared to the common n-well design.

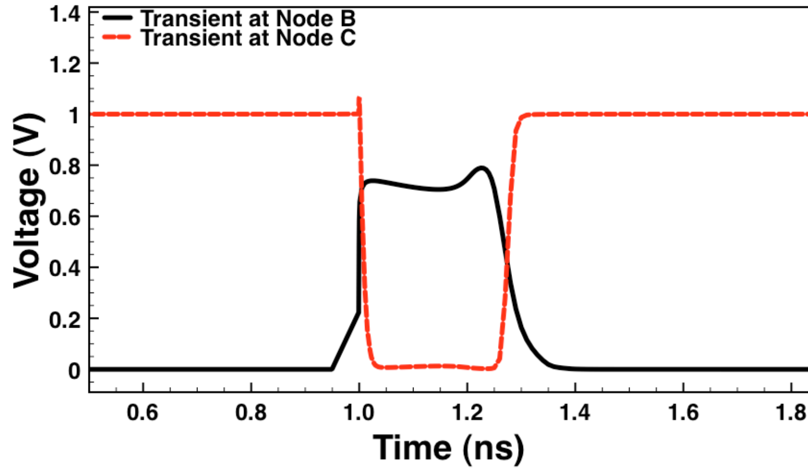

Fig.V-25. Plot showing propagation of initial SET after Node B and then after Node C. The SET is from a normal incidence LET of 58 MeV-cm^2/mg ion strike on the drain-center of the pMOS transistor at Node B in the separate n-well circuit.

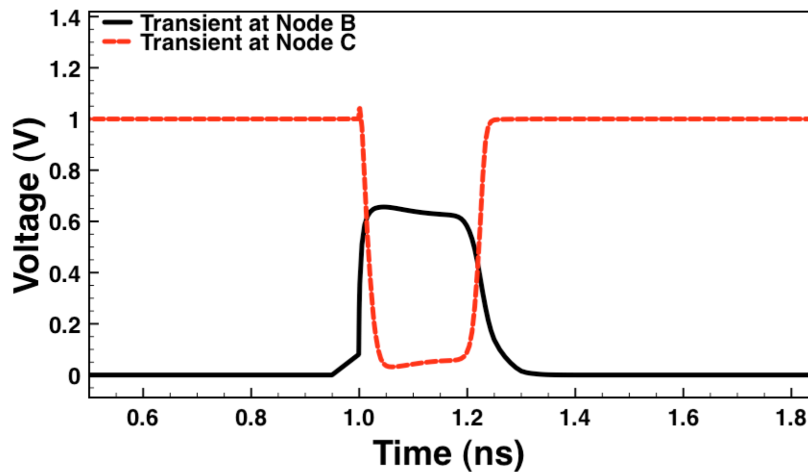

Fig. V-26. Plot showing propagation of initial SET after Node B and then after Node C. The SET is from a normal incidence LET of 58 MeV-cm^2/mg ion strike 100 nm away from the drain-center of the pMOS transistor at Node B in the separate n-well circuit.

Experimental Verification of 65 nm Layout Effects on Pulse Quenching

The 3D TCAD simulations prove that there is a difference in pulse quenching between the common n-well layout and the separate n-well layout. Upon experimental testing of these two designs in a radiation environment, the pulse quenching difference

between the two designs should manifest itself. Results should show a reduced number of SETs and a lower average SET pulse width for the common n-well design compared to the separate n-well design.

To confirm this hypothesis, the two different inverter layouts were fabricated in the IBM CMOS10SF bulk process. The inverters were designed to be current matched with pMOS transistor W/L of 400 nm x 50 nm and nMOS transistor W/L of 200 nm x 50 nm. One design consisted of inverters in a common n-well spaced 0.75 μm from gate center to gate center with a strip contact leading to a total n-well-contact-area-to-well-area percentage of 19% (Fig. V-18). The second design consisted of inverters with each pMOS transistor placed in its own separate n-well and spaced 1.3 μm from gate center to gate center (Fig. V-19). Each inverter had its own n-well contact, which created a total n-well-contact-area-to-well-area percentage of 14%.

The two different layout circuits were part of two different target circuits followed by a SET measurement circuit based on the autonomous pulse-width measurement technique described in [Na05]. This implementation of the SET measurement circuit was able to measure transient pulses ranging from 25 ps to 2 ns with a 25 ps measurement resolution. In both target designs, a chain of 1000 inverters was used and designed in 10 rows of 100 inverters, each connected in a serpentine manner.

65 nm Heavy-ion Broadbeam Results

Heavy-ion broadbeam testing was performed at Lawrence Berkley National Laboratory with the 10 MeV/nucleon ion cocktail for Ne, Ar, Cu, Kr, and Xe ions at

normal incidence and at a 60° angle of incidence. For angled strikes, the test fixture was arranged so that particle penetration was longitudinal along the well.

Over a range of ions, both the number and pulse-width of SETs were measured. An SET cross-section was calculated using total SET count for each inverter design. The SET cross-section plot in Fig. V-27 shows these results and has been normalized by the layout cell area for each design [Ah10].

Analysis of Fig. V-27 shows that at LET values below 21 MeV-cm^2/mg, the well layout scheme has a minimal effect on the cross-sections. Whereas at LET values above 21 MeV-cm^2/mg, the separate n-well layout has a higher cross section than the common n-well layout. This difference in cross sections between the separate n-well layout and common n-well layout is counter-intuitive because the common n-well design has 20% more total n-well area than the separate n-well design. In a bulk CMOS technology, pMOS transistor charge collection within the n-well typically dominates the cross-section [Ol05] [Bl05], so a larger n-well area typically results in a larger cross-section.

Pulse quenching can explain this difference. Previous work has shown that pulse quenching is driven by charge sharing [Ah09] -- a mechanism particularly efficient within common n-well regions. Simulations also show that the isolation of the n-wells mitigates or reduces pulse quenching, while a common n-well enhances quenching. In the case of the 65 nm common n-well simulations, the quenching effectively eliminates many of the SET pulses. Therefore, the data suggests some SET pulses are eliminated in the common n-well design due to pulse quenching.

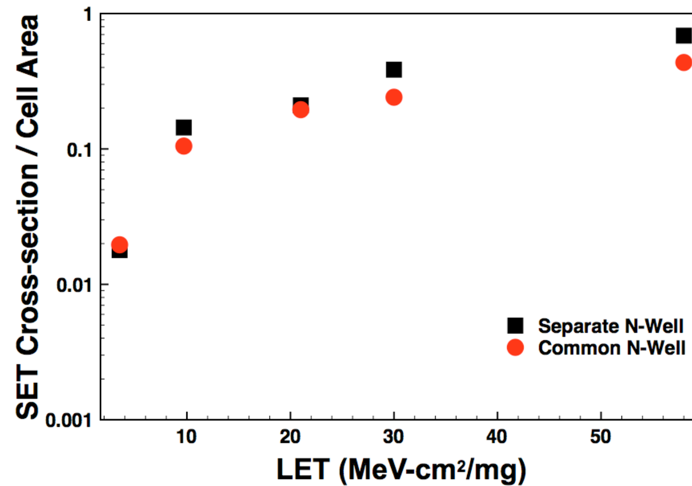

Fig. V-27. Plot of SET cross-section versus LET with the measurements normalized to the cell area.

Further confirmation of pulse quenching is seen in the 58 MeV-cm^2/mg experimental data in Fig. V-28. There is a clear shift in the pulse width distribution mean toward shorter pulses for the common n-well design. Enhanced pulse quenching in the common n-well design leads to both shorter SET pulses and fewer total numbers of SET pulses. This difference in SET pulse width distribution and the number of SETs between the common n-well and separate n-well designs is consistent for all ions and angles measured as seen in Figs. V-28 to V-32.

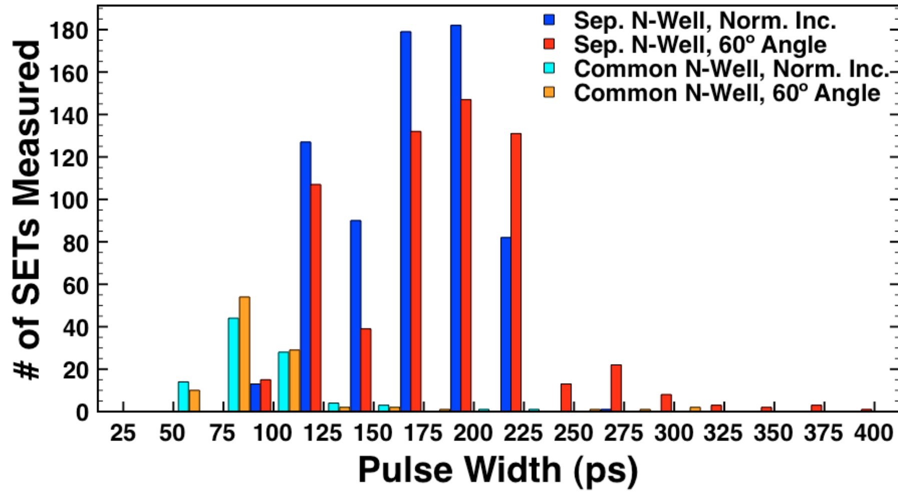

Fig. V-28. Experimental results of the 65 nm pulse width measurement circuit for the common n-well and separate n-well inverter designs for a 58 MeV-cm^2/mg ion.

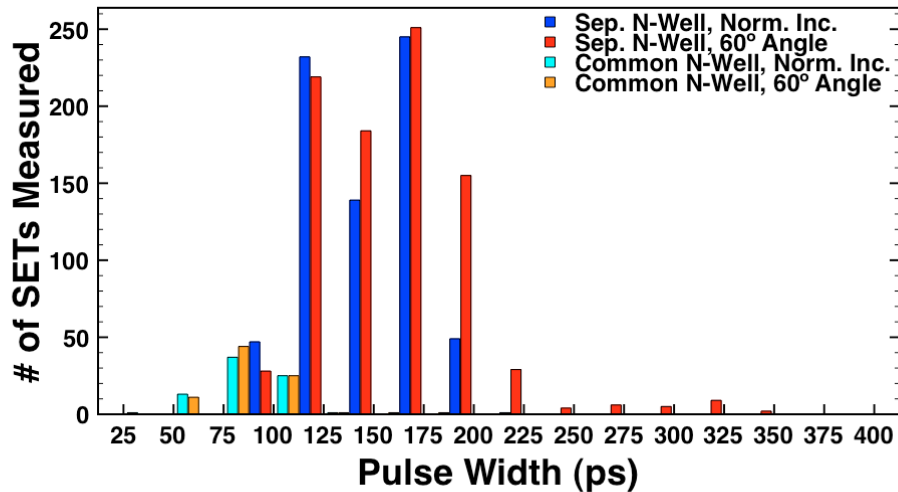

Fig. V-29. Experimental results of the 65 nm pulse width measurement circuit for the common n-well and separate n-well inverter designs for a 30 MeV-cm^2/mg ion.

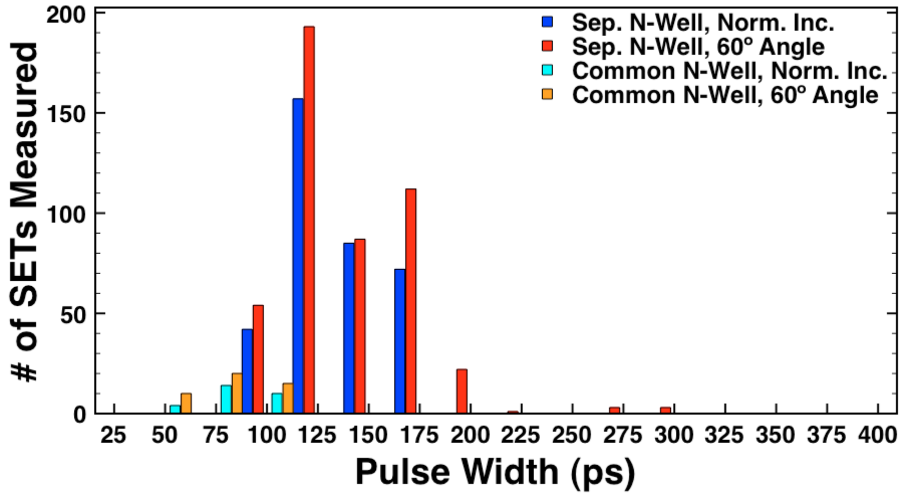

Fig. V-30. Experimental results of the 65 nm pulse width measurement circuit for the common n-well and separate n-well inverter designs for a 21 MeV-cm^2/mg ion.

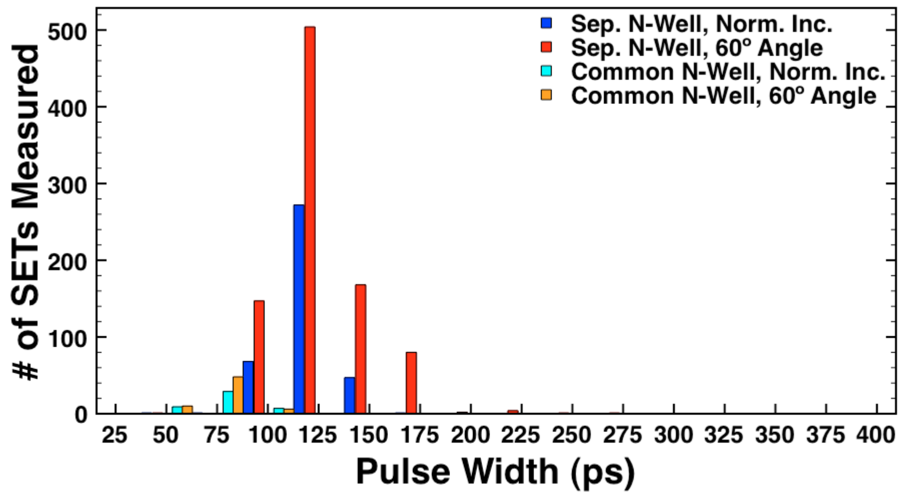

Fig. V-31. Experimental results of the 65 nm pulse width measurement circuit for the common n-well and separate n-well inverter designs for a 9.7 MeV-cm^2/mg ion.

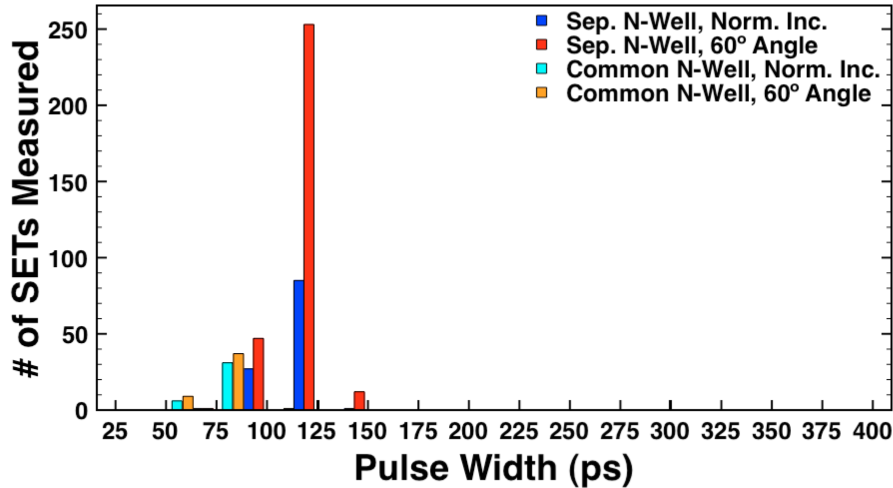

Fig. V-32. Experimental results of the 65 nm pulse width measurement circuit for the common n-well and separate n-well inverter designs for a 3.5 MeV-cm^2/mg ion.

In Table V-2 the SET pulse width averages for all normal incidence ion strikes for each target variant are stated. For each ion, the average SET pulse width for the common n-well design is smaller than the average SET pulse for the separate n-well design. Therefore, the data supports that pulse quenching occurs more frequently in the common n-well than the separate n-well design.

Table V-2 – Average SET pulse widths at normal incidence

Ion	Xenon – 58 MeV-cm^2/mg	Krypton – 30 MeV-cm^2/mg	Copper – 21MeV-cm^2/mg	Argon – 9.7 MeV-cm^2/mg	Neon – 3.5 MeV-cm^2/mg
Avg. SET Pulse Width for Common N-Well	86 ps	79 ps	80 ps	74 ps	71 ps
Avg. SET Pulse Width for Separate N-Well	149 ps	126 ps	113 ps	98 ps	94 ps

B. Two-Photon Absorption Laser Testing

As a final experiment to show that pulse quenching is more prevalent in the common n-well design compared to the separate n-well design, TPA laser testing was performed on the fabricated 65 nm test chips at the Naval Research Lab (NRL). Where as heavy-ion testing exposed the whole test chip to heavy-ion strikes, TPA testing allowed specific areas of the target circuit to be struck. The data gathered from the laser testing supported the previous pulse quenching conclusions and will be discussed in this section.

Using the 100X objective, a focused laser spot size of 1.4 μm was achieved. The laser was rastered over a 5 μm x 10 μm area for both the common n-well target circuit and the separate n-well target circuit. For each target circuit, a threshold laser energy was established by finding the laser energy where SETs began to be detected by the measurement circuit. The circuit was then rastered at its threshold energy and then the raster was repeated two more times at increasing laser energies. The rastering of the circuits created a map where each colored pixel represented a place where an SET was observed. The color of the pixel represented the SET pulse width observed at that location. Last, the layout file showing a subset of the target inverter chain was superimposed on the map.

Figs. V-33, V-34, and V-35 are the XY maps of the common n-well circuit for the laser energies of 251 pJ, 638 pJ, and 1025 pJ respectively. The first map, Fig. V-33, is taken at the threshold energy of the circuit, and the map shows a sensitive pMOS transistor located at (2.5 μm, 0.5 μm). At the next laser energy, Fig. V-34, the pMOS transistor now is producing longer SET pulse widths and shows a larger sensitive area

than the rastering done at threshold. Also an additional pMOS transistor located at (0.75 µm, 4.00 µm) becomes sensitive and produces SETs. When the circuit is rastered at 1025 pJ, Fig. V-35, very few SETs are measured for pMOS transistor at (2.5 µm, 0.5 µm). However more events and longer SET pulse widths occur for pMOS transistor at (0.75 µm, 4.00 µm) than when the circuit is rastered at 638 pJ.

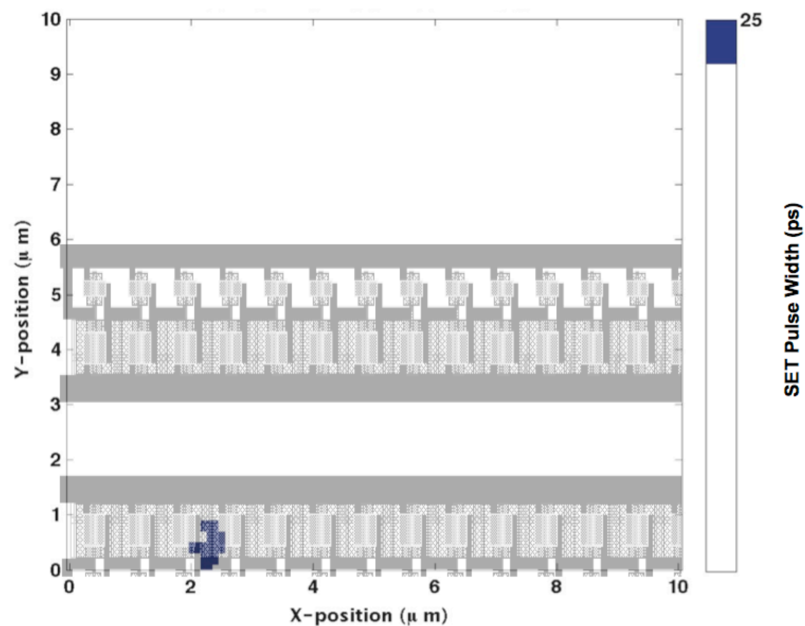

Fig. V-33. An XY map of the common n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 251 pJ laser energy.

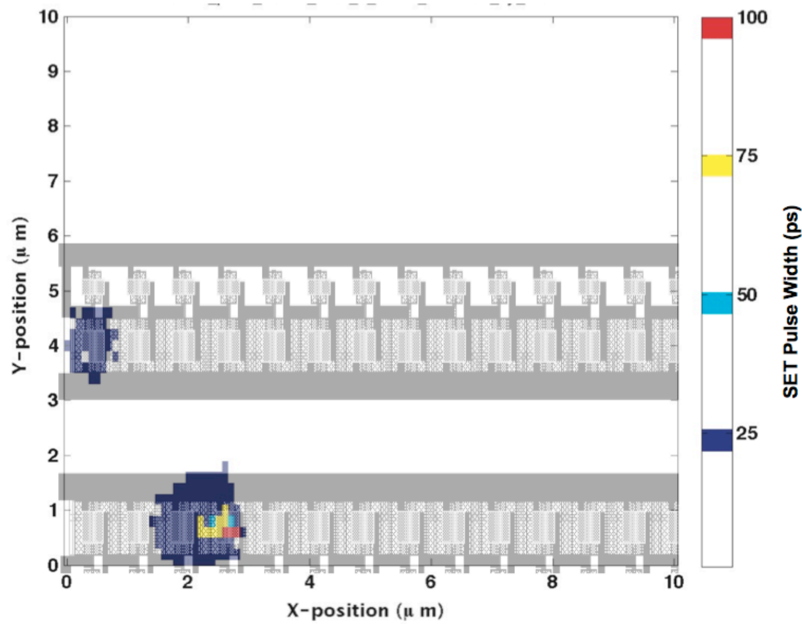

Fig. V-34. An XY map of the common n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 638 pJ laser energy.

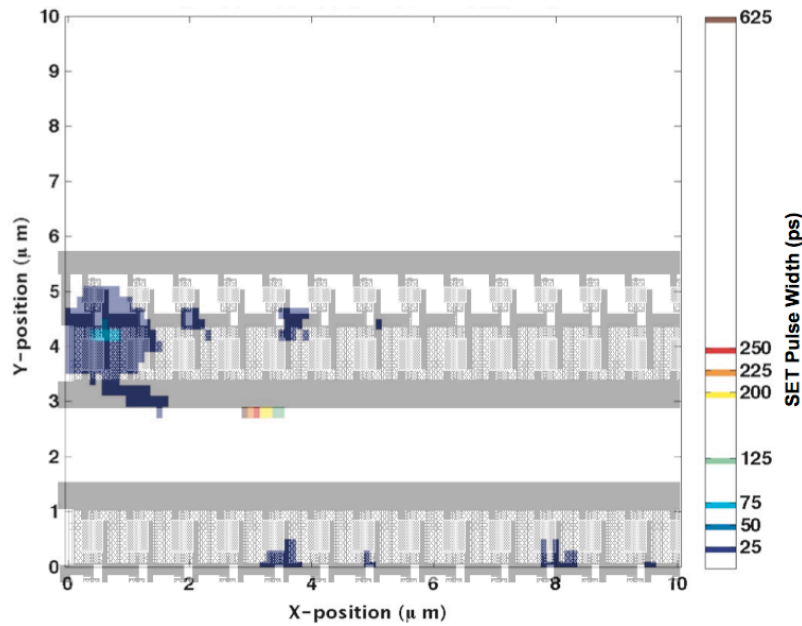

Fig. V-35. An XY map of the common n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 1025 pJ laser energy.

Figs. V-36, V-37, and V-38 are the XY maps of the separate n-well circuit for the laser energies of 386 pJ, 773 pJ, and 1160 pJ respectively. The first map, Fig. V-37, is

taken at the threshold energy of the circuit, and the map shows a sensitive pMOS transistor located at (4.0 µm, 0.5 µm). At the next laser energy, Fig. V-37, that pMOS transistor is now producing longer SET pulse widths and shows a larger sensitive area than the rastering done at threshold. Also additional pMOS transistors and nMOS transistors become sensitive and produce SETs. When the circuit is rastered at 1160 pJ, Fig. V-38, more and longer SETs are measured than at the previous laser energy.

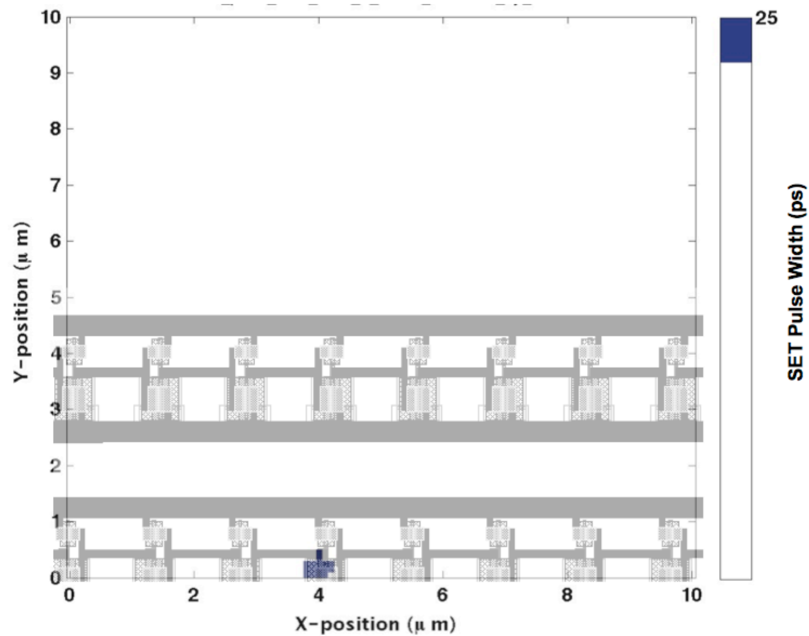

Fig. V-36. An XY map of the separate n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 386 pJ laser energy.

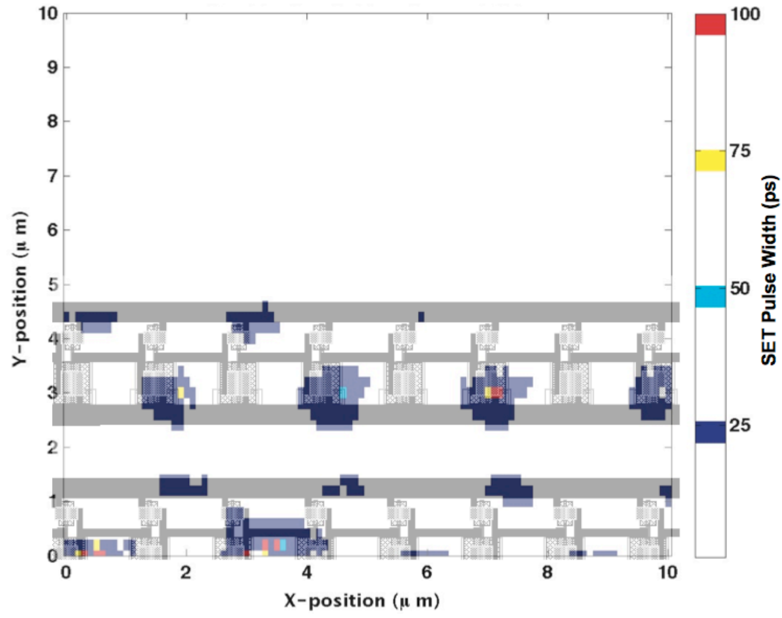

Fig. V-37. An XY map of the separate n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 773 pJ laser energy.

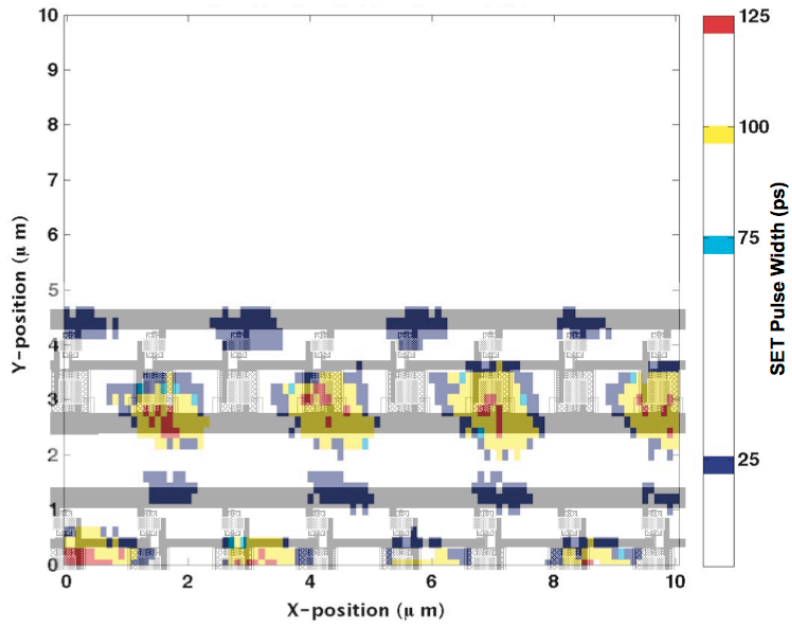

Fig. V-38. An XY map of the separate n-well 65 nm inverter target chain for a 10 µm x 5 µm area at 1160 pJ laser energy.

The maps of the two circuits at different laser energies give a visual representation of the SETs generated but are difficult to compare to each other. To quantitatively compare the maps to each other, the total number of events for each laser energy is displayed in Fig. V-39. The figure shows that as laser energy increases for the separate n-well circuit, the number of events increases linearly. Where as in the common n-well circuit, the number of events does not increase with the same slope as the separate n-well circuit over the three laser energies. The common n-well circuit has a fewer number of events than the separate n-well circuit as the laser energy increases. The reason for this difference is because pulse quenching is more prevalent in the common n-well circuit than in the separate n-well circuit.

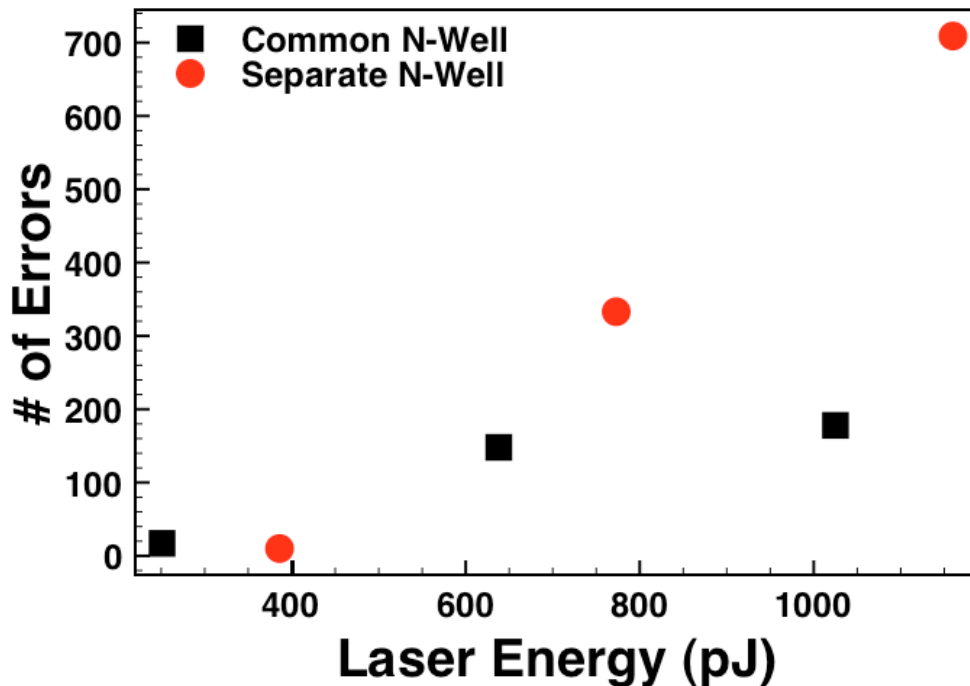

Fig. V-39. Plot showing the number of errors observed for each target chain at different laser energies. A 5 µm x 10 µm area was rastered for each target chain.

Conclusion

Using a combination of 3D mixed-mode simulations and single-event experiments, we have shown that charge sharing can shorten or quench the pulse width of an SET. Multiple sets of experimental heavy-ion and laser data prove that pulse quenching is a significant factor in affecting SET pulse width. As SET pulse width is a major factor in determining the single-event vulnerability of a given circuit and the resulting error rate, the new single-event mechanism of pulse quenching can significantly impact the vulnerability of a circuit. Therefore, pulse quenching should be assessed in the application of radiation-hardened-by-design (RHBD) techniques such as guard-banding, and in the analysis of SET pulse width test results.

CHAPTER VI

DOUBLE-PULSE-SINGLE-EVENT TRANSIENTS

Introduction

Simulations show that charge sharing can lead to multiple logic gates being upset and resulting in multiple single-event transients or double-pulse-single-event transients (DPSETs) [Ro05][Ru07]. Recent experimental work at the 65 nm technology node establishes the existence of DPSETs in digital logic [Ah11][Ha11].

In this chapter, the first experimental data from a 65 nm bulk CMOS process is discussed and analyzed showing the existence of DPSETs. DPSETs are observed in the separate n-well inverter design but not in the common n-well design. The existence of DPSETs means that soft-error rates need to be calculated differently because nominally only one error is associated with an incident ion, whereas a DPSET will show two errors for each incident ion.

Additionally, 3D TCAD simulations are used to analyze the results and explain the presence of DPSETs at the 65 nm technology node. The simulations show that DPSETs can occur in a separate n-well inverter chain design but not in a common n-well inverter chain design. TCAD simulations indicate a complex relationship among multiple phenomena such as charge sharing [Ol05][Am05], pulse quenching [Ah09] and strike location. For DPSETs to occur in the separate n-well design, various mechanisms interact to allow multiple pMOS transistors to collect charge and change state.

SET Measurement Circuit Design

To experimentally validate the presence of DPSETs at the 65 nm technology node, the same test circuits used for the pulse quenching research, previously described in Chapter V, were heavy-ion tested. The inverters were designed to be current matched with pMOS transistor W/L of 400 nm x 50 nm and nMOS transistor W/L of 200 nm x 50 nm. One design consisted of inverters in a common n-well spaced 0.75 μm from gate center to gate center with a strip contact leading to a total n-well-contact-area-to-well-area percentage of 19% (Fig. V-18). The second design consisted of inverters with each pMOS transistor placed in its own separate n-well and spaced 1.3 μm from gate center to gate center (Fig. V-19). Each inverter had its own n-well contact, which created a total n-well-contact-area-to-well-area percentage of 14%.

The two target circuits were part of an on-chip SET measurement circuit based on the autonomous pulse-width measurement technique described in [Na06], which digitizes the SET pulse width following the arrival of an SET. The SET measurement circuit was able to measure transient pulses ranging from 75 ps to 2 ns with a 25 ps measurement resolution. Thus measureable DPSETs were restricted to those separated by at least 25 ps in time. Following the generation of a DPSET and its propagation to the measurement circuit, the first pulse of the DPSET triggered the measurement circuit to "freeze" or stop acquisition, as in the nominal case of a single SET. This circuit reaction, however, is delayed in time on the order of hundreds of picoseconds (measurement lag time), thus

allowing for a second pulse to arrive within the measurement lag-time to be captured by the on-chip measurement circuit.

DPSET Experimental Results

The circuits were tested at the Lawrence Berkley National Laboratory with ions having LETs of 3.5, 9.7, 21, 30, and 58 MeV-cm^2/mg at a 60° angle of incidence. The test fixture was arranged so that particle penetration was parallel to the power rails to promote charge collection among multiple transistors. For an LET of 58 MeV-cm^2/mg the circuit was tested to an effective fluence of 5 x 10^7 particles/cm^2. Mid-range LETs of 21 and 30 MeV-cm^2/mg were tested to an effective fluence of 1 x 10^8 particles/cm^2. Effective fluences of 2 x 10^8 and 5 x 10^8 particles/cm^2 were used for LETs of 9.7 and 3.5 MeV-cm^2/mg respectively. The effective fluence differed between ion species to improve the statistics of the error counts for the lower LET ion exposures.

Fig. VI-1 shows the number of DPSETs generated for each ion LET tested in the separate n-well circuit. DPSETs occur at LETs as low as 9.7 MeV-cm^2/mg. As ion energy increases, the number of DPSETs occurring also increases, suggesting that the amount of charge deposited in the ion strike radius is a key factor in the generation of DPSETs.

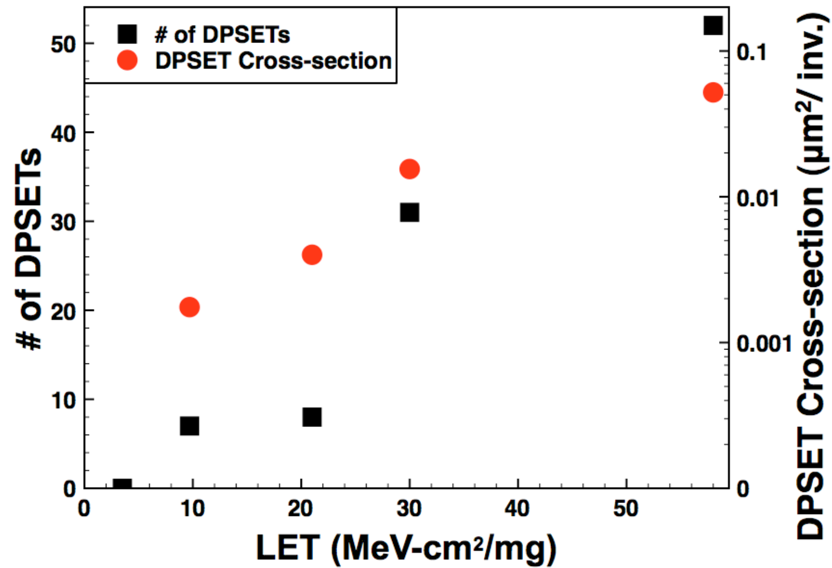

Fig. VI-1. Number of DPSETs and cross-section for separate n-well inverter target chain with all ions incident at 60° angle longitudinal to the n-well.

In addition to counting the number of DPSETs that occurred, characteristics of the DPSET pulse shape were recorded. In conventional SET measurement tests in older technologies, only a single SET was measured and a pulse width for that single SET was calculated, as shown in Fig. VI-2. However for a DPSET, two pulses were measured along with the time difference between the two of them for one ion strike.

For example, Fig. VI-3 shows a measured DPSET at an LET of 58 MeV-cm^2/mg. In this DPSET, the first pulse has a width of 150 ps and the second pulse has a pulse width of 125 ps with the two pulses occurring 75 ps apart.

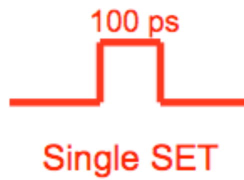

Fig. VI-2. Single pulse voltage transient.

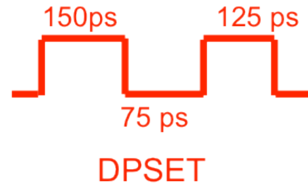

Fig. VI-3. Double pulse voltage transient

The DPSET pictured in Fig. VI-3 is one of 52 DPSETs observed at 58 MeV-cm^2/mg. Moreover, each DPSET had unique characteristics. Out of the 52 events observed at an LET of 58 MeV-cm^2/mg, only two DPSETs were identical. This trend was similarly seen in LETs below 58 MeV-cm^2/mg as well.

The DPSET's can be broken down as two distinct events, each with is own pulse width, and separated by a time constant. The pulse width data for the first and second pulses can be seen in Fig. VI-4.

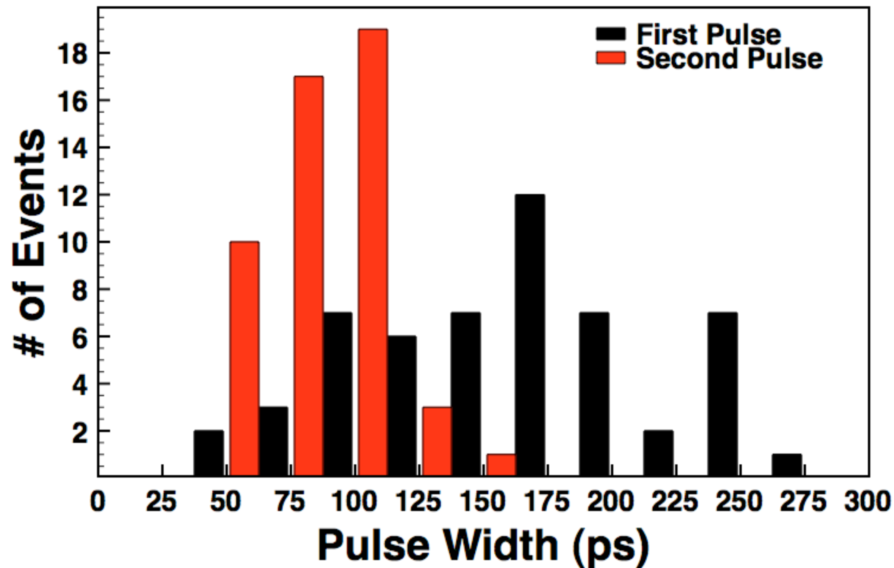

Fig. VI-4. Plot showing the different pulse widths measured for the 1st and 2nd pulses of the DPSETs that occurred during the LET of 58 MeV-cm^2/mg experimental run.

Fig. VI-4 gives insight into the generation of DPSETs by separating out the pulse widths of each event. The first pulse has a typical distribution of pulse widths similar to previously reported SET pulse width distributions for particles at normal incidence [Ga10][Ah10], which would indicate that the ion is passing through the drain region of the pMOS transistor. This first pulse has a wider distribution spanning from 25 ps to 275 ps, whereas the second pulse, has a narrower distribution of pulse widths from 50 ps to 175 ps. The second pulse would seem to be a result of substrate-related charge collection from the portion of the ion track that is passing below inverters farther down the chain because it occurs 10s to 100s of picoseconds after the initial strike. When a pulse forms 10s to 100s of picoseconds after the initial ion strike, it is indicative of being caused by diffused charge collection [Ma93].

Fig. VI-5 shows the time duration distribution between the first and second pulses for all the DPSETs observed during the LET of 58 MeV-cm^2/mg run. The interval

between double pulses appears to be uniformly distributed. The probable reason for this distribution of data is because the duration between pulses is directly related to the strike location. During heavy-ion testing, there is an equal chance an ion can strike anywhere in the sensitive area of the circuit to cause an SET. Since the double-pulse mechanism depends on diffusion of charge, and diffusion is a function of distance, the shape of the double pulse transient is a strong function of strike location.

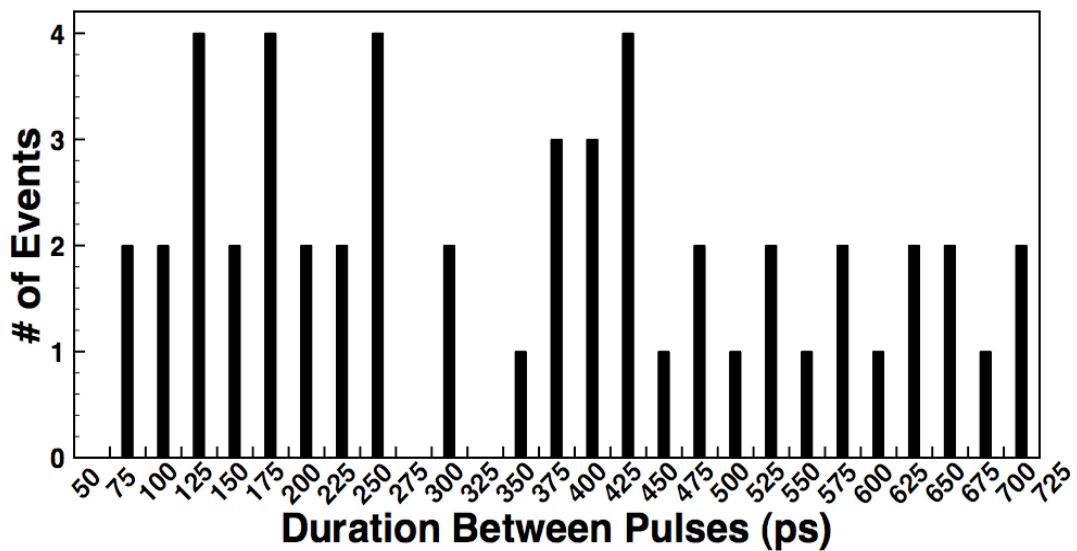

Fig. VI-5. Plot showing the time durations measured between the 1st and 2nd pulses of the DPSETs that occurred during the LET of 58 MeV-cm^2/mg experimental run.

To give further insight into the mechanisms responsible for DPSETs, an additional series of heavy-ion tests were performed on a different 65 nm chip, but with the same layout as the previously tested chip. These tests focused on varying the angle of the ion strike instead of varying only the ion energy. The chip was tested using Argon and Krypton ions with the LETs of 9.7 and 30 MeV-cm^2/mg respectively. For each ion it was struck at 30°, 45°, 60°, and 75° angles of incidence parallel to the power rails and longitudinal to the n-wells. Last, for an LET of 30 MeV-cm^2/mg the circuit was tested to

an effective fluence of 1 x 10^8 particles/cm^2 and an effective fluence of 2 x 10^8 for an LET of 9.7 MeV-cm^2/mg.

Fig. VI-6 shows the results of the heavy-ion test. The data show that as the angle of incidence increases the DPSET cross-section also increases for the separate n-well test circuit. However, no DPSETs occur for the common n-well test circuit at any angle. These results signify that the separate n-well is susceptible to DPSETS unlike the common n-well circuit. Also the results suggest that the ion is traversing across multiple sensitive junctions and inducing DPSETs because as the angle of incidence increases the probability the ion goes through multiple sensitive junctions increases [Do97].

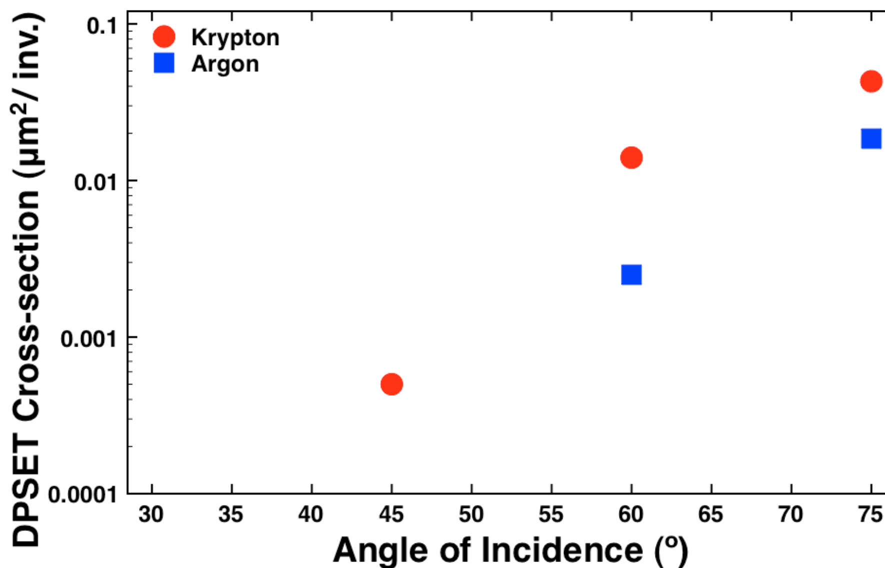

Fig. VI-6. Plot showing the DPSET cross-section of the separate n-well circuit for both the ions of Krypton and Argon. As the angle of incidence increases, the number of DPSETs that are observed also increases.

Simulation Setup

Using Synopsys 3D mixed-mode tools, the separate n-well and common n-well circuits were analyzed to understand the mechanisms behind DPSETs. Two different TCAD models were made, one for each n-well design, with each TCAD model containing five 65 nm pMOS transistors. These transistors were calibrated to match DC and AC electrical characteristics (e.g., I_d-V_d and I_d-V_g curves) based on the IBM CMOS10SF PDK. The models were sized and spaced the same as the 65 nm target structures described in Chapter V. The remainder of the simulation setup included calibrated compact models for a chain of inverters also matching the sizing of the target inverters for the SPICE-based portion of the simulation.

The TCAD models are pictured in Figs. VI-7 and VI-8. Notice the n-diffusion p-body diodes. The actual nMOS transistors are not modeled in TCAD, and are modeled as compact models because of computing limitations. These diodes represent the drains of the nMOS transistors, matching the active area size and placement to the actual nMOS transistors. The diodes are electrically biased as if they are nMOS transistors, but they are not electrically connected to the pMOS transistors. They increase the accuracy of the simulation by serving as charge sinks mimicking the actual nMOS transistors in the design. Finally, all simulations were carried out with a 9-stage inverter chain with the 3D TCAD model representing the pMOS transistors in the 2nd through 6th stages.

All the simulations used the following physical models: Fermi-Dirac statistics, SRH and Auger recombination, and the Philips mobility model. The incident heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 50 nm,

and a Gaussian temporal profile with a characteristic decay time of 2 ps. In each simulation, the ion strike occurred at 1 ns. Simulations were carried out using the Vanderbilt ACCRE computing cluster [ACCRE].

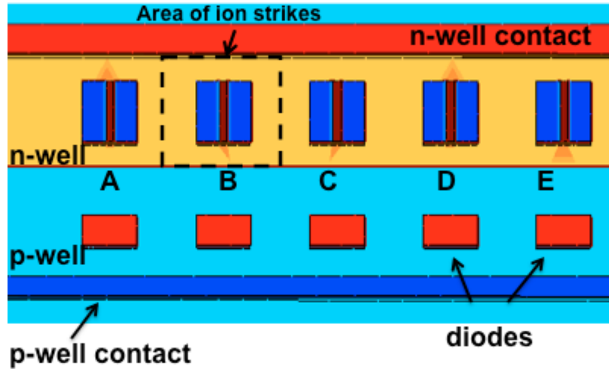

Fig. VI-7. TCAD model of 65 nm common n-well inverters with pMOS transistors modeled in TCAD and nMOS transistors as compact models.

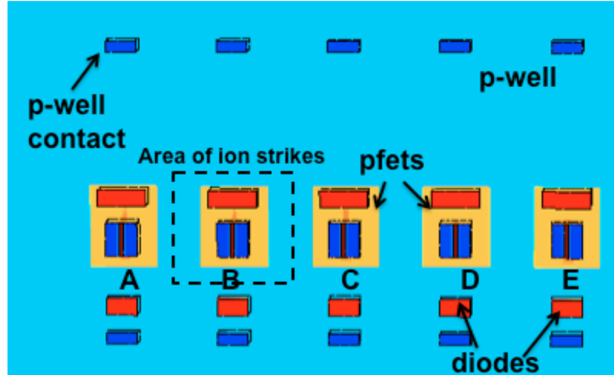

Fig. VI-8. TCAD model of 65 nm separate n-well inverters with pMOS transistors modeled in TCAD and nMOS transistors as compact models.

For these simulations, each TCAD model was struck with a single 58 MeV-cm^2/mg heavy-ion incident at 60° from the Si surface at different locations, as noted on Figs. VI-7 and VI-8. In each figure, the dotted line box represents the area rastered by the ion strikes where each ion strike location was separated by 100 nm from the previous ion

strike location. During and following the ion strike, the simulations were setup to monitor the voltage at each node of the inverter chain. Voltage monitoring of each node allowed any SETs generated to be observed during formation and propagation through the circuit.

For the common n-well circuit, the simulations do not show the existence of any DPSETs. For the majority of strike locations, pulse quenching is responsible for completely quenching the initial transient formed at node B, and then charge sharing causing a second transient to be created. For other locations, only a single pulse SET is generated or no SET is generated.

An example of the first pulse being quenched is in Fig. VI-9. Fig. VI-9 shows the results of an ion strike on the drain of the pMOS transistor at node B for the common n-well. An initial transient is created at node B and then propagates to node C. This transient is then completely quenched by the residual charge that surrounds node C. However, the transistors are spaced close enough that there is charge in the n-well that can be collected by the pMOS transistor at node D, which causes a second transient to be formed. This new transient then propagates unquenched through the chain and appears as a single pulse.

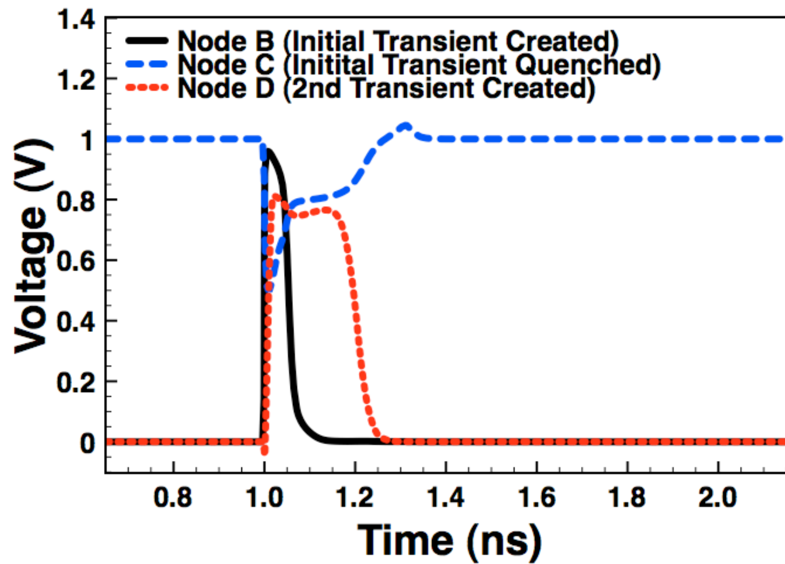

Fig. VI-9. Plot showing the generation of a transient at node B, then being quenched at node C, and then finally a second transient being generated at node D.

For the separate n-well circuit, the simulations do show the existence of a DPSET unlike the common n-well circuit simulations. Out of fifty simulations, one simulation for an ion strike location midway between pMOS transistor A and pMOS transistor B produces a DPSET. The DPSET is the result of partial pulse quenching occurring in the middle of a propagating SET. Fig. VI-10 illustrates this partial pulse quenching effect, and how it results in a DPSET.

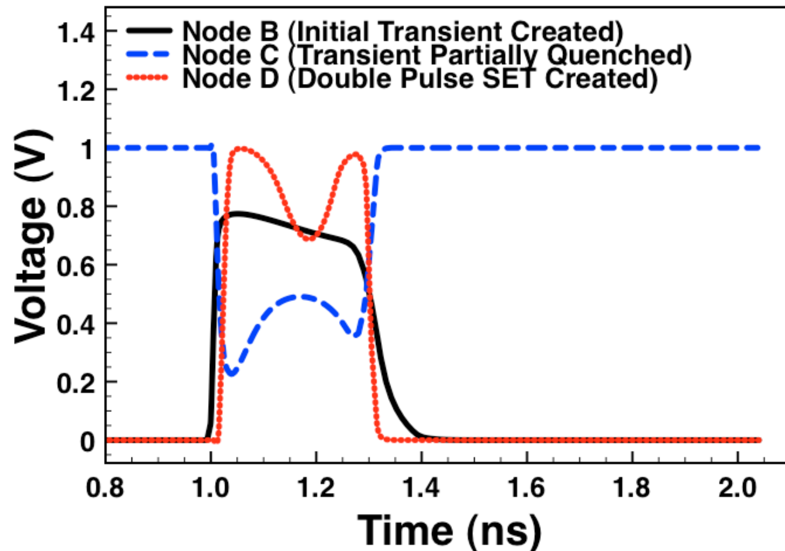

Fig.VI-10. Plot showing the generation of a DPSET in the separate n-well inverter chain simulation. An initial pulse is created at node B, then it is partially quenched at node C. It then propagates through node D and forms a DPSET.

In Fig. VI-10, the ion strike between pMOS transistor A and pMOS transistor B creates a transient at node B. This initial transient then propagates through node C. Then as a result of charge sharing from the initial ion strike, the SET is partially quenched in the middle of the pulse. Node C then returns LOW until the SET has propagated. At node D, the DPSET continues to take shape. Depending on the electrical characteristics of the circuit, the DPSET may be attenuated and propagate as a single pulse, or it may propagate through the chain as a DPSET. In the simulations, the "valley" of the DPSET is not below half-VDD causing the pulse to propagate as a single pulse at the next node. However, the TCAD simulations are only a representation of the actual circuit and do not capture the parasitics of the circuit at every node.

In order to confirm that pulse quenching was responsible for the DPSET observed in the simulations, another simulation was run. The simulation was setup the same as the previous simulation but the pMOS transistor at node C was replaced with a compact

model. Using a compact model stopped the pMOS transistor at node C from collecting any charge, which stopped pulse quenching from occurring.

Fig VI-11 show the results of the new simulation. A single pulse now propagates through nodes C and D. Thus, the simulation proves that pulse quenching is responsible for the DPSET observed in the separate n-well simulations.

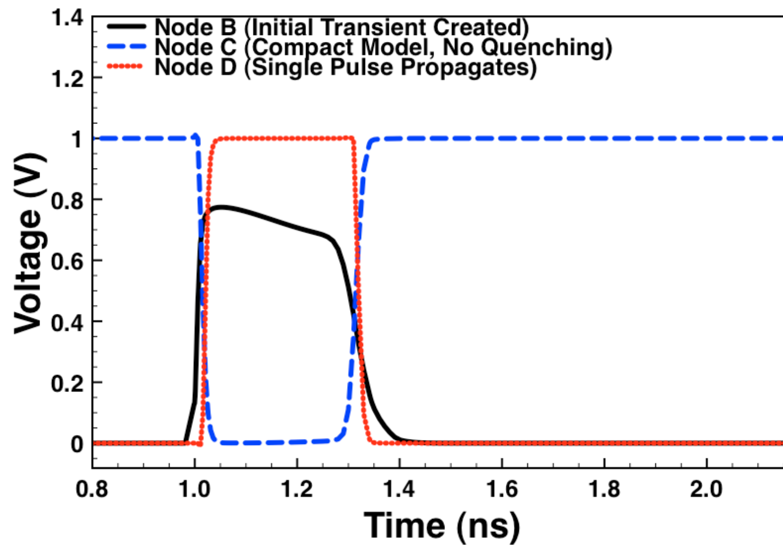

Fig. VI-11. Plot showing that pulse quenching is responsible for the generation of the DPSET. A compact model replaces the pMOS transistor at node C, which stops pulse quenching from occurring.

Discussion

In the heavy-ion data and simulation data, DPSETs only occur in the separate n-well circuit and do not occur in the common n-well circuit. Also in both the heavy-ion and simulation results, DPSETs occur infrequently.

Additionally, the DPSET from the simulation closely matches the characteristics of a few DPSETs observed during heavy-ion testing. The simulations show the

generation of a DPSET that has a first pulse width of 125 ps, a duration between pulses width of 75 ps, a second pulse width of 75 ps, and a total pulse width from the rising edge of the first pulse to the falling edge of the second pulse of 275 ps. Therefore, the simulations show that some of the heavy-ion DPSETs are the result of partial quenching of a SET.

However, the majority of heavy-ion DPSETs have a total pulse width that is greater than the total pulse width observed in the simulation. Also, the total pulse width of the DPSETs in the heavy-ion data is longer than the maximum single pulse SET measured [Ah10]. Thus, the mechanism of partial quenching does not explain all the DPSET heavy-ion data. There must be an additional mechanism that can cause the generation of a DPSET in the separate n-well circuit.

The additional mechanism is likely charge sharing affecting more than two pMOS transistors. This theory would agree with the heavy-ion data taken over multiple angles (Fig. VI-6), which shows the DPSET cross-section increasing with angle. The angle dependence signifies that multiple transistors are affected by the ion strikes [Amu07]. Also previous TCAD simulation work [Ah11] shows an LET 58 MeV-cm^2/mg ion at a 60° angle of incidence inducing a DPSET in the separate n-well design by depositing charge that causes four pMOS transistors to be upset.

Conclusion

In this chapter, experimental measurements of digital SETs in 65 nm bulk CMOS inverter strings show that a single angled particle strike can cause double-pulse-single-event transients (DPSETs). Experiments with inverter chains comprised of pMOS transistors in separate n-wells show significant DPSETs. Inverter chains comprised of pMOS transistors within a common n-well show no DPSETs. TCAD analyses suggest that the DPSET effect is a direct result of cross-boundary charge sharing (in the case of separate n-well isolation of devices) leading to either partial pulse quenching of a single pulse, which turns a single pulse into two pulses, or the separate creation of a secondary pulse. In the case of pMOS transistors within a common n-well, the second pulse is mitigated by the pulse quenching phenomenon.

CHAPTER VII

CONCLUSIONS

Conclusion

As feature sizes decrease and operating frequencies increase in digital circuits, the impact single-event transients (SETs) has on the reliability of digital circuits has become significant. Caused by single events (SEs) that can penetrate semiconductor material leaving ionized charge in their wake, SETs were previously only a reliability concern for space-deployed systems. However in modern bulk CMOS processes below 100 nm, SETs are now a reliability concern for ground-based systems.

By understanding the mechanisms that affect SETs in sub-100 nm bulk CMOS technologies, designers and researchers can better design systems to be robust to SET generation. The pulse width of SETs is directly related to whether an SET becomes an SEU or not. Using primitive digital circuits, such as inverters, minimizes additional circuit design factors that can influence SETs and allows the analysis to focus on the fundamental mechanisms that influence SETs.

This dissertation identifies parasitic BJT amplification, charge sharing, and pulse quenching as fundamental mechanisms that affect SETs in sub-100 nm bulk CMOS technologies by:

1. Modeling current-matched inverters in 130 nm, 90 nm, and 65 nm bulk CMOS using 3D TCAD simulations.

2. Developing test circuits that isolate specific SET mechanisms that can be repeated for multiple technology nodes.

3. Providing heavy-ion and TPA laser results that support the modeling work and help explain the SET mechanisms.

The following are the important contributions provided by this dissertation:

1. Experimental data that shows parasitic BJT amplification in pMOS transistors is a key mechanism that can affect SET pulse widths and can be influenced by the percentage of n-well area contacted.
2. Guidelines for the optimal amount of n-well contact area that minimizes SET pulse width.
3. Novel 3D TCAD models in 130 nm, 90 nm, and 65 nm bulk CMOS that isolate charge sharing to allow a comparison between inverters susceptible to pulse quenching and those not.
4. Simulation and experimental data that proves charge sharing can affect the pulse width of SETs.
5. Analysis of simulation and experimental data that shows the negation of guard bands as an effective RHBD solution in the presence of pulse quenching.
6. Explanation of 130 nm, 90 nm, and 65 nm bulk CMOS data that illustrates how increased transistor density in scaled bulk CMOS technologies leads to an increase in pulse quenching occurring in digital circuits.
7. Experimental and simulation data that identifies and explains a brand new type of SET called the double-pulse single-event transient (DPSET).

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APPENDIX A

PUBLICATIONS

Published Journal Articles

1. O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, and **J. R. Ahlbin**, "Design Techniques to Reduce SET Pulse Widths in Deep-Submicron Combinational Logic," *IEEE Trans. On Nucl. Sci.,* vol. 54, pp. 2060-2064, Dec. 2007.

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Nominated for Best Conference Paper

Published Non-Journal Articles

1. O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, **J. R. Ahlbin,** R. A. Reed and M. W. McCurdy, "Mitigation Techniques for Single Event Induced Charge Sharing in a 90 nm Bulk CMOS Process," Proc. 46th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 306-311, April 2008.

2. M. J. Gadlage, **J. R. Ahlbin**, B. Narasimham, V. Ramachandran, C. A. Dinkins, B. L. Bhuva, R. D. Schrimpf, and R. L. Shuler, "The Effect of Elevated Temperature on Digital Single Event Transient Pulse Widths in a Bulk CMOS Technology," Proc. 47th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 170-173, April 2009.

3. V. Ramachandran, M. J. Gadlage, **J. R. Ahlbin**, M. L. Alles, R. A. Reed, B. L. Bhuva, L. W. Massengill, J. D. Black, and C. N. Foster, "Application of a Novel Test System to Characterize Single-Event Transients at Cryogenic Temperatures," *Semiconductor Device Research Symposium, 2009. ISDRS '09*, vol., no., pp.1-2, 9-11 Dec. 2009.

4. M. J. Gadlage, **J.R. Ahlbin**, B. L. Bhuva, L. W. Massengill, and R. D. Schrimpf, "Single Event Transient Pulse Width Measurements in a 65-nm Bulk CMOS Technology at Elevated Temperatures," Proc. 48th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 763-767, May 2010.

5. **J. R. Ahlbin**, M. J. Gadlage, N. M. Atkinson, B. L. Bhuva, A. F. Witulski, W. T. Holman, and L. W. Massengill, "SET Pulse Widths in Advanced CMOS Logic Circuits," Proc. 48th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 198-202, May 2010.

6. N. N. Mahatme, I. Chatterjee, B. L. Bhuva, **J. Ahlbin**, L. W. Massengill, and R. Shuler, "Analysis of Soft Error Rates in Combinational and Sequential Logic and Implications of Hardening for Advanced Technologies," Proc. 48th Annu. IEEE International Reliability Physics Symp. (IRPS), pp. 1031-1035, May 2010.

7. **J. R. Ahlbin**, M. J. Gadlage, T. D. Loveless, D. R. Ball, B. L. Bhuva, A. F. Witulski, and L. W. Massengill, "Double-Pulse-Single-Event Transients in Combinational Logic," Proc. 49th Annu. IEEE International Reliability Physics Symp. (IRPS), April 2011.

APPENDIX B

PRESENTATIONS

Conference Presentations to Date

1. J. Black, R. Reed, L. Massengill, B. Bhuva, O. Amusan, M. Casey, A. Balasubramanian, and **J. Ahlbin**, “Circuit for Radiation Effects Self Test (CREST) Follow on for Bulk CMOS Shift Register Chain,” presented at the 2007 Single Event Effects Symposium, Long Beach, CA, April 2007.

2. O. A. Amusan, L. W. Massengill, B. L. Bhuva, S. DasGupta, A. F. Witulski, and **J. R. Ahlbin**, "Design Techniques to Reduce SET Pulse Widths in Deep-Submicron Combinational Logic," presented at the 2007 IEEE Nuclear and Space Radiation Effects Conference, Honolulu, HI, July 2007.

3. S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, O. A. Amusan, **J. R. Ahlbin**, R. D. Schrimpf, & L. W. Massengill, "Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS," presented at the 2007 IEEE Nuclear and Space Radiation Effects Conference, Honolulu, HI, July 2007.

4. **J. R. Ahlbin**, J. D. Black, L. W. Massengill, O. A. Amusan, A. Balasubramanian, M. C. Casey, D. A. Black, M. W. McCurdy, R. A. Reed, and B. L. Bhuva, "C-CREST Technique for Combinational Logic SET Testing", presented at 2008 SEE Symposium, Long Beach Island, CA, April 2008.

5. O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, **J. R. Ahlbin,** R. A. Reed and M. W. McCurdy, "Mitigation Techniques for Single Event Induced Charge Sharing in a 90 nm Bulk CMOS Process," presented at 2008 IEEE International Reliability Physics Symp. (IRPS), Phoenix, AZ, April 2008.

6. **J. R. Ahlbin**, J. D. Black, L. W. Massengill, O. A. Amusan, A. Balasubramanian, M. C. Casey, D. A. Black, M. W. McCurdy, R. A. Reed, and B. L. Bhuva, “C-CREST Technique for Combinational Logic SET Testing,” presented at the 2008 IEEE Nuclear and Space Radiation Effects Conference, Tucson, AZ, July 2008.

7. **J. R. Ahlbin**, L. W. Massengill, B. L. Bhuva, B. Narasimham, W. T. Holman, P. H. Eaton, and M. J. Gadlage, “Analysis of the Effect Multi-Node Charge Collection has on Single Event Transient Pulse Widths in Advanced CMOS Logic,” presented at the 2009 GOMACTech, Orlando, Fl, March 2009.

8. M. J. Gadlage, **J. R. Ahlbin**, B. Narasimham, V. Ramachandran, C. A. Dinkins, B. L. Bhuva, R. D. Schrimpf, and R. L. Shuler, “The Effect of Elevated Temperature on Digital Single Event Transient Pulse Widths in a Bulk CMOS Technology,” presented at 2009 IEEE International Reliability Physics Symp. (IRPS), Montreal, Canada, April 2009.

9. M. C. Casey, S. A. Nation, **J. R. Ahlbin**, R. Arora, S. A. Francis, B. L. Bhuva, D. McMorrow, H. L. Hughes, P. J. McMarr, J. S. Melinger, and L. W. Massengill, “Effect of Total Ionizing Dose on Combinational Logic Circuits Operating at Ultra-Low Power,” presented at the 2009 IEEE Nuclear and Space Radiation Effects Conference, Quebec, Canada, July 2009.

10. M. J. Gadlage, **J. R. Ahlbin**, V. Ramachandran, C. A. Dinkins, B. L. Bhuva, B. Narasimham, R. D. Schrimpf, and R. L. Shuler, "Temperature Characterization of Digital Single Event Transients in a Bulk and Fully Depleted SOI Technology," presented at the 2009 IEEE Nuclear and Space Radiation Effects Conference, Quebec, Canada, July 2009.

11. **J. R. Ahlbin**, B. L. Bhuva, M. J. Gadlage, L. W. Massengill, B. Narasimham, and P. H. Eaton, ”Single Event Transient Pulse Quenching in 130 nm CMOS Logic,” presented at the 2009 IEEE Nuclear and Space Radiation Effects Conference, Quebec, Canada, July 2009.

12. V. Ramachandran, M. J. Gadlage, **J. R. Ahlbin**, M. L. Alles, R. A. Reed, B. L. Bhuva, L. W. Massengill, J. D. Black, and C. N. Foster, “Application of a Novel Test System to Characterize Single-Event Transients at Cryogenic Temperatures,” presented at 2009 Semiconductor Device Research Symposium, College Park, MD, Dec. 2009.

13. M. J. Gadlage, **J.R. Ahlbin**, B. L. Bhuva, L. W. Massengill, and R. D. Schrimpf, “Single Event Transient Pulse Width Measurements in a 65-nm Bulk CMOS Technology at Elevated Temperatures,” presented at 2010 IEEE International Reliability Physics Symp. (IRPS), Anaheim, CA, May 2010.

14. **J. R. Ahlbin**, M. J. Gadlage, N. M. Atkinson, B. L. Bhuva, A. F. Witulski, W. T. Holman, and L. W. Massengill, “SET Pulse Widths in Advanced CMOS Logic Circuits,” presented at 2010 IEEE International Reliability Physics Symp. (IRPS), Anaheim, CA, May 2010.

15. N. N. Mahatme, I. Chatterjee, B. L. Bhuva, **J. Ahlbin**, L. W. Massengill, and R. Shuler, “Analysis of Soft Error Rates in Combinational and Sequential Logic and Implications of Hardening for Advanced Technologies,” presented at 2010 IEEE International Reliability Physics Symp. (IRPS), Anaheim, CA, May 2010.

16. S. Jagannathan, M. J. Gadlage, B. L. Bhuva, R. D. Schrimpf, B. Narasimham, J. Chetia, **J. R. Ahlbin**, and L. W. Massengill, “Independent Measurement of SET Pulse Widths From N-Hits and P-Hits in 65 nm CMOS,” presented at the 2010 IEEE Nuclear and Space Radiation Effects Conference, Denver, CO, July 2010.

17. **J. R. Ahlbin**, M. J. Gadlage, D. R. Ball, A.W. Witulski, B. L. Bhuva, R. A. Reed, G. Vizkelethy, and L. W. Massengill, “The Effect of Layout Topology on Single-Event Transient Pulse Quenching in a 65 nm Bulk CMOS Process,” presented at the 2010 IEEE Nuclear and Space Radiation Effects Conference, Denver, CO, July 2010.

18. M. J. Gadlage, **J. R. Ahlbin**, B. Narasimham, B. L. Bhuva, L. W. Massengill, R. A. Reed, R. D. Schrimpf, and G. Vizkelethy, “Scaling Trends in SET Pulse Widths in Sub-100 nm Bulk CMOS Processes,” presented at the 2010 IEEE Nuclear and Space Radiation Effects Conference, Denver, CO, July 2010.

19. N. M. Atkinson, A. F. Witulski, W. T. Holman, **J. R. Ahlbin**, B. L. Bhuva, and L. W. Massengill, “Layout Technique for Single-Event Transient Mitigation via Pulse Quenching,” presented at the 2010 IEEE Radiation and its Effects on Components and Systems, Langenfeld, Austria, Sept. 2010.

20. M. J. Gadlage, **J. R. Ahlbin**, B. L. Bhuva, N. C. Hooten, N. A. Dodds, R. A. Reed, L. W. Massengill, R. D. Schrimpf, and G. Vizkelethy, “Alpha-Particle and Focused-Ion-Beam-Induced Single-Event Transient Measurements in a Bulk 65-nm CMOS Technology,” presented at the 2010 IEEE Radiation and its Effects on Components and Systems, Langenfeld, Austria, Sept. 2010.

21. **J. R. Ahlbin**, M. J. Gadlage, T. D. Loveless, D. R. Ball, B. L. Bhuva, A. F. Witulski, and L. W. Massengill, “Double-Pulse-Single-Event Transients in Combinational Logic,” presented at 49th Annu. IEEE International Reliability Physics Symp. (IRPS), April 2011.

22. **J. R. Ahlbin**, N. M. Atkinson, M. J. Gadlage, N. J. Gaspard, B. L. Bhuva, T. D. Loveless, E. X. Zhang, L. Chen, and L. W. Massengill, “Influence of N-Well Contact Area on the Pulse Width of Single-Event Transients,” presented at 2011 IEEE Nuclear and Space Radiation Effects Conference, Las Vegas, Nevada, July 2011.

23. N. M. Atkinson, **J. R. Ahlbin,** A. F. Witulski, N. J. Gaspard, W. T. Holman, B. L. Bhuva, E. X. Zhang, L. Chen, L. W. Massengill, "Effect of Transistor Density and Charge Sharing on Single-Event Transients in 90-nm Bulk CMOS," presented at 2011 IEEE Nuclear and Space Radiation Effects Conference, Las Vegas, Nevada, July 2011.

24. N. J. Gaspard, A. F. Witulski, N. M. Atkinson, **J. R. Ahlbin,** W. T. Holman, B. L. Bhuva, T. D. Loveless, L. W. Massengill, "Impact of Well Structure on Single-Event Well Potential Modulation in Bulk CMOS," presented at 2011 IEEE Nuclear and Space Radiation Effects Conference, Las Vegas, Nevada, July 2011.

25. P. M. Gouker, B. Tyrrell, R. D'Onofrio, P. Wyatt, T. Soares, W. Hu, C. Chen, J. R. Schwank, M. R. Shaneyfelt, E. W. Blackmore, K. Delikat, M. Nelson, P. McMarr, H. Hughes, **J. R. Ahlbin**, S. Weeden-Wright, R. Schrimpf, "Radiation Effects in 3D Integrated SOI SRAM Circuits," presented at 2011 IEEE Nuclear and Space Radiation Effects Conference, Las Vegas, Nevada, July 2011.

26. P. M. Gouker, B. Tyrrell, M. Renzi, C. Chen, P. Wyatt, **J. R. Ahlbin**, S. Weeden-Wright, N. M. Atkinson, N. J. Gaspard, B. L. Bhuva, L. W. Massengill, E. Zhang, R. Schrimpf, R. A. Weller, M. P. King, M. J. Gadlage, "SET Characterization in Logic Circuits Fabricated in a 3DIC Technology," presented at 2011 IEEE Nuclear and Space Radiation Effects Conference, Las Vegas, Nevada, July 2011.