QUALITATIVE CHARACTERIZATION OF SINGLE-EVENT TRANSIENT AND LATCHUP TRENDS IN 180 nm CMOS TECHNOLOGY

By

Cody Adam Dinkins

Thesis

Submitted to the Faculty of the

Graduate School of Vanderbilt University

in partial fulfillment of the requirements

for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

May, 2011

Nashville, TN

Approved:

Professor Lloyd W. Massengill

Professor Ronald D. Schrimpf

ACKNOWLEDGEMENTS

I would like to thank both Dr. Lloyd W. Massengill and Jeff S. Kauppila for providing extraordinary guidance and advice throughout my graduate school career in academic, professional, and personal capacities. Both of these gentlemen have helped me through hard times in all of these areas of my life, and for that I would like to express my full appreciation. I would also like to thank numerous other professors who have contributed in various capacities to the completion of this work: Dr. Ronald D. Schrimpf, Dr. Bharat L. Bhuva, Dr. Arthur F. Witulski, Dr. W. Timothy Holman, and others. Each of these gentlemen's respectful contributions is greatly appreciated.

Many thanks are in order to my student peers in the Radiation Effects and Reliability Group. While it has been a pleasure working with every student in the group, I would like to give special thanks to Corey Toomey, Nelson Gaspard, Jon Ahlbin, Vishwa Ramachandran, and Nick Atkinson for technical assistance in multiple areas related to both this work and others.

Next, I would like to thank Randa, my girlfriend of nearly three years (at the time of this document's completion). You have been a constant source of encouragement for as long as I have known you. You never cease to amaze me in so many ways. I do not know what the future contains for the two of us, but I am forever appreciative for your support as a friend. Thank you.

Most importantly, I would like to thank my parents for their never-ending support and encouragement throughout my entire life. Anything I could ever need has been provided for me, and there is no amount of appreciation that speaks highly enough for

what they have both given me.   I am forever grateful and love the both of you very much. The same applies to my brother and sister who have provided encouragement and a place to come home to throughout the years. Thank you all.

Finally, I would like to thank Draper Laboratory for the financial support provided for this work. Without it, this work would not have been possible.

TABLE OF CONTENTS

Page

ACKNOWLEDGEMENTS ii

LIST OF FIGURES vi

LIST OF TABLES viii

Chapter

I. INTRODUCTION 1

1.1 Overview of Single-event Latchup 1
1.2 Typical Latchup Susceptible Structure 2
1.3 The Single-event Induced Latchup Process 4
1.4 Overview of Previous Single-event Latchup Work 5
1.5 Overview of Thesis 7

II. DEVICE MODEL CALIBRATION AND TRANSIENT CHARACTERIZATION 9

2.1 IBM 180 nm Device Creation 9
2.2 Electrical Calibration 12
2.3 Single-event Transient Characterization 13
2.3.1 Mechanisms Governing SET Response 14
2.3.2 Single-event Transient Simulation Setup 15
2.3.3 Drain Current vs. Drain Load 17
2.3.4 Drain Current vs. Supply Voltage 20
2.3.5 Drain Current vs. Heavy-ion LET 22

III. SINGLE-EVENT LATCHUP SIMULATION SETUP 26

3.1 2-D TCAD Standard Latchup Simulation Structure and Procedure 26
3.2 Latchup Structure with Added Deep-p+ Buried Layer 28
3.3 Latchup Structure with Added Guard Diffusion 29
3.4 Triple-well Latchup Structure with Non-connected and Connected N-wells 30

IV. SINGLE-EVENT LATCHUP SIMULATION RESULTS 32

4.1 1.8V VDD Bias Heavy Ion Strike Results... 33
4.2 5.0V VDD Bias Heavy Ion Strike Results... 35
4.2.1 Strike Results on Guarded Structure.................................. 37
4.2.2 Strike Results on Triple-well Device Structure 38
4.3 Results Discussion 40
4.3.1 Worst-case Strike Location – p+ Diffusion 40
4.3.2 Observed Latchup Trends and Dependencies..................... 41

V. CONCLUSION 43

REFERENCES 46

Appendix

A. DEVICE SIMULATION FILES / MODELS.. 49

A.1 Doping Profile Details: Full NMOSFET and PMOSFET Models 49
A.2 Full Model and Simulation File Scheme Scripts 51
A.2.1 Sample Standard NMOSFET Script 51
A.2.2 Sample Triple-well NMOSFET Script 60
A.2.3 Sample "3-D SE Transient" sdevice Simulation Script..... 76
A.2.4 Sample "2-D SE Latchup" Stucture Script 80
A.2.5 Sample "2-D SE Latchup" sdevice Simulation Script....... 87

B. FULL 2-D LATCHUP SIMULATION RESPONSE TABLES 90

LIST OF FIGURES

Figure Page

1. Cross-section of typical CMOS inverter, including well contacts 2

2. Typical arrangement of CMOS structures creating the cross-coupled BJT elements .. 3

3. Initial electron-hole pairs and current tracks created by incident particle strike 5

4. Standard NMOS device detail 11

5. Drain current (I_D) vs gate voltage (V_G) calibration curves 12, 13

6. Visualization of ion strike, drift / diffusion component identification 14

7. Transient simulation model / visualization 16

8. Single-event strike profile – Drain current vs. drain load (NMOSFET) 18

9. Single-event strike profile – Drain current vs. drain load (PMOSFET) 19

10. Single-event strike profile – Drain current vs. supply voltage (NMOSFET) 20

11. Single-event strike profile – Drain current vs. supply voltage (PMOSFET).............. 21

12. Single-event strike profile – Drain current vs. heavy-ion LET (NMOSFET) 23

13. Single-event strike profile – Drain current vs. heavy-ion LET (PMOSFET)............. 24

14. 2-D CMOS latchup test structure.. 27

15. 2-D TCAD latchup structure with / without deep-p^+ buried layer.............................. 29

16. 2-D TCAD latchup structure with added guard diffusion 30

17. 2-D TCAD triple-well latchup structure with connected / non-connected N-wells ... 31

18. Latchup simulation results example and explanation 32

19. Latchup simulation result – p+ diffusion, 1.8V VDD 34

20. Latchup simulation result – p+ diffusion, 5.0V VDD 36

21. Latchup simulation result – p+ diffusion, 5.0V VDD, with / without guard.............. 37

22. Latchup simulation result – p+ and n+ diffusions, triple-well NMOS structure 39

LIST OF TABLES

Table Page

1. Single-event latchup strike results – Location: p+-diffusion 41

B1. Single-event latchup strike results – Location: P-well contact 91

B2. Single-event latchup strike results – Location: n+-diffusion 92

B3. Single-event latchup strike results – Location: N-well contact................................. 93

B4. Single-event latchup strike results – Location: p+-diffusion (same as Table 1)........ 94

CHAPTER I

INTRODUCTION

The continued scaling of CMOS device sizes constantly creates new challenges in shielding electronics from single-event effects (SEE). This holds especially true for applications set in space environments wherein correct circuit operation is absolutely critical. A single-event (SE) may occur as a result of a charged particle, such as a heavy-ion, entering a semiconductor device. Upon entry, the charged particle begins losing energy through Coulombic interactions with the lattice structure of the semiconductor material such as silicon. These interactions, coupled with the resultant slowing of the particle, create free electron-hole pairs (EHPs) along the particle's path. This excess charge can then be collected at sensitive device locations to produce unwanted, and even potentially catastrophic, results such as voltage and/or current transients that can propagate to and corrupt nodes containing stored information or place devices into an unrecoverable state until power is cycled. The latter effect is known as single-event latchup (SEL) and is the main focus of this thesis [1]-[4].

1.1 Overview of Single-event Latchup

Latchup may occur when one or multiple reverse-biased p-n junctions within a device or circuit becomes freely conducting in response to either junction breakdown or junction bias change. Single-event latchup, in particular, typically results when a particle deposits or creates enough excess charge to forward-bias both the n-p-n and p-n-p

parasitic bipolar junction transistors (BJTs) inherent to the CMOS topology. If these BJTs are created in sufficiently close proximity and maintain gains greater than one, a self-sustaining latchup current path can be created. Symbolically, this is represented as

$$\beta_{\mathrm{npn}}\beta_{\mathrm{pnp}} \geq 1$$

where β_{npn} and β_{pnp} are the gains of the parasitic n-p-n and p-n-p BJTs, respectively. In some scenarios, extended duration current transients that resemble latchup will recover. However, for devices with a self-sustaining latchup path, recovery does not occur until the power is cycled. The device's or circuit's entry into this unrecoverable state defines the necessary condition to identify latchup [5]-[6].

1.2 Typical Latchup Susceptible Structure

In a typical bulk CMOS process, there exists a very common structure proven sensitive to single-event latchup, a structure created by an arrangement of n-type and p-type diffusions or implants in a p-type substrate. This structure is common because it is inherently present in even the simplest logic gate in CMOS technology—the basic inverter consisting of a single PMOS device and a single NMOS device as pictured in Figure 1.

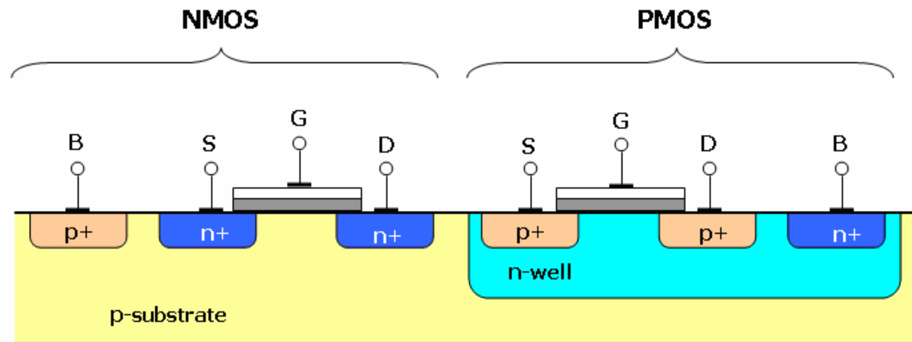


Figure 1. Cross-section of typical CMOS inverter, including well contacts.

With each created PMOS device is also created a parasitic p-n-p BJT element formed by a p-type diffusion, the n-well in which this diffusion is placed, and the p-type substrate. If an NMOS device is placed in close proximity to the PMOS device, a parasitic n-p-n BJT element is formed by an n-type diffusion, the p-type substrate, and the n-well housing the corresponding PMOS device. It is the proximity of the NMOS structure to the PMOS n-well that facilitates the interaction of the BJT structures to create the cross-coupled structure in Figure 2. This figure displays a simplified model in that it only includes one active n+ diffusion and one active p+ diffusion along with well contacts rather than the full NMOS and PMOS devices present in a CMOS inverter. However, this model contains all the elements necessary to induce latchup in the CMOS topology [7].

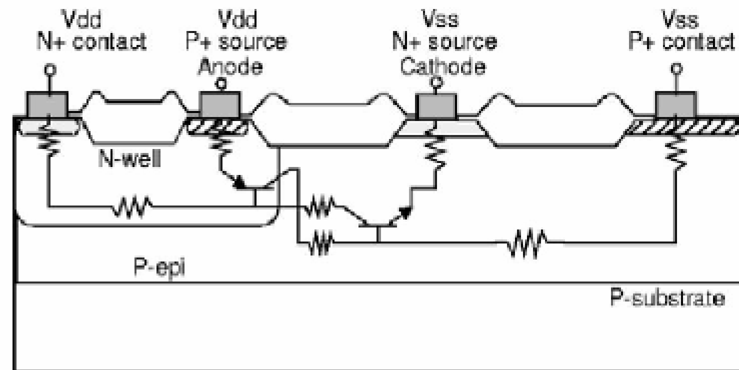


Figure 2. Typical arrangement of CMOS structures creating the cross-coupled BJT elements conducive to circuit latchup. From [7].

This figure illustrates how the collector node of the p-n-p BJT—the p-type substrate—serves as the base node of the n-p-n BJT, while the collector node of the n-p-n BJT—the n-well diffusion—serves as the base node of the p-n-p BJT. This configuration is conducive to the latchup phenomenon as the forward-biasing of one parasitic transistor can lead to the forward-biasing of the second. Once both BJTs are operating in the

"forward active" region of operation, a regenerative current may be seen, and latchup can potentially occur if the BJTs' multiplied gains exceed unity [5]-[9].

1.3 The Single-event Induced Latchup Process

The most common condition leading to single-event induced latchup is the debiasing of the n-well which houses the PMOS device or p-type diffusion as pictured in Figure 3. A heavy ion, or other charged particle, may penetrate the surface of a device and deposit or create charge in or near the n-well. The EHPs created by this excess charge produce a transient current extending through the n-well / substrate junction. This current flows from the n-well contact to the p-well contact and causes a debiasing of the n-well / substrate junction. This debiasing creates a voltage drop V_{EB} (emitter-to-base) to appear between the p+ diffusion and the n-well, which leads to the injection of holes at the p+ diffusion to counter the debiasing effect [10].

The newly injected holes from the p+ diffusion, along with those created during the heavy ion strike, are then drawn toward the substrate where they tend to raise the substrate potential at the n-p-n base. This increase in substrate voltage causes the voltage difference V_{BE} (base-to-emitter) to appear between the substrate and the n+ diffusion, in turn leading to an injection of electrons from the n+ diffusion which is held at ground. These injected electrons from the n-p-n BJT collector can then be swept toward the n-well where they tend to reinforce the initial debiasing caused by the heavy ion at the base of the p-n-p BJT. The reinforced debiasing then draws more holes from the p+ diffusion and the process may continue indefinitely, creating a regenerative current path among the p-n-p-n arrangement of structures [10].

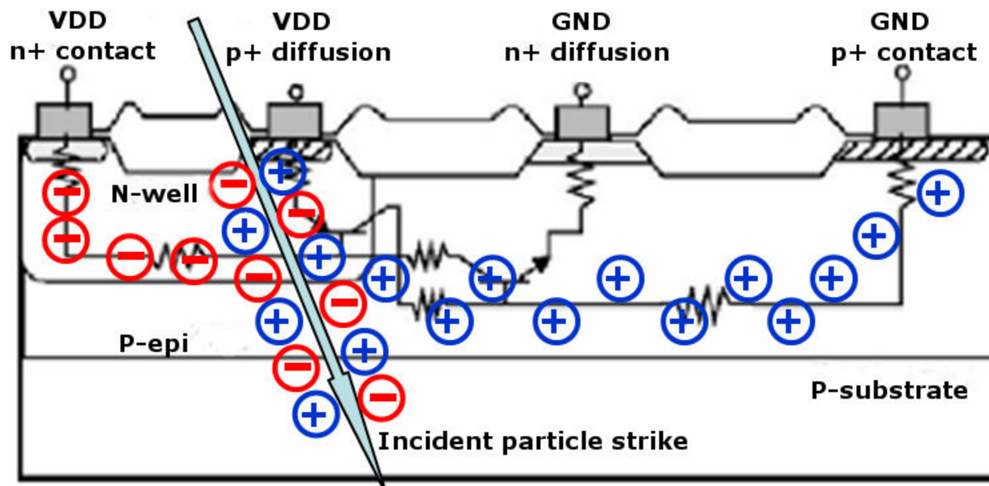


Figure 3. Initial electron-hole pairs and current tracks created by incident particle strike.

1.4 Overview of Previous Single-event Latchup Work

Limited data has been published regarding the single-event vulnerability of the 180 nm technology node. Moreover, the individual studies performed utilized processes that differ significantly regarding doping levels, inclusion of mitigation techniques, well contact placement, and other device geometries that have been shown to affect SE vulnerability [5], [11]. Testing procedures among the published studies also differ significantly, providing inconclusive agreement among results.

One such study by Boselli et. al. utilized a Texas Instruments 180 nm process. This study provided results of two standard latchup tests—overvoltage application (supply voltage increased above the standard value) at power supply pins and high current injection (+/- 200 mA, in this case) at each signal pin—applied to a structure similar to one illustrated in Figure 2. While these tests do not involve radiation or single-event strikes, latchup can still be triggered via electrical excitation, as described, since the triggering mechanisms are inherently the same. Interestingly, the study found that the overvoltage application test was unable to produce latchup regardless of the applied

supply voltage—up to 50% above nominal VDD—and is a promising result for the technology node. The second test, however, consistently resulted in latchup. While this is obviously an undesirable result, important questions were left unanswered by the study. For example, it is not stated by what metric the injected current amplitude of 200 mA was chosen. This value may or may not be a realistic condition that can be provided or sustained in this technology. It was also never explicitly stated whether this study presented experimental or simulated data, an important detail that should be evident in any technology research study [12].

Finally, it should be noted that since the aforementioned study was performed using a Texas Instruments (TI) CMOS process, the results may not be easily applicable to other 180 nm processes due to inherent fabrication differences among them. For example, the TI study reports an n-well / p-substrate avalanche breakdown voltage—the triggering source of latchup in the overvoltage application test—of about 14V [12]. Official documentation of the IBM 180 nm Process Design Kit (PDK) reports an avalanche breakdown voltage of about 8V, suggesting an inherent difference in the doping levels of the n-well and substrate [13]. The doping of these regions determines the values of the resistances in the process (Figure 3) that are fundamental to the latchup process. While there are numerous other differences between the TI process and others, the most important is the lack of a highly doped buried layer, a latchup mitigation technique that has proven to be highly effective and will be discussed in more depth in Section 3.2 [5].

Another study performed by Hutson et. al. focused on the effects of well and substrate contact spacing on single-event latchup at the 180 nm node. This previous

work is relevant as it presents very high latchup susceptibility for the 180 nm technology node regardless of contact spacing. It is important to note, however, that the simulated models utilized in this study were not tailored to any specific 180 nm process in terms of doping levels, well / contact geometries and spacing, or inherent latchup mitigation techniques. In fact, there is no apparent inclusion of shallow trench isolation (STI) in the models used [11]. The inclusion of STI, or another form of isolation, wherever active regions or diffusions are absent has become a standard for blocking undesired interaction among devices. The depth to which STI is extended in a process can greatly affect its SEL vulnerability: the deeper the isolation is extended, the more latchup resistant a technology generally is. Therefore, a complete lack of isolation would very likely give unrealistically low failure LET measurements [5]. The work is effective in its design to detail SEL vulnerability trends related to contact spacing but should not be understood as a strong representation of the overall SEL vulnerability of the 180 nm technology node.

The results of these previous works, coupled with the inherent fabrication differences of processes at the 180 nm node, provide strong motivation for continued research into the node's SEL vulnerability. This thesis presents further qualitative research on the topic and provides, to the best of the author's ability, explicit detail of the device models and experimental procedures utilized.

1.5 Overview of Thesis

This thesis focuses on a study of single-event effects performed at the 180 nm technology node with an emphasis on operation in the analog / mixed-signal (AMS) domain. The study consisted of three main parts: 1) creation and calibration of

technology computer aided design (TCAD) models for simulation of devices at the target technology node; 2) basic single-event transient characterization of the target technology; 3) single-event latchup characterization of the target technology.

The specific technology utilized in this study was the IBM 7RF bulk CMOS process which includes devices capable of 1.8V, 3.3V, and 5.0V VDD operation [13]. These operating voltages offer benefits in the form of voltage swing and noise margins over smaller technologies such as the IBM 8SF and 9SF which have lower nominal supply voltages. All TCAD simulations were performed using Synopsys TCAD tools.

Chapter II describes the process of creating TCAD models for simulation after which initial SEE characterization of the target technology process took place. A summary of this characterization is also provided in Chapter II. Chapter III introduces the single-event latchup study performed, followed by results and discussion in Chapters IV and V.

CHAPTER II

DEVICE MODEL CALIBRATION AND TRANSIENT CHARACTERIZATION

Creating 3-D TCAD models which closely represent the true properties of the IBM 180 nm devices was the first step in modeling the technology's single-event behavioral response. The single-event behavior of a deep submicron technology is directly related to properties such as drive strength, drain engineering, and threshold voltage levels. Therefore, it is necessary to replicate these original device properties with sufficient accuracy [14]. Parameters that govern these properties include structural geometries and doping profiles of the devices. Geometries and doping for the gate poly, source/drain, and LDD structures were patterned after the International Technology Roadmap for Semiconductors (ITRS) for this technology node along with previous calibration work at the 130 nm IBM node [15]. Well and substrate doping levels were obtained from a Chipworks report on the IBM 180 nm process [16]. These parameters are discussed in more detail to follow.

2.1 IBM 180 nm Device Creation

The device geometries and doping profiles used to create the nominal 180 nm NMOS and PMOS devices were the baseline for the creation of every device utilized in this study. These values, while rooted in the year 2000 ITRS, were heavily influenced by known characteristics of the IBM 130nm technology [15]. This is practical as comparing

the ITRS values of the 180 nm process to those of the 130 nm suggests that the 130 nm process is basically a geometric shrink of the larger process.

The nominal devices were created in and centered on a 10 μm^3 p-type silicon substrate doped constantly at 1 x 10^{16} cm^{-3} boron atoms. Present throughout the entire wafer in the 180 nm process is a deep-p+ buried layer which was modeled as Gaussian with a peak doping level of 1 x 10^{18} cm^{-3} boron at about 1.25 μm depth. This deep-p+ layer is a standard single-event mitigation technique that will be described in more detail in chapters to come. The nominal gate oxide thickness was chosen as 4 nm while the thickness of the polysilicon gate was chosen as 142.5 nm, both values taken from the standard model files in the IBM 180 nm PDK. Well contacts for each device were located 440 nm from the edge of the device gate, the minimum spacing allowed for the technology.

The channel region of each device includes each of the following implants: a threshold voltage (V_T) adjustment implant, lightly doped drain (LDD) implants, and "halo" implants. The V_T adjustment implant serves to provide strong first-order control over the threshold voltage by increasing the net doping concentration right at the silicon surface. The LDD implants are short source and drain extensions that provide a moderate resistance path, compared to the source and drain regions, across which voltage applied at the drain may be dropped instead of being dropped directly across the velocity-saturated diffusion region. From a circuit perspective, the LDD implants effectively determine the series resistance of a device. Finally, the halo implants are diffused adjacent to the LDDs within the channel and deter short channel effects while providing a "knob" for adjusting the slope of the device's subthreshold current [14]. A large amount of insight into the

technology's actual doping levels was gained from a third-party report by Chipworks, especially for the area of the channel region [16]. Figure 4 displays a created nominal NMOS device along with a 2-D cut view of the many individual structures described here.

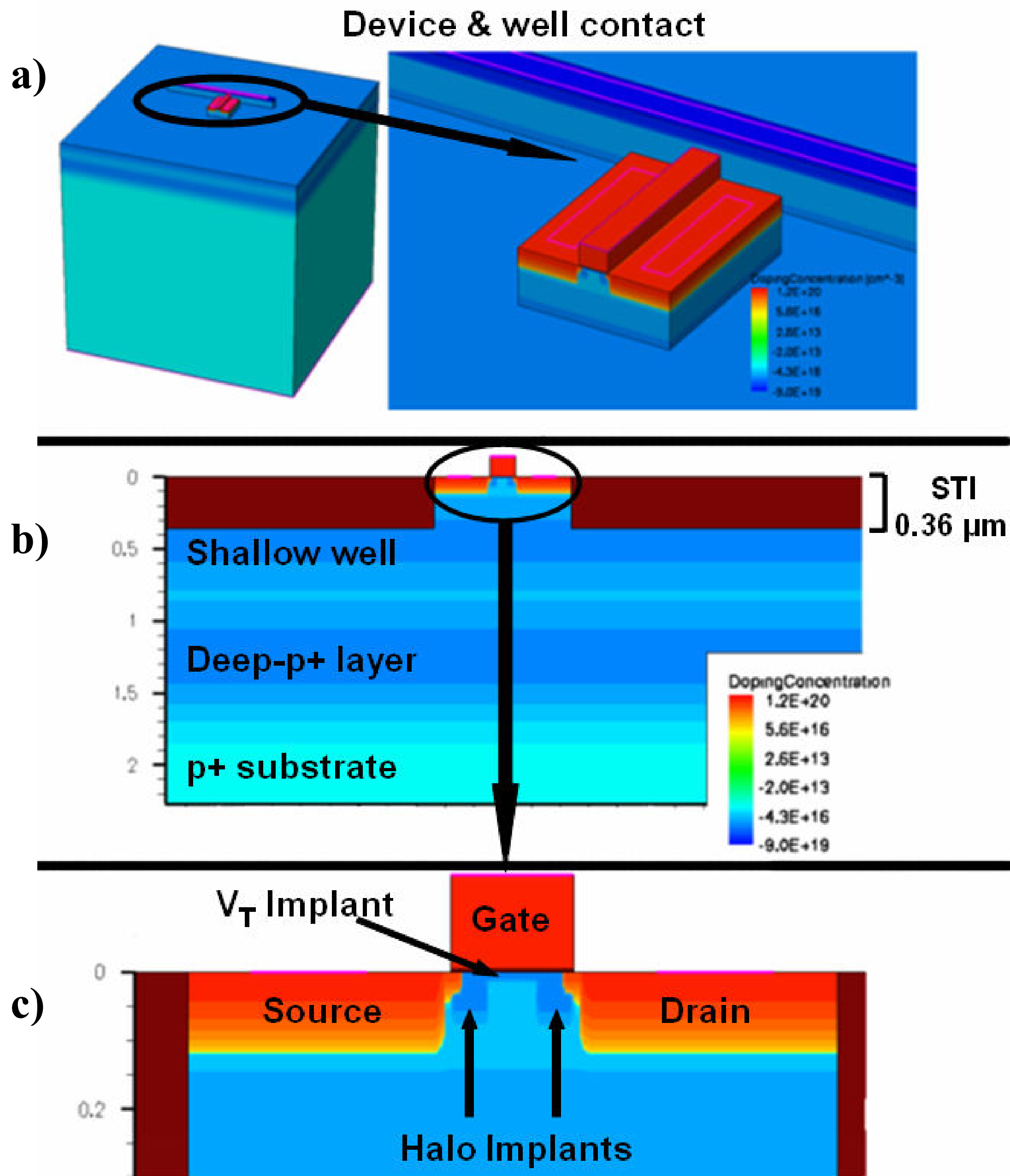
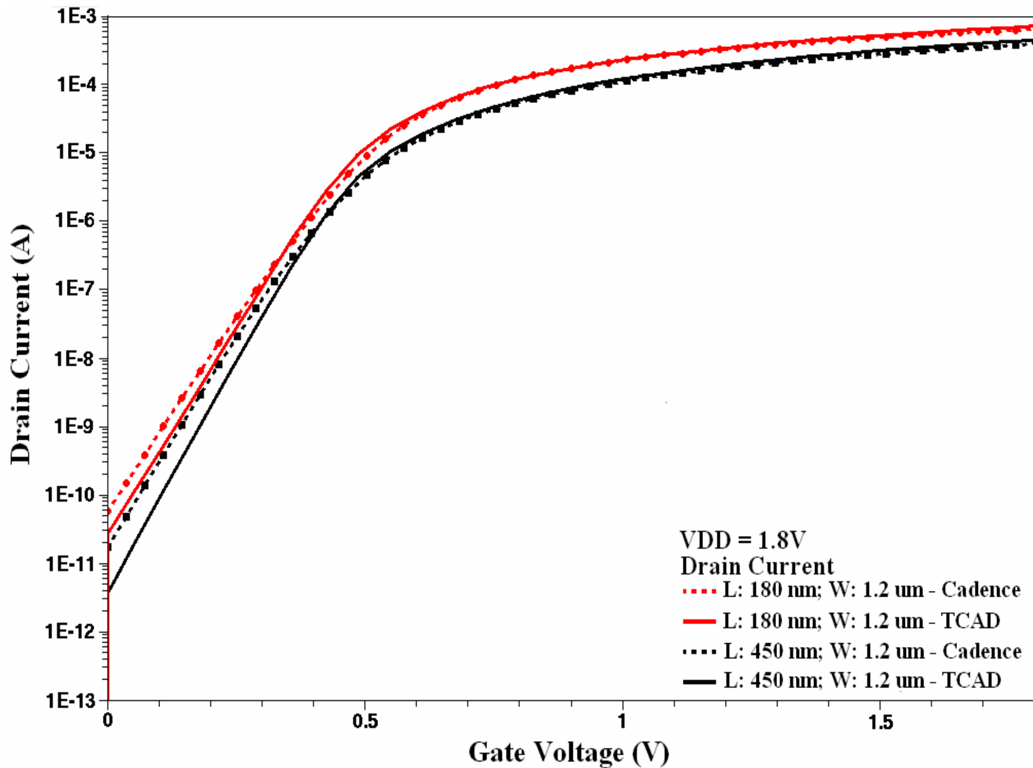


Figure 4. Standard NMOS device views: a) full 3-D device including substrate "cube" and well contact (STI not pictured), b) 2-D cut of the device illustrating STI and well and substrate doping, and c) magnified cross-section of the device, including V_T adjust and halo implants.

2.2 Electrical Calibration

Following the initial creation of the basic NMOS and PMOS devices, validation and fine-tuning of the device geometries and doping profiles were necessary. Therefore, a series of I_D vs. V_G (drain current versus gate voltage, or I_D/V_G) curves was obtained from the IBM 180 nm Process Design Kit (PDK) and compared to I_D/V_G sweeps performed on the created TCAD devices. Devices were biased at the full voltage supply rail (1.8V), and the gate terminals were swept from 0V to 1.8V, or -1.8V for the PMOS device, full supply rail while drain current was monitored. Doping levels for the V_T adjust implant, LDDs, and halo implants were iteratively adjusted to alter properties such as threshold voltage, off-state leakage current, and on-state drive current. The final calibration is illustrated below in a comparison between the ID/VG curves obtained from the PDK and those obtained from TCAD sweeps.



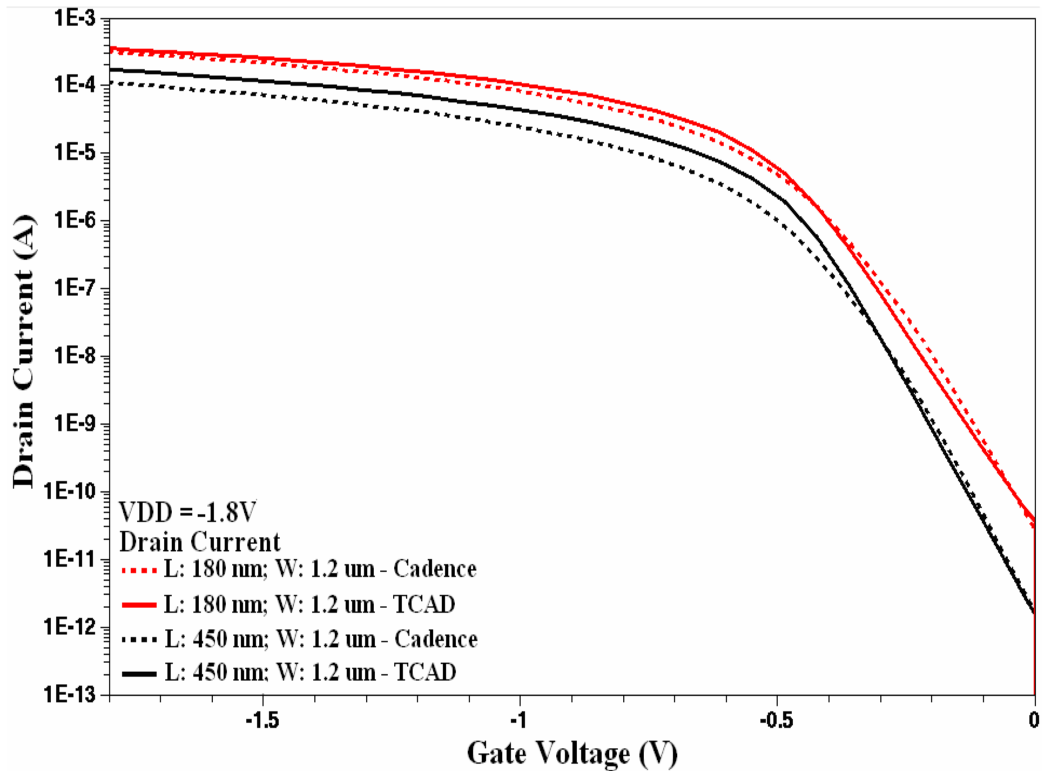


Figure 5. Drain current (I_D) vs gate voltage (V_G) calibration curves: a) full 3-D TCAD standard NMOS device, b) full 3-D TCAD standard PMOS device. Sizes of 1.2 um (W) x 180 nm (L) and 1.2 um (W) x 450 nm (L). PDK model curves displayed in dashed line and TCAD model curves displayed in solid lines.

2.3 Single-event Transient Characterization

Once accurate electrical calibration of the TCAD device models was complete, basic single-event characterization of the technology began. To accurately characterize the results of heavy-ion strikes on the calibrated device models, there must be an understanding of the mechanisms responsible for the transient response. A short description of these mechanisms along with the setup and results of the simulated heavy-ion strikes follow in this section.

2.3.1 Mechanisms Governing Single-event Transient Response

It is well understood that the shape and duration of single-event current pulses are strong functions of the incident heavy-ion strike's linear energy transfer (LET), the circuit's supply voltage, and the load connected to the struck device. Each variable plays a role in determining either or both of the mechanisms of excess charge drift and diffusion in the struck device. The height of the initial pulse immediately following the strike, the presence and duration of a generated current plateau, and the rate of falloff at the end of the transient are all affected by these factors [5], [17]-[18].

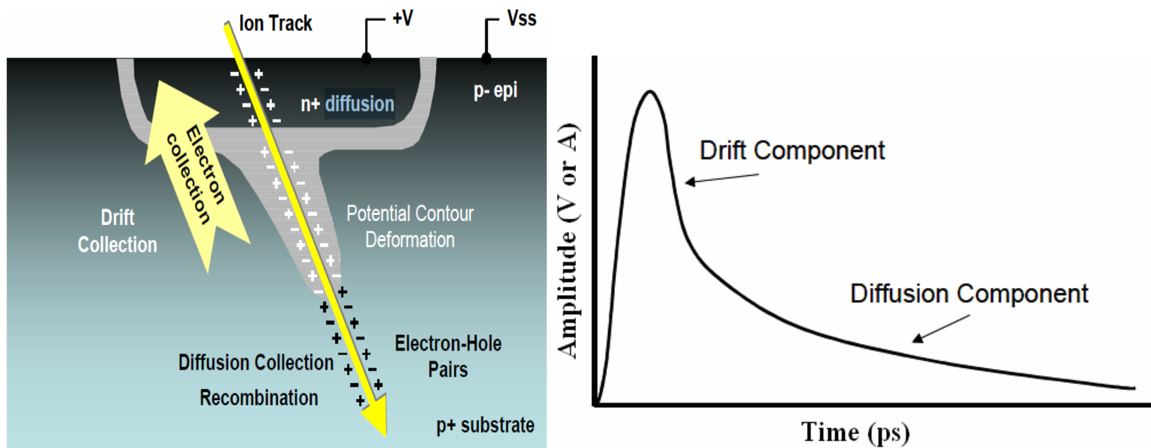


Figure 6. a) Visualization of ion strike at reverse-biased n+/p junction. b) Example of voltage amplitude vs. time for ion strike; drift and diffusion components displayed. From [17], [18].

The created electron-hole pairs at the onset of an ionizing particle strike are initially collected by the electric field created by depletion regions within the device. This drift current results in a concurrent distortion or debiasing of the original potential at the struck p / n junction, and a funnel-like contour of the depletion region is formed along the incident particle's strike path (Figure 6). This extension of the depletion region into the substrate greatly affects the device's ability to collect excess charge via drift. This

drift component is the dominating mechanism in determining the height of the initial transient pulse and can be modulated through variations in either the device's supply voltage or connected load. As the initial potential contour at the depletion region begins reforming, the shape of the transient pulse begins to be dominated by diffusion of additional excess carriers into the depletion region. This process continues until all excess carriers have been collected, recombined, or diffused away from the junction area and is responsible for the rate of falloff in the single-event transient response. The diffusion process is typically much slower and results in an overall lower amount of collected charge than the drift process [17]-[18].

2.3.2 Single-event Transient Simulation Setup

Single-events were generated in the 3-D models using the built-in heavy ion function present in the Synopsys TCAD tools [19]. The heavy-ion strike centered at a location about 0.1 um away from the center of the drain toward the gate at normal incident angle. As the depth of the silicon cube was chosen as 10 um, the length of the heavy-ion track was chosen as 11 um to extend fully through the depth of the substrate. The LET values of the simulated heavy ions were 10, 30, or 50 MeV-cm^2/mg. This initial characterization was performed over drain bias voltages of 0.3V, 0.9V, and 1.8V with varying drain resistor loads (R_{LOAD}) of 10Ω, 1 kΩ and 10 kΩ. All other terminals were held at ground to create the single reverse-biased junction at the device drain, as seen in Figure 6 below. Current at the drain of the device was monitored before, during, and after the strike. Resulting current transients at the drain were recorded to establish general single-event current trends based on drain load, supply voltage, and LET. Each

resulting current transient was then integrated with respect to time for comparison of total charge seen at the drain terminal. The following graph displays the mechanisms generally responsible for the overall shape of a current or voltage pulse due to a single-event transient.

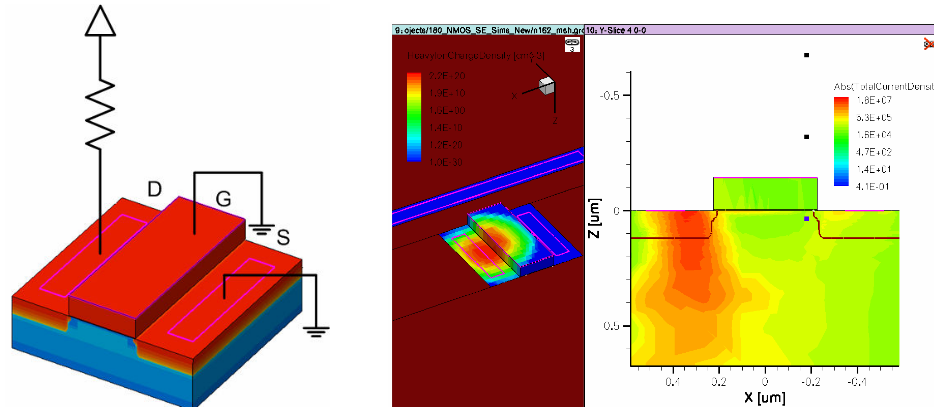


Figure 7. a) 3-D analog / mixed-signal single simulation device. b) Visualization of heavy ion strike at drain of NMOSFET.

Note: For graphing purposes, all following PMOSFET current response curves in Section 2.3 represent the ***absolute value*** *of the actual measured responses. The true PMOSFET current responses are actually of "negative" value, as opposed to the NMOSFET current responses which are presented in their original "positive" current orientation.*

2.3.3 Transient Simulation Results - Drain Current vs. Drain Load

The shape and duration of single-event current pulses are understood to be strong functions of the load connected to the struck device. Both the height of the initial pulse immediately following the strike and the presence and duration of a generated current plateau are affected by the load. In fact, the pull-up or pull-down device / load connected to the struck NMOS or PMOS device plays the most important circuit-level role in determining the resulting SET drain current pulse shape [14]. For this set of simulations, the heavy ion strike LET was held constant at a high 50 MeV-cm^2/mg and drain bias at full-rail 1.8V or -1.8V for the NMOS and PMOS devices, respectively.

The SET response of the virtually unloaded (10Ω resistor load) NMOS device follows the typical double exponential shape characteristic of struck CMOS devices: a sharp peak at around 5-10 ps after the strike followed by a steep fall-off and long tail beginning less than half of a nanosecond later. Increasing the drain load to 1kΩ results in the formation of a current "plateau," a region of the response characterized by a sustained or very slowly decaying current at an almost constant amplitude, typically beginning around 10-15 ps following the initial strike. Figure 7(b) clearly displays the plateaus and the expected trend associated with increasing the load from 10 Ω to 1 kΩ and 10 kΩ, namely lower current but greater plateau width. While the drain voltage falls lower for the heavily loaded case than the moderately loaded case (Figure 7(c)), the drain current peeks at a lower value due to the reduced pull-up drive provided by the 10 kΩ load resistor.

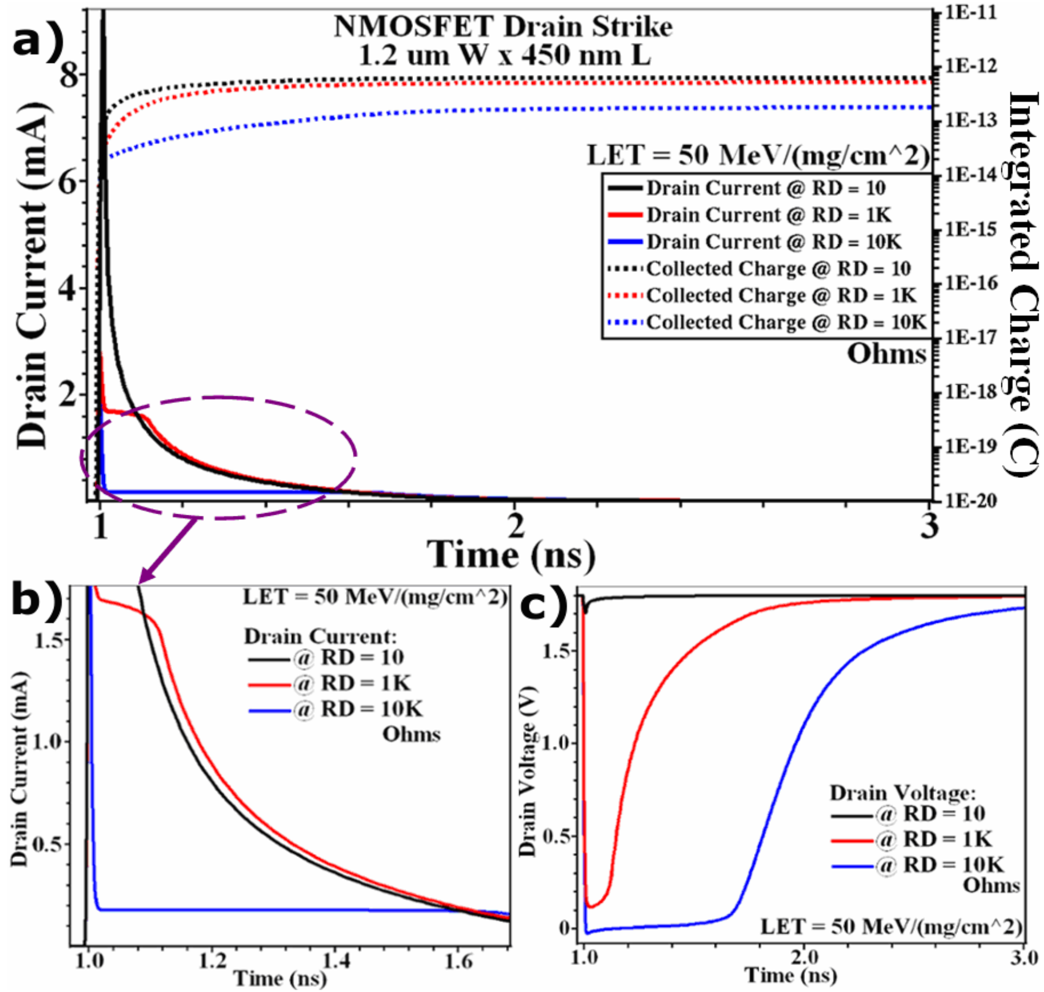


Figure 8. Single-event strike profile for NMOS device – W: 1.2 µm x L: 450 nm – with varying drain resistor load. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. LET = 50 MeV-cm^2/mg; VDD = 1.8V; R_D = 10 Ω, 1K Ω, 10K Ω.

As expected, the heavy ion strikes simulated on the PMOS device resulted in much more apparent current plateaus and greater amounts of overall integrated charge than in the NMOS device strikes. Previous research at the 90 nm node suggests this to likely be a result of bipolar amplification effects found in deep submicron technology [14]. As with the NMOS device, the rise in drain load from 1 kΩ and 10 kΩ forces the plateau to form at a lower current level, which is to be expected.

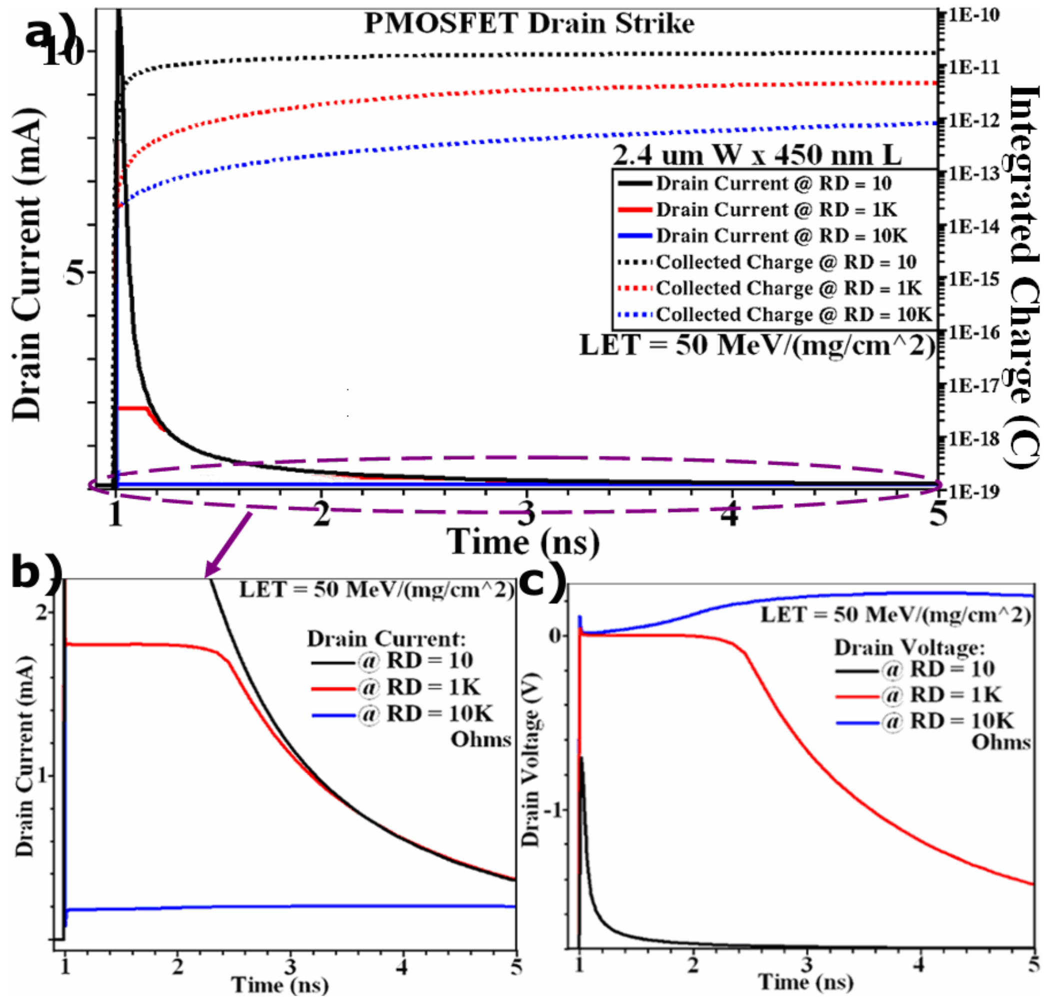


Figure 9. Single-event strike profile for PMOS device – W: 2.4 μm x L: 450 nm – with varying drain resistor load. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. LET = 50 MeV-cm^2/mg; VDD = 1.8V; R_D = 10 Ω, 1K Ω, 10K Ω.

It can be observed in both the NMOS and PMOS devices that while the heights of the transient amplitude and current plateau vary across device load, the rate of drain current falloff is approximately equal in each case. Indeed the width of each loaded device's transient response seems approximately "bounded" by the unloaded device's response. This suggests that the rate of current falloff near the end of the pulse depends almost purely on the charge diffusion mechanism, rather than drift, and is not a strong function of the attached load. Instead, the falloff is likely a function of device doping and

the amount of excess charge deposited within the substrate outside of the original junction depletion region [17]-[18].

2.3.4 Transient Simulation Results - Drain Current vs. Supply Voltage

As seen in the following images, the effects of varied supply voltage are very similar to the effects of varying the connected drain load. For this set of simulations, the heavy ion strike LET was held constant at 50 MeV-cm^2/mg and drain resistance at 1 kΩ while the supply voltage was varied among 0.3V, 0.9V, and 1.8V.

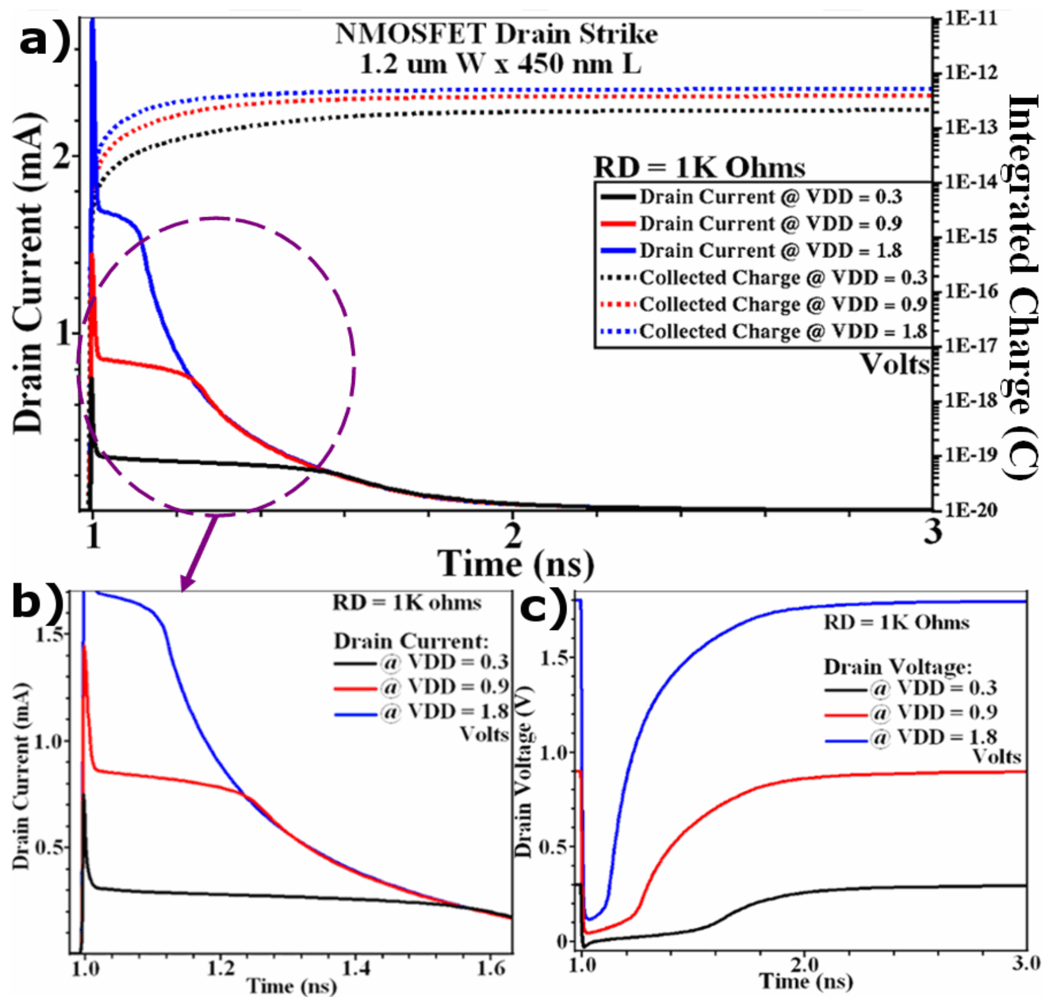


Figure 10. Single-event strike profile for NMOS device – W: 1.2 µm x L: 450 nm – with varying strike LET. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. LET = 10, 30, and 50 MeV-cm^2/mg; R_D = 1K Ω; VDD = 0.3V, 0.9V, and 1.8V.

The widths of the resulting current plaeaus reduce heavily as VDD is increased from 0.3V to 0.9V and 1.8V. This makes sense as the applied bias, along with the connected load, determines the amount of restoring current provided to the struck device. Hence, with increased bias comes increased restoring current and therefore shorter SET current plateaus. In fact, this particular set of simulations would suggest that a 50% reduction in VDD from 1.8V to 0.9V nearly doubles the width of the observed current plateau. Further reducing VDD to 0.3V results in a current plateau about five times the width of the original.

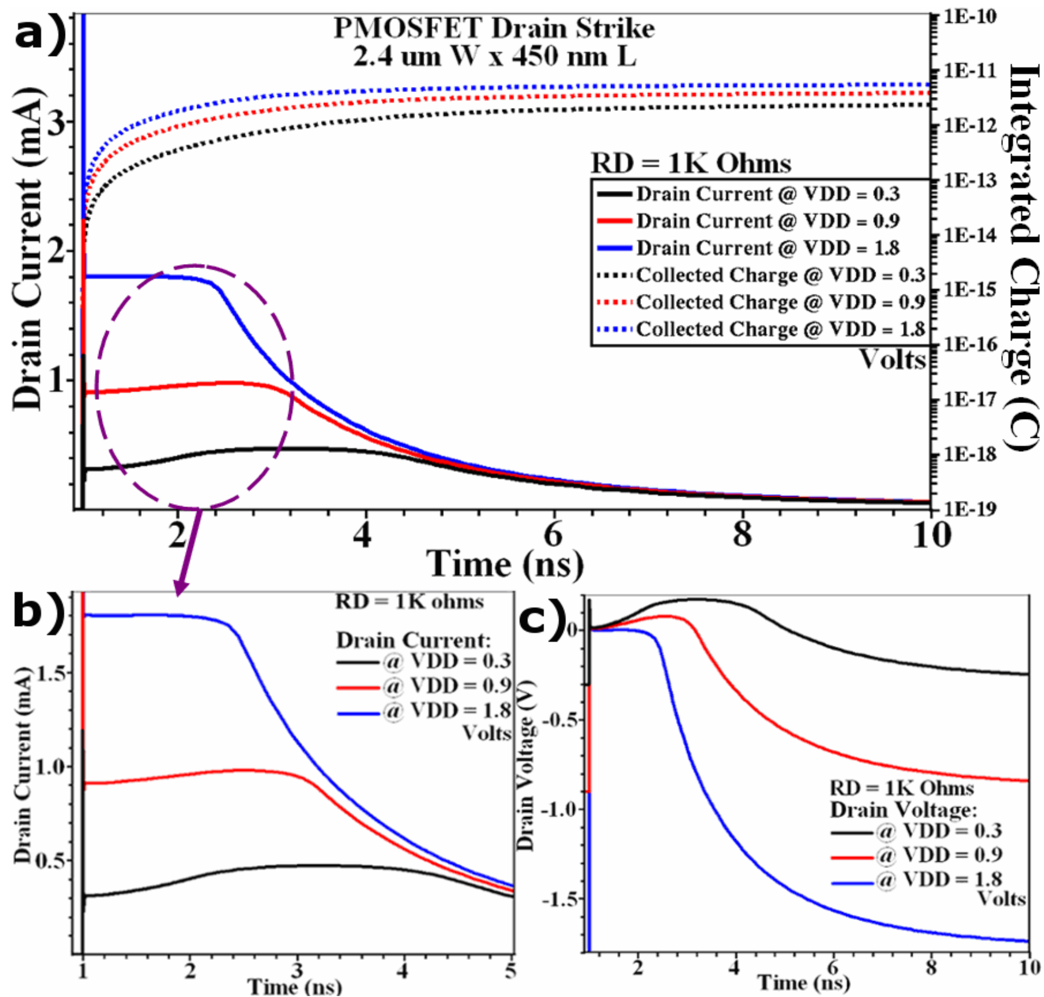


Figure 11. Single-event strike profile for PMOS device – W: 2.4 µm x L: 450 nm – with varying strike LET. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. LET = 10, 30, and 50 MeV-cm^2/mg; R_D = 1K Ω; VDD = 0.3V, 0.9V, and 1.8V.

The corresponding PMOSFET device strikes produced very similar results (Figure 12). Again, the same overall pulse shapes are maintained in comparison to the NMOSFET strikes even though they are significantly longer, a trait typically contributed to bipolar amplification in PMOSFET devices.

As observed in the results of varying device load (Section 2.3.3), the rate of falloff near the end of each simulation's current response appears approximately equal across supply voltage. This is further evidence that this region of the response is not a strong function of the external circuitry's restoring current which is altered by either changes in supply voltage or the connected load. Instead, this region of the response again appears to be dominated by the diffusion of excess charge from the substrate into the recovering junction's depletion region, a mechanism appearing dependent only on device doping and the amount of charge deposited in the substrate [17]-[18].

2.3.5 Transient Simulation Results - Drain Current vs. Heavy Ion LET

Varying the simulated incident ion's LET produced less drastic changes in the shape of the resulting SET pulse from value to value than did variances in the applied load. Below are the results of strikes on both NMOS and PMOS devices. For this set of simulations, the load on the drain of the NMOS and PMOS devices was held at a constant 1kΩ resistance. VDD was held at full-rail 1.8V or -1.8V for the NMOS and PMOS devices, respectively. The LET was varied among three different values: 10, 30, and 50 MeV-cm^2/mg.

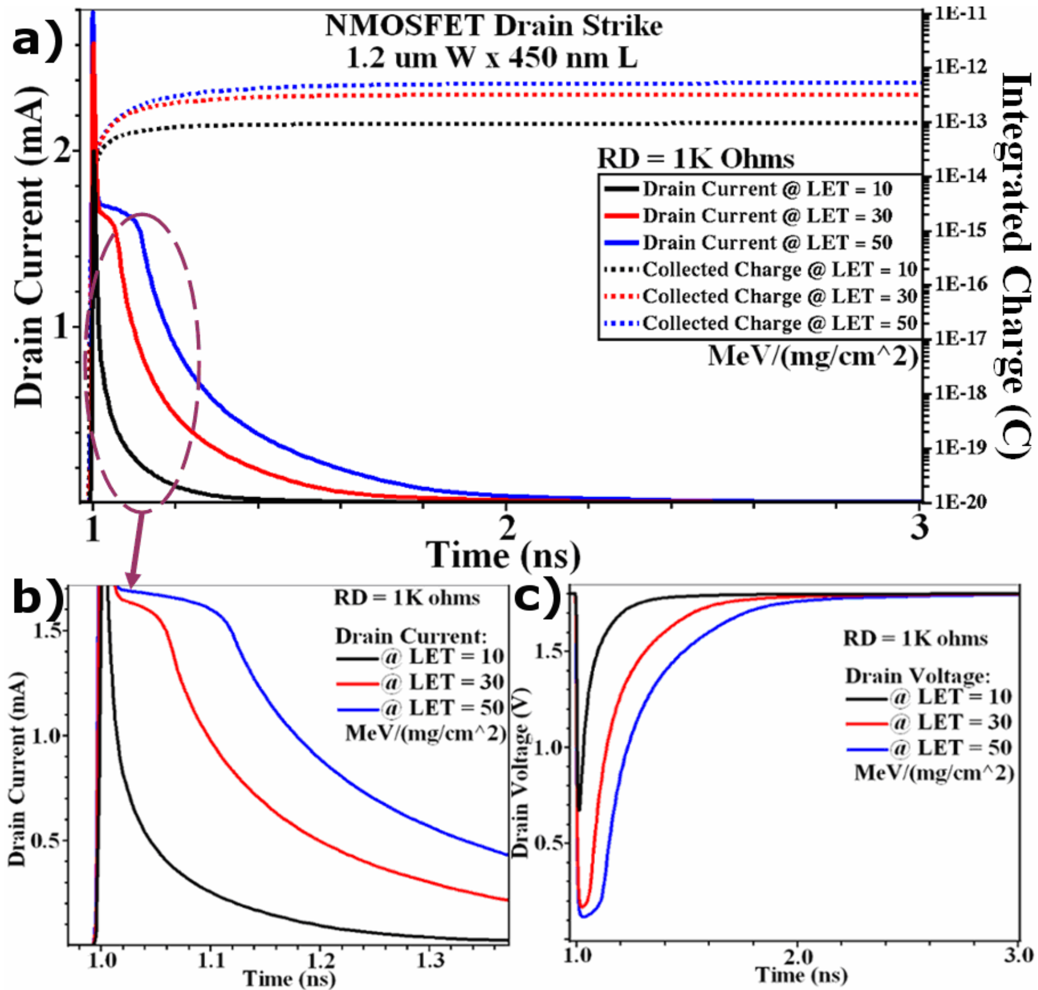


Figure 12. Single-event strike profile for NMOS device – W: 1.2 µm x L: 450 nm – with varying strike LET. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. VDD = 1.8V; R_D = 1K Ω. LET = 10, 30, and 50 MeV-cm^2/mg.

In the case of the NMOS device, no current plateau was seen for the LET of 10 MeV-cm^2/mg: the resulting SET pulse seemed to follow the standard double exponential shape once again (Figure 9(a) and (b)). However, the plateau began visibly forming as LET increased to 30 and 50 MeV-cm^2/mg.

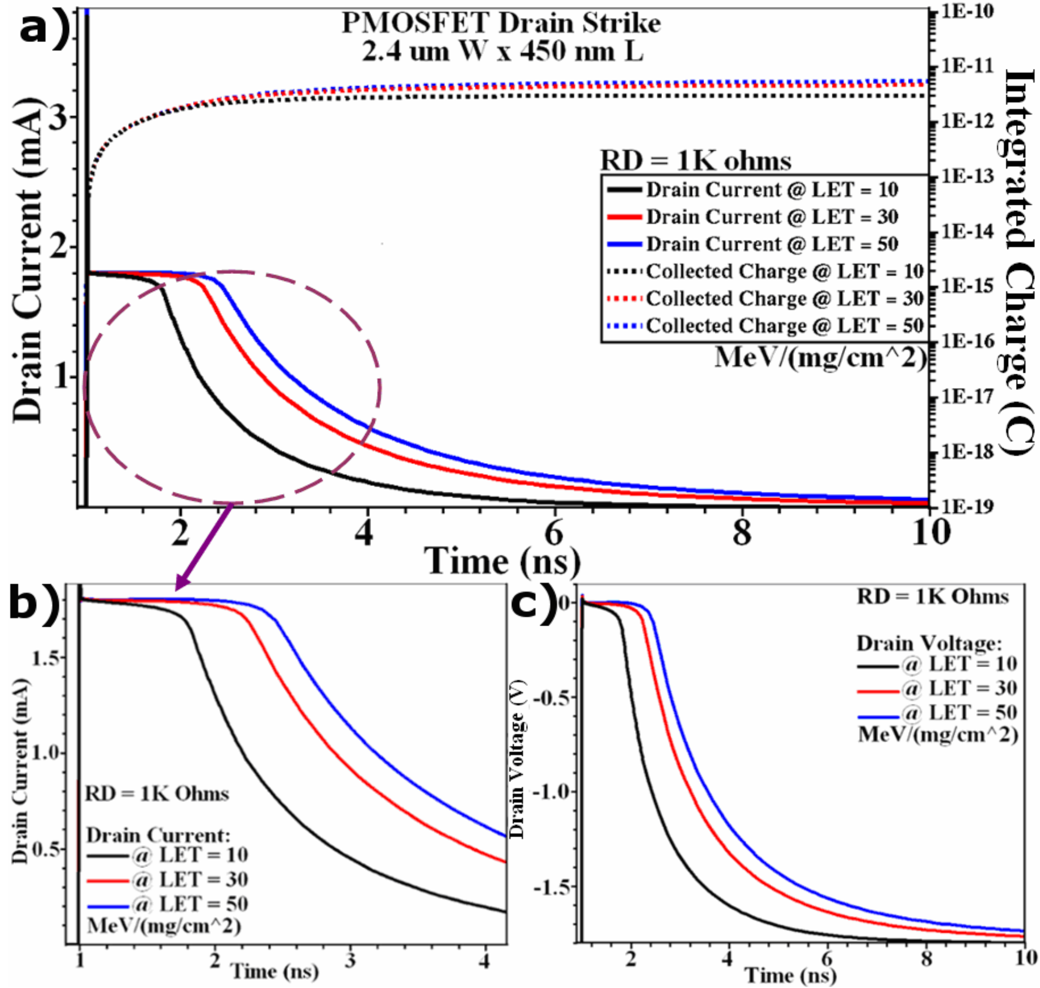


Figure 13. Single-event strike profile for PMOS device – W: 2.4 µm x L: 450 nm – with varying strike LET. a. and b.) Drain current vs. time and collected charge vs. time; c.) drain voltage vs. time. VDD = 1.8V; R_D = 1K Ω. LET = 10, 30, and 50 MeV-cm^2/mg.

Again it is obvious that PMOS device strikes result in higher maximum SET currents and much longer pulse widths than NMOS device strikes. Current plateaus form for all three given LETs, and the resulting SETs do not fully dissipate even up to 10 nanoseconds after the initial ion strike. These simulations suggest a high SET vulnerability for PMOS devices in this technology with pulse widths near and greater than 1 ns occurring regularly.

In contrast to variations in supply voltage and connected load, varying the LET does not result in transient pulses that recover at approximately the same time following

the strike. While the ability of the external circuitry to provide restoring current is held constant, the amount of excess created charge near the sensitive junction increases with LET, resulting in an extended current plateau as charge is swept to the drain contact via drift. As more charge is also deposited with increased LET in the substrate outside of the depletion region, more charge must also be collected via diffusion once the electric fields begin relaxing to their initial states. Therefore, a longer falloff current is also observed with increasing LET.

CHAPTER III

SINGLE-EVENT LATCHUP SIMULATION SETUP

As with the single-event transient characterization of the IBM 180 nm technology, simulations to analyze the latchup susceptibility of the process were performed using Synopsys TCAD tools' heavy-ion strike function. While it would have been ideal to perform all latchup simulations on full 3-D TCAD models, the amount of time required to perform the large array of simulations was not feasible. In fact, most latchup simulations performed on a 3-D TCAD minimally spaced inverter failed to complete within the time allowed on Vanderbilt's ISDE computing cluster. The solution to time and resource constraints came in the form of 2-D TCAD models representative of industry standard test structures. As it has been demonstrated that first-order latchup susceptibility predictions follow the same qualitative trends in both 2-D and 3-D TCAD simulations, this solution was practical as it allowed most simulations to complete in less than 30 minutes each instead of days [8]-[9], [11]. Descriptions of the simulation procedures follow along with presentations and explanations of the simulated latchup structures.

3.1 2-D TCAD Standard Latchup Simulation Structure and Procedure

The 2-D structure illustrated in Figure 13 is a slightly modified version of the structure originally presented by Mavis et. al. (Figure 2) and was the baseline structure utilized in all of the performed latchup simulations. It consists of two primary

diffusions—a p+ diffusion and an n+ diffusion—positioned in an n-well and a p-well, respectively, along with a single contact diffusion for each well [7]. All diffusions were created in a p-type substrate, and shallow trench isolation was present to a depth of 0.36 μm across the structure where diffusions were not defined. All doping profiles for diffusions, wells, and the substrate match those of the standard NMOS and PMOS devices presented in Chapter II.

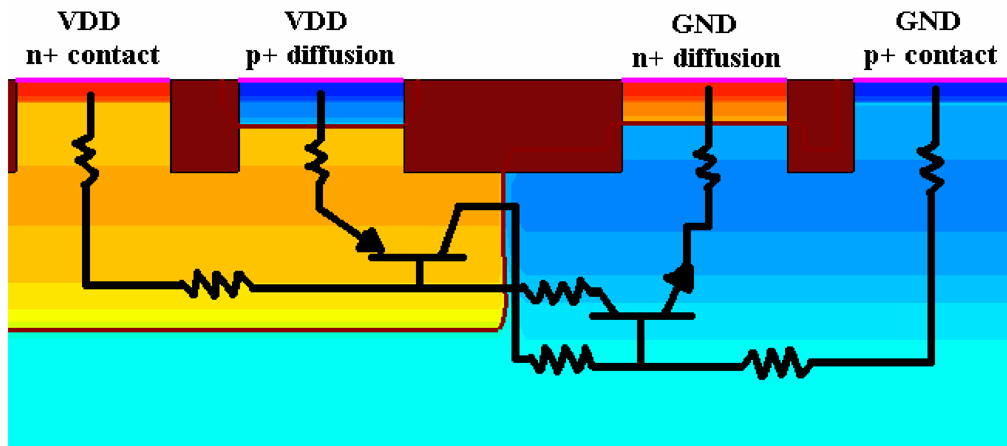


Figure 14. 2-D CMOS latchup test structure. Parasitic BJT and resistance paths superimposed. After [7].

Simulations utilizing this structure were performed with VDD bias values of 1.8V and 5.0V applied at the n-well contact and p+ diffusion as seen in the above figure. Heavy ion strikes were simulated at the center of each of the four implants. LET for the strikes was varied among eight values: 3, 5, 10, 15, 20, 25, 30, and 50 MeV-cm^2/mg. The angle of incidence varied among three values: 0°, 45°, and 60° from normal incident toward the n-well / p-well junction at the center of the substrate. Temperature was held at a constant value of 125°C (398K), or about 100° above room temperature. Total simulation time for each combination of variables was 300 ns to allow sufficient time to identify latchup.

There are numerous mitigation techniques that have been applied to the structure in Figure 13 in attempt to reduce its susceptibility to latchup. Some techniques have proven more promising or viable than others due to effectiveness and/or ease of implementation within a process. The effectiveness of three such techniques was analyzed through simulation in this study. To do this, each combination of bias, LET, and heavy ion incidence angle was also simulated along with one, both or neither of two mitigation techniques—the inclusion of a highly doped p+ buried layer and the inclusion of a highly doped n+ guard structure. The third mitigation technique, the inclusion of a triple-well NMOS variant, was simulated at each LET and incidence angle while VDD was held at 5.0V bias. No guard structure was included in the triple-well simulations. Further details and illustrations of each structures follow.

3.2 2-D TCAD Latchup Structure with Added Deep-p+ Buried Layer

The use of deep-p+ buried layers has long been studied as a method of CMOS latchup prevention [20]-[22]. It functions to reduce the resistivity of the substrate area just beneath the active devices, therefore reducing the potential voltage drop at the n-well / p-substrate junction. The buried layer also works to truncate the vertical depth of charge collection due to a single-event as the carrier lifetime of the introduced excess charge is reduced in the higher doped p+ region. This limits the diffusion length of the charge [10], [23]-[24].

While the inclusion of a deep-p+ buried layer is inherent in the IBM 180 nm process, this does not hold true for all other processes including the Texas Instruments (TI) 180 nm process which has been previously analyzed [11], [25]. Therefore,

simulations on the standard latchup structure in Figure 13 were performed with and without the inclusion of the buried layer (Figure 14) to ascertain its effectiveness at this technology node.

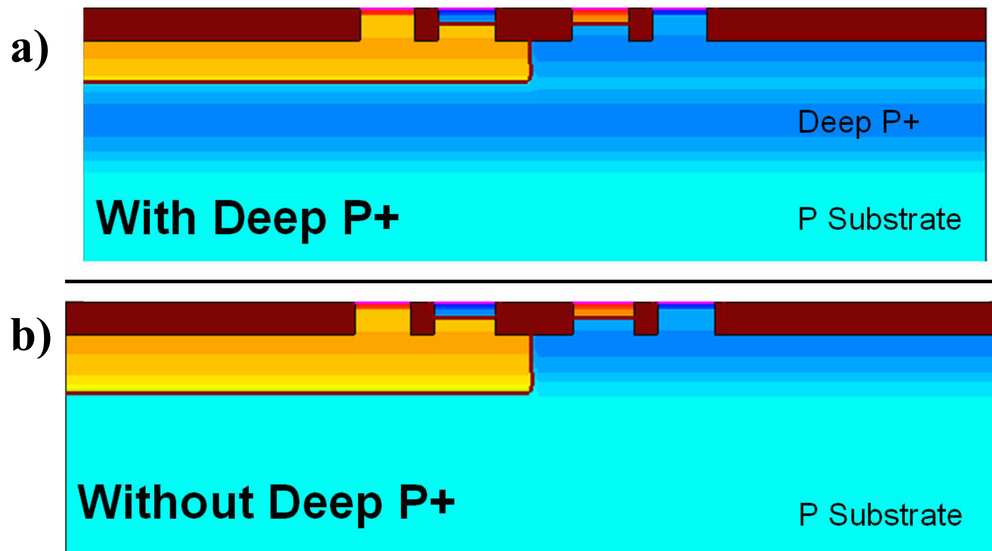


Figure 15. a). 2-D TCAD structure without deep-p^+ buried layer. b). 2-D TCAD structure with deep-p^+ buried layer (dark blue region beneath the yellow n-well).

3.3 2-D TCAD Latchup Structure with Added Guard Diffusion

The addition of guard rings to latchup-susceptible devices has become an industry standard for many heavy ion rich environment applications. Guard rings assist in latchup mitigation by providing an increased amount of contact space to the power supply rail over standard contacts, leading to increased collection of injected charge away from sensitive structure junctions [26]-[27]. PMOSFET guard rings are essentially created by "stretching" the n-well contact around the perimeter of the device. While this is easily done in a 3-D TCAD model, it is physically impossible in a 2-D model. Therefore, a second n+ diffusion identical to the n-well contact was added adjacent to the p+ diffusion and opposite the original n-well contact in the n-well. This added guard diffusion, visible

in Figure 15, provides adequate simulation of a true guard ring as the p+ diffusion is surrounded on all sides by n+ diffusions as it would be in a fully 3-D model.

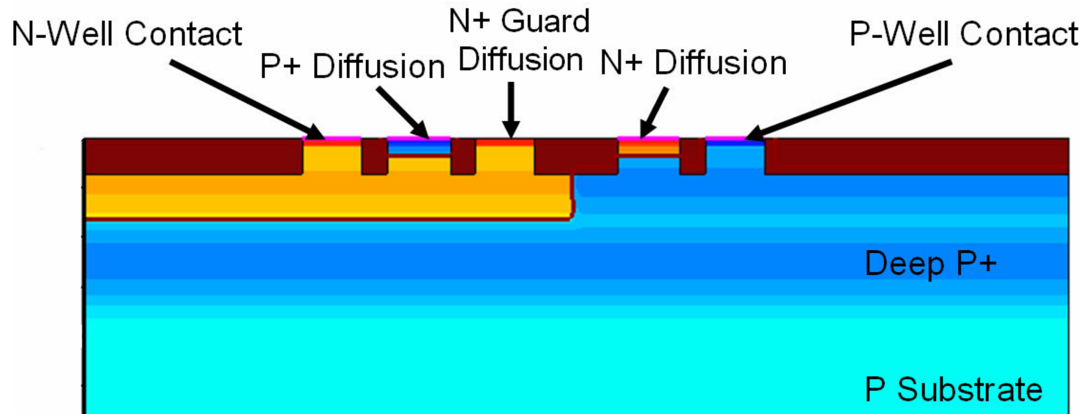


Figure 16. 2-D TCAD latchup structure with added guard diffusion

3.4 2-D Triple-well Latchup Structure with Non-connected and Connected N-wells

Triple-well devices are commonly used to electrically isolate NMOS devices from PMOS devices and the p-type substrate, therefore disabling the turn-on of the n-p-n parasitic BJT created by the n+ diffusion, the p-substrate, and the n-well. The standard triple-well NMOS device Figure 16(a) features an added n-well beneath the standard p-well which "blocks" the n-p-n path at the cost of added real estate requirements for NMOS devices. This is because the IBM 180 nm design rules state that the additional n-well must be spaced a minimum 0.8 μm from the original n-well housing the p+ diffusion.

However, the design rules also indicate that two n-wells may be connected to, or butted against, one another if held at the same potential. This rule includes the n-well of a triple-well device and the n-well housing a PMOS device, the combination of which would greatly reduce the real estate and spacing demands of a triple-well device. Therefore, the structure in Figure 16(b) was created by connecting the two n-wells of the

original structure. This effectively reduced the required spacing between each device to only 0.8 µm, the minimum spacing between a p-type diffusion and an n-type diffusion.

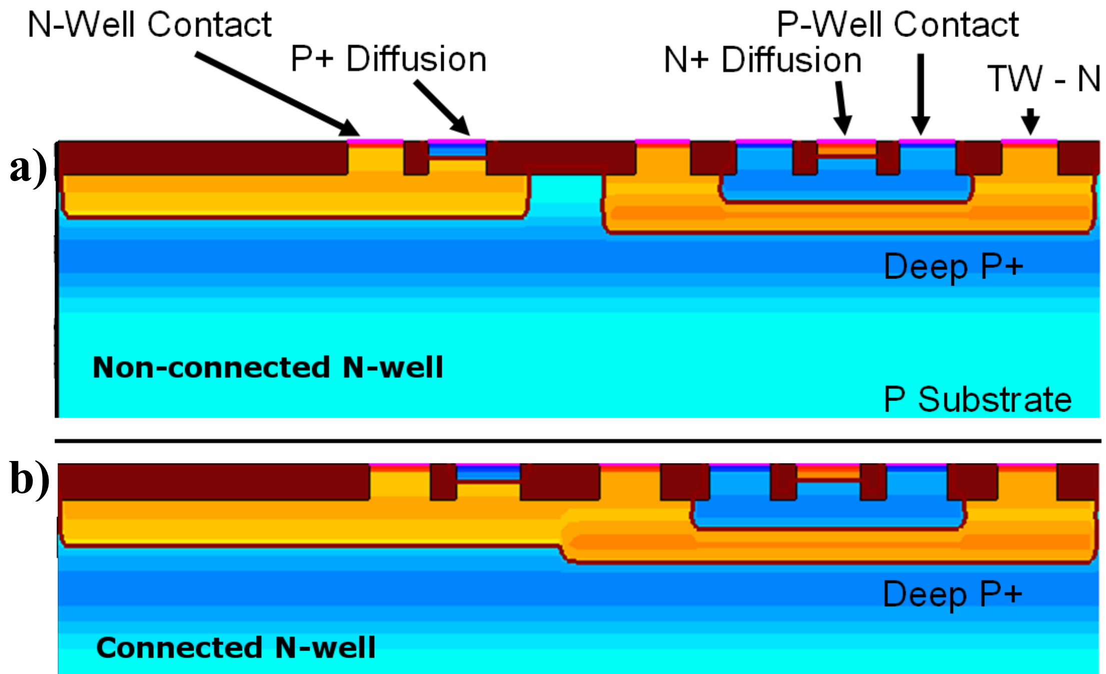


Figure 17. Triple-well latchup structure with a) non-connected n-wells and b) connected n-wells.

Heavy ion simulations were performed on both configurations in order to determine if the connected n-well altered the latchup susceptibility of the triple-well structure. Unlike the other structures, simulations on the triple-well devices were performed at only the 5.0V bias as they have historically proven to be resistant to latchup at nominal bias [28]-[30].

CHAPTER IV

SINGLE-EVENT LATCHUP SIMULATION RESULTS

The current at both the n+ diffusion and the p+ diffusion contacts was monitored and recorded before, during, and after each heavy ion strike. Following each strike, if the currents at both the n+ diffusion contact and the p+ diffusion contact were sustained at almost equal and opposite levels without dissipating to zero over time, single-event induced latchup was determined to have occurred. However, even if the currents were not sustained, one or both of the parasitic BJTs may have still turned-on, and any extended resulting pulse widths at the contacts were recorded to identify the overall potential effects of the BJTs. Figure 17(a) illustrates the circuit representation of the cross-coupled BJT structure from Figure 13 along with current monitors placed at those two diffusions. An example of current pulses recorded at these monitors is pictured in Figure 17(b), wherein both sustaining and non-sustaining currents are depicted for strikes at the n+ diffusion and p+ diffusions for LET values of 20 and 50 MeV-cm^2/mg.

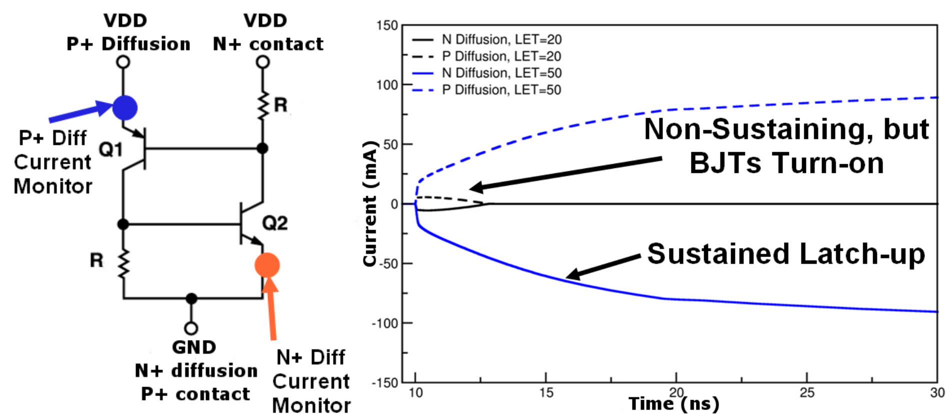


Figure 18. a) Circuit representation of cross-coupled parasitic BJTs along with current monitored sites at the p+ and n+ diffusion contacts. b) Example of resulting current pulses, both sustained latch-up current and non-sustaining current with BJT turn-on.

4.1 1.8V VDD Bias Heavy Ion Strike Results

The heavy ion strikes resulted in no latchup conditions in any 1.8V bias TCAD simulations regardless of strike location and angle or inclusion of mitigation techniques. However, results show that the parasitic BJTs did turn-on provided a high enough LET and angle of incidence even though the currents produced were not sustained indefinitely. Figure 18 presents an example of the resulting pulses recorded at the p+ and n+ diffusion contacts for a simulated heavy ion strike at the p+ diffusion with and without a deep-p+ implant and no added guard structure. The strikes displayed had LET values of 20 and 50 MeV-cm^2/mg.

While large current pulses on the order of milliamp magnitudes and nanosecond widths are prevalent for the 1.8V bias structures for most combinations of LET, incident angle, and mitigation, no latchup was seen for any simulation. In comparing Figure 18(a) to 18(b), the limit of the deep-p+ implant's effectiveness as the only present latchup mitigation technique is clearly observed. For example, for a strike with LET value of 20 MeV-cm^2/mg the buried layer decreased the amplitude of the resulting current by approximately 50% from about 2.3 mA to 1.1 mA and the resulting pulse width by 33% from 1.5 ns to about 1 ns. However, no significant difference in either pulse width or amplitude of the output currents was seen for the case of the 50 MeV-cm^2/mg LET value. Regardless, the deep-p+ layer is still standard in most current technologies due to its moderate effectiveness and ease of inclusion in fabrication [20]-[22].

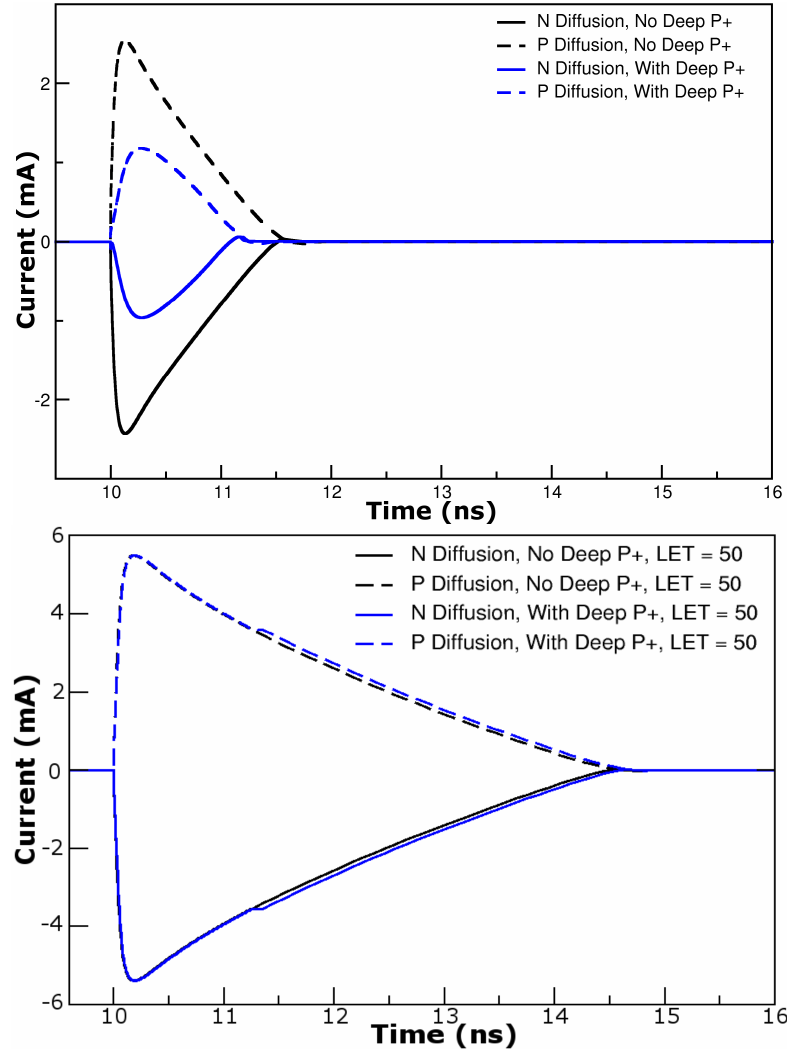


Figure 19. P+ diffusion 45° heavy-ion strike on latchup structure with and without Deep-P+ implant and no guard structure. Resulting current pulses vs. time recorded at p+ and n+ diffusions. a) LET = 20 MeV/mg/cm^2, b) LET = 50 MeV/mg/cm^2. 1.8V VDD bias.

These results differ greatly from the results of previous research performed at the 180 nm technology node. Whereas previous work reports substantial latchup vulnerability for this node, no latchup was observed for the 1.8V supply voltage in the study described in this thesis. These large discrepancies in vulnerability are attributed to the significant differences among various 180 nm processes. As explained in Section 1.4, differences in doping levels, structure spacing, isolation depth, and inclusion of a highly doped buried layer strongly alter a technology's latchup vulnerability. The IBM 7RF

process seems to vary significantly from the processes utilized in previous studies and is therefore likely to result in distinctly different latchup susceptibility at least at the core 1.8V supply voltage.

4.2 5.0V VDD Bias Heavy ion Strike Results

Unlike the 1.8V bias case, the 5.0V bias case proved to be far more susceptible to SEL. In fact, many 5.0V bias structure simulations showed latchup at a LET value of 20 MeV-cm^2/mg, a value only 40% of the maximum LET simulated. Figure 19 displays resulting current pulses from a heavy ion strike at the p+ diffusion with 5.0V bias and LET values of 20 and 50 MeV-cm^2/mg. This is in direct comparison to the simulations of Figure 18 wherein devices were biased at 1.8V VDD.

Figure 19 shows a clear latchup result as the currents at both diffusions (both black lines) increase indefinitely beyond the time of the strike occurring at 10 ns. As previously noted, while the plot's timescale extends only 20 to 40 ns after the strike occurred, total simulation time was 300 ns. The truncated timescale allows both the sustaining and non-sustaining current pulses to be highlighted on the same graph.

The limit of the deep-p+ implant's effectiveness can again be clearly seen when comparing Figure 19(a) to 19(b). When LET was limited to 20 MeV-cm^2/mg, the buried layer prevented latchup and limited the current pulse width to about 2.5 ns. However, as with the 1.8V bias case, no significant mitigation was accomplished by the inclusion of the buried layer for the high LET of 50 MeV-cm^2/mg.

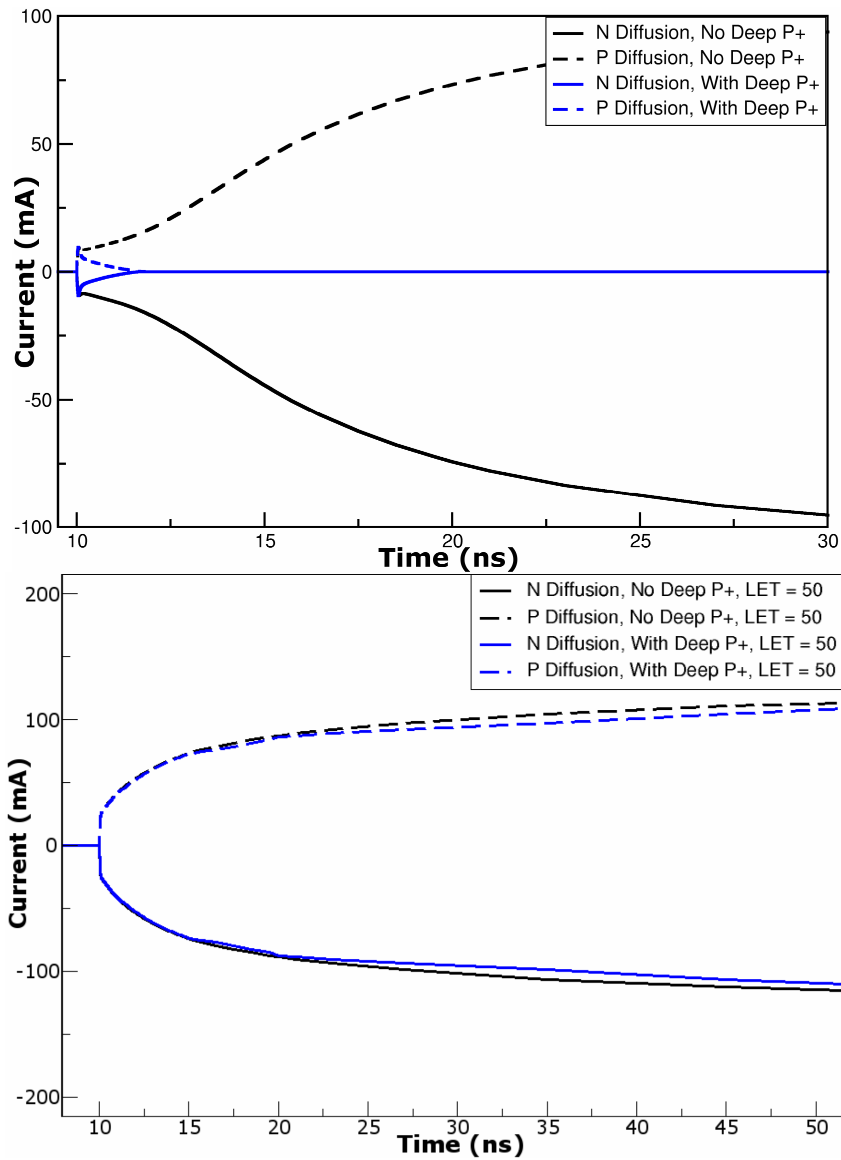


Figure 20. P+ diffusion 45° heavy-ion strike on latchup structure with and without Deep-P+ implant and no guard structure. Resulting current pulses vs. time recorded at p+ and n+ diffusions. a) LET = 20 MeV/mg/cm^2, b) LET = 50 MeV/mg/cm^2. 5.0V VDD bias.

Note: As no latchup was seen at 1.8V VDD, all following strike results in this chapter are representative of structures biased at 5.0V VDD.

4.2.1 Heavy-ion strike results on guarded structure (5.0V VDD)

The guard structure proved to have similar results to those of the deep-p+ buried layer. Figure 20 displays the results of strikes at both the p+ and n+ diffusions with an added guard structure surrounding the p+ diffusion in the n-well as depicted in Figure 15.

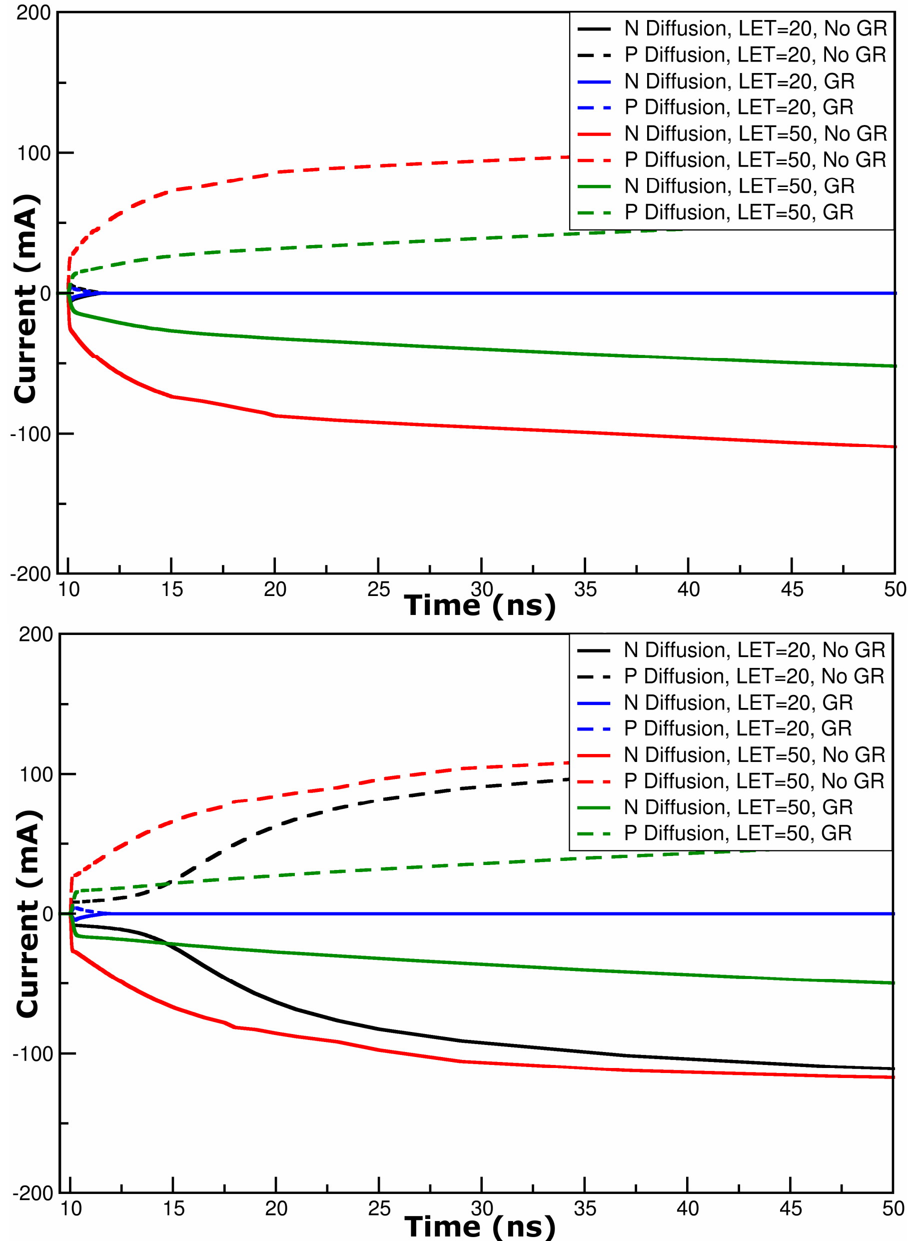


Figure 21. 45° heavy-ion strike on latchup structure with Deep-P+ implant, with and without guard structure at **a)** n+ diffusion and **b)** p+ diffusion. Resulting current pulses vs. time recorded at p+ and n+ diffusions. LET = 20 and 50 MeV/mg/cm^2. 5.0V VDD bias.

From both figures it can be concluded that the guard structure is effective in reducing both the width and the amplitude of the resulting current pulses at the monitored contacts. This is most evident in Figure 20(b) wherein the addition of the guard structure prevented latchup at a LET of 20 MeV-cm^2/mg for the strike at the n+ diffusion whereas latchup was seen without it. Also, while the structure continued to consistently latch for a LET value of 50 MeV-cm^2/mg, the amplitudes of the resulting pulses were reduced by about 50% by inclusion of the guard structure from the cases without a guard structure. This was approximately true for all strikes in which the guard structure was included. Overall, the guard structure proved to be effective in removing charge from the latchup path but not enough to consistently mitigate SEL at 5.0V VDD bias.

4.2.2 Heavy-ion strike results on triple-well device structure (5.0V VDD)

Latchup simulations were first performed on the standard “non-connected n-well” triple-well structure to verify its radiation-hard by design topology. Next, simulations were performed on the “connected n-well” topology to determine its practicality as a space saving technique. The following images (Figure 21) display the results of these simulations.

The plots in Figure 21 verify that the triple-well structure mitigated the SEL phenomenon completely as designed with the worst-case result showing only current at a single diffusion, not both as would be required to trigger latchup. While these plots display the results of strikes at LET value 20 MeV-cm^2/mg, it was verified that no latchup trends were seen at any LET up to 50 MeV-cm^2/mg whether the standard n-well structure or the connected n-well structure was used. Also, neither structure showed

significant difference in latchup susceptibility. Therefore, the connected, or butted, n-well method seems effective in this particular technology and occupies less area than the non-connected n-well configuration.

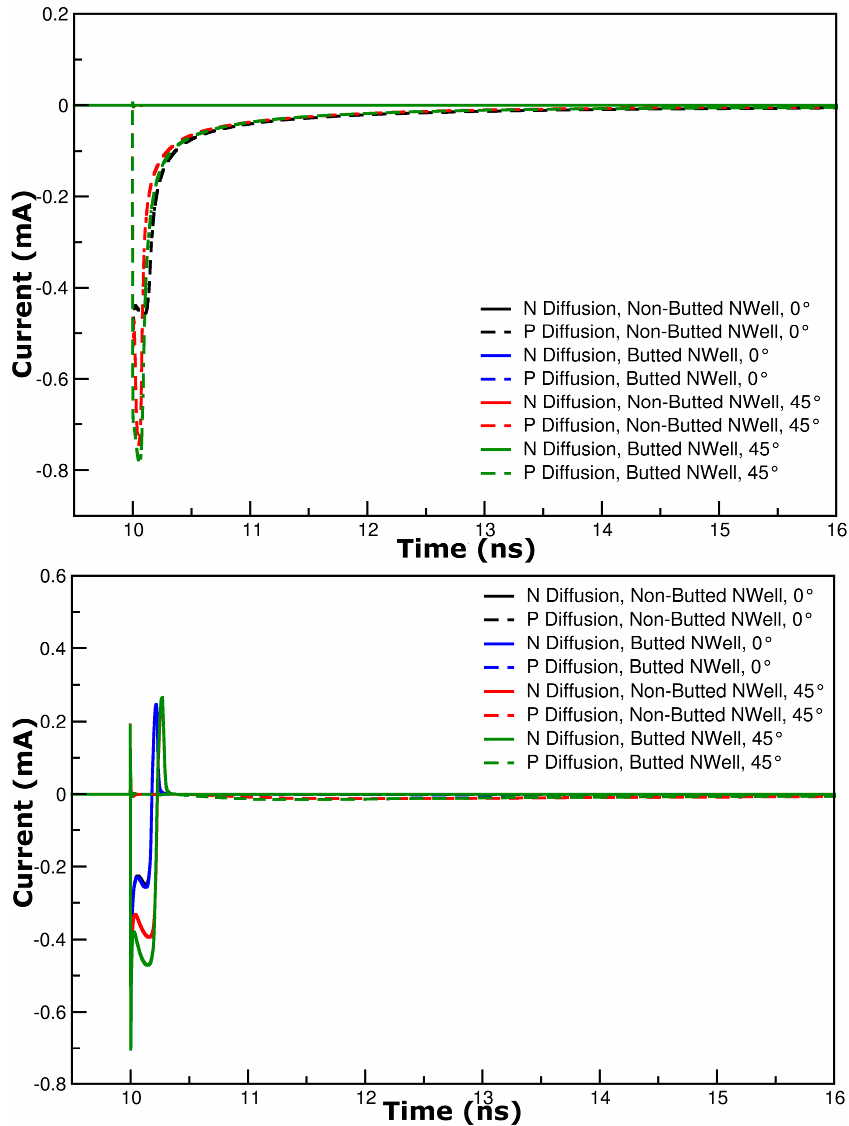


Figure 22. **a)** p+ diffusion strike. **b)** n+ diffusion strike. 45° heavy-ion strike on triple-well latchup structure with Deep-P+ implant. Resulting current pulses vs. time recorded at p+ and n+ diffusions. LET = 20 MeV/mg/cm^2. 5.0V VDD bias.

4.3 Results Discussion

As expected, variations in VDD bias, strike location, incidence angle, LET, and mitigation technique inclusion provided varying magnitudes and lengths of current pulses at the monitored contacts following a heavy ion strike. Notable trends in the technology's latchup susceptibility due to these variables were observed and are presented here. While some results may appear in truncated form for presentation here, full results for strikes at each diffusion and well contact are presented in table form in the Appendix.

4.3.1 Worst-case Strike Location—p+ Diffusion

Throughout the latchup simulations in this study, the most sensitive strike location proved to be the p+ diffusion in the n-well. While latchup was only seen for the 5.0V bias case, the BJT turn-on was triggered for every strike at this location, regardless of incident angle and 1.8V or 5.0V VDD bias. This did not hold true for all other diffusions as many strikes resulted in current pulses at only one of the two monitored diffusions rather than both.

Table 1 (below) summarizes the results of the strikes at the p+ diffusion location for both 1.8V and 5.0V bias. The table is divided into four sections, one for each possible combination of mitigation techniques, to allow for the analysis of their respective abilities to mitigate latchup at this technology node. The latchup trends for this structure at 5.0V bias are readily visible in this table. For example, the deep-p+ implant, when added to the standard structure in Figure 13, increased the critical LET to cause latchup from 20 to 25 MeV-cm^2/mg at a 60° incident angle while the guard structure was unable to clearly mitigate latchup alone. However, the inclusion of both the

deep-p+ implant and the guard structure increased the critical LET to latchup from 20 to 50 MeV-cm^2/mg.

p+ diffusion		No deep-p+ No guard		Deep-p+ No guard		No deep-p+ With guard		Deep-p+ With guard	
Angle	**LET**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**
0	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	x	x	x	x	x	x	x
	50	x	X	x	X	x	X	x	X
45	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X
60	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X

Table 1. Results for heavy-ion strikes at p+ diffusion. 1.8V and 5.0V VDD bias. A capital "X" in a red box denotes that true latchup occurred while a lowercase "x" in a yellow box denotes that both of the BJTs were triggered with no latchup result. "Deep-p+" designates the inclusion of a deep-p$^+$ layer, while "guard" designates the inclusion of an n$^+$ guard structure.

Appendix B contains similar tables for the results of SEL simulations at all other strike locations.

4.3.2 Observed Latchup Trends and Dependencies

The data recorded from these simulations clearly show a latchup dependence on device bias as no latchup is seen for the 1.8V VDD bias cases regardless of LET or

incidence angle. However, latchup is far more prevalent in every case for the 5.0V bias as the standard latchup structure showed vulnerability for any LET of 20 to 50 MeV-cm^2/mg or greater as long as the incident angle exceeded 0°.

Both the deep-p+ buried layer and the guard structure were effective in reducing latchup vulnerability at different combinations of LET, angle, and strike location, though the deep-p+ layer proved overall more effective. The inclusion of both in the structure resulted in no latchup below a threshold value of 50 MeV-cm^2/mg for the 5.0V bias case. Considering these simulations were performed in a 2-D environment, an environment which sometimes tends to overpredict single-event vulnerability, the critical latchup LET may be even higher in actual application. This suggests that 5.0V operation of this process is likely feasible, with regards to latchup, within the proper setup as long as both the deep-p+ implant and guard rings are included. This is significant as a critical latchup LET of below 5 MeV-cm^2/mg was reported in the study of a different 180 nm technology incorporating neither the p+ buried layer or guard structure [11].

Finally, as expected, the triple-well structures were the most resilient to SEL. No latchup was seen throughout any of the strikes on these structures. While milliamp magnitude currents may have been observed at a single contact following a strike, no strike was able to cause current at both monitored contacts. The same complete SEL mitigation was seen for both the standard and the connected / butted n-well structure triple-well devices. Therefore, it appears conclusive that the connected n-well structure may be incorporated into circuit designs as an area saving technique if the design allows for it.

CHAPTER V

CONCLUSION

In this thesis, the usability of 180 nm technology in a space environment setting with analog / mixed-signal based applications was explored through simulation. While a bit dated at the time of this document's creation, the technology is still applicable to this type of application and was therefore simulated in the analog / mixed-signal domain. Very limited single-event characterization of this technology has been performed in this domain, so basic transient simulations were performed across LET, drain load, and VDD bias. A thorough qualitative characterization of the technology's single-event latchup vulnerability was also performed through simulation.

Varying the LET of the simulated heavy-ion strike typically provided expected results: increased pulse widths as LET increased from 10 to 30 and 50 MeV-cm^2/mg with the same basic pulse shape maintained throughout. However, varying either the supply voltage or load resistance connected to a struck device produced much greater variances in the observed pulse shapes compared to varying the LET. Current pulses decreased in magnitude while width of any resulting current plateau increased for either increasing drain resistance or decreasing VDD from the nominal configuration. Both of these factors provide reduced restoring current from the 1.8V VDD unloaded configuration, resulting in lower amplitude pulses with wider current plateaus. This is in agreement with previously published data describing the roles of restoring current, drift, and diffusion to SET pulse width and magnitude [12], [14], [17].

However, unexpected results were obtained when basic single-event latchup tests were performed to ascertain the general latchup susceptibility of the 180 nm process. As stated in Section 1.4, previous latchup studies were performed at the 180 nm node utilizing technologies other than the IBM 7RF. These studies revealed a very high vulnerability to latchup--a critical LET of only 5 MeV-cm^2/mg was observed in one study. The previous results are in heavy contrast to the results found in this study, wherein no latchup was observed for the nominal 1.8V VDD, regardless of heavy ion LET or the presence of a deep-p+ layer or any other mitigation technique.

The most likely explanation for this sensitivity discrepancy is significant differences in fabrication details such as diffusion-to-diffusion spacing, diffusion and implant doping levels, and inclusion of mitigation techniques by default. These details strongly affect the resistance along the parasitic bipolar paths, generally the most deciding factor in a device's or technology's latchup susceptibility. However, none of these factors plays as strong of a role as the inclusion of STI or another form of isolation, a technique absent from one previous study [5], [11]-[12]. Not even increasing the supply voltage from 1.8V to 5.0V in this study resulted in as low of a critical failure LET as was presented at 1.8V in the previous work, though the latchup sensitivity was greatly increased as a result.

The final studies measuring the effects on SEL vulnerability of the various mitigation techniques provided expected results with respect to qualitative trends. Both the added guard diffusion and the added deep-p+ layer noticeably reduced the amplitudes of resulting pulses indicative of latchup. However, neither was as effective as the inclusion of the triple-well NMOSFET structure. This device, which is widely accepted

as a solution to latchup, completely mitigated the SEL phenomenon but includes the penalty of high device real estate. It therefore seems beneficial as future work to fully explore the potential use of the area-saving "connected n-well" technique presented in this thesis for future work. As both the connected and non-connected configurations produced virtually the same SEL vulnerability results, the space-saving technique may prove useful in future designs, at least at this technology node.

The results in this thesis are to be understood as qualitative, giving general trends regarding the single-event response of the process. Overall, this study's results serve as a promising basis for the use of the 180 nm technology in space analog / mixed-signal applications. With the correct planning and inclusion of single-event mitigation techniques, the process may prove very usable in such applications.

REFERENCES

[1] K. Kinoshita, C.T. Kleiner, and E.D. Johnson, "Radiation Induced Regeneration Through the P-N Junction in Monolithic IC's", *IEEE Trans. Nuc. Sci.,* vol. NS-12, no. 5, Oct. 1965, pp. 83-90.

[2] L.W. Massengill, "SEU modeling and prediction techniques", *IEEE NSREC Short Course*, 1993, pp. III-1 – III-93.

[3] Y. Boulghassoul, L.W. Massengill, A.L. Sternberg, B.L. Bhuva, "Effects of technology scaling on the SET sensitivity of RF CMOS Voltage-controlled oscillators", *IEEE Trans. Nuc. Sci.*, vol. 52, no. 6, Dec. 2005, pp. 2426 – 2432.

[4] R. Koga, S.D. Pinkerton, S.C. Moss, D.C. Mayer, S. LaLumondiere, S.J. Hansel, K.B. Crawford, W.R. Crain, "Observation of single event upsets in analog circuits", *IEEE. Trans. Nuc. Sci*, vol. 40, no. 6, 1993, pp. 1838 – 1844.

[5] Steven H. Voldman, *Latchup*, Wiley, 2008. Print.

[6] J.F. Leavy and R.A. Poll, "Radiation-induced Integrated Circuit Latchup", *IEEE Trans. Nuc. Sci.,* vol. NS-16, Dec. 1969, pp. 96-103.

[7] David G. Mavis and David R. Alexander, "Employing Radiation Hardness by Design Techniques with Commercial Integrated Circuit Processes", Digital Avionics Systems Conference, 1997, 16th DASC, AIAA/IEEE, Vol. 1, Oct. 1997, pp. 26-30.

[8] Y. Moreau, H. de La Rochette, G. Bruguier, J. Gasiot, F. Pelanchon, C. Sudre, and R. Ecoffet, "The Latchup Risk of CMOS-Technology in Space", *IEEE Trans. Nuc. Sci.*, vol. 40, no. 6, Dec 1993, pp. 1831-1837.

[9] G. Bruguier and J.M. Palau, "Single Particle Induced Latchup", *IEEE Trans. Nuc. Sci.*, vol. 43, no. 2, Apr. 1996, pp. 522-532.

[10] A.H. Johnston, "The influence of VLSI technology evolution on radiation-induced latchup in space systems", *IEEE Trans. Nuc. Sci.*, vol. 43, no. 2, April 1996, pp. 505 – 521.

[11] J.M. Hutson, R.D. Schrimpf, and L.M. Massengill, "The Effects of Scaling and Well and Substrate Contact Placement on Single Event Latchup in Bulk CMOS Technology", *8th European Conference on Radiation and Its Effects on Components and Systems, 2005*. pp. PC24-1 – PC24-5, 19-23. Sept. 2005.

[12] C. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective", *43rd Annual IEEE International Reliability Physics Symposium Proceedings*, 2005, pp. 137 – 144.

[13] IBM, CMOS7RF Design Manual and Model Guide, Sep. 2007. Online.

[14] S. Dasgupta, "Trends in Single Event Pulse Widths and Pulse Shapes in Deep Submicron CMOS", M. S. Thesis, December 2007.

[15] O.A. Amusan, "Charge Collection and Charge Sharing in a 130 nm CMOS Technology", *IEEE Trans. Nuc. Sci.*, vol. 53, no. 6, Dec. 2006, pp. 3253 – 3258.

[16] Chipworks, "nVIDIA GeForce FX 5700 Ultra (NV36) Graphics Processor Structural Analysis", Jan. 2005, pp. 5-16 and 5-17.

[17] R. Baumann, "Single-Event Effects in Advanced CMOS Technology", *IEEE NSREC Short Course*, 2005, pp. II-1 – II-59.

[18] S. Buchner and D. McMorrow, "Single-Event Transients in Linear Integrated Circuits", *IEEE NSREC Short Course*, 2005, pp. IV-1 – IV-77.

[19] Synopsys Sentaurus Device and Structure Editor Manuals, Release Version A-2007.12, 2007.

[20] D.B. Estreich, A. Ochoa, and R.W. Dutton, "An analysis of latch-up prevention in CMOS IC's using an epitaxial-buried layer process", *International Electron Devices Meeting*, vol. 24, 1978, pp. 230 – 234.

[21] W. Morris, L. Rubin, and D. Wristers, "Buried layer / connecting layer high energy implantation for improved CMOS latch-up", *International Conference on Ion Implantation Technology Proceedings*, 1996, pp. 796 – 799.

[22] L.M. Rubin, K.H. Lee, J.G. Oh, J.Y. Lee, and S.K. Lee, "High dose p+ buried layers for reduced diode leakage", *International Conference on Ion Implantation Technology Proceedings*, vol. 1, 1999, pp. 102 – 105.

[23] Jae-Geun Oh, Jung-Ho Lee, Kil-Ho Lee, Sahng-Kyoo Lee, "Dependence of the effective p+ buried layer implant dose for reducing junction leakage on well-to-buried layer spacing", *1998 International Conference on Ion Implantation Technology Proceedings*, vol. 1, 1999, pp. 75 – 78.

[24] K.C. Leong, P.C. Liu, W. Morris, L. Rubin, C.H. Gan, L. Chan, "Superior latch-up resistance of high dose, high energy implanted p+ buried layers", *1998 International Conference on Ion Implantation Technology Proceedings*, vol. 1, 1999, pp. 99 – 101.

[25] J.M. Hutson, J.A. Pellish, A.D. Tipton, et. al, "Evidence for Lateral Angle Effect on Single-Event Latchup in 65 nm SRAMs", *IEEE Trans. Nuc. Sci.*, vol. 55, no. 6, Dec. 2008, pp. 2880-2885.

[26] S. Liao, C. Niou, K. Chien, A. Guo, W. Dong, C. Huang, "New observance and analysis of various guard-ring structures on latch-up hardness by backside photo emission image", *IEEE International Reliability Physics Symposium (IRPS) Proceedings*, 2003, pp. 92 – 98.

[27] B. Narasimham, J.W. Gambles, R.L. Shuler, B.L. Bhuva, and L.W. Massengill, "Quantifying the Effect of Guard Rings and Guard Drains in Mitigating Charge Collection and Charge Spread", *IEEE Trans. Nuc. Sci.*, vol. 55, no. 6, Dec. 2008, pp. 3456 – 3460.

[28] T. Roy, A.F. Witulski, R.D. Schrimpf, M.L. Alles, L.W. Massengill, "Single Event Mechanisms in 90 nm Triple-Well CMOS Devices", *IEEE Trans. Nuc. Sci.*, vol. 55, no. 6, Dec. 2008, pp. 2948 – 2956.

[29] D. Kontos, K. Domanski, R. Gauthier, K. Chatty, M. Muhammad, C. Seguin, R. Halbach, C. Russ, D. Alvarez, "Investigation of External Latchup Robustness of Dual and Triple Well Designs in 65nm Bulk CMOS Technology", *44th Annual IEEE International Reliability Physics Symposium Proceedings*, 2006, pp. 145 – 150.

[30] H. Puchner, R. Kapre, S. Sharifzadeh, J. Majjiga, R. Chao, D. Radaelli, and S. Wong, "Elimination of single event latchup in 90 nm SRAM technologies", *Proc. IEEE Int. Reliability Physics Symp.*, Mar. 2006, pp. 721 – 722.

APPENDIX

A. Device simulation files / models

As explained in Sections 2.1 and 2.2, the doping profiles and device geometries utilized in the creation of the models for this study were based heavily on the year 2000 ITRS with influences from known characteristics of the IBM 8SF (130 nm) process and a ChipWorks report detailing the process [16]. These sections should be referenced for more detail on the iterative model calibration performed before simulation took place.

A.1 Doping profile details: Full NMOS and PMOS models

Common NMOSFET / PMOSFET profiles

a) Substrate:

Size: 10 um x 10 um x 10 um

Doping: Constant 1e16 p-type boron.

b) Gate oxide thickness: 4 nm SiO_2

c) Shallow trench isolation (STI): 0.36 um depth extension from surface. Present everywhere diffusions / implants are absent.

d) Deep-p+ buried layer:

Size: extends through entire substrate in x- and y- directions.

Doping: p-type boron. 1.25 um from surface. Peak value 1e18. 1e16 value at depth 0.5 um. Gaussian distribution, factor “0.0001”

Similar NMOSFET / PMOSFET profiles

a) Gate region (PolySi):

Thickness: 138.5 nm

Doping: Constant 1e20 n-type arsenic (NMOSFET) / p-type boron (PMOSFET)

b) Retrograde well regions:

NMOSFET p-well: p-type boron. Peak value 8e17, 0.45 um from surface.

2e16 value at depth 0.45 um. Gaussian distribution, factor "0.01".

PMOSFET n-well: n-type arsenic. Peak value 2e17, 0.45 um from surface.

2e16 value at depth 0.45 um. Gaussian distribution, factor "0.01".

c) Well contacts:

Location: 0.5 um from edge of gate polySi

Doping: n-type arsenic (NMOSFET) / p-type boron (PMOSFET).

Peak value 9e19 at surface. 3e17 value at depth 0.08. 220 nm width, full length of substrate. Gaussian distribution, factor "0.01."

d) Source and drain regions:

Doping: n-type arsenic (NMOSFET) / p-type boron (PMOSFET).

Peak value 8e19 at surface. 1e17 value at depth 0.12 um. 365 nm width. Gaussian distribution, factor "0.1".

e) Threshold voltage (V_T) adjust implant:

Doping: n-type arsenic (NMOSFET) / p-type boron (PMOSFET).

Peak value 1.8e18 at surface. 6.2e17 value at depth 0.010 um. 0.03 um long, under full width of gate. Gaussian distribution, factor "0.001."

A.2 Full model and simulation file Scheme scripts

A.2.1 Sample standard NMOSFET script:

```
;-----------------------------------------------------------
; IBM 7RF/SF Device File
; NMOS
;-----------------------------------------------------------
; Jeff Kauppila and Cody Dinkins
; Under the Draper IR&D 2009 Contract
;-----------------------------------------------------------

;-----------------------------------------------------------
; Define Variables and Major Dimensions
;-----------------------------------------------------------
(define subxmin -5.0)   ;2D/3D   X-direction max / leftside extension
(define subxmax  5.0)   ;2D/3D   X-direction max / rightside extension
(define subymin -5.0)   ;3D      Y-direction max / frontside extension
(define subymax  5.0)   ;3D      Y-direction max / backside extension
(define subzmin  0.0)   ;3D      Z-direction min / topside extension
(define subzmax   10)   ;3D      Z-direction max / bottomside extension

(define gatexmin -@HALFL@)    ;3D   X-dir GATE min /leftside extension
(define gatexmax  @HALFL@)    ;3D   X-dir GATE max /rightside extension
(define gateymin -@HALFW@)    ;3D   Y-dir GATE min /frontside extension
(define gateymax  @HALFW@)    ;3D   Y-dir GATE max /backside extension
(define gatezmin -0.1425)     ;2D   Z-dir GATE min /topside extension
(define gatezmax -0.004)      ;2D   Z-dir GATE max /bot. side extension
; - Defines Tox : 180nm Tox = 4.45 nm

;-----------------------------------------------------------
;-----------------------------------------------------------
; ABA means old replaces new
;-----------------------------------------------------------
(isegeo:set-default-boolean "ABA")
;-----------------------------------------------------------

;-----------------------------------------------------------
;-------- DEVICE REGIONS -----------------------------------
;-----------------------------------------------------------
;-----------------------------------------------------------
; This is the full silicon bulk
;-----------------------------------------------------------
(isegeo:create-cuboid    (position subxmin subymin subzmin) (position
subxmax subymax subzmax) "Silicon" "R.Bulk")
;-----------------------------------------------------------

;-----------------------------------------------------------
; Defines the gate oxide and gate poly
;-----------------------------------------------------------
(isegeo:create-cuboid (position gatexmin gateymin gatezmax ) (position
gatexmax gateymax 0)  "SiO2"    "R.GateOxideA")
```

```
(isegeo:create-cuboid (position gatexmin gateymin gatezmin ) (position
gatexmax gateymax gatezmax) "PolySi"  "R.PolyGateA")
;------------------------------------------------------------

;------------------------------------------------------------
; Shallow trench isolation STI
;------------------------------------------------------------
;Region #1: Above p-well contact to y-max
(isegeo:create-cuboid (position subxmin (+ gateymax 0.67) 0)(position
subxmax subymax 0.36) "SiO2" "R.STI1")

;Region #2: Between p-well contact and device
(isegeo:create-cuboid (position subxmin gateymax  0) (position subymax
(+ gateymax 0.39) 0.36)  "SiO2" "R.STI2")

;Region #3: Left side of gate to x-min
(isegeo:create-cuboid (position subxmin gateymin 0) (position (-
gatexmin 0.385) gateymax 0.36)  "SiO2" "R.STI3")

;Region #4: Right side of device to x-max
(isegeo:create-cuboid (position (+ gatexmax 0.385) gateymin 0)
(position subxmax gateymax 0.36)  "SiO2" "R.STI4")

;Region #5: Below device to y-min
(isegeo:create-cuboid (position subxmin gateymin  0) (position subxmax
subymin 0.36)  "SiO2" "R.STI5")

;Region #6:  Left of p-well contact
(isegeo:create-cuboid (position subxmin (+ gateymax 0.39) 0) (position
(- gatexmin 1.705) (+ gateymax 0.67) 0.36)  "SiO2" "R.STI5")

;Region #7:  Right of p-well contact
(isegeo:create-cuboid (position subxmax (+ gateymax 0.39) 0) (position
(+ gatexmax 2.775) (+ gateymax 0.67) 0.36)  "SiO2" "R.STI5")
;------------------------------------------------------------

;------------------------------------------------------------
; Contacts defined
;------------------------------------------------------------
(isegeo:define-contact-set "DrainA" 4.0  (color:rgb 1.0 0.0 0.0 ) "##")
(isegeo:define-contact-set "GateA"  4.0  (color:rgb 0.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "SourceA" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "Subst." 4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "Pwell"  4.0  (color:rgb 0.0 1.0 1.0 ) "##")
;------------------------------------------------------------


;------------------------------------------------------------
; Gate contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position gatexmin gateymin gatezmin) (position
gatexmax gateymax -2) "Metal" "GateAmetal")
(isegeo:define-3d-contact (find-face-id (position 0 0 gatezmin))
"GateA")
(isegeo:delete-region (find-body-id (position 0 0 -1)))
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; P-well contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position (- gatexmin 1.405) (+ gateymax 0.44) 0)
(position (+ gatexmax 2.475) (+ gateymax 0.62) -2) "Metal"
"Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position 0 (+ gateymax 0.53)
0)) "Pwell")
(isegeo:delete-region (find-body-id (position 0 (+ gateymax 0.53) -1)))
;------------------------------------------------------------

;------------------------------------------------------------
; Substrate contact placement, represents the entire bottom surface of
the silicon
;------------------------------------------------------------
(isegeo:define-3d-contact (find-face-id (position 0 0 10))
"Substrate")
;------------------------------------------------------------

;------------------------------------------------------------
; Source contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position (- gatexmin 0.2925) (- gateymax 0.15)
0) (position (- gatexmin 0.1215) (+ gateymin 0.15) -2) "Metal"
"SourceAmetal")
(isegeo:define-3d-contact (find-face-id (position (- gatexmin 0.207) 0
0)) "SourceA")
(isegeo:delete-region (find-body-id (position (- gatexmin 0.207) 0 -
1)))
;------------------------------------------------------------

;------------------------------------------------------------
; Drain contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position (+ gatexmax 0.2925) (- gateymax 0.15)
0) (position (+ gatexmax 0.1215) (+ gateymin 0.15) -2) "Metal"
"DrainAmetal")
(isegeo:define-3d-contact (find-face-id (position (+ gatexmax 0.207) 0
0)) "DrainA")
(isegeo:delete-region (find-body-id (position (+ gatexmax 0.207) 0 -
1)))
;------------------------------------------------------------

;------------------------------------------------------------
;-------- Begin adding device dopings ----------------------
;------------------------------------------------------------
;------------------------------------------------------------
; Poly, Substrate, and Deep P implant are the same for both NMOS and
PMOS Devices
;------------------------------------------------------------
; Constant Doping in the poly - N-Type
;------------------------------------------------------------
(isedr:define-constant-profile "Profile.Polyconst.Phos"
"ArsenicActiveConcentration" 1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1"
"Profile.Polyconst.Phos" "PolySi")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Constant Doping in the silicon substrate region - P-Type
;------------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid"
(position subxmin subymin subzmin) (position subxmax subymax subzmax))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;------------------------------------------------------------

;------------------------------------------------------------
; Deep P Implant - Boron doping in the silicon
; Assumes deep pwell implant goes through whole die
;------------------------------------------------------------
;Matches profile from ChipWorks report

(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle"
(position subxmax subymax 1.25) (position subxmin subymin 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth"
1e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1"
"Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace"
"Eval")



;------------------------------------------------------------
;-------- Below Here is NMOS Specific ----------------------
;------------------------------------------------------------
;------------------------------------------------------------
; Retrograde P-well implant
; Matches profile from ChipWorks report
;------------------------------------------------------------
(isedr:define-refinement-window "Window.PWell.Bor.2" "Rectangle"
(position subxmax subymax 0.45) (position subxmin subymin 0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.2"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.2"
"Profile.PWell.Bor.2" "Window.PWell.Bor.2" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------

;------------------------------------------------------------
; Pwell contact doping
;------------------------------------------------------------
(isedr:define-refinement-window "Window.PWellCon.Bor.3A" "Rectangle"
(position  (- gatexmin 1.705) (+ gateymax 0.39) 0) (position (+
gatexmax 2.775) (+ gateymax 0.67)  0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3A"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3A"
"Profile.PWellCon.Bor.3A" "Window.PWellCon.Bor.3A" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------
```

```
;-----------------------------------------------------------
;------- Drain, Source, and LDD Dopings -------------------
; Most of this information was derived from IRTS Roadmap - 2000
;-----------------------------------------------------------

;-----------------------------------------------------------
;------- Drain LDD -----------------------------------------
; Peak at surface - 2E19
; Gausian Profile with 1E17 at depth of 40nm
; LDD is from active edge to 13nm inside the gate edge in X direction
(length direction)
;-----------------------------------------------------------
(isedr:define-refinement-window "drainldd.Profile.RegionA" "Rectangle"
(position (- gatexmax 0.013) gateymax 0) (position (+ gatexmax 0.385)
gateymin 0))
(isedr:define-gaussian-profile "drainldd.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2E19 "ValueAtDepth"
1e17 "Depth" 0.04 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceA"
"drainldd.ProfileA" "drainldd.Profile.RegionA" "Symm" "NoReplace"
"Eval")

;-----------------------------------------------------------
;------- Source LDD ----------------------------------------
; Peak at surface - 2E19
; Gausian Profile with 1E17 at depth of 40nm
; LDD is from active edge to 13nm inside the gate edge in X direction
(length direction)
;-----------------------------------------------------------
(isedr:define-refinement-window "sourceldd.Profile.RegionA" "Rectangle"
(position (+ gatexmin 0.013) gateymax 0) (position (- gatexmin 0.385)
gateymin 0))
(isedr:define-gaussian-profile "sourceldd.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2E19 "ValueAtDepth"
1e17 "Depth" 0.04 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceA"
"sourceldd.ProfileA" "sourceldd.Profile.RegionA" "Symm" "NoReplace"
"Eval")
;-----------------------------------------------------------

;-----------------------------------------------------------
;------- Drain Side, Main Doping ---------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;-----------------------------------------------------------
(isedr:define-refinement-window "drain.Profile.RegionA" "Rectangle"
(position (+ gatexmax .02) gateymax 0) (position (+ gatexmax 0.385)
gateymin 0))
(isedr:define-gaussian-profile "drain.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceA"
"drain.ProfileA" "drain.Profile.RegionA" "Symm" "NoReplace" "Eval")
;-----------------------------------------------------------
```

```
;-----------------------------------------------------------
;------- Source Side, Main Doping -------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;-----------------------------------------------------------
(isedr:define-refinement-window "source.Profile.RegionA" "Rectangle"
(position (- gatexmin 0.02) gateymax 0) (position (- gatexmin 0.385)
gateymin 0))
(isedr:define-gaussian-profile "source.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceA"
"source.ProfileA" "source.Profile.RegionA" "Symm" "NoReplace" "Eval")
;-----------------------------------------------------------


;-----------------------------------------------------------
;------- Channel Engineering and VT Adjustments ------------
; Most of this information was derived from IRTS Roadmap - 2000
;-----------------------------------------------------------

;-----------------------------------------------------------
;------- Threshold Voltage Adjust Implant ------------------
; Peak at surface - 1.8E18
; Gausian Profile with 6.2E17 at depth of 10nm
; Extends to +/- 15nm outide of the gate edges in X direction (length
direction)
; 1.8E18, 6.2E17, and 10nm matched the SPICE model for long channel
devices (450nm was calibration length)
;-----------------------------------------------------------
(isedr:define-refinement-window "implant.Profile.RegionA" "Rectangle"
(position (- gatexmin 0.015) gateymax 0) (position (+ gatexmax 0.015)
gateymin 0))
(isedr:define-gaussian-profile "implant.ProfileA"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1.8E18 "ValueAtDepth"
6.2E17 "Depth" .010 "Gauss" "Factor" 0.001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceA"
"implant.ProfileA" "implant.Profile.RegionA" "Symm" "NoReplace" "Eval")
;-----------------------------------------------------------

;-----------------------------------------------------------
;------- Halo Implant A for Drain to Source Leakage --------
; Peak at 37.5nm below surface - 1E18
; Gausian Profile with 1E17 at depth of +/-37.5nm
; Extends from 5nm inside the gate edge to 55nm inside the gate edge
; 55nm was a tuned parameter to get leakage and threshold correct when
compared to SPICE model
; Significant for short channel devices (180nm calibration length)
;-----------------------------------------------------------
(isedr:define-refinement-window "limplant.Profile.RegionA" "Rectangle"
(position (+ gatexmin 0.005) gateymax 0.0375) (position (+ gatexmin
0.055) gateymin 0.0375))
(isedr:define-gaussian-profile "limplant.ProfileA"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1E18 "ValueAtDepth"
1E17 "Depth" 0.0375 "Gauss" "Factor" 0.0001)
```

```
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceA"
"limplant.ProfileA" "limplant.Profile.RegionA" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------

;------------------------------------------------------------
;------- Halo Implant B for Drain to Source Leakage --------
; Peak at 37.5nm below surface - 1E18
; Gausian Profile with 1E17 at depth of +/-37.5nm
; Extends from 5nm inside the gate edge to 55nm inside the gate edge
; 55nm was a tuned parameter to get leakage and threshold correct when
compared to SPICE model
; Significant for short channel devices (180nm calibration length)
;------------------------------------------------------------
(isedr:define-refinement-window "limplant.Profile.RegionB" "Rectangle"
(position (- gatexmax 0.055) gateymax 0.0375) (position (- gatexmax
0.005) gateymin 0.0375))
(isedr:define-gaussian-profile "limplant.ProfileB"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1E18 "ValueAtDepth"
1E17 "Depth" 0.0375 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceB"
"limplant.ProfileB" "limplant.Profile.RegionB" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------


;------------------------------------------------------------
;------- MESHING --------------------------------------------
;------------------------------------------------------------
;------------------------------------------------------------
; P-well and Deep P Implant Meshing
; Top part of the bulk silicon
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole" 0.5 0.5 0.25 0.250 0.250
0.125)
(isedr:define-refinement-window "window.whole" "Cuboid" (position
subxmax subymin 0) (position subxmin subymax 2))
(isedr:define-refinement-function "size.whole" "DopingConcentration"
"MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.whole" "size.whole"
"window.whole" )
;------------------------------------------------------------

;------------------------------------------------------------
; Bottom part of the bulk silicon
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole2" 0.75 0.75 0.75 0.5 0.5 0.5)
(isedr:define-refinement-window "window.whole2" "Cuboid" (position
subxmin subymin 2) (position subxmax subymax 10))
(isedr:define-refinement-placement "placement.whole2" "size.whole2"
"window.whole2" )
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Mesh around the P-Well Contact
;------------------------------------------------------------
(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.1 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmesha"
"DopingConcentration" "MaxTransDiff" 1)

(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position
subxmin (+ gateymax 0.37)  0) (position subxmax (+ gateymax 0.69)
0.35))
(isedr:define-refinement-placement "placement.dopingmesha"
"size.dopingmesha" "window.dopingmesha" )
;------------------------------------------------------------

;------------------------------------------------------------
; Dynamic Mesh in Z Axis to refine the channel and LDD Mesh
;------------------------------------------------------------
(isedr:define-multibox-size "MBSize_x" 0.02 0.1 0.02 0.001 0.002 0.001
1 1 3 )
(isedr:define-refinement-window "MBWindow.xn1" "Cuboid"  (position (-
gatexmin 0.015) gateymin 0) (position (+ gatexmax 0.015) gateymax
0.06))
(isedr:define-multibox-placement "MBPlace.xn1" "MBSize_x"
"MBWindow.xn1" )
;------------------------------------------------------------

;------------------------------------------------------------
; Refine the Drain, Source, and Channel over whole active area
;------------------------------------------------------------
(isedr:define-refinement-size "active" 0.05 0.1 0.05 0.005 0.02 0.005)
(isedr:define-refinement-window "active" "Cuboid" (position (- gatexmin
0.4) gateymin 0) (position (+ gatexmax 0.4) gateymax 0.2))
(isedr:define-refinement-function "active" "DopingConcentration"
"MaxTransDiff" 0.3)
(isedr:define-refinement-placement "active" "active" "active" )
;------------------------------------------------------------

;------------------------------------------------------------
; Save the resulting file
;------------------------------------------------------------
(ise:save-model "n@node@_msh")
;------------------------------------------------------------
;------------------------EOF---------------------------------
```

A.2.2 Sample triple-well NMOSFET script:

```
;-------------------------------------------------------------
; IBM 7RF/SF Device File
; NMOS – Triple-well version
;-------------------------------------------------------------
; Jeff Kauppila and Cody Dinkins
; Under the Draper IR&D 2009 Contract
;-------------------------------------------------------------

;-------------------------------------------------------------
; Define Variables and Major Dimensions
;-------------------------------------------------------------
(define subxmin -5.0)   ;2D/3D X-direction max / leftside extension
(define subxmax  5.0)   ;2D/3D X-direction max / rightside extension
(define subymin -5.0)   ;3D    Y-direction max / frontside extension
(define subymax  5.0)   ;3D    Y-direction max / backside extension
(define subzmin  0.0)   ;3D    Z-direction min / topside extension
(define subzmax   10)   ;3D    Z-direction max / bottomside extension

(define gatexmin -@HALFL@)    ;3D   X-dir GATE min /leftside extension
(define gatexmax  @HALFL@)    ;3D   X-dir GATE max /rightside extension
(define gateymin -@HALFW@)    ;3D   Y-dir GATE min /frontside extension
(define gateymax  @HALFW@)    ;3D   Y-dir GATE max /backside extension
(define gatezmin -0.1425)     ;2D   Z-dir GATE min /topside extension
(define gatezmax -0.004)      ;2D   Z-dir GATE max /bot. side extension
;- Defines Tox : 180nm Tox = 4.45 nm
;-------------------------------------------------------------

;-------------------------------------------------------------
; ABA means old replaces new
;-------------------------------------------------------------
(isegeo:set-default-boolean "ABA")
;-------------------------------------------------------------

;-------------------------------------------------------------
;-------- DEVICE REGIONS -------------------------------------
;-------------------------------------------------------------
;-------------------------------------------------------------
; This is the full silicon bulk
;-------------------------------------------------------------
(isegeo:create-cuboid    (position subxmin subymin subzmin) (position
subxmax subymax subzmax)        "Silicon" "R.Bulk")
;-------------------------------------------------------------

;-------------------------------------------------------------
; Defines the gate oxide and gate poly
;-------------------------------------------------------------
(isegeo:create-cuboid (position gatexmin gateymin gatezmax ) (position
gatexmax gateymax 0)  "SiO2"    "R.GateOxideA")
(isegeo:create-cuboid (position gatexmin gateymin gatezmin ) (position
gatexmax gateymax gatezmax) "PolySi"  "R.PolyGateA")
;-------------------------------------------------------------
```

```
;------------------------------------------------------------
; Shallow trench isolation STI
;------------------------------------------------------------
(isegeo:create-cuboid (position (+ gatexmax 1.1) gateymax 0) (position
(- gatexmin 1.1) (+ gateymax 0.64) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (+ gatexmax 1.1) gateymin 0) (position
(- gatexmin 1.1) (- gateymin 0.64) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (+ gatexmax 0.385) gateymin 0)
(position  (+ gatexmax 1.1) gateymax 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 0.385) gateymin 0)
(position  (- gatexmin 1.1) gateymax 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (+ gatexmax 1.54) (+ gateymax 1.7) 0)
(position  (+ gatexmax 2.04) (- gateymin 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 1.54) (+ gateymax 1.7) 0)
(position  (- gatexmin 2.04) (- gateymin 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 2.04) (+ gateymax 1.08) 0)
(position  (+ gatexmax 2.04) (+ gateymax 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 2.04) (- gateymin 1.08) 0)
(position  (+ gatexmax 2.04) (- gateymin 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.84) (+ gateymax 1.7) 0)
(position  (- gatexmin 3.1) subymax 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.84) (- gateymin 1.7) 0)
(position  (- gatexmin 3.1) subymin 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.84) (+ gateymax 1.7) 0)
(position  (+ gatexmax 2.48) (- gateymin 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 3.1) (+ gateymax 1.7) 0)
(position  (- gatexmin 2.48) (- gateymin 1.7) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 3.1) (- subymax 2) 0)
(position  subxmin subymax 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 3.1) (+ subymin 2) 0)
(position  subxmin subymin 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- gatexmin 3.54) (- subymax 2) 0)
(position  subxmin (+ subymin 2) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.4) (- subymax 1) 0)
(position  subxmax (+ subymin 1) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.84 ) subymax 0) (position
subxmax (- subymax 1) 0.36) "SiO2" "R.STI1")
(isegeo:create-cuboid (position (- subxmax 0.84 ) subymin 0) (position
subxmax (+ subymin 1) 0.36) "SiO2" "R.STI1")
;------------------------------------------------------------

;------------------------------------------------------------
; Contacts defined
;------------------------------------------------------------
(isegeo:define-contact-set "DrainA" 4.0  (color:rgb 1.0 0.0 0.0 ) "##")
(isegeo:define-contact-set "GateA"  4.0  (color:rgb 0.0 1.0 0.0 ) "##")
(isegeo:define-contact-set "SourceA" 4.0 (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "Subst." 4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "Pwell"  4.0  (color:rgb 0.0 1.0 1.0 ) "##")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Gate contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position gatexmin gateymin gatezmin) (position
gatexmax gateymax -2) "Metal" "GateAmetal")
(isegeo:define-3d-contact (find-face-id (position 0 0 gatezmin))
"GateA")
(isegeo:delete-region (find-body-id (position 0 0 -1)))
;------------------------------------------------------------

;------------------------------------------------------------
; Substrate contact placement, represents the entire bottom surface of
the silicon
;------------------------------------------------------------
(isegeo:define-3d-contact (find-face-id (position 0 0 10))
"Substrate")
;------------------------------------------------------------

;------------------------------------------------------------
; Source contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position (- gatexmin 0.2925) (- gateymax 0.15)
0) (position (- gatexmin 0.1215) (+ gateymin 0.15) -2) "Metal"
"SourceAmetal")
(isegeo:define-3d-contact (find-face-id (position (- gatexmin 0.207) 0
0)) "SourceA")
(isegeo:delete-region (find-body-id (position (- gatexmin 0.207) 0 -
1)))
;------------------------------------------------------------

;------------------------------------------------------------
; Drain contact placement
;------------------------------------------------------------
(isegeo:create-cuboid (position (+ gatexmax 0.2925) (- gateymax 0.15)
0) (position (+ gatexmax 0.1215) (+ gateymin 0.15) -2) "Metal"
"DrainAmetal")
(isegeo:define-3d-contact (find-face-id (position (+ gatexmax 0.207) 0
0)) "DrainA")
(isegeo:delete-region (find-body-id (position (+ gatexmax 0.207) 0 -
1)))
;------------------------------------------------------------


;------------------------------------------------------------
;-------- Begin adding device dopings ----------------------
;------------------------------------------------------------
;------------------------------------------------------------
; Poly, Substrate, and Deep P implant are the same for both NMOS and
PMOS Devices
;------------------------------------------------------------
; Constant Doping in the poly - N-Type
;------------------------------------------------------------
(isedr:define-constant-profile "Profile.Polyconst.Phos"
"ArsenicActiveConcentration" 1e20)
(isedr:define-constant-profile-material "Place.Polyconst.Phos1"
"Profile.Polyconst.Phos" "PolySi")
;------------------------------------------------------------
```

```
;-----------------------------------------------------------
; Constant Doping in the silicon substrate region - P-Type
;-----------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Cuboid"
(position subxmin subymin subzmin) (position subxmax subymax subzmax))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;-----------------------------------------------------------

;-----------------------------------------------------------
; Deep P Implant - Boron doping in the silicon
; Assumes deep pwell implant goes through whole die
;-----------------------------------------------------------
;Matches profile from ChipWorks report
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Rectangle"
(position subxmax subymax 1.25) (position subxmin subymin 1.25))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth"
1e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1"
"Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace"
"Eval")
;-----------------------------------------------------------


;-----------------------------------------------------------
;-------- Below Here is NMOS Specific ----------------------
;-----------------------------------------------------------
;-----------------------------------------------------------
; Retrograde P-well implant
; Matches profile from ChipWorks report
;-----------------------------------------------------------
(isedr:define-refinement-window "Window.PWell.Bor.2" "Rectangle"
(position (+ gatexmax 1.7) (+ gateymax 1.24) 0.45) (position (-
gatexmin 1.7) (- gateymin 1.24) 0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.2"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.2"
"Profile.PWell.Bor.2" "Window.PWell.Bor.2" "Symm" "NoReplace" "Eval")
;-----------------------------------------------------------

;-----------------------------------------------------------
; Pwell contact doping - Guard Ring, single device, version
;-----------------------------------------------------------
;Top
(isedr:define-refinement-window "Window.PWellCon.Bor.3A" "Rectangle"
(position (+ gatexmax 1.54) (+ gateymax 1.08) 0) (position (- gatexmin
1.54) (+ gateymax 0.64) 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3A"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3A"
"Profile.PWellCon.Bor.3A" "Window.PWellCon.Bor.3A" "Symm" "NoReplace"
"Eval")
```

```
;Metal contact
(isegeo:create-cuboid (position (+ gatexmax 1.23) (+ gateymax 0.95) 0)
(position (- gatexmin 1.23) (+ gateymax 0.77) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position 0 (+ gateymax 0.86)
0)) "Pwell")
(isegeo:delete-region (find-body-id (position 0 (+ gateymax 0.86) -1)))


;Bottom
(isedr:define-refinement-window "Window.PWellCon.Bor.3B" "Rectangle"
(position (+ gatexmax 1.54) (- gateymin 1.08) 0) (position (- gatexmin
1.54) (- gateymin 0.64) 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3B"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3B"
"Profile.PWellCon.Bor.3B" "Window.PWellCon.Bor.3B" "Symm" "NoReplace"
"Eval")

;Metal contact
(isegeo:create-cuboid (position (+ gatexmax 1.23) (- gateymin 0.95) 0)
(position (- gatexmin 1.23) (- gateymin 0.77) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position 0 (- gateymin 0.86)
0)) "Pwell")
(isegeo:delete-region (find-body-id (position 0 (- gateymin 0.86) -1)))

;Left
(isedr:define-refinement-window "Window.PWellCon.Bor.3C" "Rectangle"
(position (+ gatexmax 1.1) (+ gateymax 1.08) 0) (position (+ gatexmax
1.54) (- gateymin 1.08) 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3C"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3C"
"Profile.PWellCon.Bor.3C" "Window.PWellCon.Bor.3C" "Symm" "NoReplace"
"Eval")

;Metal contact
(isegeo:create-cuboid (position (+ gatexmax 1.23) (+ gateymax 0.95) 0)
(position (+ gatexmax 1.41) (- gateymin 0.95) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position (+ gatexmax 1.32) 0
0)) "Pwell")
(isegeo:delete-region (find-body-id (position (+ gatexmax 1.32) 0 -1)))


;Right
(isedr:define-refinement-window "Window.PWellCon.Bor.3D" "Rectangle"
(position (- gatexmin 1.1) (+ gateymax 1.08) 0) (position (- gatexmin
1.54) (- gateymin 1.08) 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.3D"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.3D"
"Profile.PWellCon.Bor.3D" "Window.PWellCon.Bor.3D" "Symm" "NoReplace"
"Eval")
```

```
;Metal contact
(isegeo:create-cuboid (position (- gatexmin 1.23) (+ gateymax 0.95) 0)
(position (- gatexmin 1.41) (- gateymin 0.95) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position (- gatexmin 1.32) 0
0)) "Pwell")
(isegeo:delete-region (find-body-id (position (- gatexmin 1.32) 0 -1)))

;-------------------------------------------------------------

;-------------------------------------------------------------
; Outer P-well implant
; Matches profile from ChipWorks report
;-------------------------------------------------------------
; Top outer p-well
(isedr:define-refinement-window "Window.PWell.Bor.Top" "Rectangle"
(position subxmax (+ gateymax 3.34) 0.45) (position subxmin subymax
0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.Top"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.Top"
"Profile.PWell.Bor.Top" "Window.PWell.Bor.Top" "Symm" "NoReplace"
"Eval")

; Bottom outer p-well
(isedr:define-refinement-window "Window.PWell.Bor.Bot" "Rectangle"
(position subxmax (- gateymin 3.34) 0.45) (position subxmin subymin
0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.Bot"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.Bot"
"Profile.PWell.Bor.Bot" "Window.PWell.Bor.Bot" "Symm" "NoReplace"
"Eval")

; Left outer p-well
(isedr:define-refinement-window "Window.PWell.Bor.Left" "Rectangle"
(position (+ gatexmax 3.8) subymax 0.45) (position subxmax subymin
0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.Left"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.Left"
"Profile.PWell.Bor.Left" "Window.PWell.Bor.Left" "Symm" "NoReplace"
"Eval")

; Right outer p-well
(isedr:define-refinement-window "Window.PWell.Bor.Right" "Rectangle"
(position (- gatexmin 3.8) subymax 0.45) (position subxmin subymin
0.45))
(isedr:define-gaussian-profile "Profile.PWell.Bor.Right"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWell.Bor.Right"
"Profile.PWell.Bor.Right" "Window.PWell.Bor.Right" "Symm" "NoReplace"
"Eval")
;-------------------------------------------------------------
```

```
;------------------------------------------------------------
; N-well addition
;------------------------------------------------------------

; Buried n-well
;------------------------------------------------------------
(isedr:define-refinement-window "Window.NWell.Ars.2" "Rectangle"
(position (+ gatexmax 2.7) (+ gateymax 2.24) 0.8) (position (- gatexmin
2.7) (- gateymin 2.24) 0.8))
(isedr:define-gaussian-profile "Profile.NWell.Ars.2"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 7.5e17
"ValueAtDepth" 2e16 "Depth" 0.35 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "Place.NWell.Ars.2"
"Profile.NWell.Ars.2" "Window.NWell.Ars.2" "Symm" "NoReplace" "Eval")

;"Ring" around standard P-well
;------------------------------------------------------------
; "Top" n-well ring piece
(isedr:define-refinement-window "Window.NWell.Ars.Top" "Rectangle"
(position (+ gatexmax 3.8) (+ gateymax 3.34) 0.45) (position (-
gatexmin 3.8) (+ gateymax 1.24) 0.45))
(isedr:define-gaussian-profile "Profile.NWell.Ars.Top"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWell.Ars.Top"
"Profile.NWell.Ars.Top" "Window.NWell.Ars.Top" "Symm" "NoReplace"
"Eval")

; "Bottom" n-well ring piece
(isedr:define-refinement-window "Window.NWell.Ars.Bot" "Rectangle"
(position (+ gatexmax 3.8) (- gateymin 3.34) 0.45) (position (-
gatexmin 3.8) (- gateymin 1.24) 0.45))
(isedr:define-gaussian-profile "Profile.NWell.Ars.Bot"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWell.Ars.Bot"
"Profile.NWell.Ars.Bot" "Window.NWell.Ars.Bot" "Symm" "NoReplace"
"Eval")

; "Left" n-well ring piece (drain side)
(isedr:define-refinement-window "Window.NWell.Ars.Left" "Rectangle"
(position (+ gatexmax 3.8) (+ gateymax 1.24) 0.45) (position (+
gatexmax 1.7) (- gateymin 1.24) 0.45))
(isedr:define-gaussian-profile "Profile.NWell.Ars.Left"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWell.Ars.Left"
"Profile.NWell.Ars.Left" "Window.NWell.Ars.Left" "Symm" "NoReplace"
"Eval")

; "Right" n-well ring piece (source side)
(isedr:define-refinement-window "Window.NWell.Ars.Right" "Rectangle"
(position (- gatexmin 3.8) (+ gateymax 1.24) 0.45) (position (-
gatexmin 1.7) (- gateymin 1.24) 0.45))
(isedr:define-gaussian-profile "Profile.NWell.Ars.Right"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
```

```
(isedr:define-analytical-profile-placement "Place.NWell.Ars.Right"
"Profile.NWell.Ars.Right" "Window.NWell.Ars.Right" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------


;------------------------------------------------------------
; N-well contacts
;------------------------------------------------------------
; Contacts to buried layer - Left and right
---------------------------------------------
; "Left" (drain) n-well buried layer contact doping
(isedr:define-refinement-window "Window.NWellCon.Ars.A" "Rectangle"
(position  (+ gatexmax 2.48) (+ gateymax 1.7) 0) (position (+ gatexmax
2.04) (- gateymin 1.7)  0))
(isedr:define-gaussian-profile "Profile.NWellCon.Ars.A"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "Place.NWellCon.Ars.A"
"Profile.NWellCon.Ars.A" "Window.NWellCon.Ars.A" "Symm" "NoReplace"
"Eval")

; Metal contact
(isegeo:create-cuboid (position (+ gatexmax 2.35) (+ gateymax 1.57) 0)
(position (+ gatexmax 2.17) (- gateymin 1.57) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position (+ gatexmax 2.26) 0
0)) "Pwell")
(isegeo:delete-region (find-body-id (position (+ gatexmax 2.26) 0 -1)))


; "Right" (source) n-well buried layer contact doping
(isedr:define-refinement-window "Window.NWellCon.Ars.B" "Rectangle"
(position  (- gatexmin 2.48) (+ gateymax 1.7) 0) (position (- gatexmin
2.04) (- gateymin 1.7)  0))
(isedr:define-gaussian-profile "Profile.NWellCon.Ars.B"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "Place.NWellCon.Ars.B"
"Profile.NWellCon.Ars.B" "Window.NWellCon.Ars.B" "Symm" "NoReplace"
"Eval")

; Metal contact
(isegeo:create-cuboid (position (- gatexmin 2.35) (+ gateymax 1.57) 0)
(position (- gatexmin 2.17) (- gateymin 1.57) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position (- gatexmin 2.26) 0
0)) "Pwell")
(isegeo:delete-region (find-body-id (position (- gatexmin 2.26) 0 -1)))


; Extra outer n-well contact strip doping to match Draper layout -
Source (right) side
(isedr:define-refinement-window "Window.NWellCon.Ars.C" "Rectangle"
(position  (- gatexmin 3.1) (- subymax 2) 0) (position (- gatexmin
3.54) (+ subymin 2)  0))
(isedr:define-gaussian-profile "Profile.NWellCon.Ars.C"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
```

```
(isedr:define-analytical-profile-placement "Place.NWellCon.Ars.C"
"Profile.NWellCon.Ars.C" "Window.NWellCon.Ars.C" "Symm" "NoReplace"
"Eval")

; Metal contact
(isegeo:create-cuboid (position (- gatexmin 3.23) (- subymax 2.13) 0)
(position (- gatexmin 3.41) (+ subymin 2.13) -2) "Metal" "Nwellmetal")
(isegeo:define-3d-contact (find-face-id (position (- gatexmin 3.32) 0
0)) "Nwell")
(isegeo:delete-region (find-body-id (position (- gatexmin 3.32) 0 -1)))
;------------------------------------------------------------


;------------------------------------------------------------
; Top-side P-well contact (Drain side, far-"left")
;------------------------------------------------------------
(isedr:define-refinement-window "Window.PWellCon.Bor.D" "Rectangle"
(position (- subxmax 0.4) (- subymax 1) 0) (position (- subxmax 0.84)
(+ subymin 1) 0))
(isedr:define-gaussian-profile "Profile.PWellCon.Bor.D"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "Place.PWellCon.Bor.D"
"Profile.PWellCon.Bor.D" "Window.PWellCon.Bor.D" "Symm" "NoReplace"
"Eval")

;Metal contact
(isegeo:create-cuboid (position (- subxmax 0.53) (- subymax 1.13) 0)
(position (- subxmax 0.71) (+ subymin 1.13) -2) "Metal" "Pwellmetal")
(isegeo:define-3d-contact (find-face-id (position (- subxmax 0.62) 0
0)) "PwellSub")
(isegeo:delete-region (find-body-id (position (- subxmax 0.62) 0 -1)))



;------------------------------------------------------------
;------- Drain, Source, and LDD Dopings -------------------
; Most of this information was derived from IRTS Roadmap - 2000
;------------------------------------------------------------

;------------------------------------------------------------
;------- Drain LDD ----------------------------------------
; Peak at surface - 2E19
; Gausian Profile with 1E17 at depth of 40nm
; LDD is from active edge to 13nm inside the gate edge in X direction
(length direction)
;------------------------------------------------------------
(isedr:define-refinement-window "drainldd.Profile.RegionA" "Rectangle"
(position (- gatexmax 0.013) gateymax 0) (position (+ gatexmax 0.385)
gateymin 0))
(isedr:define-gaussian-profile "drainldd.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2E19 "ValueAtDepth"
1e17 "Depth" 0.04 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "drainldd.Profile.PlaceA"
"drainldd.ProfileA" "drainldd.Profile.RegionA" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
;------- Source LDD -----------------------------------------
; Peak at surface - 2E19
; Gausian Profile with 1E17 at depth of 40nm
; LDD is from active edge to 13nm inside the gate edge in X direction
(length direction)
;------------------------------------------------------------
(isedr:define-refinement-window "sourceldd.Profile.RegionA" "Rectangle"
(position (+ gatexmin 0.013) gateymax 0) (position (- gatexmin 0.385)
gateymin 0))
(isedr:define-gaussian-profile "sourceldd.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2E19 "ValueAtDepth"
1e17 "Depth" 0.04 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "sourceldd.Profile.PlaceA"
"sourceldd.ProfileA" "sourceldd.Profile.RegionA" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------

;------------------------------------------------------------
;------- Drain Side, Main Doping ----------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;------------------------------------------------------------
(isedr:define-refinement-window "drain.Profile.RegionA" "Rectangle"
(position (+ gatexmax .02) gateymax 0) (position (+ gatexmax 0.385)
gateymin 0))
(isedr:define-gaussian-profile "drain.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "drain.Profile.PlaceA"
"drain.ProfileA" "drain.Profile.RegionA" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------

;------------------------------------------------------------
;------- Source Side, Main Doping ---------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;------------------------------------------------------------
(isedr:define-refinement-window "source.Profile.RegionA" "Rectangle"
(position (- gatexmin 0.02) gateymax 0) (position (- gatexmin 0.385)
gateymin 0))
(isedr:define-gaussian-profile "source.ProfileA"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceA"
"source.ProfileA" "source.Profile.RegionA" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------
```

```
;-------------------------------------------------------------
;------- Channel Engineering and VT Adjustments ------------
; Most of this information was derived from IRTS Roadmap - 2000
;-------------------------------------------------------------

;-------------------------------------------------------------
;------- Threshold Voltage Adjust Implant ------------------
; Peak at surface - 1.8E18
; Gausian Profile with 6.2E17 at depth of 10nm
; Extends to +/- 15nm outide of the gate edges in X direction (length
direction)
; 1.8E18, 6.2E17, and 10nm matched the SPICE model for long channel
devices (450nm was calibration length)
;-------------------------------------------------------------
(isedr:define-refinement-window "implant.Profile.RegionA" "Rectangle"
(position (- gatexmin 0.015) gateymax 0) (position (+ gatexmax 0.015)
gateymin 0))
(isedr:define-gaussian-profile "implant.ProfileA"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1.8E18 "ValueAtDepth"
6.2E17 "Depth" .010 "Gauss" "Factor" 0.001)
(isedr:define-analytical-profile-placement "implant.Profile.PlaceA"
"implant.ProfileA" "implant.Profile.RegionA" "Symm" "NoReplace" "Eval")
;-------------------------------------------------------------

;-------------------------------------------------------------
;------- Halo Implant A for Drain to Source Leakage --------
; Peak at 37.5nm below surface - 1E18
; Gausian Profile with 1E17 at depth of +/-37.5nm
; Extends from 5nm inside the gate edge to 55nm inside the gate edge
; 55nm was a tuned parameter to get leakage and threshold correct when
compared to SPICE model
; Significant for short channel devices (180nm calibration length)
;-------------------------------------------------------------
(isedr:define-refinement-window "limplant.Profile.RegionA" "Rectangle"
(position (+ gatexmin 0.005) gateymax 0.0375) (position (+ gatexmin
0.055) gateymin 0.0375))
(isedr:define-gaussian-profile "limplant.ProfileA"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1E18 "ValueAtDepth"
1E17 "Depth" 0.0375 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceA"
"limplant.ProfileA" "limplant.Profile.RegionA" "Symm" "NoReplace"
"Eval")
;-------------------------------------------------------------
```

```
;------------------------------------------------------------
;------- Halo Implant B for Drain to Source Leakage --------
; Peak at 37.5nm below surface - 1E18
; Gausian Profile with 1E17 at depth of +/-37.5nm
; Extends from 5nm inside the gate edge to 55nm inside the gate edge
; 55nm was a tuned parameter to get leakage and threshold correct when
compared to SPICE model
; Significant for short channel devices (180nm calibration length)
;------------------------------------------------------------
(isedr:define-refinement-window "limplant.Profile.RegionB" "Rectangle"
(position (- gatexmax 0.055) gateymax 0.0375) (position (- gatexmax
0.005) gateymin 0.0375))
(isedr:define-gaussian-profile "limplant.ProfileB"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1E18 "ValueAtDepth"
1E17 "Depth" 0.0375 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "limplant.Profile.PlaceB"
"limplant.ProfileB" "limplant.Profile.RegionB" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------



;------------------------------------------------------------
;------- MESHING - Original scheme, results in ~550k elements
;------------------------------------------------------------
;------------------------------------------------------------
; P-well and Deep P Implant Meshing
; Top part of the bulk silicon
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole" 0.75 0.75 0.75 0.1 0.1 0.1)
(isedr:define-refinement-window "window.whole" "Cuboid" (position
subxmax subymin 0) (position subxmin subymax 1.2))
(isedr:define-refinement-function "size.whole" "DopingConcentration"
"MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.whole" "size.whole"
"window.whole" )

(isedr:define-refinement-size "size.STImesh_A" 0.5 0.5 0.5 0.05 0.05
0.05)
(isedr:define-refinement-window "window.STImesh_A" "Cuboid" (position
(+ gatexmax 0.38) gateymax 0) (position (+ gatexmax 1.2) gateymin 0.5))
(isedr:define-refinement-function "size.STImesh_A"
"DopingConcentration" "MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.STImesh_A"
"size.STImesh_A" "window.STImesh_A" )

(isedr:define-refinement-size "size.STImesh_B" 0.5 0.5 0.5 0.05 0.05
0.05)
(isedr:define-refinement-window "window.STImesh_B" "Cuboid" (position
(- gatexmin 0.38) gateymax 0) (position (- gatexmin 1.2) gateymin 0.5))
(isedr:define-refinement-function "size.STImesh_B"
"DopingConcentration" "MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.STImesh_B"
"size.STImesh_B" "window.STImesh_B" )
```

```
(isedr:define-refinement-size "size.TOP_A" 0.25 0.25 0.25 0.01 0.01
0.01)
(isedr:define-refinement-window "window.TOP_A" "Cuboid" (position (-
subxmax 0.45) subymin 0) (position subxmax subymax 0.5))
(isedr:define-refinement-function "size.TOP_A" "DopingConcentration"
"MaxTransDiff" 0.3)
(isedr:define-refinement-placement "placement.TOP_A" "size.TOP_A"
"window.TOP_A" )

;------------------------------------------------------------

;------------------------------------------------------------
; Bottom part of the bulk silicon
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole2" 0.75 0.75 0.75 0.5 0.5 0.5)
(isedr:define-refinement-window "window.whole2" "Cuboid" (position
subxmin subymin 1.2) (position subxmax subymax 10))
(isedr:define-refinement-placement "placement.whole2" "size.whole2"
"window.whole2" )
;------------------------------------------------------------

;------------------------------------------------------------
; Mesh at P-well / N-well junctions
;------------------------------------------------------------
; "Top"
(isedr:define-refinement-size "size.dopingmesha" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmesha"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesha" "Cuboid" (position
(- gatexmin 1.9) (+ gateymax 1.1)  0) (position (+ gatexmax 1.9) (+
gateymax 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmesha"
"size.dopingmesha" "window.dopingmesha" )

; "Bottom"
(isedr:define-refinement-size "size.dopingmeshb" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshb"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshb" "Cuboid" (position
(- gatexmin 1.9) (- gateymin 1.1)  0) (position (+ gatexmax 1.9) (-
gateymin 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshb"
"size.dopingmeshb" "window.dopingmeshb" )

; "Left"
(isedr:define-refinement-size "size.dopingmeshc" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshc"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshc" "Cuboid" (position
(+ gatexmax 1.6) (- gateymin 1.3)  0) (position (+ gatexmax 2.0) (+
gateymax 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshc"
"size.dopingmeshc" "window.dopingmeshc" )
```

```
; "Right"
(isedr:define-refinement-size "size.dopingmeshd" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshd"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshd" "Cuboid" (position
(- gatexmin 1.6) (- gateymin 1.3)  0) (position (- gatexmin 2.0) (+
gateymax 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshd"
"size.dopingmeshd" "window.dopingmeshd" )



; "Left" Outer N-well/substrate junction
(isedr:define-refinement-size "size.dopingmeshe" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshe"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshe" "Cuboid" (position
(+ gatexmax 3.7) (- gateymin 1.3)  0) (position (+ gatexmax 3.9) (+
gateymax 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshe"
"size.dopingmeshe" "window.dopingmeshe" )

; "Right"
(isedr:define-refinement-size "size.dopingmeshf" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshf"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshf" "Cuboid" (position
(- gatexmin 3.7) (- gateymin 1.3)  0) (position (- gatexmin 3.9) (+
gateymax 1.3) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshf"
"size.dopingmeshf" "window.dopingmeshf" )

; "Bottom"
(isedr:define-refinement-size "size.dopingmeshg" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshg"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshg" "Cuboid" (position
(+ gatexmax 3.9) (- gateymin 3.2)  0) (position (- gatexmin 3.9) (-
gateymin 3.5) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshg"
"size.dopingmeshg" "window.dopingmeshg" )

; "Top"
(isedr:define-refinement-size "size.dopingmeshh" 0.2 0.2 0.2 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshh"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshh" "Cuboid" (position
(+ gatexmax 3.9) (+ gateymax 3.2)  0) (position (- gatexmin 3.9) (+
gateymax 3.5) 0.8))
(isedr:define-refinement-placement "placement.dopingmeshh"
"size.dopingmeshh" "window.dopingmeshh" )
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Added mesh for buried n-well / substrate junctions
;------------------------------------------------------------
 (isedr:define-refinement-size "size.dopingmeshc" 0.1 0.1 0.1 0.01 0.01
0.01)
(isedr:define-refinement-function "size.dopingmeshc"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshc" "Cuboid" (position
subxmin subymin  0) (position subxmax subymax 0.9))
(isedr:define-refinement-placement "placement.dopingmeshc"
"size.dopingmeshc" "window.dopingmeshc" )

;------------------------------------------------------------
; Dynamic Mesh in Z Axis to refine the channel and LDD Mesh
;------------------------------------------------------------
(isedr:define-multibox-size "MBSize_x" 0.02 0.1 0.02 0.001 0.002 0.001
1 1 3 )
(isedr:define-refinement-window "MBWindow.xn1" "Cuboid"  (position (-
gatexmin 0.015) gateymin 0) (position (+ gatexmax 0.015) gateymax
0.06))
(isedr:define-multibox-placement "MBPlace.xn1" "MBSize_x"
"MBWindow.xn1" )
;------------------------------------------------------------

;------------------------------------------------------------
; Refine the Drain, Source, and Channel over whole active area
;------------------------------------------------------------
(isedr:define-refinement-size "active" 0.05 0.1 0.05 0.005 0.02 0.005)
(isedr:define-refinement-window "active" "Cuboid" (position (- gatexmin
0.4) gateymin 0) (position (+ gatexmax 0.4) gateymax 0.2))
(isedr:define-refinement-function "active" "DopingConcentration"
"MaxTransDiff" 0.3)
(isedr:define-refinement-placement "active" "active" "active" )
;------------------------------------------------------------


;------------------------------------------------------------
; Save the resulting file
;------------------------------------------------------------
(ise:save-model "n@node@_msh")
;------------------------------------------------------------
;-----------------------EOF----------------------------------
```

A.2.3 Sample “3-D SE Transient” sdevice heavy-ion simulation script:

```
File  {
  Plot    = "n@node@_des.dat"
  Current = "n@node@_des.plt"
  SPICEPath = "." ###path where your spice models are ###
      }

DEVICE NMOS {
File  {
        Grid    = "@grid@"
        Doping  = "@doping@"
      }

Electrode {

      { Name="DrainA"          Voltage=0.0 }
      { Name="GateA"           Voltage=0.0 }
      { Name="SourceA"         Voltage=0.0 }
      { Name="Pwell"           Voltage=0.0 }
      { Name="Substrate"       Voltage=0.0 }

      }

Physics {
      Recombination(SRH Auger) #TPA_gen
      Mobility( Phumob HighFieldsat Enormal)
      EffectiveIntrinsicDensity( OldSlotboom )
      Fermi
      HeavyIon(
      time=1e-9
      length=11
      wt_hi=0.05
      location=(0.1825,0,0)
      direction=(0,0,1)
      LET_f=0.5
      Gaussian
      Picocoulomb )

      }


Plot  {
        Potential Electricfield
        eDensity hDensity
        eCurrent/Vector hCurrent/Vector
        TotalCurrent/Vector
        SRH Auger Avalanche
        eMobility hMobility
        eQuasiFermi hQuasiFermi
        eGradQuasiFermi hGradQuasiFermi
        eEparallel hEparallel
        eMobility hMobility
        eVelocity hVelocity
        DonorConcentration Acceptorconcentration
```

```
        Doping SpaceCharge
        ConductionBand ValenceBand
        BandGap Affinity
        xMoleFraction
        eTemperature hTemperature
        HeavyIonChargeDensity
      }
}

Math  {
  WallClock
  Extrapolate
  Derivatives
  RelErrControl
  Iterations=15
  notdamped=100
  -Newdiscretization
  Method=ILS
  RecBoxIntegr
  ExitOnFailure
  Transient=BE
      }


System      {

      Vsource_pset VDD  (HIGH 0)  {dc = 1.8}  ###voltage source (HIGH
0) are node names###

      Vsource_pset GROUND (GD 0)  {dc = 0.0}  ###voltage source (GD 0)
are node names###

      Vsource_pset DATAA (A1 0)   {dc = 0.0}  ###voltage source (A1 0)
are node names###



      NMOS  device1     (
                   "DrainA"=A3
                   "GateA"=A2
                   "SourceA"=A4
                   "Substrate"=GD
                   "Pwell"=GD)


       Resistor_pset R1 (A3 HIGH) { resistance = 2.917e3 }
       Capacitor_pset C1 (A3 GD) { capacitance = 10e-15 }



Initialize (A2 = 0.0)
Initialize (A4 = 0.0)



      Plot "n10_initial" (time()  v(A1) v(A2) v(A3) v(A4))
}
```

```
Solve{
    Coupled (iterations=100) {Circuit}
    Coupled (iterations=100) {Poisson}
    Coupled (iterations=100) {Poisson Circuit}
    Coupled (iterations=100) {Poisson Circuit Contact}
    Coupled (iterations=100) {Poisson Hole Contact Circuit}
    Coupled (iterations=100) {Poisson Electron Hole Contact Circuit}



NewCurrentFile="n@node@_transient"


Transient (
    InitialTime=0
    FinalTime=9.99e-10
    InitialStep=1e-12
    MaxStep=1e-10
      )
    { Coupled (Iterations=25 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
    }

Transient (
    InitialTime=9.99e-10
    FinalTime=1.001e-9
    InitialStep=2e-13
    MaxStep=1e-12
      )
    { Coupled (Iterations=25 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}

Plot ( FilePrefix="n@node@_strTNA_hit_chain" Time=(1e-9) NoOverwrite)
    }

Transient (
    InitialTime=1.001e-9
    FinalTime=1.25e-9
    InitialStep=5e-12
    MaxStep=5e-12
    )
    { Coupled (Iterations=25 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}

Plot ( FilePrefix="n@node@_imTNA_hit_chain" Time=(1.01e-9;1.05e-9;1.1e-
9;1.25e-9) NoOverwrite)
    }
```

```
Transient (
    InitialTime=1.25e-9
    FinalTime=2.25e-9
    InitialStep=1e-11
    MaxStep=1e-11
    )
    { Coupled (Iterations=25 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}

Plot ( FilePrefix="n@node@_laterTNA_hit_chain" Time=(1.5e-9;2e-9;2.25e-
9) NoOverwrite)

    }


Transient (
    InitialTime=2.25e-9
    FinalTime=5e-9
    InitialStep=1e-10
    MaxStep=1e-10 )
    { Coupled (Iterations=25 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}

Plot ( FilePrefix="n@node@_later2TNA_hit_chain" Time=(1.5e-9;2e-
9;2.25e-9) NoOverwrite)

    }

}
```

A.2.4 Sample 2-D latchup structure script:

```
;------------------------------------------------------------
; IBM 7RF/SF Device File
; Standard latchup test structure - industry standard
;------------------------------------------------------------
; Jeff Kauppila and Cody Dinkins
; Under the Draper IR&D 2009 Contract
;------------------------------------------------------------


;------------------------------------------------------------
; Define Variables and Major Dimensions
;------------------------------------------------------------
;-----Substrate Dimensions-----
(define subxmin -5.0)  ;2D/3D X-direction max / leftside extension
(define subxmax  5.0)  ;2D/3D X-direction max / rightside extension
(define subymin    0)  ;2D Y-direction max / frontside extension
(define subymax   5)   ;2D Y-direction max / backside extension

;-----Implant Dimensions-----
(define xmin_n 0.42)
(define xmax_n (+ xmin_n @W_N@))

(define xmax_p -0.42)
(define xmin_p (- xmax_p @W_P@))

;------------------------------------------------------------
;------------------------------------------------------------
; ABA means old replaces new
;------------------------------------------------------------
(isegeo:set-default-boolean "ABA")
;------------------------------------------------------------

;-------BEGIN DEVICE CREATION------

;------------------------------------------------------------
;-------- DEVICE REGIONS, STI, AND METAL CONTACTS ----------
;------------------------------------------------------------
;------------------------------------------------------------

;------------------------------------------------------------
; Full silicon bulk creation
;------------------------------------------------------------
(isegeo:create-rectangle  (position subxmin subymin 0) (position
subxmax subymax 0)        "Silicon" "R.Bulk")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Shallow trench isolation STI
;------------------------------------------------------------
(isegeo:create-rectangle (position xmax_p 0 0)   (position xmin_n 0.36
0)  "SiO2" "R.STI1")
(isegeo:create-rectangle (position xmax_n 0 0)   (position (+ (+ xmax_n
0.26) @PW_dist@) 0.36 0)  "SiO2" "R.STI1")
(isegeo:create-rectangle (position (+ (+ xmax_n 0.86) @PW_dist@) 0 0)
(position subxmax 0.36 0)  "SiO2" "R.STI1")
(isegeo:create-rectangle (position xmin_p 0 0)   (position (- (- xmin_p
0.26) @NW_dist@) 0.36 0)  "SiO2" "R.STI1")
(isegeo:create-rectangle (position (- (- xmin_p 0.86) @NW_dist@) 0 0)
(position subxmin 0.36 0)  "SiO2" "R.STI1")



;------------------------------------------------------------
; Contacts defined
;------------------------------------------------------------
(isegeo:define-contact-set "Ndiff"  4.0  (color:rgb 0.0 0.0 1.0 ) "##")
(isegeo:define-contact-set "Pdiff"  4.0  (color:rgb 0.0 0.0 1.0 ) "##")
;(isegeo:define-contact-set "Subs"  4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "PwellA" 4.0  (color:rgb 0.0 1.0 1.0 ) "##")
(isegeo:define-contact-set "NwellA" 4.0  (color:rgb 0.0 1.0 1.0 ) "##")
;------------------------------------------------------------


;------------------------------------------------------------
;--------------------DEFINE CONTACTS-------------------------
;------------------------------------------------------------

;--------------------Substrate contact----------------------
;(isegeo:define-2d-contact (find-edge-id (position 0 subymax 0))
"Substrate")
;------------------------------------------------------------

;--------------------Diffusion contacts---------------------
; N-region
(isegeo:define-2d-contact (find-edge-id (position (+ xmin_n 0.1) 0 0))
"Ndiff")
; N-region P-well
(isegeo:define-2d-contact (find-edge-id (position (+ (+ xmax_n 0.6)
@PW_dist@) 0 0)) "PwellA")
; P-region
(isegeo:define-2d-contact (find-edge-id (position (- xmax_p 0.1) 0 0))
"Pdiff")
; P-region N-well
(isegeo:define-2d-contact (find-edge-id (position (- (- xmin_p 0.6)
@NW_dist@) 0 0)) "NwellA")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Silicon substrate - Constant doping - P-Type
;------------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Rectangle"
(position subxmin subymin 0) (position subxmax subymax 0))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;------------------------------------------------------------


;------------------------------------------------------------
; Deep P Implant - Boron doping in the silicon
; Assumes deep pwell implant goes through whole die
;------------------------------------------------------------
;Matches profile from ChipWorks report
(isedr:define-refinement-window "Window.DeepPWell.Bor.1" "Line"
(position subxmax 1.25 0) (position subxmin 1.25 0))
(isedr:define-gaussian-profile "Profile.DeepPWell.Bor.1"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 1e18 "ValueAtDepth"
1e16 "Depth" 0.5 "Gauss" "Factor" 0.0001)
(isedr:define-analytical-profile-placement "Place.DeepPWell.Bor.1"
"Profile.DeepPWell.Bor.1" "Window.DeepPWell.Bor.1" "Symm" "NoReplace"
"Eval")
;------------------------------------------------------------


;------- Begin N-region-------------
;------------------------------------------------------------
; Retrograde P-well implant
; Matches profile from ChipWorks report
;------------------------------------------------------------
(isedr:define-refinement-window "Window.PWellA.Bor.2" "Line" (position
0 0.45 0) (position 5 0.45 0))
(isedr:define-gaussian-profile "Profile.PWellA.Bor.2"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.PWellA.Bor.2"
"Profile.PWellA.Bor.2" "Window.PWellA.Bor.2" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Pwell contact doping:
; This section defines both the "top" and "bottom" Pwell contact
"strip" dopings required for the guard drain layout
; Guard drain, single-device version
;------------------------------------------------------------
(isedr:define-refinement-window "Window.PWellCon_Bottom.Bor.3B" "Line"
(position (+ (+ xmax_n 0.26) @PW_dist@) 0 0) (position (+ (+ xmax_n
0.86) @PW_dist@) 0 0))
(isedr:define-gaussian-profile "Profile.PWellCon_Bottom.Bor.3B"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement
"Place.PWellCon_Bottom.Bor.3B" "Profile.PWellCon_Bottom.Bor.3B"
"Window.PWellCon_Bottom.Bor.3B" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------



;------------------------------------------------------------
;------------------ N-region doping-------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;------------------------------------------------------------
(isedr:define-refinement-window "source.Profile.RegionN" "Line"
(position xmin_n 0 0) (position xmax_n 0 0))
(isedr:define-gaussian-profile "source.ProfileN"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceN"
"source.ProfileN" "source.Profile.RegionN" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------


;------- End N-region-------------


;------- Begin P-region-------------
;------------------------------------------------------------
; Retrograde N-well implant
; Matches profile from ChipWorks report
;------------------------------------------------------------
(isedr:define-refinement-window "Window.NWellA.Bor.2" "Line" (position
0 0.45 0) (position -5 0.45 0))
(isedr:define-gaussian-profile "Profile.NWellA.Bor.2"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 2e17 "ValueAtDepth"
2e16 "Depth" 0.45 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWellA.Bor.2"
"Profile.NWellA.Bor.2" "Window.NWellA.Bor.2" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Nwell contact doping
; This section defines both the "top" and "bottom" Nwell contact
"strip" dopings required for the guard drain layout
; Guard drain, single-device version
;------------------------------------------------------------
(isedr:define-refinement-window "Window.NWellCon_Top.Bor.3A" "Line"
(position (- (- xmin_p 0.26) @NW_dist@) 0 0) (position (- (- xmin_p
0.86) @NW_dist@) 0 0))
(isedr:define-gaussian-profile "Profile.NWellCon_Top.Bor.3A"
"ArsenicActiveConcentration" "PeakPos" 0 "PeakVal" 9e19 "ValueAtDepth"
3e17 "Depth" 0.08 "Gauss" "Factor" 0.01)
(isedr:define-analytical-profile-placement "Place.NWellCon_Top.Bor.3A"
"Profile.NWellCon_Top.Bor.3A" "Window.NWellCon_Top.Bor.3A" "Symm"
"NoReplace" "Eval")
;------------------------------------------------------------


;------------------------------------------------------------
;------------------ P-region doping-------------------------
; Peak at surface - 8E19
; Gausian Profile with 1E17 at depth of 0.12um
;------------------------------------------------------------
(isedr:define-refinement-window "source.Profile.RegionP" "Line"
(position xmin_p 0 0) (position xmax_p 0 0))
(isedr:define-gaussian-profile "source.ProfileP"
"BoronActiveConcentration" "PeakPos" 0 "PeakVal" 8e19 "ValueAtDepth"
1e17 "Depth" 0.12 "Gauss" "Factor" 0.1)
(isedr:define-analytical-profile-placement "source.Profile.PlaceP"
"source.ProfileP" "source.Profile.RegionP" "Symm" "NoReplace" "Eval")
;------------------------------------------------------------



;------------------------------------------------------------
;------- MESHING --------------------------------------------
;------------------------------------------------------------
;------------------------------------------------------------

;------------------------------------------------------------
; Top part of the bulk silicon: N- and P-wells
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole" 0.25 0.25 0.125 0.1250
0.1250 0.125)
(isedr:define-refinement-window "window.whole" "Rectangle" (position
subxmax 0 0) (position subxmin 2 0))
(isedr:define-refinement-function "size.whole" "DopingConcentration"
"MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.whole" "size.whole"
"window.whole" )
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; P-well and N-well junction refined meshing
;------------------------------------------------------------
;------------------------------------------------------------
(isedr:define-refinement-size "size.junct" 0.1 0.1 0.1 0.05 0.05 0.05)
(isedr:define-refinement-window "window.junct" "Rectangle" (position
subxmax 0 0) (position subxmin 1 0))
(isedr:define-refinement-function "size.junct" "DopingConcentration"
"MaxTransDiff" 0.5)
(isedr:define-refinement-placement "placement.junct" "size.junct"
"window.junct" )
;------------------------------------------------------------


;------------------------------------------------------------
; Bottom part of the bulk silicon (below well implants)
;------------------------------------------------------------
(isedr:define-refinement-size "size.whole2" 0.75 0.75 0.75 0.5 0.5 0.5)
;------------------------------------------------------------
; Silicon substrate - Constant doping - P-Type
;------------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Rectangle"
(position subxmin subymin 0) (position subxmax subymax 0))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;------------------------------------------------------------
;------------------------------------------------------------
; Silicon substrate - Constant doping - P-Type
;------------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Rectangle"
(position subxmin subymin 0) (position subxmax subymax 0))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;------------------------------------------------------------
;------------------------------------------------------------
; Silicon substrate - Constant doping - P-Type
;------------------------------------------------------------
(isedr:define-refinement-window "Window.Silconst.Bor" "Rectangle"
(position subxmin subymin 0) (position subxmax subymax 0))
(isedr:define-constant-profile "Profile.Silconst.Bor"
"BoronActiveConcentration" 1e16)
(isedr:define-constant-profile-placement "Place.Silconst.Bor"
"Profile.Silconst.Bor" "Window.Silconst.Bor")
;------------------------------------------------------------
(isedr:define-refinement-window "window.whole2" "Rectangle" (position
subxmin 2 0) (position subxmax subymax 0))
(isedr:define-refinement-placement "placement.whole2" "size.whole2"
"window.whole2" )
;------------------------------------------------------------
```

```
;------------------------------------------------------------
; Mesh around the N- and P-Well Contacts
;------------------------------------------------------------
; NFET P-well contact
(isedr:define-refinement-size "size.dopingmesha" 0.1 0.1 0.05 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmesha"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmesha" "Rectangle"
(position (+ xmax_n 0.2) 0 0) (position (+ xmax_n 0.9) 0.4 0))
(isedr:define-refinement-placement "placement.dopingmesha"
"size.dopingmesha" "window.dopingmesha" )
; PFET N-well contact
(isedr:define-refinement-size "size.dopingmeshb" 0.1 0.1 0.05 0.05 0.05
0.05)
(isedr:define-refinement-function "size.dopingmeshb"
"DopingConcentration" "MaxTransDiff" 1)
(isedr:define-refinement-window "window.dopingmeshb" "Rectangle"
(position (- xmin_p 0.2) 0 0) (position (- xmin_p 0.9) 0.4 0))
(isedr:define-refinement-placement "placement.dopingmeshb"
"size.dopingmeshb" "window.dopingmeshb" )
;------------------------------------------------------------


;------------------------------------------------------------
; Save the resulting file
;------------------------------------------------------------
(ise:save-model "n@node@_msh")
;------------------------------------------------------------
;-----------------------EOF--------------------------------
```

A.2.5 Sample "2-D SE Latchup" sdevice heavy-ion simulation script:

```
####################################################################

File  {
  Plot    = "n@node@_bias_des.dat"
  Current = "n@node@_bias_des.plt"
  Output  = "n@node@_bias.log"
 SPICEPath = "." ###path where your spice models are ###
      }


DEVICE NMOS {
File  {
        Grid    = "@grid@"
        Doping  = "@doping@"
     }


Electrode {

        { Name="Ndiff"         Voltage=0.0 }
        { Name="Pdiff"         Voltage=0.0 }
        { Name="PwellA"        Voltage=0.0 }
  ###   { Name="Substrate"     Voltage=0.0 }
        { Name="NwellA"        Voltage=0.0 }

     }


Physics {
      Recombination(SRH Auger Avalanche) #TPA_gen
      Mobility( Phumob HighFieldsat Enormal)
      EffectiveIntrinsicDensity( OldSlotboom )
      Fermi
      Temperature = 398
      HeavyIon(
      time=10e-9
      length=11
      wt_hi=0.05
      location=(@XLOC@,@YLOC@,@ZLOC@)
      direction=(-0.8660254, 0.5, 0)
      LET_f=@LET@
      Gaussian
      Picocoulomb )
 }
```

```
Plot  {
        Potential Electricfield
        eDensity hDensity
        eCurrent/Vector hCurrent/Vector
        TotalCurrent/Vector
        SRH Auger Avalanche
        eMobility hMobility
        eQuasiFermi hQuasiFermi
        eGradQuasiFermi hGradQuasiFermi
        eEparallel hEparallel
        eMobility hMobility
        eVelocity hVelocity
        DonorConcentration Acceptorconcentration
        Doping SpaceCharge
        ConductionBand ValenceBand
        BandGap Affinity
        xMoleFraction
        eTemperature hTemperature
        HeavyIonChargeDensity
 }

}

Math {
      WallClock
      Extrapolate
      Derivatives
      RelErrControl
      Iterations=15
      notdamped=100
      Newdiscretization
      Method=ILS
      RecBoxIntegr
      ExitOnFailure
      Transient=BE
      Number_of_threads=1
 }


File  {
      Output = "LOG_LET_@LET@_log.out"
      SPICEPath = "."
#     Load(FilePrefix= "Biased_Amplifier_Cascode_Alone")
#     Parameter = "pmos.par"
    }


System {
 Vsource_pset  VDD  (VDD 0)  {dc = 1.8}  ###voltage source (HIGH 0) are node names###
 Vsource_pset  HIGH (HIGH 0) {dc = 1.8}  ###voltage source (HIGH 0) are node names###
 Vsource_pset  LOW  (LOW 0)  {dc = 0.0}  ###voltage source (HIGH 0) are node names###
 Vsource_pset  VSS  (VSS 0)  {dc = 0.0}  ###voltage source (HIGH 0) are node names###
```

```
######## mosfet (drain gate source bulk)  ###################
###This is the TCAD device,I am referencing the device above, and
connecting the electrodes to spice nodes##
 NMOS device1 (
    "Pdiff"= HIGH
    "Ndiff"= LOW
    "NwellA"= VDD
    "PwellA"= VSS
### "Substrate"= 0

)

}

Solve{

NewCurrentFile="Results_LET_@LET@_n@node@_transient"


Transient (
    InitialTime=0
    FinalTime=9.90e-9
    InitialStep=1e-12
    MaxStep=1e-9
      )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
        }

Transient (
    InitialTime=9.900E-9
    FinalTime=9.980e-9
    InitialStep=10e-12
    MaxStep=10e-12
      )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_1_T0-1n"
Time=(9.901e-9) NoOverwrite)
        }

Transient (
    InitialTime=9.980e-9
    FinalTime=10.020e-9
    InitialStep=1e-12
    MaxStep=1e-12
      )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_2_T0-20p"
Time=(9.98e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_3_T0" Time=(10e-9)
NoOverwrite)
        }
```

```
 Transient (
    InitialTime=10.020e-9
    FinalTime=10.250e-9
    InitialStep=5e-12
    MaxStep=5e-12
    )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_4_T0+15p"
Time=(10.015e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_5_T0+100p"
Time=(10.1e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_6_T0+200p"
Time=(10.2e-9) NoOverwrite)
        }

  Transient (
    InitialTime=10.25e-9
    FinalTime=11.25e-9
    InitialStep=10e-12
    MaxStep=10e-12
    )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
             Plot ( FilePrefix="Device_LET_@LET@_n@node@_7_T0+500ps"
Time=(10.5e-9) NoOverwrite)
             Plot ( FilePrefix="Device_LET_@LET@_n@node@_8_T0+1ns"
Time=(11e-9) NoOverwrite)
    }

  Transient (
    InitialTime=11.25e-9
    FinalTime=15e-9
    InitialStep=1e-10
    MaxStep=1e-10 )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
        }

  Transient (
    InitialTime=15e-9
    FinalTime=20e-9
    InitialStep=1e-10
    MaxStep=1e-9 )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_9_T0+5ns" Time=(15e-
9) NoOverwrite)
        }
```

```
  Transient (
    InitialTime=20e-9
    FinalTime=300e-9
    InitialStep=1e-9
    MaxStep=1e-8 )
    { Coupled (Iterations=10 Method=ILS) {device1.poisson
device1.electron device1.hole device1.contact circuit}
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+92_10ns"
Time=(20e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+93_20ns"
Time=(30e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+94_30ns"
Time=(40e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+95_40ns"
Time=(50e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+96_50ns"
Time=(60e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+97_100ns"
Time=(110e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+98_200ns"
Time=(210e-9) NoOverwrite)
      Plot ( FilePrefix="Device_LET_@LET@_n@node@_T0+99_300ns"
Time=(310e-9) NoOverwrite)
        }
}

;------------------------------------------------------------
;-----------------------EOF---------------------------------
```

B. Full 2-D latchup simulation response tables

Thus far, only the worst-case strike location (the p+ diffusion) results for 5.0V VDD have been presented in detail. In this section, the full spectrum of single-event latchup responses for each strike location and bias is presented. The following tables are separated by strike location and supply voltage. Within each table, each box is color-coded to distinguish among the following results: true latchup (red box, large **X**), both parasitic BJTs triggered (yellow box, small **x**), or only one or neither BJT triggered (green box, empty). Results tables begin on the following page.

<u>**Single-event latchup results table key**</u>

One / neither BJT triggered:

Both BJTs triggered:

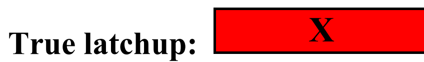
True latchup: 

Table B1: Single-event latchup strike results – Location: P-well contact

P-well contact		No deep-p+ No guard		Deep-p+ No guard		No deep-p+ With guard		Deep-p+ With guard	
Angle	LET	1.8V VDD	5.0V VDD	1.8V VDD	5.0V VDD	1.8V VDD	5.0V VDD	1.8V VDD	5.0V VDD
0	3						x		
	5				x		x		
	10		x		x		x		x
	15		x		x		x		x
	20		x		x		x		x
	25		x		x		x		x
	30		x		x		x		x
	50	x	x	x	x	x	x	x	x
45	3		x				x		
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	x	x	x	x	x	x	x
	50	x	x	x	x	x	x	x	x
60	3	x	x	x	x	x	x		
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	x	x	x	x	x	x	x
	50	x	x	x	x	x	x	x	x

Single-event latchup results table key

One / neither BJT triggered:

Both BJTs triggered: x

True latchup: X

Table B2: Single-event latchup strike results – Location: n+ diffusion

n+ diffusion		No deep-p+ No guard		Deep-p+ No guard		No deep-p+ With guard		Deep-p+ With guard	
Angle	**LET**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**
0	3		x		x	x	x		
	5		x	x	x	x	x		x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	X	x	X	x	x	x	x
	50	x	X	x	X	x	x	x	x
45	3	x	x		x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	X	x	x	x	x
	25	x	X	x	X	x	x	x	x
	30	x	X	x	X	x	x	x	x
	50	x	X	x	X	x	x	x	X
60	3	x	x	x	x	x	x		x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	X	x	X	x	x	x	x
	50	x	X	x	X	x	x	x	X

Single-event latchup results table key

One / neither BJT triggered: (blank)

Both BJTs triggered: x

True latchup: X

Table B3: Single-event latchup strike results – Location: N-well contact

N-well contact		No deep-p+ No guard		Deep-p+ No guard		No deep-p+ With guard		Deep-p+ With guard	
Angle	**LET**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**
0	3								
	5								
	10								
	15								
	20								
	25								
	30								
	50								
45	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X
60	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X

Single-event latchup results table key

One / neither BJT triggered: (green)

Both BJTs triggered: x

True latchup: X

Table B4: Single-event latchup strike results – Location: p+ diffusion

p+ diffusion		No deep-p+ No guard		Deep-p+ No guard		No deep-p+ With guard		Deep-p+ With guard	
Angle	**LET**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**	**1.8V VDD**	**5.0V VDD**
0	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	x	x	x	x	x	x	x
	25	x	x	x	x	x	x	x	x
	30	x	x	x	x	x	x	x	x
	50	x	X	x	X	x	X	x	X
45	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X
60	3	x	x	x	x	x	x	x	x
	5	x	x	x	x	x	x	x	x
	10	x	x	x	x	x	x	x	x
	15	x	x	x	x	x	x	x	x
	20	x	X	x	x	x	X	x	x
	25	x	X	x	X	x	X	x	x
	30	x	X	x	X	x	X	x	x
	50	x	X	x	X	x	X	x	X

Single-event latchup results table key

One / neither BJT triggered: (green cell)

Both BJTs triggered: x

True latchup: X