ANALYSIS OF PARAMETER VARIATION IMPACT ON THE SINGLE EVENT RESPONSE IN SUB-100 NM CMOS STORAGE CELLS

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"Now to Him who is able to do immeasurably more than all we ask or imagine, according to His power that is at work within us, to Him be glory in the church and in Christ Jesus throughout all generations, for ever and ever! Amen." Ephesians 3:20-21

TABLE OF CONTENTS

Page

ACKNOWLEDGMENTS iii

LIST OF TABLES v

LIST OF FIGURES vi

LIST OF ABBREVIATIONS xii

Chapter

I. INTRODUCTION 1
II. TRANSISTOR PARAMETER VARIATION AND SINGLE EVENT OVERVIEW 3
Process Variation 4
Single Event Radiation Overview 11
Impact of Process Variation on Single Event Response 16
III. IMPACT OF PROCESS VARIATIONS ON SRAM SINGLE EVENT UPSETS 20
SRAM Analysis Approach 20
SRAM Analysis 34
SRAM Intradie Analysis 41
IV. IMPACT OF PROCESS VARIATIONS AND CHARGE-SHARING ON THE SINGLE EVENT UPSET RESPONSE OF FLIP-FLOPS 48
V. VERIFICATION OF THE PROCESS VARIATION IMPACT ON SINGLE EVENT UPSET 63
Simulation Results Literature Survey 63
Negative Bias Temperature Instability Literature Survey 67
Negative Bias Temperature Instability Experimental Data 72
VI. IMPACT OF PROCESS VARIATIONS ON UPSET REVERSAL IN A 65 NM FLIP-FLOP 85
Upset Reversal Mechanism 86
Parametric Variation Impact on Upset Reversal 94
Error Source Analysis 102
VII. CONCLUSIONS 106

REFERENCES 110

LIST OF TABLES

Table Page

1. The anticipated percentage of threshold voltage variability due to doping variabilities.....12

2. The critical charge values for the SRAMs with nominal parameter values for off-state NMOS and PMOS hits 28

3. SRAM peak-to-peak upset probability variations.....40

4. Select Parameter Variations from Simulations on the 65 nm Flip-Flop B 43

5. The Correlation Coefficients of the Highest-Impacting Transistor Parameters.....69

6. Current and Future Work Roadmap.....72

LIST OF FIGURES

Figure Page

1. Flash and DRAM ½ Pitch (nm) values by year [30] 5

2. The figure shows data from multiple lithography processes as reported by different laboratories[4]. Line edge roughness does not scale with linewidth. 8

3. The mean number of dopant atoms in the channel according to the technology node[39] 9

4. Current (2005) and anticipated future threshold voltage distributions[39] 11

5. Development of photocurrent from initial ion strike to current / voltage transient[27] 13

6. Soft error failure rate as a function of power supply voltage for multiple manufacturers and technologies[85] 15

7. The probability density function of Q_C values across a memory array[113] 18

8. Histogram of individual values of feedback resistors fabricated in the Sandia IIIA technology. The intended value for each feedback resistor was 400 kΩ[120] 18

9. Variations in the SET pulse width with the variations in threshold voltage. Ten thousand Monte Carlo simulations were conducted on inverters in a 90 nm CMOS process[107] 20

10. The 6T SRAM cell with the hit NMOS and PMOS transistors highlighted 22

11. The number of SRAM upsets that occur at each charge value for an off-state PMOS hit on a 65 nm SRAM cell. The two vertical lines show the range of charge values used for simulations 26

12. The total number of simulation runs and the number of simulation runs that resulted in an upset as assigned to a set of parameter-value segments 28

13. The upset rate of PMOS threshold voltage over its value segment range of the entire Monte-Carlo set of simulations

at an injected charge value of 7.25 fC for an off-state NMOS hit on a 90 nm SRAM 30

14. The extracted upset probability binned by PMOS threshold voltage and injected charge values for an off-state NMOS hit on a 90 nm SRAM 31

15. The extracted upset probability over the PMOS V_{THO} values and injected charge values for an off-state NMOS hit on a 90 nm SRAM. The blue lines represent the upset probability values that would occur if the threshold voltage variation did not impact upset probability 32

16. The differential upset probability is the difference between the parameter-value extracted upset probability and the charge-level upset probability 33

17. The variation in upset probability for PMOS V_{THO} (compared to the charge impact) on the SRAM upset rate over the range of charges for a 90 nm SRAM and an off-state NMOS hit. The peak-to-peak upset probability variation is shown 34

18. The variation in upset probability over the range of PMOS V_{THO} values and the nominal charge-level upset probability for a 90 nm SRAM and an off-state NMOS hit 35

19. The extracted upset probability binned by PMOS V_{THO} values and injected charge values for an off-state NMOS hit on a 65 nm SRAM 36

20. The variation in upset probability for PMOS VTHO (compared to the charge impact) on the SRAM upset rate over the range of charges for a 65 nm SRAM and an off-state NMOS hit 36

21. The impact of TOXE shifts on the relative rate of SRAM upsets for an off-state PMOS hit at 90 nm 38

22. The impact of TOXE shifts on the SRAM differential upset probability for an off-state PMOS hit at 90 nm 38

23. The impact of TOXE shifts on the relative rate of SRAM upsets for an off-state PMOS hit at 65 nm 39

24. The variation in upset probability over the range of PMOS TOXE values and the nominal charge-level upset probability for a 90 nm SRAM and an off-state PMOS hit 39

25. The variation in differential upset probability of SRAM upsets for XL shifts for an off-state NMOS hit at 65 nm 41

26. 6T SRAM cell with labeled transistors..43

27. Variation in upset probability for a single event hit on transistor T5 over the range of extracted threshold voltage values for transistor T1 44

28. The variation in upset probability over the range of T1 V_{THO} values and the nominal charge-level upset probability for a 65 nm SRAM and SE hit on T5...44

29. Variation in upset probability for a single event hit on transistor T5 over the range of extracted width variation values for transistor T1 45

30. Variation in upset probability for a single event hit on transistor T0 over the range of extracted threshold voltage values for transistor T4 46

31. Variation in upset probability for a single event hit on transistor T0 over the range of extracted width variation values for transistor T4 47

32. The charge-level upset probabilities and the ranges of possible upset probability due to interdie threshold voltage variation. The single event strike was simulated on T0 and the upset response was correlated to the PMOS threshold voltage 47

33. The charge-level upset probabilities and the ranges of possible upset probability due to intradie threshold voltage variation. The single event strike was simulated on T0 and the upset response was correlated to the T4 threshold voltage 48

34. The percentage of simulations resulting in an upset for a strike to a transistor that causes upset through charge sharing in flip-flop B..52

35. The percentage of simulations with a threshold voltage value in each segment. The average value of each segment is shown as a fraction of the nominal VTHO value...54

36. The impact of threshold voltage variations on the parameter-value upset probability for a strike in flip-flop B 54

37. The impact of threshold voltage variations on the differential upset probability for flip-flop B...55

38. The impact of TOXE variations on the differential upset probability for flip-flop A 56

39. The impact of TOXE variations on the differential upset probability for flip-flop B 57

40. The variation in upset probability over the range of PMOS TOXE values and the nominal charge-level upset probability for a flip-flop B 57

41. The variation in upset probability for variations in NMOS XL for flip-flop A, a 45 nm flip-flop. The nominal value of XL is negative 59

42. The differential upset probability for variations in NMOS XW for flip-flop A, a 45 nm flip-flop 59

43. Peak-to-peak upset-probability variation values for flip-flop A, a 45 nm flip-flop 60

44. Peak-to-peak upset-probability variation values for flip-flop B, a 65 nm flip-flop 61

45. The ranges of injected charge values for neighboring transistors in FF A. The charge range for a strike on Transistor A is 9fC to 13fC. The charge range for a strike on Transistor B is 52fC to 69fC 63

46. The spread of critical charge values required for a bit flip in a 65 nm CMOS SRAM cell for an off-state NMOS transistor SE strike[107] 65

47. Critical charge as a function of threshold voltages of the transistors in the cross-coupled inverters for the SRAM pictured in Fig. 43 [125] 66

48. SRAM with injected charge onto the drain of M_{nA}. The voltage value at Node A begins at '1' and the value at Node B begins at '0'[125] 67

49. SRAM critical charge as a function of the change in channel length[125] 68

50. Threshold voltage degradation after negative bias temperature stress. The W/L of the device geometries in a) is 10 μm/0.18μm and 10μm/0.5μm in b)[58] 70

51. Simulation results showing the SRAM critical charge as a function of the circuit operating time in years[129] 72

52. Negative bias temperature instability induced increase in SRAM failure count as a function of I^*_{CRIT}[131] 73

53. A simplified schematic of the slave portion of the D-latch 74

54. Layout-aware simulation image highlighting the sensitive NMOS transistors[137] 76

55. Increase in flip-flop upset probability corresponding to the increase in the LET of a SE strike on the most sensitive NMOS transistor. The threshold voltage is nominal and the clock state is HIGH 77

56. NBTI-induced increase in the threshold voltage magnitude of PMOS transistors based on the stress-time[148] 78

57. Change in upset probability due to increase in threshold voltage magnitude due to NBTI 79

58. Comparison of the pre-stress cross-section, the post-stress cross-section, and the process-variation simulation-based post-stress cross-section approximation 81

59. Comparison of the pre-stress cross-section, the post-stress cross-section, and the overall upset probability based estimation of the post-stress cross-section 83

60. Relationship between the change in threshold voltage and the resulting change in flip-flop cross-section for an incident ion LET of 3.49 MeV-cm^2/mg 84

61. A partial schematic of the master-slave flip-flop. It shows the progression of the upset-reversal mechanism 89

62. The voltage signal at the output of inverter 0 (INV0) after a single event strike to the drain of the NMOS transistor in the inverter 89

63. An illustration of the sharing of charge between N_INV0 and T6 after a single-event hit 90

64. The voltage signal at NODE 0 given that insufficient charge is collected by T6 in order to draw current through the transistor. The voltage signal changes from the correct value of LOW to the SE – induced value of HIGH 90

65. The voltage signal at NODE 0 given that sufficient charge is collected by T6. If so, charge collected by T6 prevents the SE–induced transient from changing the voltage at NODE 0 91

66. The voltage signal at the output of INV0 if the reversal charge was reached. The signal changes

back to the correct value of HIGH. The change takes approximately 0.5ns....91

67. The voltage signal at the output of INV0 if the reversal charge was reached. The signal changes back to the correct value of HIGH. The change takes approximately 0.5ns....92

68. The voltage signals at NODE 0 and the output of INV0 given that insufficient charge is collected by T6 in order to cause upset reversal....93

69. The voltage signals at NODE 0 and the output of INV0 given that sufficient charge is collected by T6 in order to cause upset reversal....93

70. The normalized cross-sections for multiple 32 nm devices[144]....95

71. The spectrum of the reversal charge values for a single event hit on the N_INV0....97

72. A scatter plot showing the correlation between the electrical gate oxide thickness and the upset-reversal charge....98

73. A scatter plot showing the correlation between the channel width variation and the upset-reversal charge....99

74. A scatter plot showing the correlation between the channel length variation and the upset-reversal charge....100

75. A scatter plot showing the correlation between the threshold voltage and the upset-reversal charge....101

LIST OF ABBREVIATIONS

β	Charge Enhancement Factor
BTI	Bias Temperature Instability
CGDL	Drain-gate Overlap Capacitance
CGDO	Drain-gate Overlap Capacitance per Unit Channel Width
CJ	Junction Capacitance Density
CJSWG	Gate-side Junction Capacitance
DICE	Dual Interlocked Storage Cells
E_{CM}	Circuit Modeling Error
E_S	Monte-Carlo Sampling Error
E_{TM}	Manufacturer Modeling Error
E_{TOTAL}	Total RMS Error
HCI	Hot-Carrier Injection
HVT	High-V_T
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors

LER	Line Edge Roughness
LET	Linear Energy Transfer
LSB	Least Significant Bit
NBTI	Negative Bias Temperature Instability
PDK	Process Design Kit
PVTI	Process, Voltage, Temperature, and Input
Q_C, Q_{CRIT}	Critical Charge
RCC	Reinforcing Charge Collection
RDF	Random Dopant Fluctuations
RDSW	Resistance per Unit Width
RMS	Root-Mean-Square
SE	Single Event
SEE	Single Event Effects
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SRAM	Standard Random Access Memory

SVT	Standard-V_T
TDDB	Time-Dependent Dielectric Breakdown
TOXE	Electrical Gate Oxide Thickness
U0	Mobility
VLSI	Very Large Scale Integration
VTHO, V_{THO}	Threshold Voltage
XL	Length Variation due to Masking and Etching
XW	Width Variation due to Masking and Etching

CHAPTER I

INTRODUCTION

Over the past few decades, the study of radiation effects has greatly impacted the field of electronics. The design, testing, and implementation of circuits, from the transistor level to the very large scale integration (VLSI) chip level, have been affected by some sub-facet of radiation effects. For example, the advent of circuit simulators, including PREDICT, ECAP, NET-1, CIRCUS, SPICE, and SCEPTRE, was directed, at least in part, by the need to model radiation effects in circuits [1], [2]. Studies show that with shrinking device sizes comes an increased impact of radiation effects, specifically single event radiation, on the performance of military, space, and commercial electronics [3]. The most important era for radiation effects may be in the days ahead.

The study of radiation effects possesses multiple facets. It primarily includes the analysis of total dose radiation, neutron-displacement damage, dose-rate radiation, and single event (SE) radiation. Each subset has different methods of analysis, metrics of error, and approaches to mitigation. All four areas are vital to provide an overall view of how radiation impacts electronic devices and to provide approaches for the amelioration of harmful radiation effects. This work centers on the impact of single event radiation.

In addition to the challenges presented by radiation, transistor and chip design also faces a challenge from the variations that are inherent to the manufacturing process. During chip fabrication, extreme measures are taken to ensure precision. However,

variations in lithography, random dopant fluctuations, gate depletion, surface state charge, and line-edge roughness cause changes in individual transistor behavior and therefore, changes in the behavior-describing transistor parameters. The non-standard behavior then affects circuit performance and therefore impacts single event response. It is anticipated that the effects of process variations will substantially increase with shrinking device sizes. Thus, the potential impact of process variations on SE circuit response is significant. Parameter variations may also occur after the fabrication process. Circuit use, particularly in environments of high electrical, temperature, or mechanical stress, can cause device degradation. Device degradation can impact transistor parameter values and thus affect the functional performance and behavior of a circuit or system. This work analyzes the impact of process variations and device degradation on single-event upset (SEU) response of sub-100 nm CMOS memory storage circuits.

CHAPTER II

TRANSISTOR PARAMETER VARIATION AND SINGLE EVENT OVERVIEW

Predictive ability in circuit design is at the core of the functionality of electronics. The response of a transistor ought to be determined based on the set of inputs. Loss of predictive ability disconnects the efforts of design and purpose from the actual performance of circuits. Both parameter variations and single events can affect the deterministic nature of devices. Parameter variations are caused by fabrication process variations and by device degradation over the lifetime of a circuit. Significant studies have been conducted analyzing the impact of parameter variations, from both sources, on device and chip function [4]-[18]. Also, analyses have been conducted studying the impact of single events on device and chip function. However, the simultaneous impact of both single events and parameter variations due to process variations and device degradations, specifically negative bias temperature instability, has had limited discussion in technological literature. Since the effects of single events and process variations are anticipated to increase with decreasing device sizes [3], [19]-[27], the analysis and discussion of the relationship between single events and parameter variation should be explored.

Process Variation

Since approximately 1959, the number of transistors that can be inexpensively placed on an integrated circuit has doubled approximately every two years, as predicted by Moore's Law [28-30]. One of the reasons for the increase in components is the decrease in device size. Figure 1 shows the DRAM ½ pitch size by year [30]. This decrease in device size has enabled significant increases in technology including increased memory capacity, faster switching times, processing speed, etc.

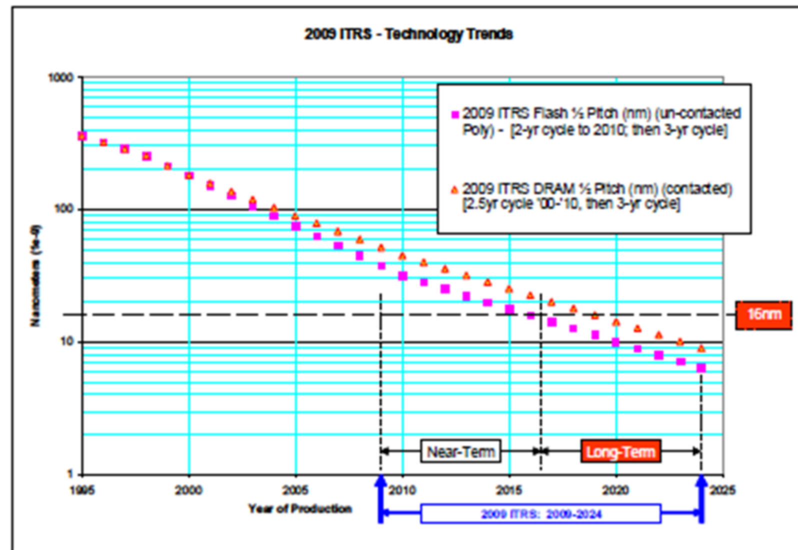

Fig. 1. Flash and DRAM ½ Pitch (nm) values by year [30].

The increasingly small transistor sizes have been enabled through advances in process technology. Improvements in process technology have stemmed from improvements in lithography, materials, patterning, and masks. As devices sizes

decrease, several changes are imposed upon circuits. These include smaller voltage rails, decreased storage node capacitance, and increased operating speeds [3]. Such changes accommodate the continuance of Moore's Law, but contribute to the sensitivity of a circuit to process variations.

The manufacturing processes that produce integrated circuits inherently, like all manufacturing, have process disturbances [26], [31]. Such disturbances result from fluctuations in oven temperature, equipment properties, and chemical properties of materials [26]. They cause process variations, which Duvall defines as "random fluctuations in process conditions and material properties leading to variations in the local or global characteristics of a product" [26]. For instance, chemical polishing results in variations due to non-uniform polishing. The changes in polishing speed result from a non-uniform layout density. The denser portions of the circuit slow the polishing. Thus, the denser portions of the chip are more highly polished than the less-dense portions. This effect can cause differences in the inner-layer dielectric thickness in the thousands of angstroms [25]. Another process disturbance results from lithography issues, which have increased with decreasing device size. The stepper causes a sizeable portion of the variations due to lithography. Stepper lens heating and improper lens focusing cause variabilities during exposure [25]. Additionally, the spin-on resist causes thickness variations, etching causes depth and line-width variations, and doping processes cause random dopant variations [25].

Variations in the manufacturing process may be modeled in multiple ways – using process parameter, physical parameters, model parameters (BSIM4) [32], and electrical/behavioral parameters [26]. When modeled as BSIM4 parameters, the process

variations show the resulting large shifts in the individual transistor parameters. For instance, as the polysilicon gate doping concentration decreases, the gate capacitance decreases [33]-[37]. The degradation is credited to the voltage drop across the gate due to the formation of a depletion layer near the polysilicon/silicon interface [33]. Another manufacturing variation is the variation in the surface-state charge density. Deviations in the charge density cause shifts in the threshold voltage [38]. Variations in channel length, along with variations in threshold voltage, cause increased variation in the standby current [6].

Line edge roughness (LER) results from limitations in the materials and tools used in lithography [4]. LER is becoming an issue of increasing concern since it does not scale with linewidth, as shown in Fig. 2 [4]. LER causes variations in the threshold voltage and may cause enhanced short-channel effects where the channel is shortened by LER [4].

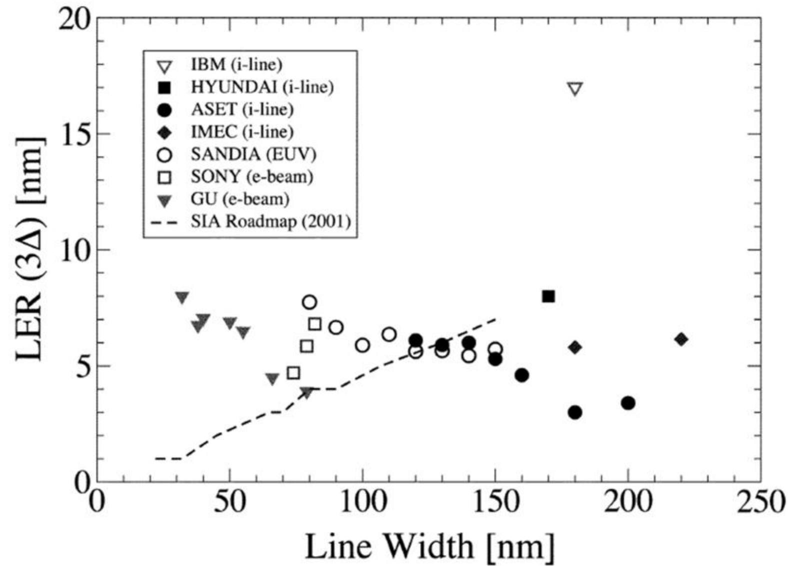

Fig. 2. The figure shows data from multiple lithography processes as reported by different laboratories [4]. Line edge roughness does not scale with linewidth.

Variations in threshold voltage are also caused by random dopant fluctuations (RDF). Random dopant fluctuations result from the finite number of dopant atoms in the channel of a transistor [5], [39], [20]-[21], [40]-[46]. Channel regions are doped to control the threshold voltage of the transistor. Shrinking device sizes have decreased the number of atoms in the channel region so that in the 16 nm – 32 nm devices, the number of atoms in the channel region is in the tens. Fig. 3 shows the decrease in dopant atoms with decreasing device size [39]. The small numbers and discreteness of the atoms in the channel leads to variations in the electrical characteristics of the transistor. The inconsistent distribution of dopant atoms causes variations in the threshold voltage, which in turn affect drive current and transistor performance. One challenge with threshold voltage variations due to RDF is its impact on matching since the threshold voltage values can vary from transistor to transistor [46]. RDF has been discussed for decades in

the literature [44]-[45], [36]-[37] and is anticipated to increase in its impact on circuit performance. One of the earliest discussions of parameter variation and of RDF in the literature was written by William Shockley in 1961. He discussed the impact of the random distribution of dopant atoms on transistor voltages. Research has been conducted to examine the impact of various doping profiles, including undoped channel regions, on the effect of random dopant fluctuations [47]-[49].

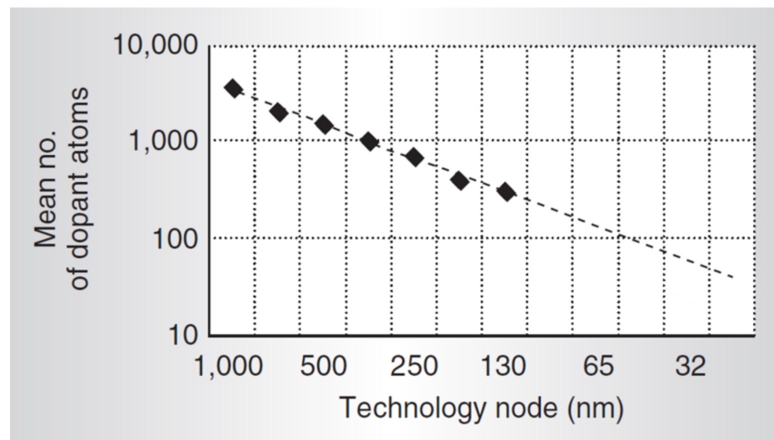

Fig. 3. The mean number of dopant atoms in the channel according to the technology node [39].

Behavioral parameter variations are typically sorted into the categories of die-to-die (interdie) fluctuations and within-die (intradie) fluctuations. Die-to-die fluctuations are the consequence of factors like processing temperature, wafer polishing, and wafer placement [24], [50]. With interdie variations, the general assumption is that the variations do not vary within the die and that the variations equally affect each transistor in the circuit. Within-die variations are the consequence of factors like random dopant fluctuations and channel length variations across a single die [25]. Within-die variations

impact devices across the same die differently. This results in mismatch issues and potentially reduces functional yield [24], [26]. Historically, interdie fluctuations have been considered more significant than intradie variations since the intradie variations have been small in magnitude, compared to interdie variations, and could largely be managed with design techniques. However as device sizes have decreased, intradie variations have increased in magnitude so that they increasingly threaten circuit performance [26]. Both die-to-die and within-die parameter fluctuations are important to circuit performance [50], [51].

The effects of process variations have increased with decreasing device sizes and are anticipated to become a significant concern for circuit performance [39], [22]-[25]. Performance/power variability, device behavioral parameter variability, and "uncontrollable threshold voltage variability" have been identified by the International Roadmap for Semiconductors as key design challenges [30]. Process variability has also been noted as a difficult challenge for reliability and scaling [30]. For example, table I shows the anticipated percentage of threshold voltage variability due to doping variabilities [52]. (The variability is shown as a peak-to-peak difference. For instance, an 81% variation can also be represented as +/- 40.5% from the nominal value.) A significant increase has been shown in the threshold voltage 4-sigma (4-σ) distribution as the gate oxide thickness is decreased from 150 Å to 30 Å. At 150 Å the 4- σ range is less than +/- 2% [20]. A gate oxide thickness of 30 Å corresponds to a 4- σ range of almost +/- 25% [19]. Increased variability will flatten the distribution of threshold voltage as compared to the present distribution, as shown in Fig. 4 [39].

TABLE I.
THE ANTICIPATED PERCENTAGE OF THRESHOLD VOLTAGE VARIABILITY DUE TO DOPING VARIABILITIES [52].

Year of Production	DRAM ½ Pitch (nm) Contacted	% V_{TH} Variability (Doping Variability Impact on V_{TH})
2009	52	40%
2010	45	40%
2011	40	40%
2012	36	58%
2013	32	58%
2014	28	81%
2015	25	81%
2016	22.5	81%
2017	20	81%
2018	17.9	112%
2019	15.9	112%
2020	14.2	112%
2021	12.6	112%
2022	11.3	112%
2023	10.0	112%
2024	8.9	112%

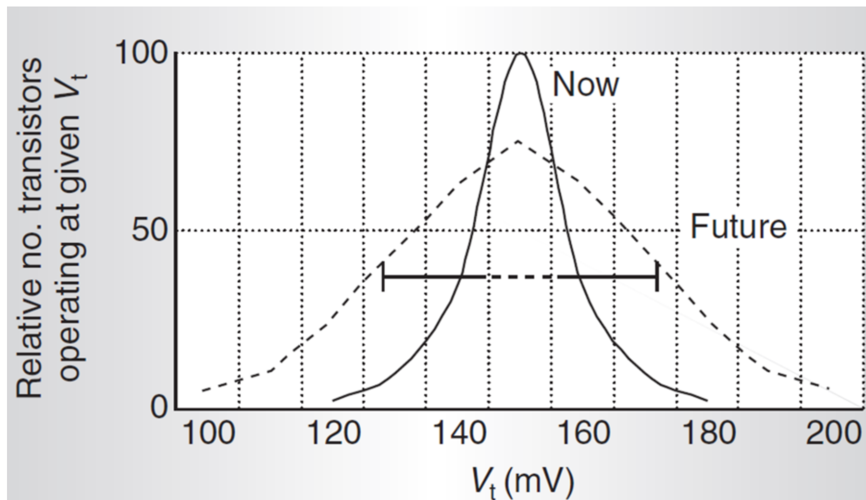

Fig. 4. Current (2005) and anticipated future threshold voltage distributions [39].

The process- and transistor-parameter variations pose a serious challenge for circuit design at advanced technology nodes [43], [53]-[56]. Parameter variations, which model the deviations from nominal transistor behavior caused by process variations, have significant impact on drive current, current leakage, yield problems, timing issues, and power issues. For instance, Unsal reports that parameter-variation-induced gate-delay variability causes a significant portion of the minimum and maximum delay margins at 130nm [25]. Chip design teams must determine how to manage the process variations for both circuit performance and yield problems [24]. Changing design parameters can affect the impact of process variations [22]. Designers must consider variations due to process, voltage, temperature, and input (PVTI) values. The necessary safety margins are becoming an important facet of design [24], [25].

Single Event Radiation Overview

Single event effects (SEE) encapsulates the study of the effect of single event radiation on electronic devices. Single event effects are related to the impact of energetic particles (such as protons, neutrons, alpha particles, or heavy ions) on microelectronic circuits. When an energetic particle strikes a device, some of the energy of the particle may generate electron-hole pairs [57]. Linear energy transfer (LET) is used to describe the amount of energy that is lost by the particle per unit of path length. LET can be correlated to the deposited charge through the guideline that a particle with an LET of approximately 100 MeV-cm^2/mg deposited approximately 1 pC/μm [57]-[58]. As the

particle moves through the semiconducting material, electron-hole pairs are freed [57]-[58]. The electron-hole pairs serve as “new” mobile charge carriers. If the mobile carriers exist in or near a depletion region, the carriers are collected and they produce a photocurrent [59], [60]. The progression from ionized particle to current and voltage transient is shown in Fig. 5 [27].

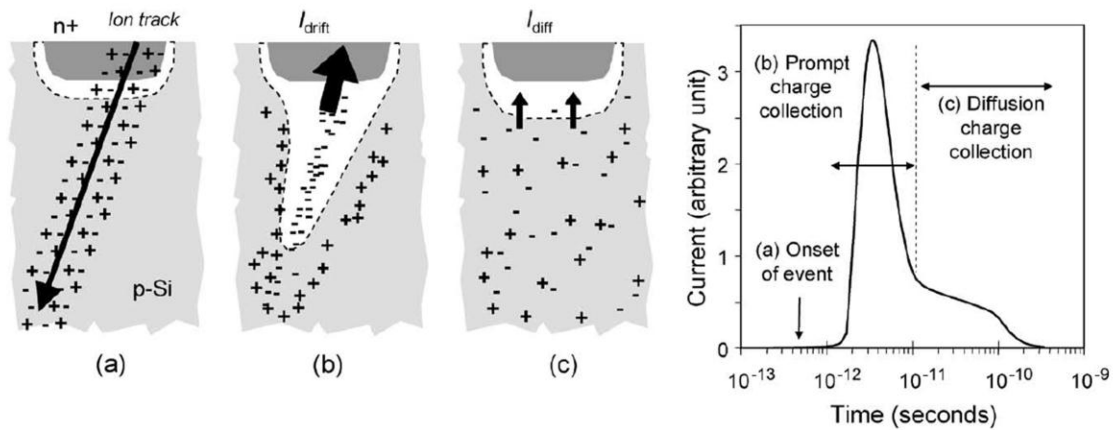

Fig. 5. Development of photocurrent from initial ion strike to current / voltage transient [27].

The impact of the photocurrent depends on the LET of the energetic particle, strike location, circuit topology, and circuit state. An induced photocurrent creates a localized current transient and resulting voltage transient. Such transients are called single event transients (SET). SETs are expected to become the dominant contributor to soft error rates [61]. If a single event transient is latched so that it corrupts stored information, it leads to a single event upset.

Single events were initially predicted by Wallmark and Marcus in 1962 [62] and the anomalies in digital circuits on satellites were attributed to single events, based on experimental testing, in 1975 [63]. Significant works during the 1970's brought attention to the challenges caused by single events and helped spur the area's research [64]-[71]. Pickel and Blandford, in 1978, introduced a model for estimating the cosmic-ray-induced bit error rate and used it to sufficiently estimate the actual bit error rate of dynamic RAMs in an operating satellite system [66]. In 1979, an early report of single event upsets was made by Guenzer et al. during the description of irradiated DRAM circuits [68]. In the same year, single event latchup was first reported in the literature [70]. (Further discussion of the single event history can be found in [58], [72].)

May and Woods reported terrestrial soft errors in 1979. Early terrestrial soft error issues were determined to be the result of alpha-particle emission from radioactive contaminants in chip packaging [65], [73]. Significant effort went into improved packaging material and shielding coatings to prevent terrestrial single event effects [73], [74]. Due to that work, terrestrial single events resulting from alpha particles were a non-issue for a number of years until shrinking device sizes reawakened the issue. However, terrestrial circuits showed sensitivity to upset from particles produced by cosmic rays, particularly neutrons. In 1993, dense SRAM cells were shown to be susceptible to neutron-induced upset at terrestrial levels [75]. Dodd et al. experimentally demonstrated the neutron-induced latchup in high density SRAM cells [76] as shown in Fig. 6. Additionally, neutrons were demonstrated to be the cause of SEUs in implantable cardiac defibrillators [77]. In 2000, it was reported that high-end servers made by Sun Microsystems were susceptible to terrestrial single event radiation [78]. Soft errors from

both alpha-particles and cosmic ray neutrons are a significant concern in terrestrial environments due to decreasing internal circuit capacitances and operating voltages [27], [75], [76], [79]-[81]. In fact, terrestrial soft errors have been noted as a concern for terrestrial electronics below 16 nm in the International Technology Roadmap for Semiconductors (ITRS) [82].

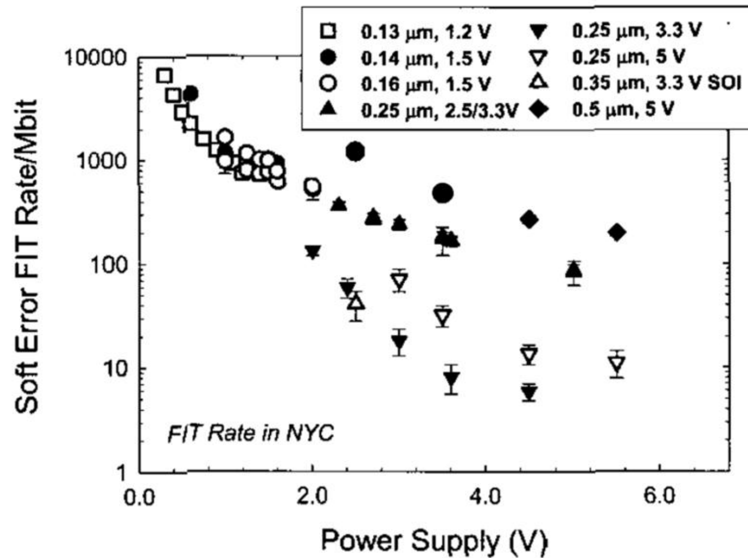

Fig. 6. Soft error failure rate as a function of power supply voltage for multiple manufacturers and technologies [76].

Current deep sub-micron technologies are particularly susceptible to single events. The challenge derives from a conglomeration of effects that affect circuits' radiation response. For instance, decreasing device size has led to decreased storage charge and increased operating speeds [3]. Decreased storage charge contributes to single event sensitivity since the charge deposited by the ionized particle is now more on par

with the storage node charge. The increased operating speeds increase circuit sensitivity since they are now comparable to the speed of a single event transient. It has been postulated that single event transients in digital circuits may set limits on the operating speeds of rad-hard electronics [3]. Without including new mechanisms, scaling rules predict a 43% increase in sensitivity to soft errors per technology generation [83]. Single event upsets are currently the dominant failure mode of all reliability mechanisms (in qualified products) [84]. Not surprisingly, soft errors have been identified as one of the top technology challenges for reliability [30]. Since single events are expected to dominate other reliability concerns in deep sub-micrometer devices due to decreased transistor currents and nodal capacitances, it is vital to understand and quantify the impact of contributing mechanisms.

As technologies continue to scale, single event radiation has resulted in increasingly challenging failure mechanisms in integrated circuits (IC). New phenomena have begun to affect radiation response, including charge sharing [85]-[90], pulse quenching [91], [92], multiple-bit upset [86], [87], [93], [94], and process-parameter variation [95]-[99]. These phenomena add to the complexity of the circuit-level SE response. Charge sharing is a problem for advanced technologies due to decreased storage node charge and increased packing densities [85]-[87]. Charge-sharing occurs because of the diffusion of the carriers in the substrate/well [86] and results in charge collection at multiple nodes to a single incident ion [85]-[88]. It increases the susceptibility to SE radiation of many circuits [85]-[87], including some hardened circuits since more than one storage node can be affected at one time [85], [89]. Techniques used to harden circuits to charge-sharing effects include separating sensitive transistor pairs in

the layout and guard rings [86]. It has, though, been suggested that charge sharing may itself be exploited in specific cases to provide circuit hardening [100]-[102].

Impact of Process Variation on Single Event Response

Variations in process parameters have been demonstrated to significantly affect the single-event response of circuits [95], [97]-[99], [103]-[108]. The impact of parameter variations on radiation response has been discussed, albeit not extensively, in the literature for decades. In 1989, Kohler and Koga discussed the impact that the feedback resistor value has on the minimum linear energy transfer required for upset in SRAMs [109]. A few years later, Massengill et al. discussed the spread of critical charge (Q_C) values as shown by the probability density function in Fig. 7 [103]. It was determined that the spread was due to a variation in the charge enhancement factor (β) due to line width variations, doping variations, and non-uniform dislocation densities of the starting material, along with a distribution of strike locations [103]. Additional work in the 1990's further confirmed the influence of process variations on circuit parameters, as shown in Fig. 8 for feedback resistance [110], and consequently on the single event response of circuits [104], [105], [110], [111].

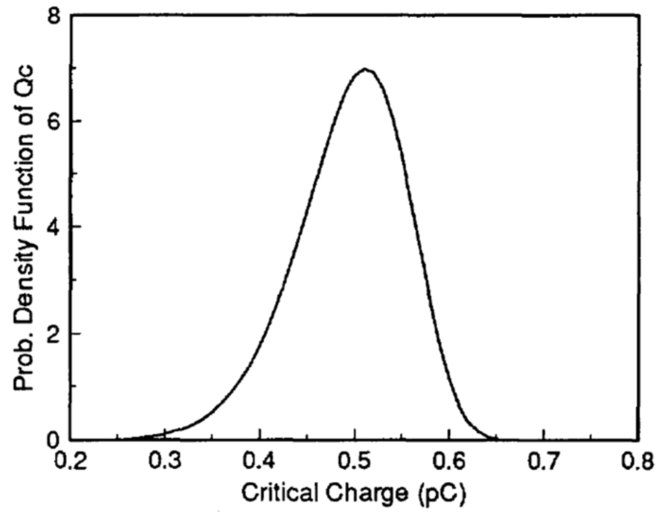

Fig. 7. The probability density function of Q_C values across a memory array [103].

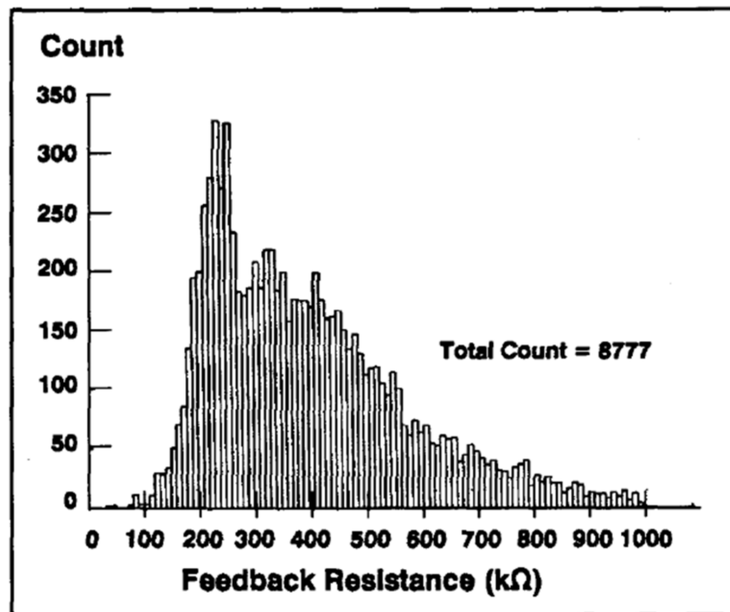

Fig. 8. Histogram of individual values of feedback resistors fabricated in the Sandia IIIA technology. The intended value for each feedback resistor was 400 kΩ [110].

As early as 1998, the impact of process variation on the radiation response of circuits was identified as a challenge in scaled devices [19]. Since that time, the significance of the impact of process variations on circuit performance has increased sizably. Recent work has analyzed the impact of process variation in advanced technologies and has shown that circuits in the sub-100 nm region have a significant SEU sensitivity to process parameter variations [95]-[100]. Balasubramanian examined the impact of the threshold voltage variation on inverter performance. Fig. 9 correlates SET pulse widths with both PMOS and NMOS threshold voltages [98]. A similar study shows the impact of PMOS and NMOS threshold voltages on the critical charge of 130 nm SRAM [99]. A spread in critical charge will significantly affect the overall SRAM cross-section and error rates. In order to accurately predict the single-event response of circuits as device sizes continue to scale, it is necessary to identify and quantify the impact of the specific process variations.

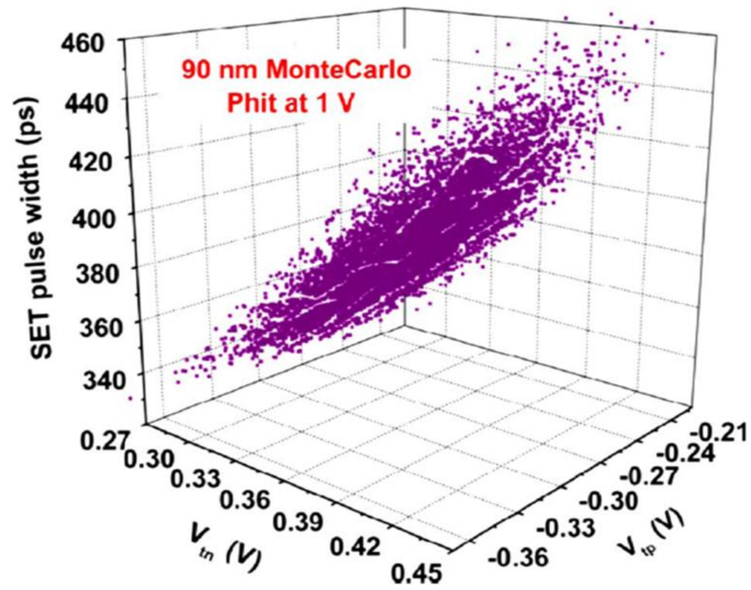

Fig. 9. Variations in the SET pulse width with the variations in threshold voltage. Ten thousand Monte Carlo simulations were conducted on inverters in a 90 nm CMOS process [98].

CHAPTER III

IMPACT OF PROCESS VARIATIONS ON SRAM SINGLE EVENT UPSETS

The impact of process variations are increasing with technology scaling. The resulting transistor parameter variations present challenges for circuit design in the advanced technologies. Single event effects further complicate circuit design difficulties. The interaction between parameter variations and single event response can impact circuit performance. Earlier work acknowledged the impact of process parameter distributions on single event upset cross-section data [103], [104]. This work utilizes Monte-Carlo circuit simulation techniques to assess the impact of process variations.

SRAM Analysis Approach

The impact of process variation on single event response was simulated to determine the impact of each varying parameter. An example study has been carried out on a six transistor (6T) SRAM cell targeted to commercially available 65 nm and 90 nm processes. SE hits were modeled to occur individually on the off-state NMOS and PMOS transistors in the SRAM cell, as shown in Fig. 10. SE currents were modeled using a bias-dependent single-event model that was calibrated to the 90 nm process using 3-D TCAD simulations [112]. The bias-dependent SE model was implemented in Verilog-A

and incorporated into the SPICE BSIM4 transistor model. The single-event models were integrated into the 90 nm process-design kit (PDK) and calibrated using known collection depths and the estimate that a charged particle with an LET of 1 MeV-cm^2/mg deposits approximately 10 fC/µm of track length [57]. The bias-dependent SE model was adapted to work with the 65 nm process design kit (PDK) and the collection length was linearly scaled for the 65 nm technology.

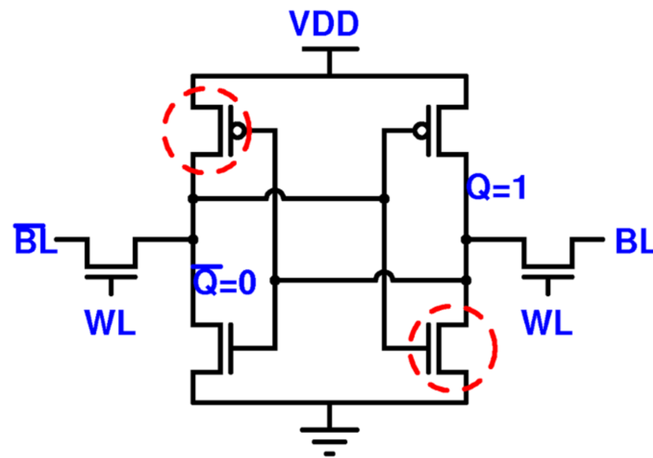

Fig. 10. The 6T SRAM cell with the hit NMOS and PMOS transistors highlighted.

Simulations conducted on the SRAM cells accounted for different SE hit locations by varying the injected-charge value. Simulation studies were performed on each of the processes with the process-nominal supply voltages. In all cases, ten thousand simulations were conducted at several levels of injected charge. The Monte-Carlo simulations provided a representation of the statistical variations during chip manufacturing using the process variabilities included in the process design kits. No single parameter was varied individually since many of the parameters have

interdependencies; all parameters were varied together in accordance with the PDK. For example, channel width and length are related to the threshold voltage value. Also, the mobility is related to the oxide thickness and threshold voltage. A list of the varying parameters is shown in Tables II and III for 90 nm and 65 nm respectively. The parameter variation was accomplished globally (local mismatch was not included). The Monte-Carlo parameter space is the manufacturer's representation of the real-world process variations seen in fabrication. These process variabilities are reflected in shifts in the SPICE transistor parameters. While all model parameter shifts were included in the simulations, the analysis isolated the impact of each parameter. The total number of analyzed parameters was reduced by removing from analysis all parameters that were directly correlated with another parameter. The injected-charge value ranged from a level at which none of the ten thousand simulations resulted in an upset to a level at which all ten thousand simulations resulted in upsets. The charge values were incremented in 0.25 fC steps in between these levels for all other simulations.

TABLE II
VARYING PARAMETERS FOR THE 90 NM CMOS PROCESS

Name	Description	Type
cgdl	Overlap capacitance between gate and lightly-doped drain region	Electrical
cgdo	Non-LDD region drain-gate overlap capacitance per unit channel width	Electrical
cgsl	Overlap capacitance between gate and lightly-doped source region	Electrical
cgso	Non-LDD region source-gate overlap capacitance per unit channel width	Electrical
cj	Zero-bias junction bottom capacitance density	Electrical
cjd	Zero-bias bottom junction capacitance per unit area	Electrical
cjs	Zero-bias bottom junction capacitance per unit area	Electrical
cjsw	Zero-bias junction sidewall capacitance density	Electrical
cjswd	Zero-bias junction sidewall capacitance density	Electrical
cjswg	Zero-bias gate side junction capacitance density	Electrical
cjswgd	Zero-bias gate side junction capacitance density	Electrical
cjswgs	Zero-bias gate side junction capacitance density	Electrical
cjsws	Zero-bias junction sidewall capacitance density	Electrical
dlc	Delta L for capacitance model	Electrical
lint	Lateral diffusion for one side	Physical
lu0	U0 width sensitivity	Electrical
noia	Flicker noise parameter a	Electrical
noib	Flicker noise parameter b	Electrical
noic	Flicker noise parameter c	Electrical
rdsw	Zero-bias LDD resistance per unit width for RDSMOD=0	Physical
toxe	Electrical gate oxide thickness	Physical
toxp	Electrical gate oxide thickness	Physical
u0	Low field surface mobility at 'tnom'	Electrical
vbox	Oxide breakdown voltage	Physical
vtho	Threshold voltage at zero body bias for long-channel devices	Electrical
wu0	U0 width sensitivity	Electrical
xl	Length variation due to masking and etching	Physical
xw	Width variation due to masking and etching	Physical

TABLE III
VARYING PARAMETERS FOR THE 65 NM CMOS PROCESS

Name	Description	Type
cgdl	Overlap capacitance between gate and lightly-doped drain region	Electrical
cgdo	Non-LDD region drain-gate overlap capacitance per unit channel width	Electrical
cgsl	Overlap capacitance between gate and lightly-doped source region	Electrical
cgso	Non-LDD region source-gate overlap capacitance per unit channel width	Electrical
cj	Zero-bias junction bottom capacitance density	Electrical
cjd	Zero-bias bottom junction capacitance per unit area	Electrical
cjs	Zero-bias bottom junction capacitance per unit area	Electrical
cjsw	Zero-bias junction sidewall capacitance density	Electrical
cjswd	Zero-bias junction sidewall capacitance density	Electrical
cjswg	Zero-bias gate side junction capacitance density	Electrical
cjswgd	Zero-bias gate side junction capacitance density	Electrical
cjswgs	Zero-bias gate side junction capacitance density	Electrical
cjsws	Zero-bias junction sidewall capacitance density	Electrical
dlc	Delta L for capacitance model	Electrical
lint	Lateral diffusion for one side	Physical
lu0	U0 width sensitivity	Electrical
noia	Flicker noise parameter a	Electrical
noib	Flicker noise parameter b	Electrical
noic	Flicker noise parameter c	Electrical
toxe	Electrical gate oxide thickness	Physical
toxp	Electrical gate oxide thickness	Physical
u0	Low field surface mobility at 'tnom'	Electrical
vbox	Oxide breakdown voltage	Physical
vtho	Threshold voltage at zero body bias for long-channel devices	Electrical
wu0	U0 width sensitivity	Electrical
xl	Length variation due to masking and etching	Physical
xw	Width variation due to masking and etching	Physical

The process variations resulted in a spread of the number of SRAM upsets at each injected-charge value. Fig. 11 shows the number of Monte-Carlo simulations that resulted in an SRAM upset at each charge value for an off-state NMOS hit on a 90 nm SRAM. The slope of the curve within the two vertical lines, shown in Fig. 11, is representative of the effect of the process parameters. The vertical lines correspond to the smallest charge

that causes an upset and the largest charge that causes less than 10,000 upsets. For comparison purposes, the critical charge values for the 65 nm and 90 nm SRAMs with nominal parameter values for off-state NMOS and PMOS hits are shown in Table IV.

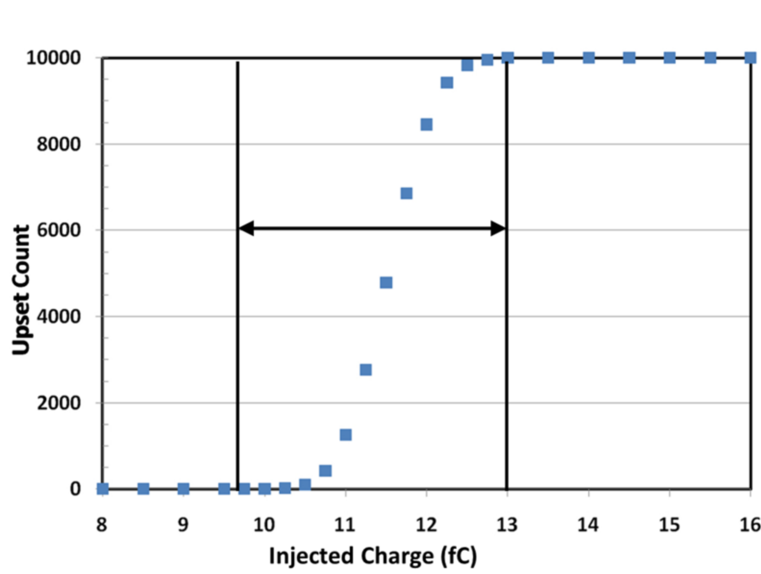

Fig. 11. The number of SRAM upsets that occur at each injected charge value for an off-state PMOS hit on a 65 nm SRAM cell. The two vertical lines show the range of charge values used for simulations.

TABLE IV
THE CRITICAL CHARGE VALUES FOR THE SRAMS WITH NOMINAL PARAMETER VALUES FOR OFF-STATE NMOS AND PMOS HITS.

	65 nm	**90 nm**
PMOS hit	11.548 fC	20.103 fC
NMOS hit	4.027 fC	7.091 fC

In order to determine the impact of the parameter values, the upset simulations were carried out over the expected range of injected-charge values for the SRAM cells. For each injected-charge value, 10,000 simulation runs were carried out by varying transistor parameters using foundry supplied Monte-Carlo models. For the simulation set, each parameter value range was divided into an equal number of segments. From parameter to parameter, the numerical values associated with each segment changed. However, the percentage of the variation stayed the same. For instance, the range of one bin of the threshold voltage covered approximately 4% of the nominal value and the range of the oxide thickness bin covered approximately 2%, but both bins covered 10% of the overall range of variation for both parameters. The number of segments should be loosely associated with the number of Monte Carlo simulations. If the number of simulations is low, the number of segments should be decreased to ensure an adequate number of simulations in each segment. A larger number of simulations would enable a larger number of bins. A larger bin count increases the accuracy of the analysis by enabling a more detailed expression of the SE response.

For this simulation set, the range of parameter values used was divided into ten segments. For each simulation, the parameter value was checked and assigned to one of these segments. Fig. 12 shows a cartoon illustration of the simulation parameter segments assignments. Each white column represents the total number of simulations runs for which the parameter value falls into the parameter segment. Each associated blue column, which is contained in the white columns, represents the number of those simulation runs that resulted in an SRAM upset. Thus, each simulation run had a specific injected-charge value and a specific segment of parameter-value assigned to it.

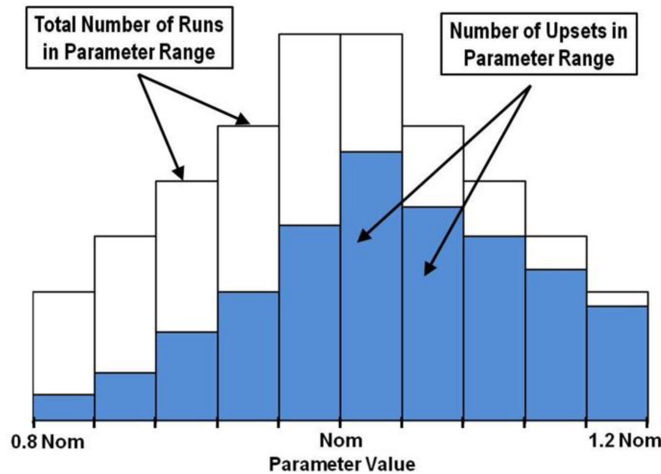

Fig. 12. The total number of simulation runs and the number of simulation runs that resulted in an upset as assigned to a set of parameter-value segments.

The simulation results were used to determine the SRAM upset probability over the range of possible parameter values for a given injected charge. For each parameter-value segment, the total number of simulations and the total number of simulations resulting in an upset were binned. This segregation enabled the comparison of the probability-of-upsets over the parameter-value range to the probability-of-upsets at the corresponding injected-charge level. The upset probability used in this paper is defined as the percentage of the total number of simulations that resulted in an upset out of all of the simulation runs (i.e., 5,000 upsets for 10,000 simulation runs will result in a 50% upset probability). (For this work, probability is based upon empirical data.) The charge-level upset probability is the percentage of the total simulations that result in an upset for a particular value of the injected charge. The parameter-value upset probability is the percentage of the simulations for each parameter-value segment that result in SRAM upsets.

Fig. 13 depicts the upset probability of the PMOS threshold voltage SPICE parameter (V_{THO}) over its value segments (bins) and lists the upset probability of the entire Monte-Carlo simulation set at the injected charge value of 7.25 fC for an off-state NMOS hit on a 90 nm SRAM. The parameter values for Fig. 13 and the following figures are normalized to the nominal parameter value, which is shown as Nom. The upset probabilities provide a quantitative description of the impact of each individual process parameter on the upset probability of an SRAM. For the example in Fig. 13, the value of the PMOS V_{THO} significantly affects the likelihood of an SRAM upset. For the largest magnitude of V_{THO}, the upset probability is approximately 36% greater than that for the overall charge upset probability, and for the smallest magnitude of V_{THO} it is almost 44% less with respect to the overall charge upset probability. An increase in threshold voltage magnitude will result in a decrease in transistor current. The decrease in transistor current will result in a lowering of critical charge as restoring current is decreased. This will result in an overall increase in upset probability as observed in these simulations.

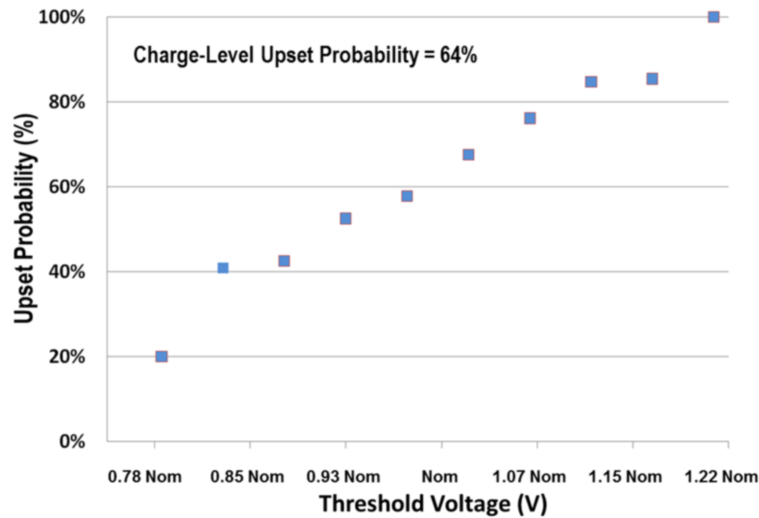

Fig. 13. The upset rate of PMOS threshold voltage over its value segment range of the entire Monte-Carlo set of simulations at an injected charge value of 7.25 fC for an off-state NMOS hit on a 90 nm SRAM.

The upset probabilities over the PMOS threshold-voltage values and injected-charge values are shown in Fig. 14. A comparison of these upset probabilities to the charge-level upset probability, shown in Fig. 11, can elucidate the impact of the threshold voltage on the SRAM upset probability. The comparison of the parameter-value upset probability and the charge-level upset probability highlights the impact of the parameter on the upset probability. PMOS V_{THO} has the most significant impact near the center of the range of injected-charge values. At the low end of injected-charge values, the charge level is too low to upset many of the SRAM cells regardless of the process parameter values. At the high end of injected-charge values, the charge level is high enough to upset most of the SRAM cells regardless of the process parameter values. In the middle of the charge range, the impact of the parameters is the most evident.

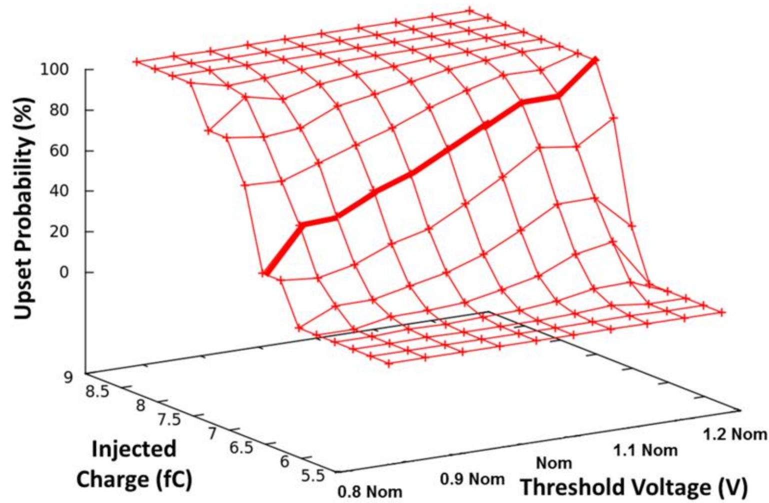

Fig. 14. The extracted upset probability binned by PMOS threshold voltage and injected charge values for an off-state NMOS hit on a 90 nm SRAM.

The impact of the process variations is shown in the increase in the upset probability for a given injected charge over the range of the threshold voltage, as highlighted in Fig. 14. Fig. 15 overlays, onto the plot from Fig. 14, the upset probability values that would occur if the threshold voltage variation did not impact upset probability. Those values correspond to the charge-level upset values. The difference between the parameter-value extracted upset probability and the charge-level upset probability, the differential upset probability as shown in Fig. 16, isolates the impact of the individual parameter. The differential upset probability is calculated by subtracting the charge-value upset probability from the parameter-value upset probability. The differential upset probability is important because it allows the measurement of the peak-to-peak upset probability variation. The peak-to-peak upset-probability variation is the delta between the two differential upset probability extremes, which can serve as types of radiation corners for process variation. The peak-to-peak upset-probability variation

shows the maximum variation in single event response due to the variation in process parameters. Radiation "corners" that bound the impact of process variations provide quantitative information for evaluation of the effects of parameter variation. They also afford an approach for the comparison of the impacts of multiple parameters.

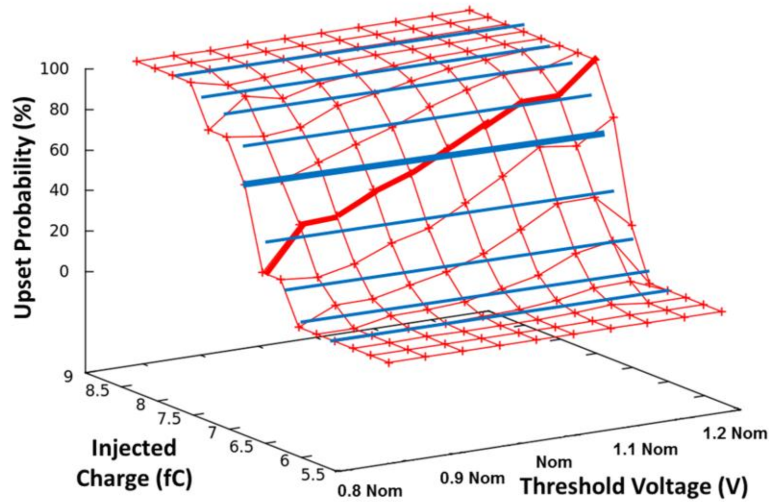

Fig. 15. The extracted upset probability over the PMOS V_{THO} values and injected charge values for an off-state NMOS hit on a 90 nm SRAM. The blue lines represent the upset probability values that would occur if the threshold voltage variation did not impact upset probability.

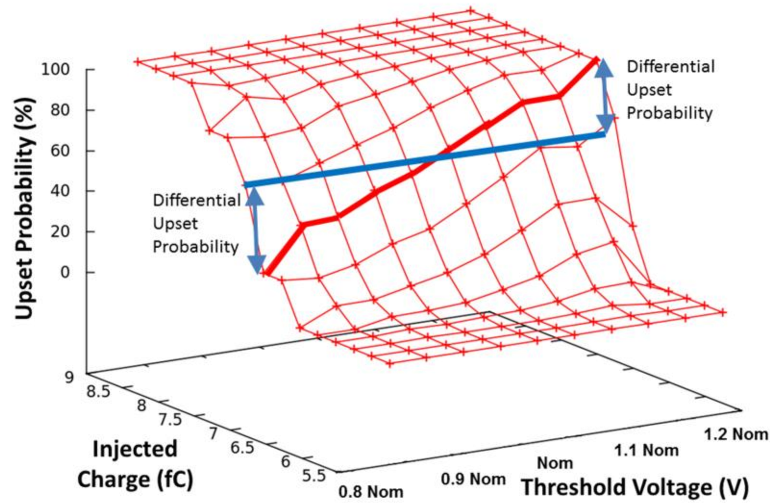

Fig. 16. The differential upset probability is the difference between the parameter-value extracted upset probability and the charge-level upset probability.

Fig. 17 shows the difference between the PMOS V_{THO} upset probability and the charge-level upset probability for an NMOS hit on a 90 nm CMOS SRAM. It also highlights the peak-to-peak upset probability variation. The middle portion of the charge range shows that a smaller threshold voltage magnitude results in a lower likelihood of an SRAM upset and that a larger threshold voltage magnitude results in a greater likelihood of an SRAM upset. The main reason for this effect is the decreased critical-charge requirements for SRAMs. For any given SRAM cell (or any storage cell), an upset occurs when the SET pulse-width generated by an ion hit exceeds the feedback delay of the SRAM cell. When the magnitude of the PMOS transistor threshold voltage is higher, the current provided by the transistor is lower. As the PMOS transistor for N-hits act as the restoring transistor, lower current results in longer SET pulse-widths and higher likelihood of an upset. Similarly, for lower threshold-voltage-magnitude transistors higher restoring current results in shorter SET pulse-width and subsequently lower

probability for an upset.

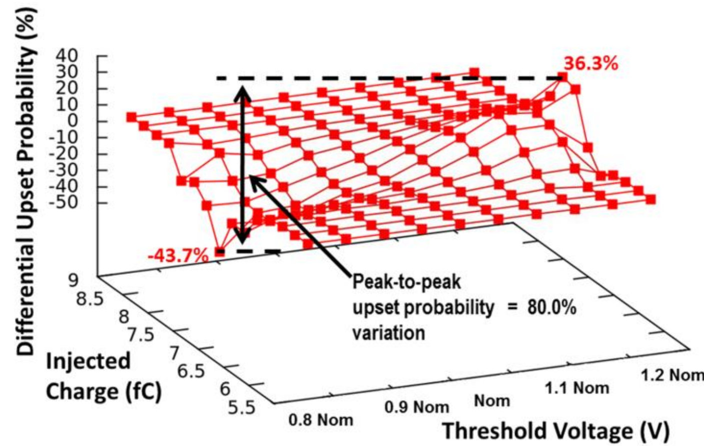

Fig. 17. The variation in upset probability for PMOS V_{THO} (compared to the charge impact) on the SRAM upset rate over the range of charges for a 90 nm SRAM and an off-state NMOS hit. The peak-to-peak upset probability variation is shown.

The differential upset probability can be used to show the potential range in upset probabilities due to process variation. Fig. 18 displays the charge-level upset probability values, in blue diamonds, and the range of upset probabilities over the range of threshold voltage variation at each injected charge value, in red lines. The red lines show the extent of the potential upset probabilities due to process variation.

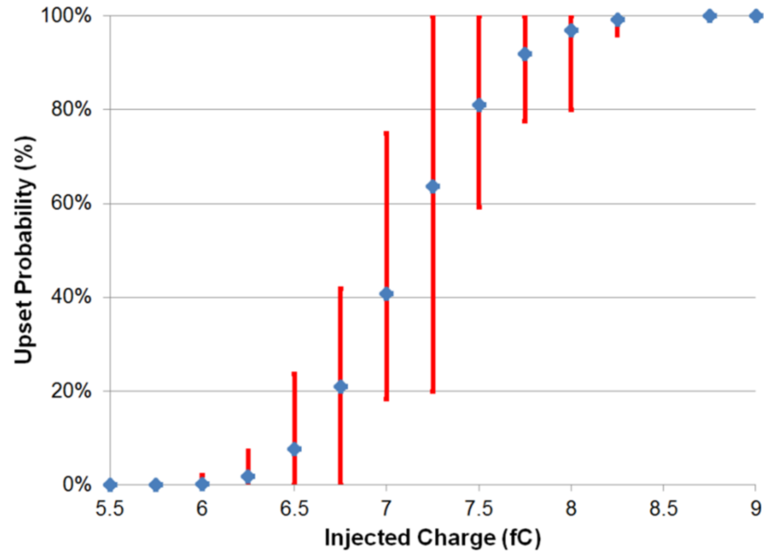

Fig. 18. The variation in upset probability over the range of PMOS V_{THO} values and the nominal charge-level upset probability for a 90 nm SRAM and an off-state NMOS hit.

SRAM Analysis

The examination of the parameter related SRAM upsets illustrates the significance that process variations can have on single event circuit response. The parameter analysis was conducted on all varying parameters. Some of the most significant results are presented here. The upset probability over the range of possible PMOS threshold voltages and over the series of charge values is shown in Fig. 19 for an off-state NMOS hit for a 65 nm SRAM. The variation in upset probability for shifts in PMOS V_{THO} is shown in Fig. 20. The trend at 65 nm is the same as for 90 nm; the greater magnitude threshold voltages result in an increased likelihood of SRAM upset and the lesser magnitude threshold voltages result in a decreased likelihood of SRAM upset.

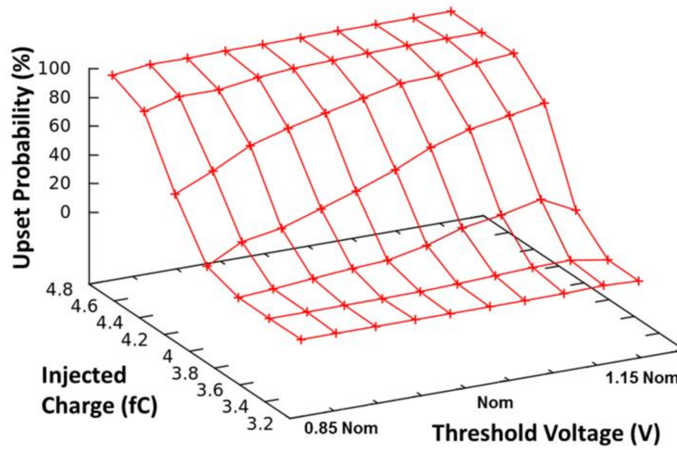

Fig. 19. The extracted upset probability binned by PMOS V_{THO} values and injected charge values for an off-state NMOS hit on a 65 nm SRAM.

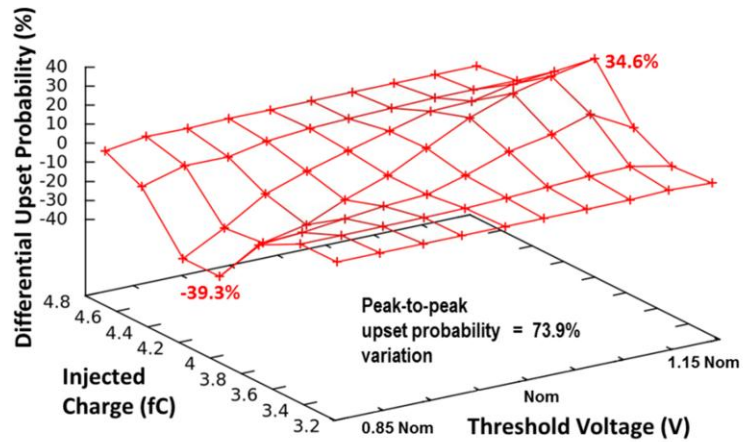

Fig. 20. The variation in upset probability for PMOS VTHO (compared to the charge impact) on the SRAM upset rate over the range of charges for a 65 nm SRAM and an off-state NMOS hit.

Several process parameter variations impact the SRAM upset probability. For instance, variations in oxide thickness can be discerned by examining TOXE, the electrical gate oxide thickness used in device modeling. Changes in TOXE will affect the threshold voltage, mobility, substrate current, gate-tunneling current, and the capacitance of the circuit node. As TOXE increases, the drain current decreases resulting in subsequent increases in the upset probability. Correspondingly, a decrease in TOXE would increase the drain current and decrease the probability of upsets. Additionally, increases in TOXE would also decrease the storage-node capacitance values and would increase the probability of SRAM upset. Fig. 21 shows the extracted upset probability binned by TOXE. The variation in upset probability for TOXE shifts on the difference probability of SRAM upsets is shown in Fig. 22 for an off-state PMOS hit at 90 nm. (The charge axes on Figs. 21 and 22 are reversed in order to improve the clarity of the graphs.) The corresponding variation in upset probability for a 65 nm SRAM is shown in Fig. 23. At 90 nm, the largest values for TOXE result in large increases, of up to 77.8%, in the likelihood of an SRAM upset. The smallest values of TOXE sizably reduce the relative likelihood of an SRAM upset. At 65 nm, the largest values for the gate oxide thickness result in a 72% increase in the likelihood of an SRAM upset for an injected charge of 11.25 fC. Additionally, the smallest values for TOXE show a decreased likelihood for SRAM upset. For an off-state PMOS SE hit for the 90 nm SRAM cell, fig. 24 shows the range of possible upset probabilities due to variations in TOXE and the nominal charge-level upset probabilities. The graph indicates that changes in the process affecting TOXE will have a large impact on the SEU error probability.

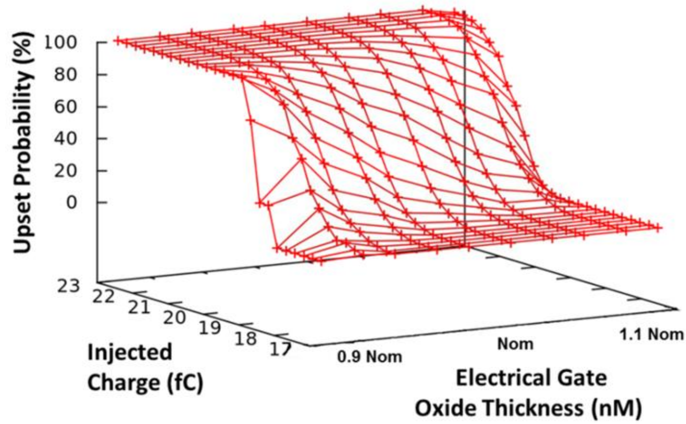

Fig. 21. The impact of TOXE shifts on the rate of SRAM upsets for an off-state PMOS hit at 90 nm.

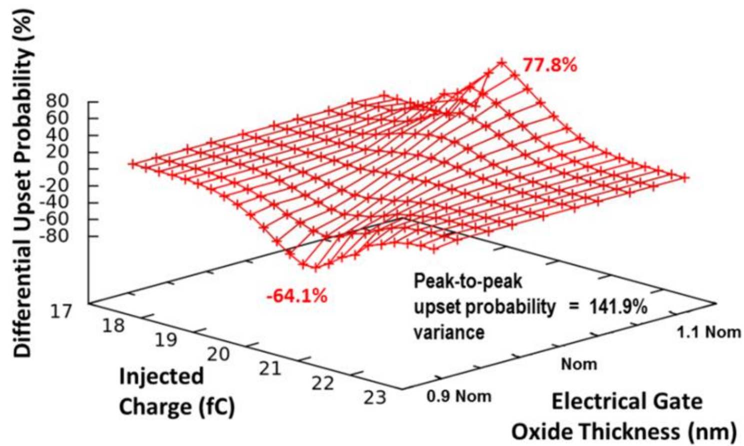

Fig. 22. The impact of TOXE shifts on the SRAM differential upset probability for an off-state PMOS hit at 90 nm.

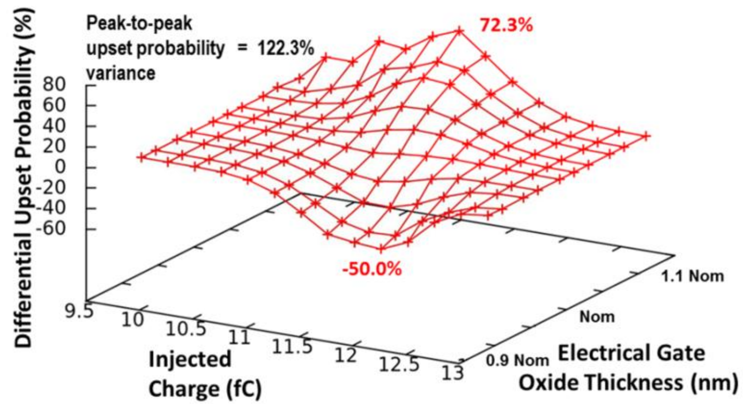

Fig. 23. The impact of TOXE shifts on the relative rate of SRAM upsets for an off-state PMOS hit at 65 nm.

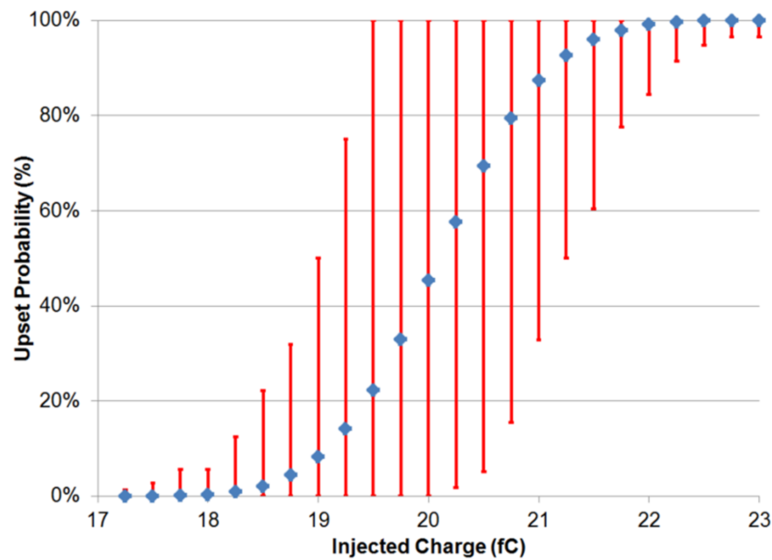

Fig. 24. The variation in upset probability over the range of PMOS TOXE values and the nominal charge-level upset probability for a 90 nm SRAM and an off-state PMOS hit.

Another common process concern is the issue of over-and under-etching. The SPICE parameter XL, length variation due to masking and etching, is affected by variants in etching. Length variation shifts can impact the effective channel length, the intrinsic

capacitances, and the transit time. Increases in XL increase the effective channel length and therefore decrease the drain current. The impact of the length variations on the variation in SRAM upset probability is shown in Fig. 25 for an off-state NMOS hit in 65 nm. (The nominal value of XL is negative.) As shown for TOXE, the shifts in XL have a notable impact on the SRAM upset probability. At 65 nm, the large XL values result in an increase in the relative likelihood of an SRAM upset. Also, the smaller XL values decrease the differential upset probability. The figures illuminate the impact that process variations have on the radiation response of the SRAM. A summary of the peak-to-peak upset probability variations for the SRAM is shown in Table V. Quantifying the impact of the SPICE parameter shifts provides the circuit designer with numerical information that can be applied to help increase the radiation hardness of a potential circuit. It can be used to anticipate the impact of process variations on a circuit's radiation response and can lead to the development of mitigation techniques. For instance, analysis could reveal a sensitivity of dual interlocked storage cells (DICE) to the variation of a specific set of parameters. DICE latches employ dual node feedback control and demonstrate single event upset immunity unless multiple nodes are upset due to a single particle impact [85], [89], [113]. Mitigation techniques could then be applied to harden the DICE cells.

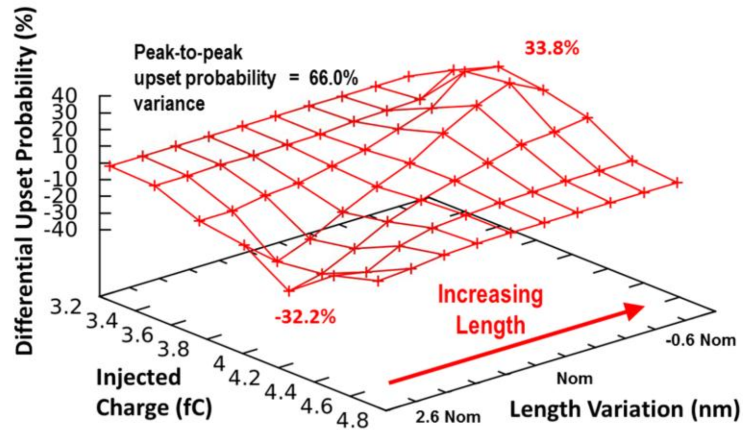

Fig. 25. The variation in differential upset probability of SRAM upsets for XL shifts for an off-state NMOS hit at 65 nm.

TABLE V
SRAM PEAK-TO-PEAK UPSET PROBABILITY VARIATIONS.

Parameter Name	**Process**	**Peak-to-peak upset probability variation**
VTHO	90 nm	80.0%
VTHO	65 nm	73.9%
TOXE	90 nm	141.9%
TOXE	65 nm	122.3%
XL	65 nm	66.0%

SRAM Intradie Analysis

Die-to-die variations have historically been considered more impactful on circuit performance than within-die variations. However, within-die process variations can have significant impact on circuit performance, particularly for circuits that rely on transistor matching [24]. In order to study the impact of the within-die variations on SRAM single event radiation sensitivity, another Monte-Carlo-based simulation study was conducted on the 65 nm 6T SRAM cell, shown in Fig. 26. In this study, the parameters were varied, according to the process design kit, to mimic the effects of within-die process variations. The affected BSIM4 model parameters are shown in Table VI. As in the previously discussed Monte-Carlo simulation study, the single event hits were conducted on the off-state NMOS and PMOS transistors and were modeled using the same bias-dependent single-event model [112]. Two thousand simulations were conducted at each value of injected-charge. The values of the varying parameters were recorded for each of the six transistors in the SRAM cell along with the injected charge value and the upset result.

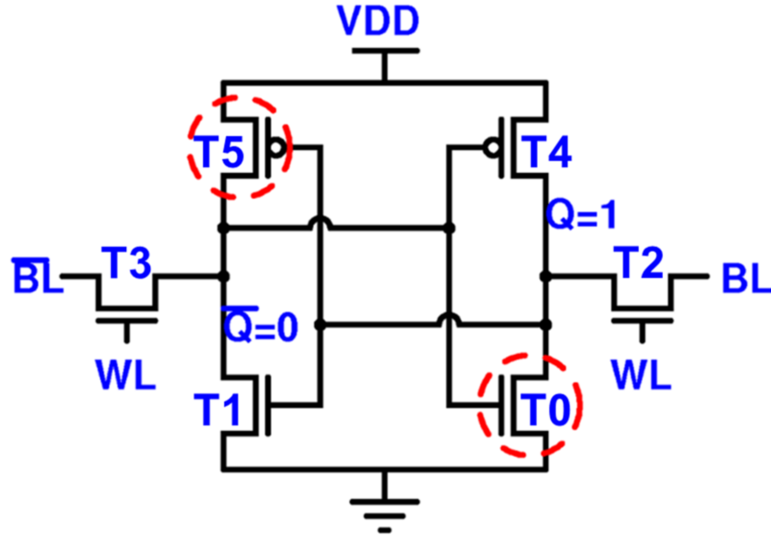

Fig. 26. 6T SRAM cell with labeled transistors.

TABLE VI
WITHIN-DIE VARYING PARAMETERS FOR THE 65 NM CMOS PROCESS

Name	Description
rdsw	Zero-bias LDD resistance per unit width for RDSMOD=0
u0	Low field surface mobility at 'tnom'
vtho	Threshold voltage at zero body bias for long-channel devices
xl	Length variation due to masking and etching
xw	Width variation due to masking and etching

For a SE strike on the off-state PMOS transistor, T5, the parameters that have the most impact on the upset probability are the channel width variation (XW) and the threshold voltage (VTHO) for the T1 transistor. Fig. 27 shows the differential upset probability of the SRAM for the extracted threshold voltage of transistor T1. As the threshold voltage increases, the variation in upset probability increases. The increase in threshold voltage decreases the T1 drain current. The decrease in drain current reduces the ability of T1 to dissipate charge on the node between the drains of T5 and T1 that

results from the charge injected onto the drain of T5. Fig. 28 shows the range of the upset probabilities due to VTHO variation and the charge-level upset probabilities.

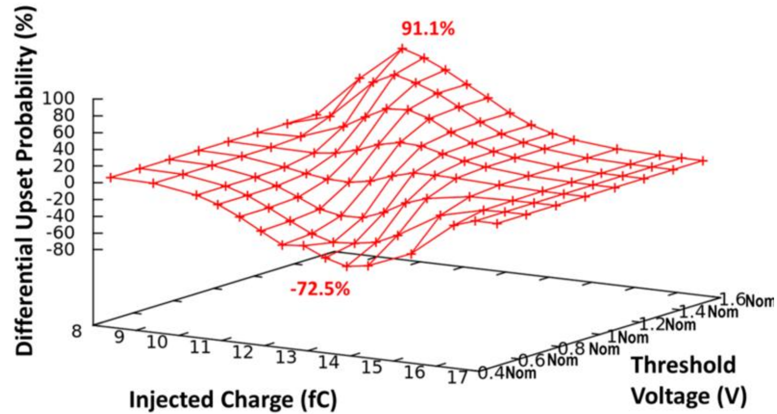

Fig. 27. Variation in upset probability for a single event hit on transistor T5 over the range of extracted threshold voltage values for transistor T1.

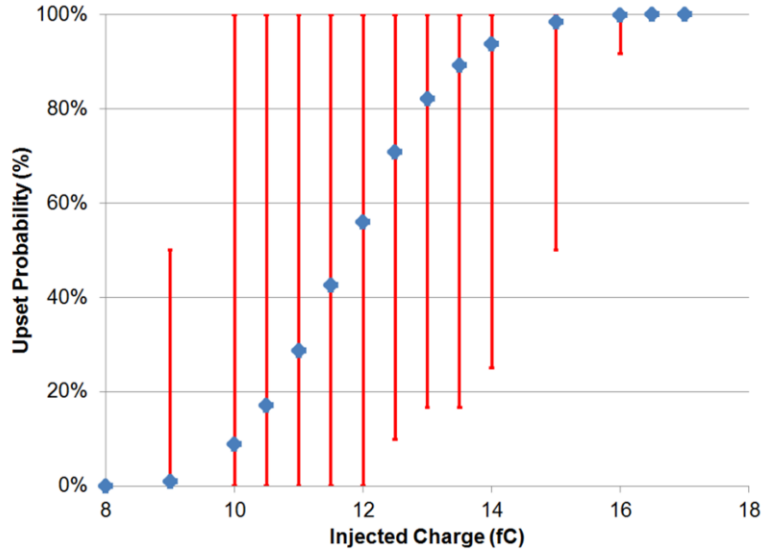

Fig. 28. The variation in upset probability over the range of T1 V_{THO} values and the nominal charge-level upset probability for a 65 nm SRAM and SE hit on T5.

The width variation, XW, of T1 also has a strong impact on the variation in upset probability due to a single event strike on transistor T5. Fig. 29 shows the relationship between the width variation of T1 and the variation in upset probability. Decreases in channel width, due to a smaller XW value (which is nominally negative), correspond to an increase in the variation in upset probability. As the channel width for transistor T1 decreases, the drain current also decreases. The decrease in drain current increases the susceptibility of the node between T5 and T1 to upset and thus increases the likelihood of overall SRAM upset.

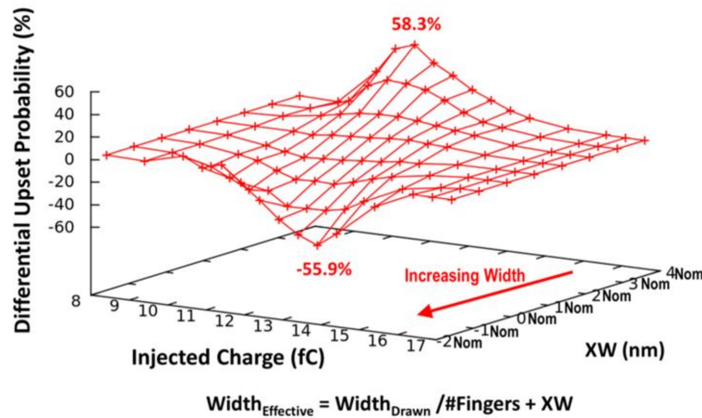

Fig. 29. Variation in upset probability for a single event hit on transistor T5 over the range of extracted width variation values for transistor T1.

Similarly, variations in the VTHO and XW parameters of transistor T4 sizably affect the sensitivity of the SRAM to upset due to a SE hit on T0. Figs. 30 and 31 show the relationship between the variations in upset probability and the parameter variation for threshold voltage and width variation, respectively. The increase in VTHO and the decrease in channel width both decrease the drain current for T4. The decrease in drain current increases the sensitivity of the node between T0 and T4 to the charge injected

onto T0.

Figs. 32 and 33 compare the charge-level upset probabilities and the ranges of possible upset probability due to interdie and intradie, respectively, threshold voltage variation. Both figures correspond to a single event strike on T0. Fig. 32 correlates the upset probability to the PMOS threshold voltage value and Fig. 33 correlates the upset probability to the T4 threshold voltage value. The upset response in Fig. 33 is elongated due to a greater threshold voltage variation.

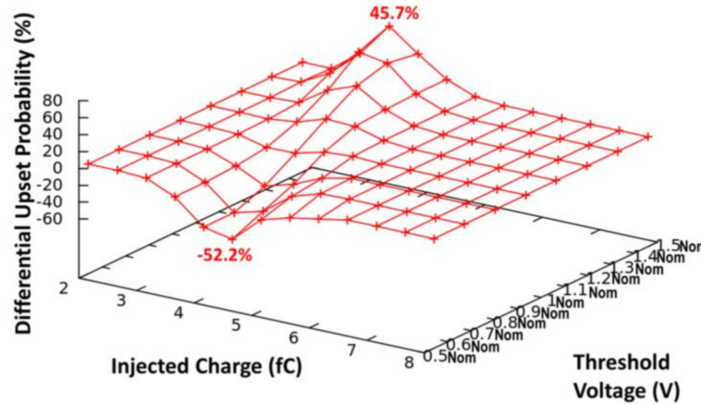

Fig. 30. Variation in upset probability for a single event hit on transistor T0 over the range of extracted threshold voltage values for transistor T4.

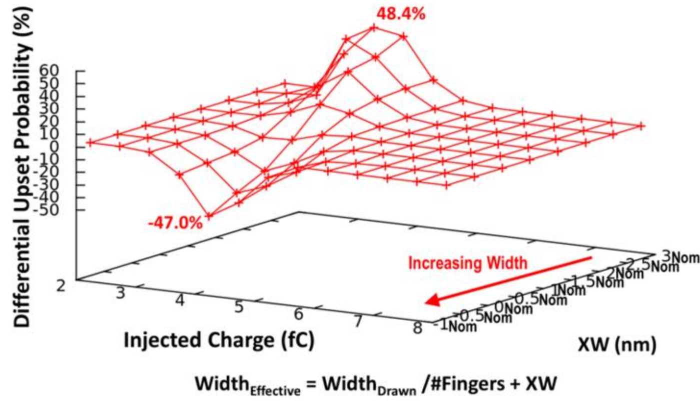

Fig. 31. Variation in upset probability for a single event hit on transistor T0 over the range of extracted width variation values for transistor T4.

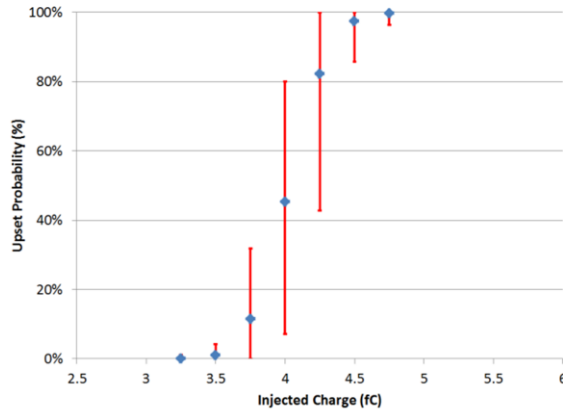

Fig. 32. The charge-level upset probabilities and the ranges of possible upset probability due to interdie threshold voltage variation. The single event strike was simulated on T0 and the upset response was correlated to the PMOS threshold voltage.

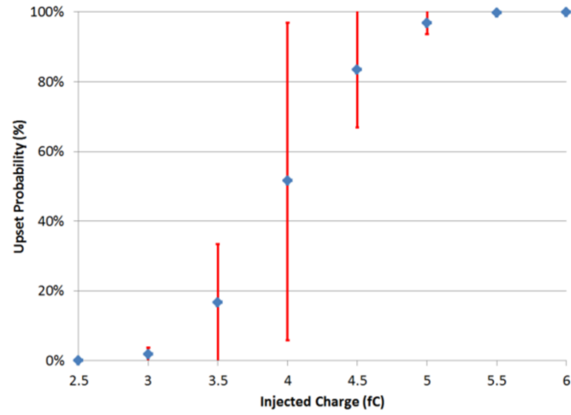

Fig. 33. The charge-level upset probabilities and the ranges of possible upset probability due to intradie threshold voltage variation. The single event strike was simulated on T0 and the upset response was correlated to the T4 threshold voltage.

CHAPTER IV

IMPACT OF PROCESS VARIATIONS AND CHARGE SHARING ON THE SINGLE EVENT UPSET RESPONSE OF FLIP-FLOPS

An analysis was conducted on flip-flops by employing the same approach used with the SRAM circuits. It correlates the shifts in radiation response to specific device and process-parameter variations by quantifying the impact of process variability on the range of SEU critical charge. However since charge-sharing reduces the effective upset threshold and increases the circuit's vulnerability to SEU [86], [87], a combined analysis of parameter variation, charge sharing, and single events is performed. The combination of the mechanisms provides a more accurate analysis of single event response. In advanced technologies, latches have become vulnerable to upset at decreasing values of deposited charge and have become more susceptible to charge-sharing effects. The investigation leverages Monte-Carlo simulations to assess the impact of process variations on the SEU response of flip-flops.

To examine the impact of process variations on single event upset response, a simulation study was conducted using two unhardened, D flip-flop designs. Both designs function at very high frequencies (up to 4GHz) and one is optimized for low power. One flip-flop was targeted to a commercially-available 45 nm CMOS process, and the other to a commercially-available 65 nm CMOS process. In this work, the flip-flops will be referred to as FF A (45 nm) and FF B (65 nm).

Single event hits were modeled on each of the individual transistors using the previously-described bias-dependent single-event model [112]. The model was integrated into the 45 nm and 65 nm process design kits and was calibrated using TCAD simulations. Charge-sharing was incorporated into the simulations by modeling the multiple-node charge collection with additional injected charge. The secondary charge-sharing-induced currents were modeled on transistors that neighbor the primarily struck device in the layout. The amount of collected charge was calculated based on the distance between the struck device and a neighboring device. In order to determine the relationship between collected charge and distance, TCAD simulations were performed on a series of diodes. The TCAD data provided the charge collection and time profiles of junctions located at varying distances from the strike. A similar approach has been used in other research to perform a layout-aware analysis of multiple flip-flops [112]. The profiles enabled the development of a collected-charge-versus-distance function that was empirically fitted to the TCAD data.

Simulations performed on the flip-flop accounted for charged particles with different linear energy transfer values by varying the amount of injected charge. For each level of injected charge, approximately six hundred Monte-Carlo simulations were conducted. The Monte-Carlo simulations varied the BSIM4 transistor parameters according to the PDKs. The full, statistical parameter variations were imported directly from the PDKs and provided the "best representation of long-term manufacturing performance" [114]. Table VII lists approximate parameter variations from simulations conducted on FF B. The variations represent the anticipated real-life variances that could occur in the specific process in which flip-flop B was fabricated. Results from the

simulations show the effect of each of the BSIM4 parameter variations on the single-event response of the flip-flop designs.

TABLE VII.
SELECT PARAMETER VARIATIONS FROM SIMULATIONS ON THE 65 NM FLIP FLOP B.

Parameter Abbreviation	Parameter Description	% Variation
CGDL	Drain-gate overlap capacitance	+/- 8.7
CGDO	Drain-gate overlap capacitance per unit channel width	+/- 9.3
CJ	Junction capacitance density	+/- 15.1
CJSWG	Gate-side junction capacitance	+/- 8.6
RDSW	Resistance per unit width	+/- 21.3
TOXE	Electrical gate oxide thickness	+/- 4.7
U0	Mobility	+/- 4.3
VTH0	Threshold voltage	+/- 14.3
XL	Length variation due to masking and etching. XL, which has a negative nominal value, must be added to the drawn channel length to get the effective channel length. The variation is approximately -25% to 2% of the drawn length for the most sensitive transistor.	+/- 105.1%
XW	Width variation due to masking and etching. XW, which has a negative nominal value, must be added to the drawn channel width, which is divided by the number of fingers, to get the effective channel width. The variation in XW is approximately -8% to 1% of the drawn width for the most sensitive transistor.	+/- 119.4%

Ideally, a set of flip-flops from the same design and process would have a single critical charge value. However, the combined contribution of charge sharing and process variation causes a spread in the critical charge values. As the value of the primary injected-charge increases, the subset of the total number of flip-flops resulting in an upset

also increases. Fig. 34 shows the percentage of Monte-Carlo simulations that resulted in an upset at each injected-charge value for a transistor strike in FF B. (In this work, specific, numeric injected-charge values refer to the value of the primary injected charge.) In order to facilitate further analysis, specific information is recorded during the Monte-Carlo simulations. After each simulation, the value of each parameter, the upset or no-upset response of the flip-flop, and the injected charge value are recorded. Such information allows the calculation of the charge-level upset probability. Fig. 34, in essence, shows the charge-level upset probability for a transistor strike on FF B since it shows the percentage of upset-resulting simulations at each level of injected charge.

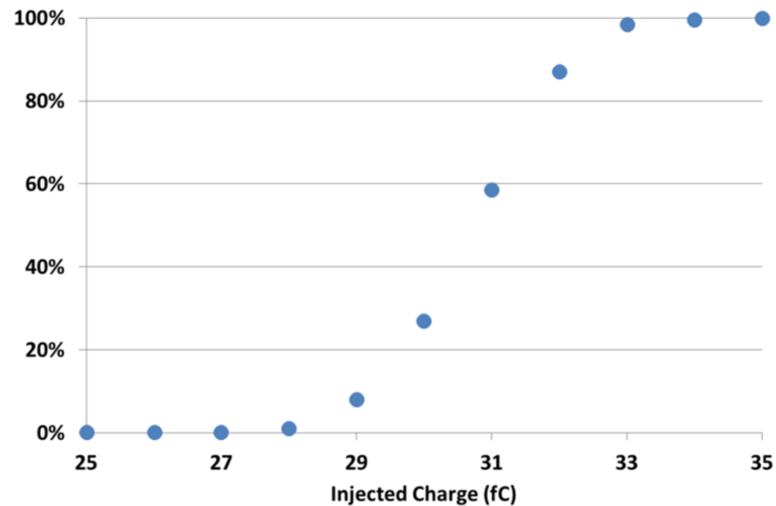

Fig. 34. The percentage of simulations resulting in an upset for a strike to a transistor that causes upset through charge sharing in flip-flop B.

In order to analyze the contribution of parameter values, the range of variation for each parameter was divided into eight segments of equal size. After each simulation run, the parameter value was binned according to its value. Fig. 35 shows the percentage of the simulations with a process parameter value in each segment. In the figure, the segments are noted by their mean value as a fraction of the nominal parameter value.

Information from the simulations allows the correlation of parameter value to upset response. Fig. 36 shows the parameter-value upset probability for a hit on FF B. Fig. 37 shows the variation in upset probability (which isolates the impact of the individual parameter variation) for a transistor strike on FF B. It contains the differential upset probability between the upset probability data from Fig. 36 and the upset probability data in Fig. 34. In Fig. 37, the peak-to-peak upset-probability variation indicates that the possible 28% change in the threshold voltage can result in an 89.8% change in the differential upset probability or, in other words, that the flip-flop can have a possible delta around the nominal upset probability of 89.8%.

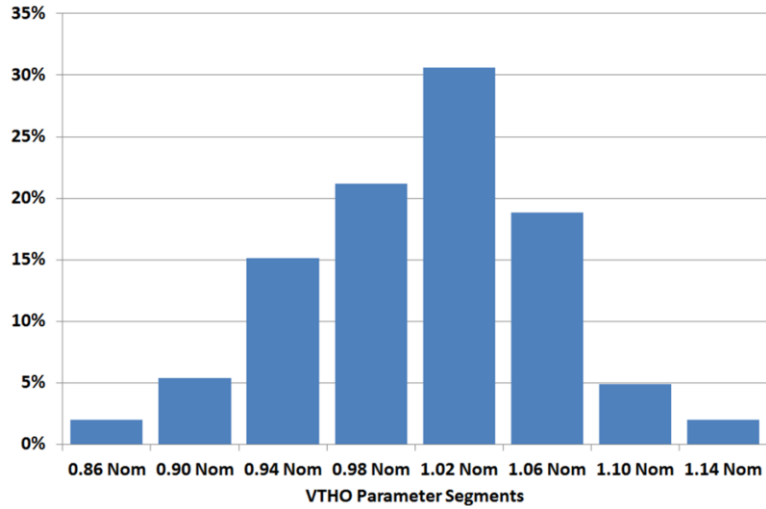

Fig. 35. The percentage of simulations with a threshold voltage value in each segment. The average value of each segment is shown as a fraction of the nominal VTHO value.

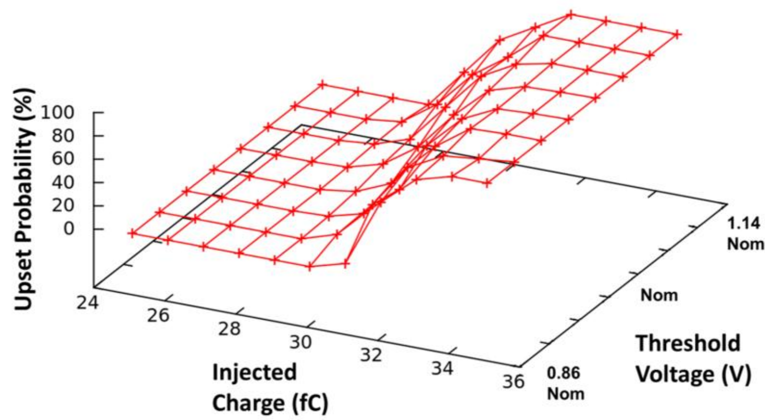

Fig. 36. The impact of threshold voltage variations on the parameter-value upset probability for a strike in flip-flop B.

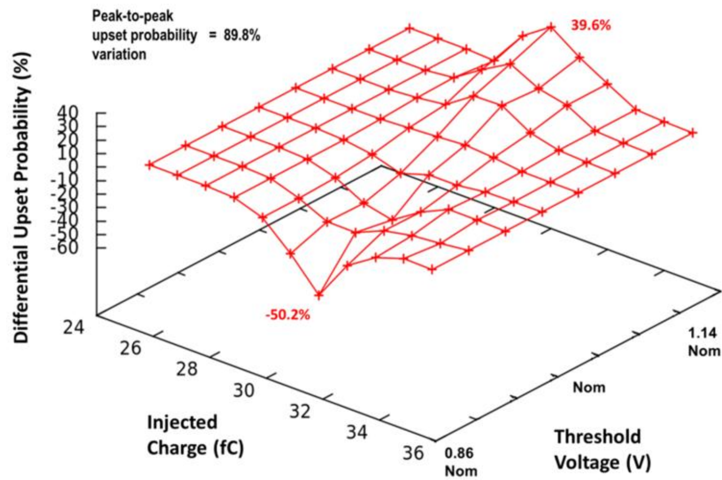

Fig. 37. The impact of threshold voltage variations on the differential upset probability for flip-flop B.

The analysis of parameter impact focused on the examination of physically measurable parameters. If the impact of a parameter variation is known and the ability to determine the specific parameter value exists, it may be possible to evaluate the sensitivity of a batch of chips based on the parameter value. One measurable parameter is threshold voltage. Changes in threshold voltage can significantly affect both circuit performance and soft-error rates. The impact of the threshold voltage variations on FF B is shown in Fig. 37. As the threshold voltage increases, the differential upset probability increases. Decreasing values of VTH0 result in a lower differential upset probability. After chip fabrication, knowledge of the actual threshold voltage, which could be determined from fabrication testing, compared to the nominal VTH0, could indicate the sensitivity of fabricated chips to single event radiation.

Another measurable parameter is the electrical gate oxide thickness, TOXE. For the same reasons discussed for SRAMs, both flip-flops showed an increase in the differential upset probability as the oxide thickness increased. Figs. 38 and 39 emphasize this effect by showing the impact of TOXE on the 45 nm and 65 nm flip-flops, respectively. The peak-to-peak upset-probability variation value for 45 nm, 181.9%, was greater than the value at 65 nm, 137.4%. This corresponds to the expected increase of parameter variation impact with decreasing device size. Fig. 40 shows the range in upset probabilities over the TOXE parameter variation and the charge-level upset probability for each injected-charge value.

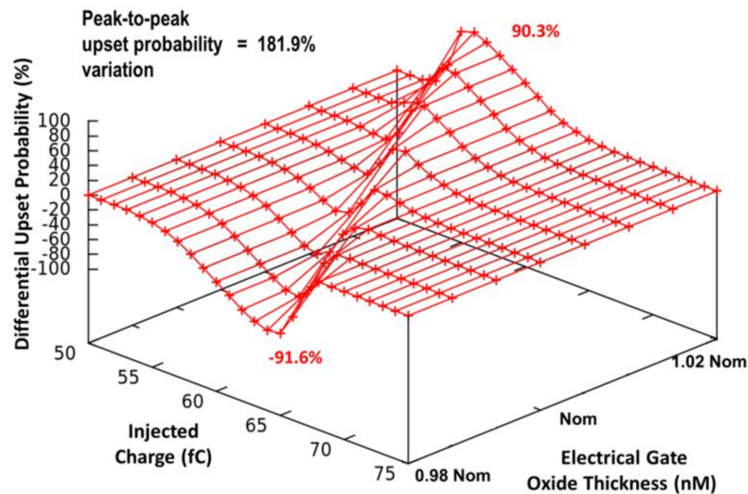

Fig. 38. The impact of TOXE variations on the differential upset probability for flip-flop A.

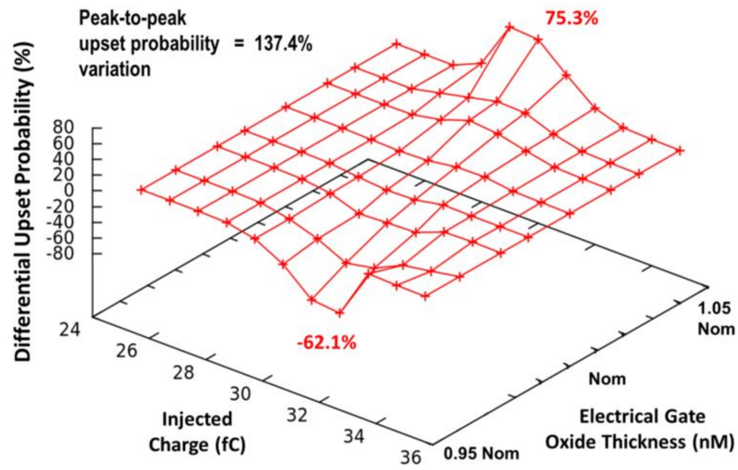

Fig. 39. The impact of TOXE variations on the differential upset probability for flip-flop B.

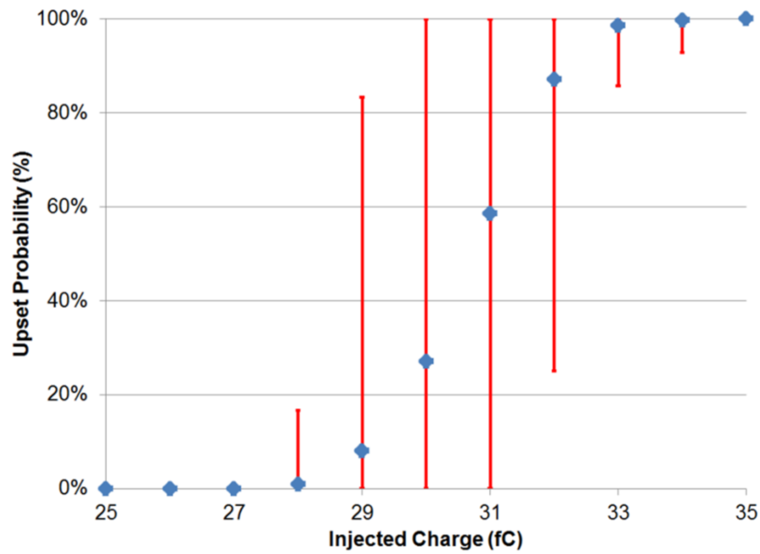

Fig. 40. The variation in upset probability over the range of PMOS TOXE values and the nominal charge-level upset probability for a flip-flop B.

Shifts in the masking and etching aspects of fabrication, caused by over- and under-etching, result in length and width variations, which are represented by variations in the XL and XW BSIM4 parameters. The effective channel length is determined by adding the variation, XL, to the drawn length of the struck transistor. For the 45 nm flip-flop, the magnitude of the nominal value of XL is approximately 9% of the drawn length of the struck transistor. The range of XL magnitudes over the Monte Carlo simulations is approximately -8% to -11% of the drawn value. As XL increases, the effective channel length increases.

The effective channel width is determined by adding the variation, XW, to the drawn width divided by the number of fingers. For FF B (45 nm), XW is approximately 2% of the drawn width of the struck transistor. For the Monte Carlo simulations, the range of XW magnitudes is approximately 0.5% to 4% of the drawn width of the struck transistor. For both XW and XL, the percentage change of the nominal parameter value is large, but the percentage change of the drawn width and length values is relatively small.

Increases in channel length cause a decrease in drain current and decreases in channel width cause a decrease in drain current. Decreases in drain current increase single event sensitivity. The impact of XL on the variation in upset probability of FF A is shown in Fig. 41. The impact of XW on the variation in upset probability of FF A is shown in fig. 42. The peak-to-peak upset-probability variation values, shown in the figures, describe the significance that channel length and width variations can have on the flip-flop soft-error rates. With shrinking device sizes, XL and XW may become increasingly dominant due to limitations in process etching and lithography.

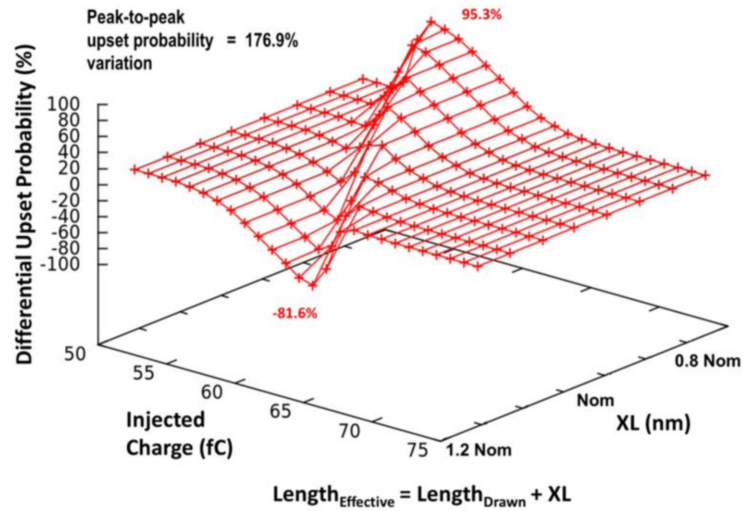

Fig. 41. The variation in upset probability for variations in NMOS XL for flip-flop A, a 45 nm flip-flop. The nominal value of XL is negative.

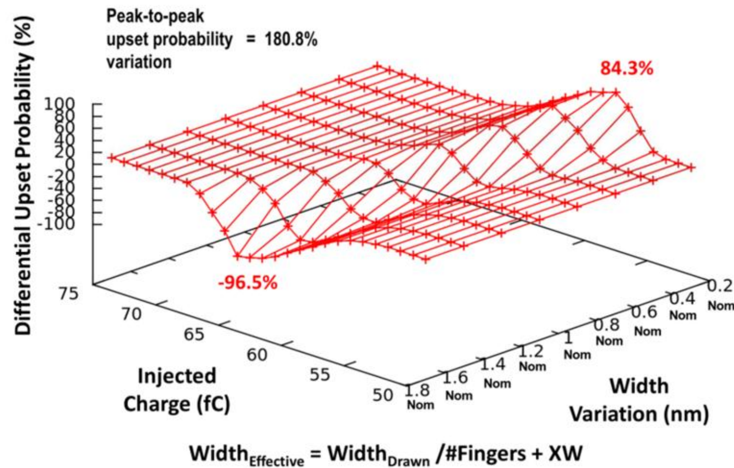

Fig. 42. The differential upset probability for variations in NMOS XW for flip-flop A, a 45 nm flip-flop.

Summaries of significant peak-to-peak upset-probability variation values for the FF A and FF B are shown in Figs. 43 and 44. For both flip-flops, certain parameters, including TOXE, XL, XW, and VTH0, show sizeable impact on SEU response. The parameter variations effect on the radiation response of the latch circuits is also consistent with the previous analysis of SRAM cells [50]. This consistency suggests that a select subset of parameters has significance over a range of circuits and processes. The existence of an impactful subset of parameters implies that certain design considerations and process controls could ameliorate the rate of SEUs caused by process variations. The impact of process variation, as shown in the peak-to-peak upset-probability variation values, increased from 65n to 45 nm. An increase in variation impact reflects the expected increase in process variation described in Table I.

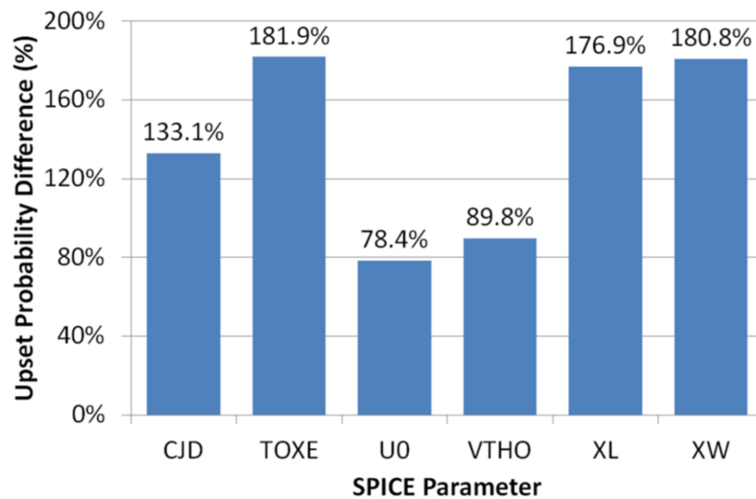

Fig. 43. Peak-to-peak upset-probability variation values for flip-flop A, a 45 nm flip-flop.

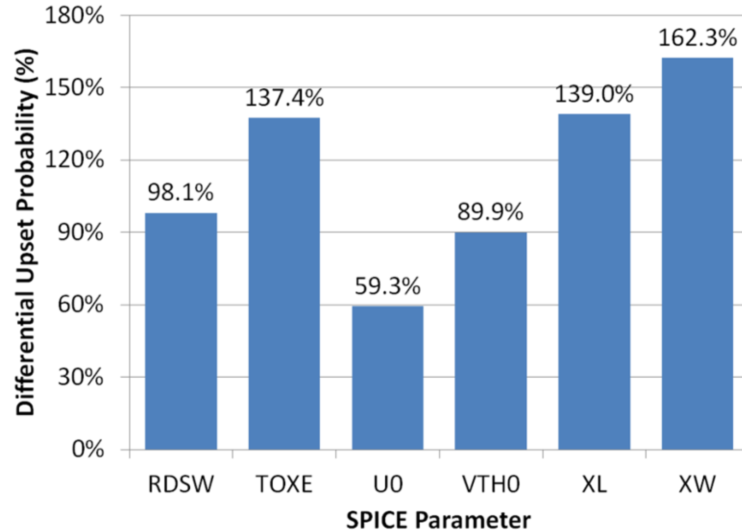

Fig. 44. Peak-to-peak upset-probability variation values for flip-flop B, a 65 nm flip-flop.

Charge sharing impacts the radiation response of circuits, particularly those fabricated in advanced technologies [4], [53]-[56], [105]-[107]. Charge sharing has been demonstrated to cause multiple-bit upsets, decrease LET threshold, and increase upset cross-sections. The combination of process variations and charge sharing can aggravate the effects of single events on integrated circuits. Without charge sharing, a strike with sufficient charge causes an upset if it hits a sensitive transistor, but not if it hits an insensitive transistor. When charge sharing is included in the simulations, strikes on insensitive transistors may cause an upset if they neighbor a sensitive transistor. The primary strike on the device injects charge into the sensitive transistor. Therefore, charge sharing expands the area in the circuit that is sensitive to single events since SEUs can be caused by strikes to transistors that would otherwise not cause an upset.

Additionally, through the generated secondary currents, charge sharing extended the charge range of upset-causing strikes. Without charge sharing, the range of injected

charge values over which process variations affect upset response is limited. Charge sharing significantly increased the charge range for process variation impact and thus amplified the effect that parameter variation can have on the single event response of a circuit. Fig. 45 shows this progression for strikes simulated in FF A. Transistor A, the sensitive transistor, had an upset range of 9 fC to 13 fC. Strikes on transistor B did not result in an upset during simulations without charge sharing effects. However, when charge sharing was included in simulations, strikes to Transistor B resulted in SEUs. The upsets were caused by the current shared with Transistor A. Since the charge is attenuated over the distance between the two transistors, the injected charge values of the transition region increased. Transistor B has a transition charge range of 52 fC to 69 fC. Charge sharing significantly increased the total range of values for which parameter variations impact the SE response of the flip-flop.

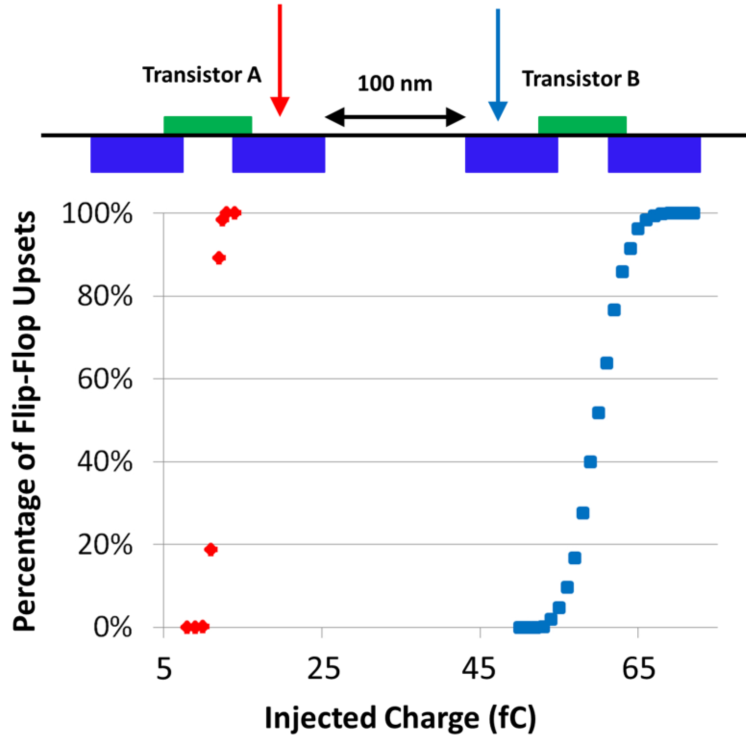

Fig. 45. The ranges of injected charge values for neighboring transistors in FF A. The charge range for a strike on Transistor A is 9fC to 13fC. The charge range for a strike on Transistor B is 52fC to 69fC.

Quantifying the influence of BSIM4 parameter shifts shows the significance that process variations can have on SE response. For the two flip-flop designs examined in this work, measurable process parameters were highlighted and shown to impact the flip-flops' SE responses in a consistent manner. Charge sharing was demonstrated to increase the charge range for parameter variation SE response impact. A quantified assessment of process-variation impact provides designers and fabrication engineers with the ability to determine important factors affecting the soft-error rates for flip-flops. Additionally, the ability to predict the radiation response of circuit lot based on determinable parameters could provide meaningful information about SEU likelihood.

CHAPTER V

VERIFICATION OF THE PROCESS VARIATION IMPACT ON SINGLE EVENT UPSET

When conducting research, particularly research based largely in simulations, it is vital to verify the veracity of the research through outside resources and experimental data. Toward that end, an extensive literature search was conducted and experiments were performed in order to confirm the impact of process variations on single event upset response.

Simulation Results Literature Survey

Previously mentioned papers by A. Balasubramanian, et al. relate the effect of random dopant fluctuations on threshold voltage and consequently on the radiation hardness of SRAM circuits [98], [99]. In both papers, simulations, in which threshold voltage was singularly varied, were conducted to determine the impact on single event upset response of the threshold voltage shifts caused by RDF. Balasubramian, et al. argues that an increase in the absolute value of the threshold voltage of the PMOS

transistors in an SRAM cell decreases the critical charge and increases the SEU sensitivity of the SRAM. Fig. 46 shows the change in the critical charge over the range of NMOS and PMOS threshold voltages for an off-state NMOS hit [98]. The cited research by A. Balasubramanian, et al., concurs with the correlation between the increased threshold voltage magnitude and increased SEU sensitivity presented in this work.

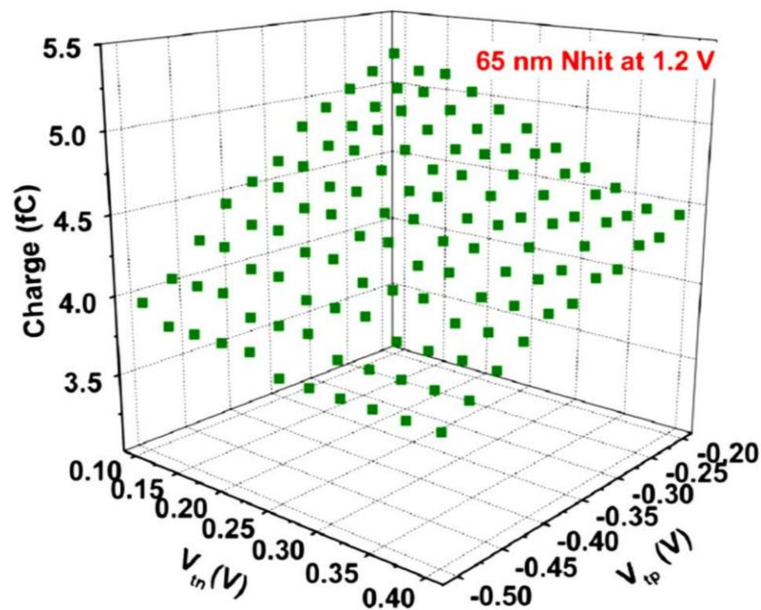

Fig. 46. The spread of critical charge values required for a bit flip in a 65 nm CMOS SRAM cell for an off-state NMOS transistor SE strike [98].

Jahinuzzaman, et al., develops an analytical model for critical charge as a method to analyze the soft error vulnerability of SRAM cells [115]. Simulation verification of the model compares the model to SPICE simulations and analyzes the impact of process variations on the SRAM single event response. Fig. 47 shows the relationships between threshold voltage and critical charge for NMOS and PMOS transistors for the SRAM

pictured in Fig. 48 [115]. For a single event strike on M_{nA}, the threshold voltage of M_{pA} has the greatest impact on the critical charge. As the threshold voltage of M_{pA} increases, the restoring current decreases and thus decreases the Q_c requires for SRAM upset. Similarly, an increase in the threshold voltage of M_{nB} causes a decreased restoring current for Node B. The decreased restoring current increases the sensitivity of Node B and lowers the critical charge for the SRAM. A decreased threshold voltage for M_{pB} would increase the ability of the transistor to turn on and supply current to Node B. Therefore, a decreased threshold voltage for M_{pB} increases the soft error sensitivity of the SRAM and lowers its critical charge.

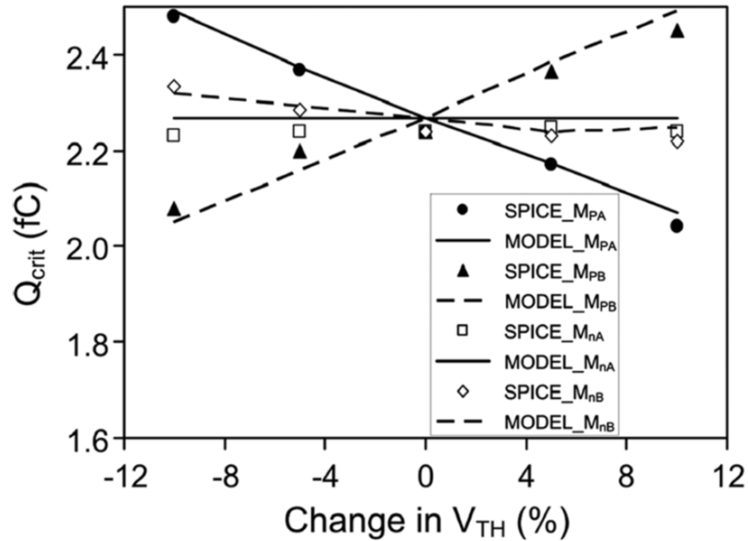

Fig. 47. Critical charge as a function of threshold voltages of the transistors in the cross-coupled inverters for the SRAM pictured in Fig. 43 [115].

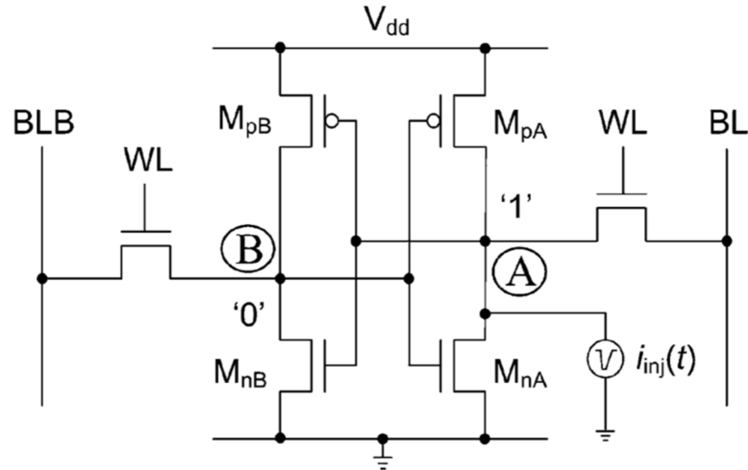

Fig. 48. SRAM with injected charge onto the drain of M_{nA}. The voltage value at Node A begins at '1' and the value at Node B begins at '0' [115].

The research conducted by Jahinuzaman, et al., also examined the impact of channel length and width variation on SRAM critical charge [115]. Fig. 49 shows the impact of the change in length on the SRAM critical charge. In general, an increase in channel length causes a decrease in drain current. For transistor M_{pA}, the decrease in drain current associated with an increase in channel length causes a decrease in the critical charge. For M_{pB}, an increase in drain current associated with a decrease in channel length provides a stronger pull-up current for Node B, once M_{pB} turns on. The effect of channel width variations was observed, during simulations, to be approximately the opposite of the effect of channel length variations. The change in effect occurs since an increase in channel width increased drain current. The impact of threshold voltage and channel length variation on soft error rates, as discussed by Jahinuzaman et al., is consistent with the research presented here.

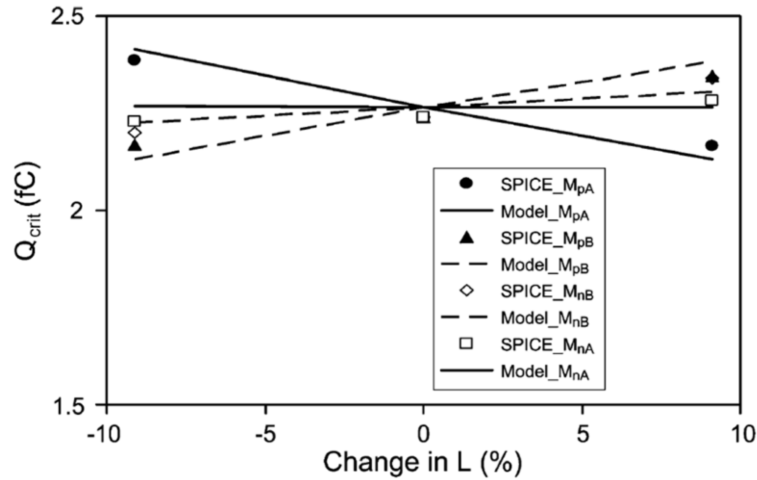

Fig. 49. SRAM critical charge as a function of the change in channel length [115].

Negative Bias Temperature Instability Literature Survey

Experimental verification of the impact of process variations on the single event response of latches provides additional confidence in the accuracy and reliability of the simulation results. It is necessary to add sufficient credence to simulation analyses of parametric variation on SEU response. One challenge of experimental analysis of process variations and their impact on single event upset response is the difficulty of identifying and varying the parameter values. Negative bias temperature instability, a type of device degradation, can be used to affect the threshold voltage of PMOS transistors. Device degradations, which include hot-carrier injection (HCI), gate-oxide breakdown, time-dependent dielectric breakdown (TDDB), and bias temperature instability (BTI), cause alterations in the characteristics of transistors over time [116]. They lead to behavioral parameter drifts during circuit operation [117]. Of the various

device degradation mechanisms, negative bias temperature instability is considered one of, if not the most critical [16]-[18].

Bias temperature instability, which describes the CMOS-device-characteristic changes that result from the application of bias at elevated temperatures, has emerged as one of the most important reliability issues for advanced CMOS technologies [16]-[18], [116], [118]-[121]. Bias temperature instability is particularly pronounced in PMOS devices under negative bias [116], [122], [123]. Deal et al. discussed facets of negative bias temperature instability in 1967 [124] and Jeppson et al. presented work focused on negative bias stress in 1977 [125]. Bias temperature instability stems from the trapped charges that are generated when bias is applied to the gate for a long duration or at elevated temperatures. The trapped charges cause changes in threshold voltage magnitude, mobility degradation, and transconductance [118], [122], [126]. Fig. 50 shows the degradation of threshold voltage after negative bias temperature stress [120].

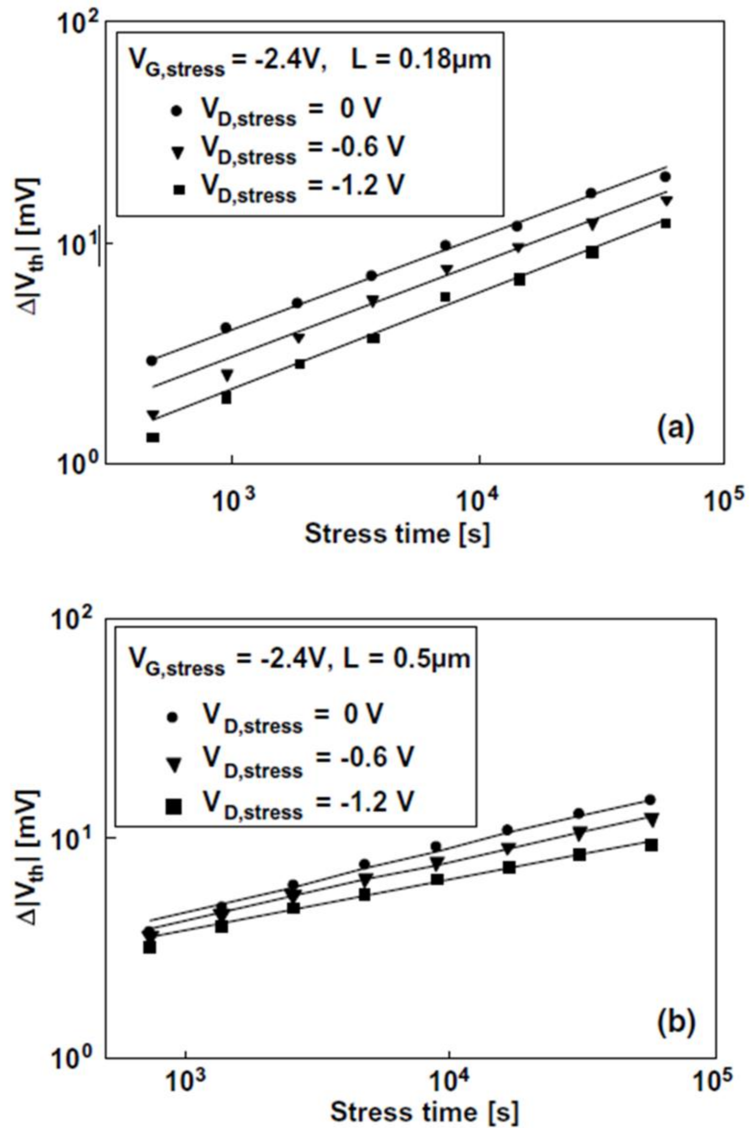

Fig. 50. Threshold voltage degradation after negative bias temperature stress. The W/L of the device geometries in a) is 10 µm/0.18µm and 10µm/0.5µm in b) [120].

Negative bias temperature instability has been demonstrated to cause increasingly challenging problems with circuit performance [118]. The threshold voltage shift caused by NBTI is a major reliability concern, particularly for circuits that employ matching [118]. In digital circuits, NBTI-induced shifts can lead to timing issues, reduced current,

frequency degradation in ring oscillators, and reduced noise margins in SRAMs [56]. Additionally, the issue of NBTI has been aggravated in advanced technologies due to thin gate dielectrics and higher oxide fields [55], [117], [118], [126], [127]. It has emerged as the dominant PMOS device failure mechanism at the advanced technology nodes.

The change in PMOS transistor threshold voltages due to NBTI can be used as an instrument to analyze the impact that a variation in threshold voltage has on SEU sensitivity. The effects of long-term NBTI can be replicated in accelerated testing by stressing circuits at high temperature and electric field [73]. Research conducted by D. Rossi, et al., relates the effects of NBTI to soft error susceptibility [128]. Simulations on combinational circuits and latches were conducted to determine the impact of NBTI on the critical charge of the circuits. In the simulations, the impact on the PMOS threshold voltage was determined by the model in [129]. The voltage shifts were used to customize the transistor model in order to simulate the circuits with the appropriate amount of NBTI-induced voltage shift. Fig. 51 shows the change in critical charge over the range of circuit operating time for an SRAM cell that stores a signal equal to 1 50% of the time (α=0.5) and for an SRAM cell that stores a static signal for the entire ten years (α=1) [129]. NBTI causes an increase in the PMOS threshold voltage. The increase in PMOS threshold voltage would lower drain current in the ON transistor and increase the susceptibility of the SRAM to soft errors. The simulation results agree with the parametric analysis presented in this paper.

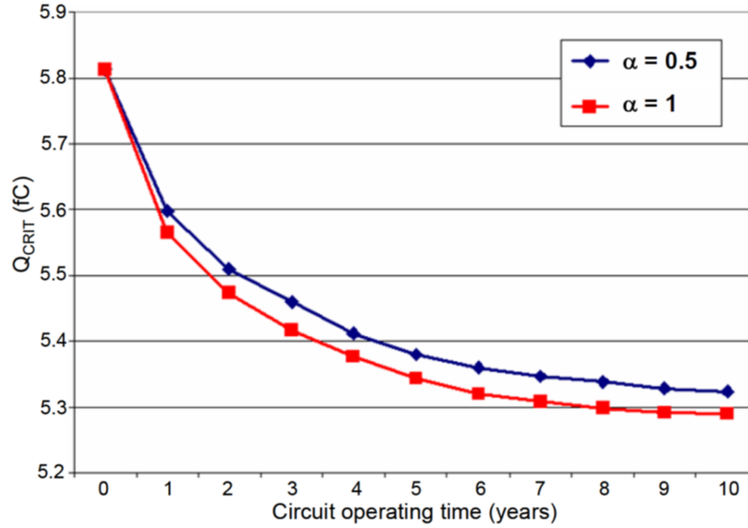

Fig. 51. Simulation results showing the SRAM critical charge as a function of the circuit operating time in years [128].

Experimental data documented by G. La Rosa, et al., relates the impact of negative bias temperature instability to the stability of SRAM cells. Fig. 52 shows the increase in SRAM failure count due to NBTI as a function of I_{CRIT}, which is the peak current of the "N Curve" [130]. The increase in the PMOS threshold voltage due to NBTI results in an increase in the soft error sensitivity of the SRAM. The SER increase is consistent with the other research presented here.

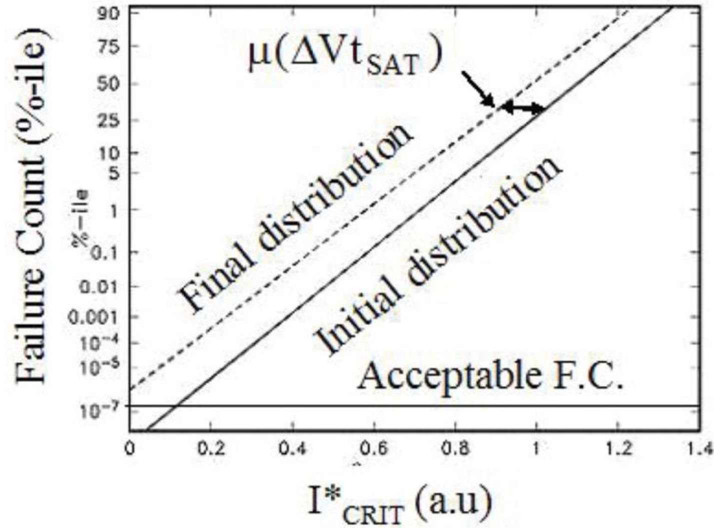

Fig. 52. Negative bias temperature instability induced increase in SRAM failure count as a function of I^*_{CRIT} [130].

Negative Bias Temperature Instability Experimental Data

The following work is purposed to determine the correlation between the process-variation simulations and negative bias temperature instability (NBTI) experimental data. Two methods were used to evaluate the predictive ability of the simulations. The first method estimated the increase in flip-flop sensitive area due to the NBTI-induced increase in PMOS threshold voltage magnitude. The second approximated the change in SEU likelihood based on simulation-based upset probabilities. Both approaches showed good correlation between the experimental and simulation data.

Experimental analysis of fifteen flip-flop designs with varying area, power, speed, and radiation-tolerance parameters was conducted. The flip-flops were stressed to induce

the effects of negative bias temperature instability. The NBTI-induced change in threshold voltage increased the single event upset likelihood of the flip-flops. The analysis presented here deals with one D flip-flop design. The analysis SEU cross-section trends observed in these two flip-flops were consistent for the others in the test set, and the analysis method is applicable to those designs as well.

The flip-flop designs were fabricated in a commercial 40 nm bulk dual-well, CMOS process using the CREST approach [131]. The simplified schematic in Fig. 53 generally describes the D flip-flop, which has approximately 16K stages. All support circuits (PLL, error detection, etc.) were designed on-chip and triple-modular redundancy (TMR) was used. As a result, all observed errors were solely due to the errors generated in the shift register.

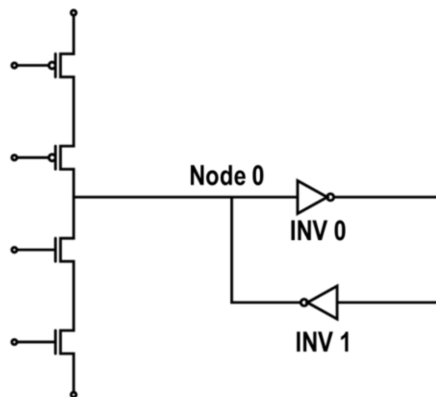

Fig. 53. A simplified schematic of the slave portion of the D-latch.

The chips were stressed at 80 °C with an increase over the nominal power supply voltage by approximately 15%. The overstress was carried out for approximately 12 hours and the ICs were allowed to cool to room temperature for a short time before being exposed to the ion beam. The heavy-ion testing was performed, both before and after stressing, using the 88-inch Cyclotron at the Lawrence Berkeley National Laboratory [132]. For both tests, all inputs to the shift registers during testing were kept at logic 1 to eliminate effects of ion hits on clock lines. The clock was active during the stress and test. All, but one of the tests, were performed to a fluence of $5x10^7$ particles/cm^2, with the one test having a fluence of $1.5x10^7$ particles/cm^2. The linear energy transfer (LET) of the incident particles was varied up to 58 MeV-cm^2/mg. The angle of incidence was varied between 0 degrees and 30 degrees.

NBTI causes an increase in threshold voltage (VTH) magnitude for PMOS transistors. Such an increase will cause a decrease in the PMOS transistor currents. For FF designs that are the most sensitive to n-hits (for which PMOS transistors provide restoring current), the effects of NBTI on SE error rates will be significant. On the other hand, if the most sensitive hits are p-hits (NMOS transistors provide restoring current drive), the effects of NBTI on the SE error rates may not be as significant. A decrease in restoring current may, depending on the specific circuit topology, result in a lowered critical charge value due to the decreased restoring current. The decreased critical charge value will increase the susceptibility of a flip-flop to single events.

In order to examine the veracity of the process-variation simulation analysis, a comparison of the simulation analysis and experimental data was conducted. For DFF1, the sensitive NMOS transistors were identified, as shown in Fig. 54 [133]. The NMOS

transistors were specifically selected since the SEU sensitivity of the NMOS transistors would be affected by negative bias temperature instability. Using the previously-described Monte-Carlo simulation approach, the effect of parameter variation on the sensitive NMOS transistors was determined. Fig. 55 shows the increase in upset probability with the increase in the LET of the incident particle for a simulated strike on the sensitive NMOS transistor for a HIGH clock state.

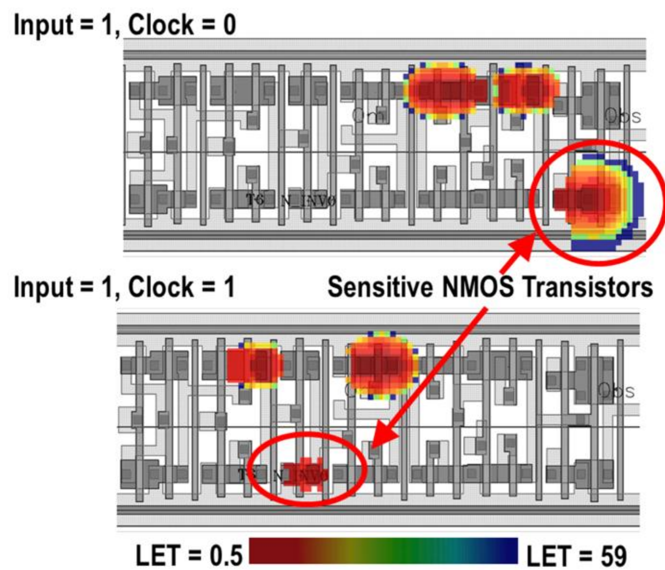

Fig. 54. Layout-aware simulation image highlighting the sensitive NMOS transistors [133].

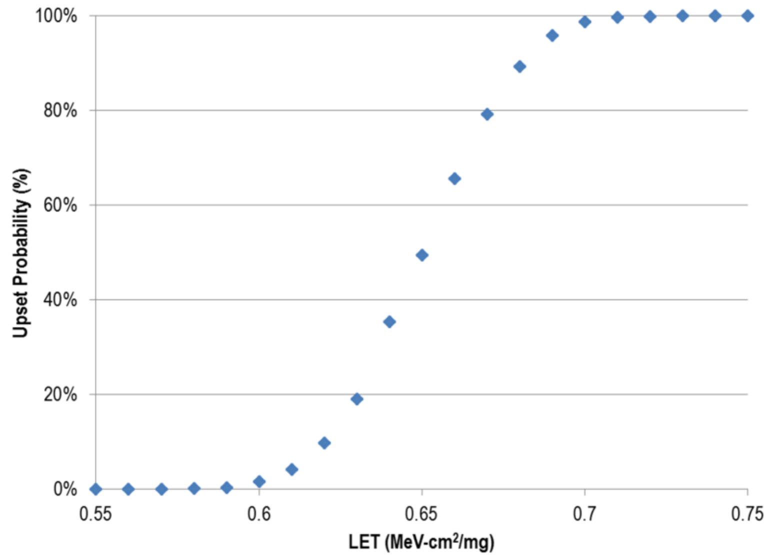

Fig. 55. Increase in flip-flop upset probability corresponding to the increase in the LET of a SE strike on the most sensitive NMOS transistor. The threshold voltage is nominal and the clock state is HIGH.

In order to determine the impact of NBTI on the PMOS threshold voltage, the NBTI model described in the IBM 65nm CMOS process design kit was used to calculate the NBTI-induced increase in the magnitude of threshold voltage [134]. Fig. 56 shows the increase of threshold voltage over time. For the stress time of 12 hours, the change in threshold voltage is approximated to be -17 mV. During the analysis of the Monte-Carlo simulations, the range of parameter values for each parameter is divided into bins. Quantification of the NBTI-induced threshold voltage shift allows the identification of the bin that corresponds to the NBTI-induced threshold voltage. Once the appropriate threshold voltage bin is determined for the post-stress threshold voltage, the sensitivity of DFF1 to the NBTI-altered threshold voltage may be determined via the parameter value upset probabilities. Fig. 57 shows the change in the upset probability over incident LET values for the nominal and NBTI-induced threshold voltages. The NBTI-shifted

threshold voltage results in a more sensitive flip-flop due to the decrease in PMOS restoring current. The increase of the SEU sensitivity of DFF1 should result in an increase in SEU upsets and consequently in an increase in cross-section. Estimating the increase in cross-section based on the process-variation simulations would allow the comparison of the experimental data and the process-variation simulations.

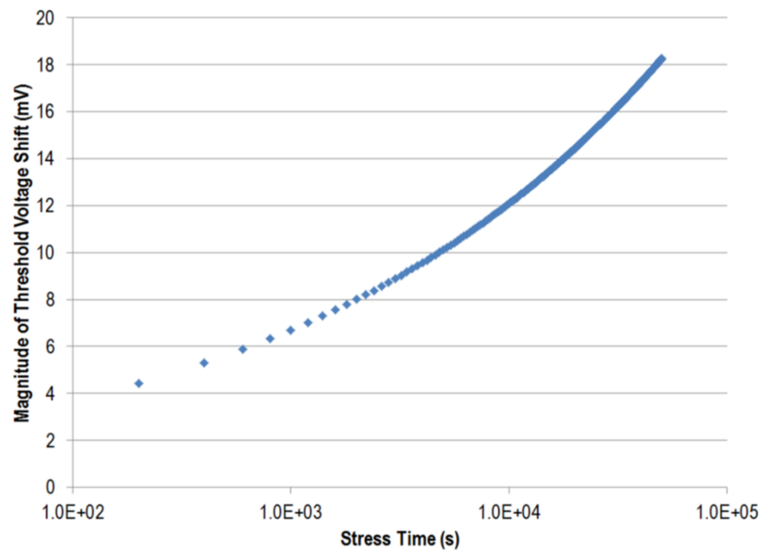

Fig. 56. NBTI-induced increase in the threshold voltage magnitude of PMOS transistors based on the stress-time [134].

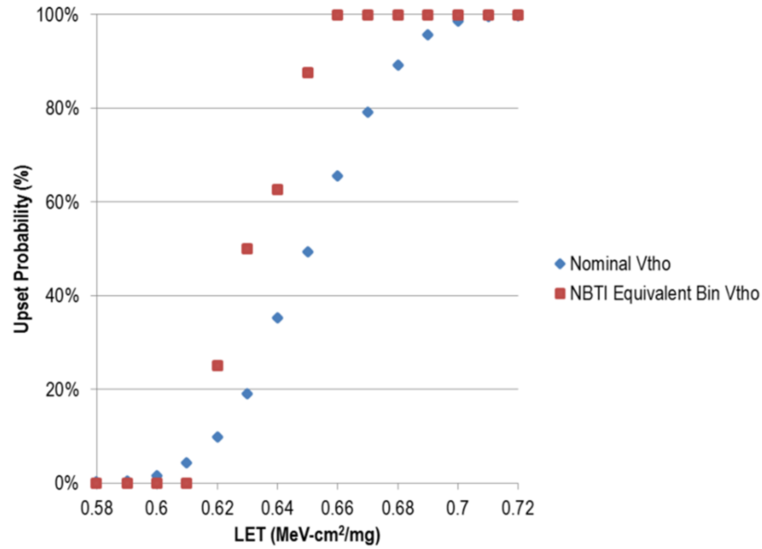

Fig. 57. Change in upset probability due to increase in threshold voltage magnitude due to NBTI.

Two different approaches were used to determine the correlation between the simulation and the lower-LET experimental data. The first estimates the increase in sensitive area resulting from NBTI stress. Due to charge-sharing, a single event may strike a circuit at one location and the charge may spread through the substrate to a sensitive transistor. The charge collected by the sensitive transistor can then result in an SEU. Previous work has used a 3D-TCAD calibrated relationship in order to determine the amount of charge collected by multiple devices based on the distance between primarily-struck transistor and secondary transistor [96], [100], and [135]. The relationship used the injected charge in the primary transistor and the distance between the primary and secondary transistor to determine the approximate charge collected by the secondary transistor. In this work, the 3-D TCAD based charge sharing relationship was used to solve for the maximum strike distance from the sensitive device, which still

results in a collected charge capable of upsetting the flip-flop. The estimation of the maximum distance between a single event strike and a transistor given a specific collected charge can be used to approximate the sensitive area for a specific transistor by using the distance as the radius of a sensitive area circle. The area difference between the nominal threshold voltage sensitive area circle and the sensitive area circle for the NBTI collected charge is equivalent to the increase in cross-section due to strikes near the NMOS transistor as a result of NBTI-induced PMOS threshold voltage shift.

The SEU response of a flip-flop is particularly sensitive to process variations at an upset probability of 50%. Therefore, the LET value selected for the sensitive distance estimation was the value that corresponds to an upset probability of 50%. The LET values corresponding to a 50% upset probability were determined for both the nominal and the NBTI-shifted PMOS threshold voltages. Since the LET value that corresponds to the NBTI-shifted threshold voltage is lower than the value associated with the nominal threshold voltage, the maximum allowable distance between a SE strike and the sensitive transistor is greater after NBTI. The difference between the approximate sensitive area after negative bias temperature instability and the nominal sensitive area for a specific transistor is the amount of sensitive area increase due to NBTI for strikes near the specific NMOS transistor being examined. The increase in area for each of the sensitive NMOS transistors was summed to get a total sensitive area for each clock state. Then, the increase in sensitive area for the LOW and HIGH clock states was averaged for a 50% duty cycle, which was the condition during testing. This determines the sensitive area increase that is equivalent to the increase that might be observed under test conditions.

The sensitive NMOS transistors for both clock LOW and clock HIGH states were identified and process-variation simulations were conducted to mimic the test condition of a 50% duty cycle. Then, the difference between the NBTI-induced sensitive area approximation and the nominal sensitive area approximation was determined for the sensitive transistors. The increase in sensitive area for both clock states was averaged to find the approximate increase in overall sensitive area due to NBTI. The increase in sensitive area was added to the pre-stress cross-section values for the experimental data and compared to the post-stress cross-section values. Fig. 58 shows the pre-stress cross-section, the post-stress cross-section, and the simulation-based post-stress cross-section approximation.

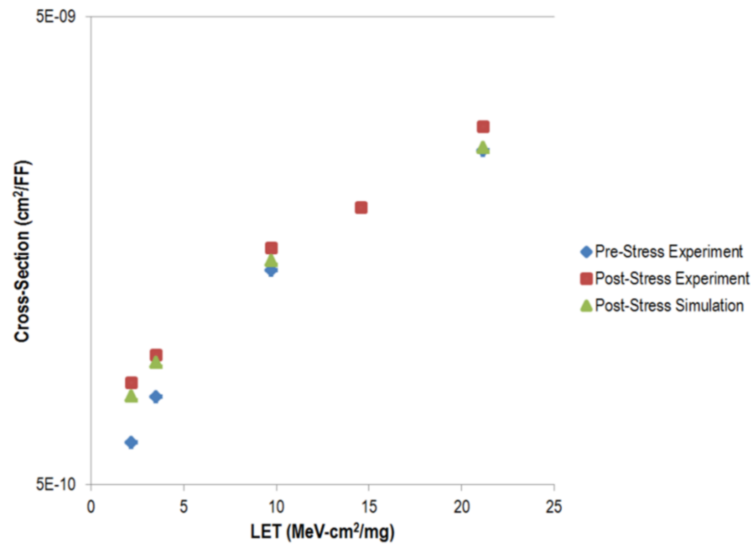

Fig. 58. Comparison of the pre-stress cross-section, the post-stress cross-section, and the process-variation simulation-based post-stress cross-section approximation.

The second approach for the comparison of the process-variation simulations and the experimental data uses a ratio of the upset probabilities that correspond to the nominal bin and the NBTI-shift associated bin. For each of the sensitive NMOS transistors at the nominal threshold voltage, the average upset probability is calculated over the range of LET values that produce a 0% upset probability to a 100% upset probability. The average upset probability for the NBTI-shifted threshold voltage is calculated for the same range of LET values. The nominal and NBTI-associated overall upset probabilities for each sensitive transistor are each averaged to determine the average upset probability for each clock state. Those upset probabilities, for both nominal and NBTI-shifted threshold voltage bins, are then averaged over the clock HIGH and clock LOW states. The resulting overall upset probabilities provide first-order representations of the likelihood of SEU for the flip-flop before and after NBTI stressing.

The ratio of the NBTI-associated upset probability to the nominal upset probability represents the average increase in upset likelihood. Multiplying the pre-stress experimental data cross-section values by the ratio representing the NBTI-induced increase in overall upset likelihood provides an estimation of the simulation-predicted NBTI impact. Fig. 59 compares the pre-stress cross-section, the post-stress cross-section, and the estimation of the post-stress cross-section. The correlation between the post-stress cross-section and the simulated post-stress cross-section is significant. The correlation for the larger LET values is limited since the method does not include the LET-associated SEU variations related to variations in collection distance. The ratio is developed for the smallest LET values where the process variation is significant, and where the SE strikes are not at the saturated maximum distance for charge sharing.

However, this approach does not require TCAD calibration or in-depth knowledge of the circuit layout.

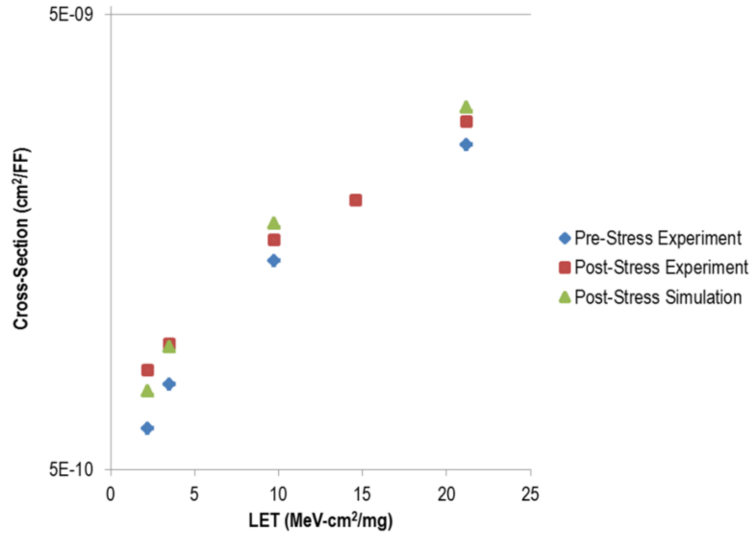

Fig. 59. Comparison of the pre-stress cross-section, the post-stress cross-section, and the overall upset probability based estimation of the post-stress cross-section.

The same approach using the overall upset probability can be used to estimate the relationship between the change in threshold voltage and the resulting change in cross-section. For each threshold voltage bin (which can be represented as the nominal threshold voltage plus some threshold voltage delta), the average change in upset probability was determined by taking the ratio of the associated upset probability to the nominal threshold voltage upset probability. Then, the anticipated cross-section corresponding to the threshold voltage bins was determined by multiplying the pre-stress cross-section by the expected change in upset probability. The change in threshold

voltage (from the nominal threshold voltage) was correlated to the delta between the anticipated cross-sections and the cross-section associated with nominal V_{THO}. Fig. 60 shows the relationship between the change in PMOS threshold voltage and the corresponding change in cross-section for an LET strike of 3.49 MeV-cm^2/mg. The figure shows that a decrease in the threshold voltage, which is actually an increase in the threshold voltage magnitude for PMOS V_{THO}, typically causes the cross-section of the flip-flop to increase. The description of the relationship between the change in threshold voltage and the change in flip-flop cross-section provides insight the effect of NBTI-induced threshold voltage variations over varying times of NBTI exposure.

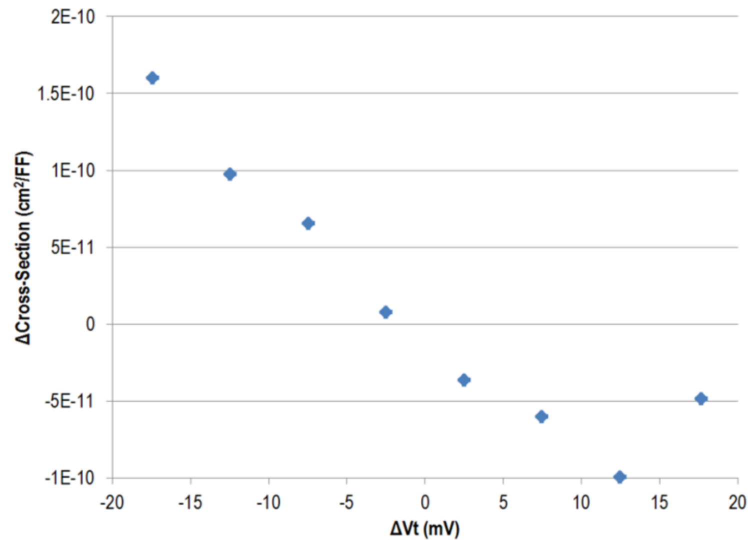

Fig. 60. Relationship between the change in threshold voltage and the resulting change in flip-flop cross-section for an incident ion LET of 3.49 MeV-cm^2/mg.

Both of the methods used for simulation data assessment show good correlation between the simulation and experimental data. For the collection distance analysis, correlation is greatest for the lowest LET values in the experimental data since the low LET values correspond to the values indicated in the simulation data to be the most sensitive to parameter variation. The overall upset probability analysis shows good first–order agreement between the simulation and the experimental data over the entire range of LET values. The analysis provides further verification to the veracity of the process-variation simulations.

There are five instances of experimental and simulation data that have been documented in the literature and that corroborate the conclusions drawn in this research. Also, the NBTI tests reveal an increase in sensitive area with the increase in PMOS threshold voltage. The corroboration of data from the literature and the negative bias temperature instability experiments provides further credence to the presented parameter analysis.

CHAPTER VI

IMPACT OF PROCESS VARIATIONS ON UPSET REVERSAL IN A 65 NM FLIP-FLOP

In advanced integrated circuits, multiple node charge collection increases due to the decreasing device size and the proximity of transistors. The increase in charge sharing leads to an increase in the incidence of competition between electrical propagation and charge propagation. This leads to the possibility of multiple thresholds in SEU response. Analysis of flip-flop single event upset response demonstrated the existence of a second threshold to the SEU response due to an upset reversal mechanism. The impact of process variations on the critical charge threshold has been examined for 6T SRAM cells and for DICE and D flip-flops. Analysis of the impact of process variations on the upset reversal threshold was also conducted.

Simulations were conducted using a low-power version of D flip-flop design to analyze the impact of process variations on upset-reversal. The flip-flop has a master-slave topology. The flip-flop was targeted to both a 45 nm and a 65 nm commercially-available, bulk-CMOS process. Single events strikes were modeled using a bias-dependent SE model [112]. Charge sharing was included by modeling the multiple-node charge collection with additional injected charge as previously described.

Preliminary simulations were conducted to isolate the transistors demonstrating sensitivity to upset reversal. The simulations covered all input options and all clock input options (High, High; High, Low; Low, High; and Low, Low). Then, Monte-Carlo simulations were conducted on sensitive transistors to determine the impact of process variations. The Monte-Carlo simulations simultaneously varied the BSIM4 transistor parameters according to the statistical variations supplied by the manufacturer in the process design kits for the 45 nm and 65 nm bulk-CMOS processes.

Upset Reversal Mechanism

Simulations elucidated the upset reversal mechanism in the flip-flop under each of the input and clock possibilities. In each instance, the upset reversal effect reflected the same general pattern. At its core, the mechanism is a product of charge sharing. After a single event strike occurs on a transistor, the deposited charge spreads to other nearby transistors. In a manner similar to pulse quenching [91], [92], the secondary currents combined with the feedback in the latch cause the altered output that was triggered by the initial SE strike to reverse to its original state.

One set of transistors showed particular sensitivity to upset reversal. It was affected by upset reversal for both the HIGH and LOW input values when the initial clock state is LOW. It also occurred in the master sub-circuit and the identical slave sub-circuit. A partial schematic of the slave sub-circuit is shown in Fig. 61. Upset reversal occurs for a strike on the NMOS transistor in Inverter 0 (N_INV0). The following steps, which correspond to the numbers in Fig. 61, describe the progression.

1) A single event strike occurs on the drain of N_INV0.

2) When the SE hits N_INV0, the deposited charge pulls the inverter output from the original value of HIGH to the SE-induced value of LOW, as shown in Fig. 62.

3) The change in the output of INV0 propagates through INV1. At the same time, the deposited charge spreads through the substrate and reaches Transistor T6. In the circuit layout, T6 is a neighboring transistor to N_INV0, as shown in Fig. 63. It is part of a tri-state inverter. The charge deposited by the SE hit spreads to T6 and gets collected by the drain region of T6. The output of INV1 switches from LOW to HIGH, as shown in Fig. 64, on a similar timescale as when T6 starts to collect charge.

4) The charge collected at the drain of T6 negates the charge provided to NODE 0 by the PMOS transistors in INV1. Given sufficient charge, the collected charge effectively prevents the SE-induced transient from altering the voltage at NODE 0. NODE 0 changes from LOW to HIGH only momentarily. After brief fluctuation, NODE 0 reverts back to the correct value of LOW, as shown in Fig. 65. The minimum injected-charge value to prevent flip-flop upset is called the reversal charge since the change in voltage effectively reverses the SE induced pulse at NODE 0.

5) The change in the INV0 input signal causes the INV0 output to return to the original high value, as shown in Fig. 66.

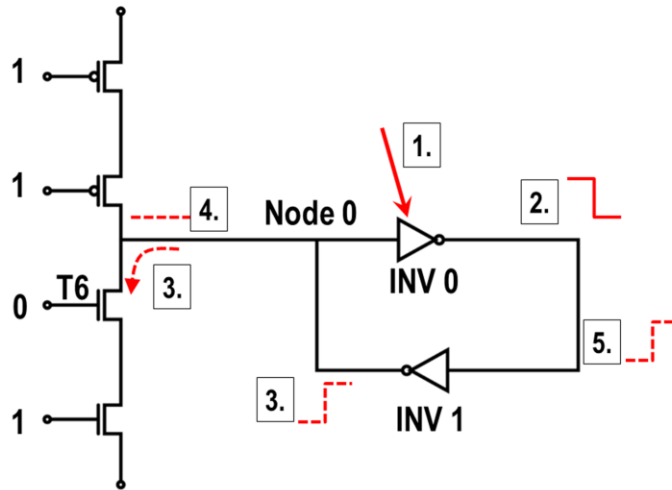

Fig. 61. A partial schematic of the master-slave flip-flop. It shows the progression of the upset-reversal mechanism.

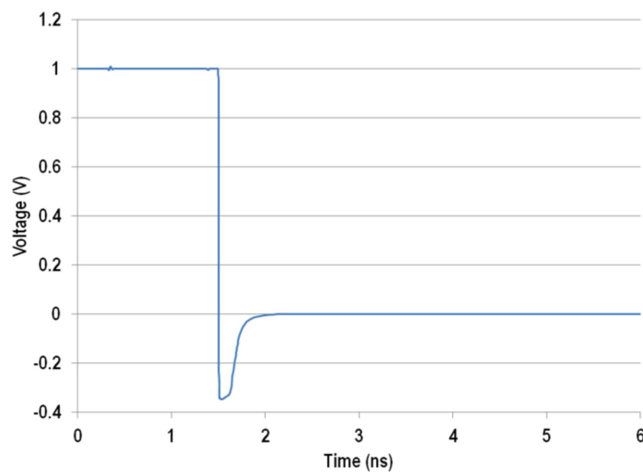

Fig. 62. The voltage signal at the output of inverter 0 (INV0) after a single event strike to the drain of the NMOS transistor in the inverter.

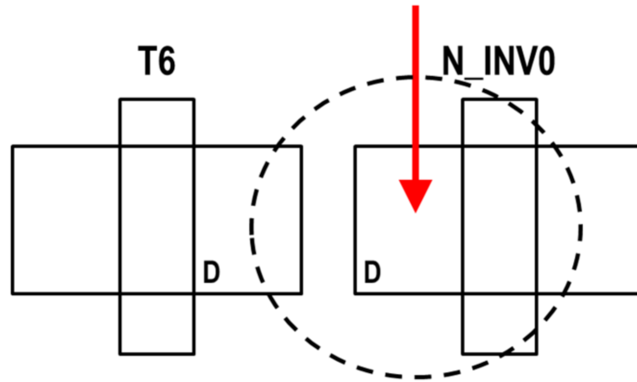

Fig. 63. An illustration of the sharing of charge between N_INV0 and T6 after a single-event hit.

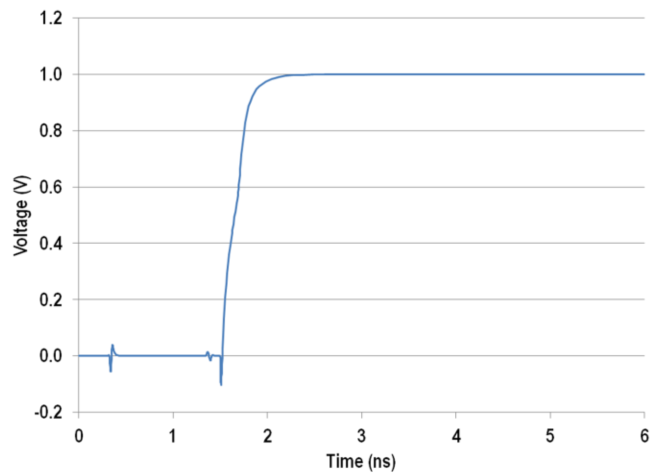

Fig. 64. The voltage signal at NODE 0 given that insufficient charge is collected by T6 in order to draw current through the transistor. The voltage signal changes from the correct value of LOW to the SE – induced value of HIGH.

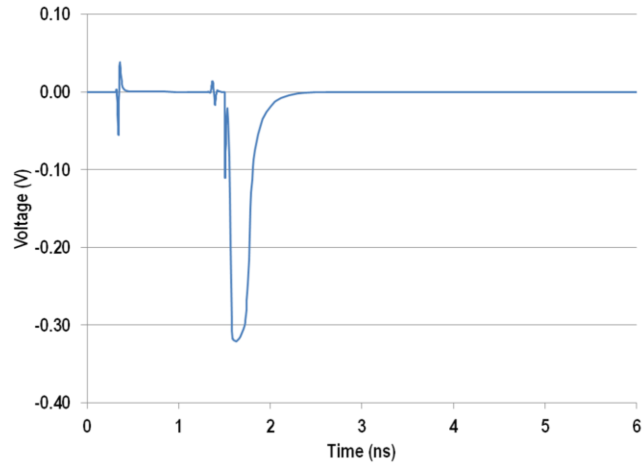

Fig. 65. The voltage signal at NODE 0 given that sufficient charge is collected by T6. If so, charge collected by T6 prevents the SE–induced transient from changing the voltage at NODE 0.

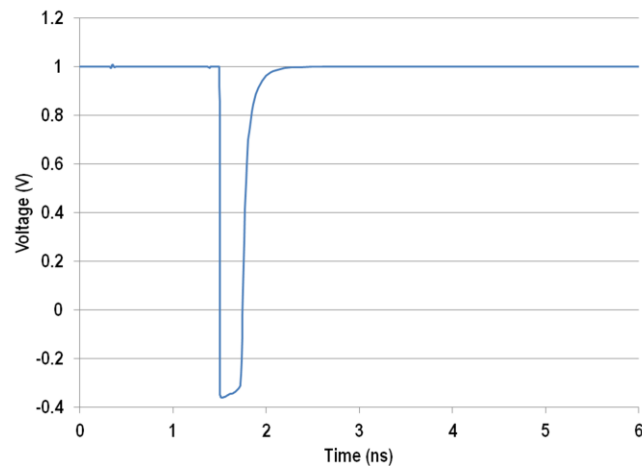

Fig. 66. The voltage signal at the output of INV0 if the reversal charge was reached. The signal changes back to the correct value of HIGH. The change takes approximately 0.5ns.

Three-dimensional mixed mode technology computer-aided design (TCAD) simulations were conducted on the flip-flop to further analyze the upset reversal mechanism. Using mixed-mode simulations allowed T6 and N_INV0 (the NMOS transistor from INV0) to be modeled using calibrated 3-D TCAD and the remaining transistors to be modeled using compact models. The transistor sizing and spacing was

based on the fabricated flip-flop layout. Fig. 67 shows the 3-D structures used in the TCAD simulations (For clarity, the field oxides are not shown in the image). The simulations used Fermi-Dirac statistics, SRH and Auger recombination, and the Carrier-Carrier Scattering mobility model. The simulated ion strikes occurred in the center of N_INV0. The heavy-ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 25nm, and a Gaussian temporal profile with a characteristic decay time of 2ps.

The mixed-mode simulations demonstrated the upset reversal mechanism. Fig. 68 shows both the NODE 0 and the INV0 output node voltage signals given that insufficient charge is collected by T6 in order to cause upset reversal. Fig. 69 shows both node voltages given that a sufficient charge is collected by T6 to cause upset reversal.

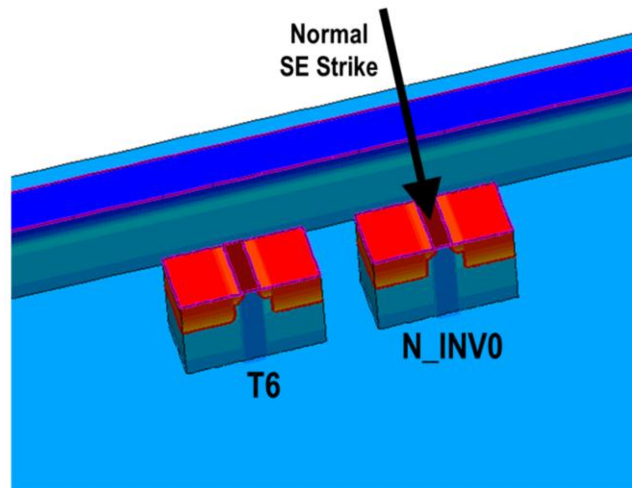

Fig. 67. Three-dimensional TCAD model of T6 and the NMOS transistor in INV0. In the picture, the field oxides are removed for better clarity.

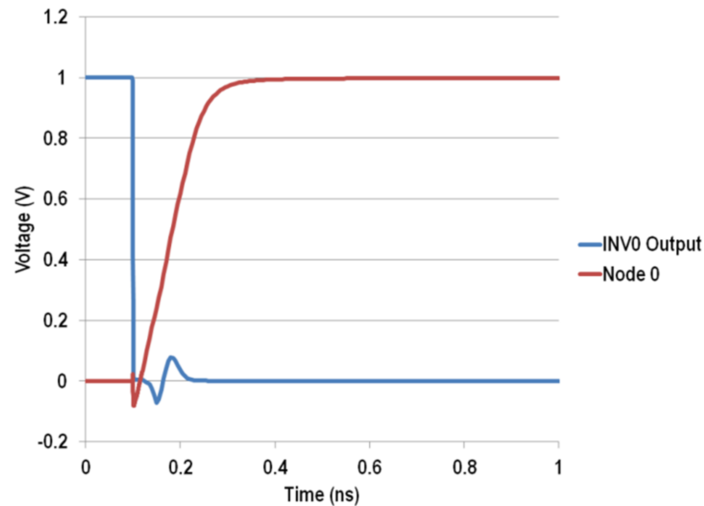

Fig. 68. The voltage signals at NODE 0 and the output of INV0 given that insufficient charge is collected by T6 in order to cause upset reversal.

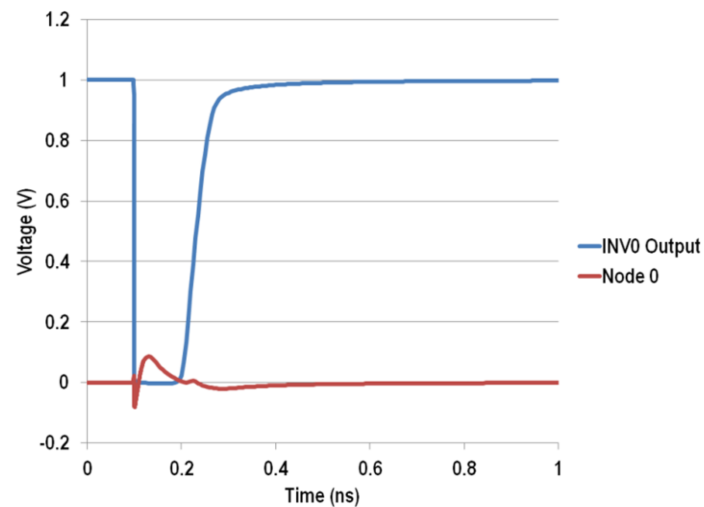

Fig. 69. The voltage signals at NODE 0 and the output of INV0 given that sufficient charge is collected by T6 in order to cause upset reversal.

Upset reversal can only occur under a precise set of conditions. There must exist a set of transistors consisting of the primarily struck transistor and the secondary transistor(s) in proximity. Also, the charge collected by the secondary transistor(s) must cause a voltage shift in the opposite direction than the voltage transient induced by a SE

strike on the primary transistor. The transistors must be close enough in the circuit layout that charge deposited in the primary transistor spreads through charge sharing to the secondary transistor(s). Under these conditions, upset reversal will result in a charge window for which a flip-flop will experience an upset. If the deposited charge is less than a certain threshold (usually the critical charge of the flip-flop), the flip-flop will not experience an upset. If the deposited charge is higher than a particular tolerance, upset reversal will result in a no-upset condition. One advantage of using upset reversal as a hardening mechanism is the minimal space requirement. In the example flip-flop, no extra transistors were added for the purpose of upset reversal.

As a whole, the conditions required for upset reversal can be determined during circuit and layout design. If desired, a designer could intentionally create the conditions necessary for upset reversal in order to use the mechanism as a hardening technique. In this way, upset reversal could function as a type of common-mode-rejection that reverses the impact of an SET. Previous research has indicated that another technique that employs layout proximity and common mode rejection can be used to assist in SET rejection [101]. Additionally, reinforcing charge collection (RCC) and single event upset reversal employ multiple node charge collection to reduce soft error rates [136]-[138]. RCC uses two main principles: 1) Placing state reinforcing nodes and diffusions as closely as possible together and 2) Maximizing the separation of nodes that increase the critical charge [137], [138]. N. Seifert, et al., performed proton irradiation testing on multiple SRAM designs to determine the effect of design on radiation response. Fig. 70 shows the resulting cross sections [138]. The RCC latches (CNL: RCC and IUCF: RCC)

show decreased cross-sections compared to the standard latches (CNL: Latch and IUCF: Latch).

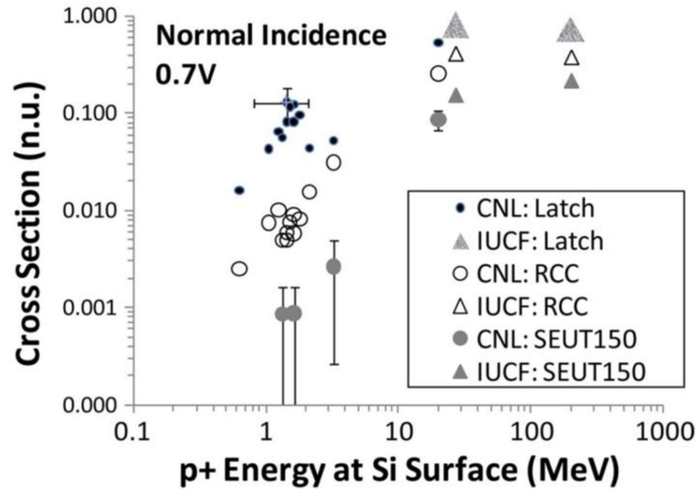

Fig. 70. The normalized cross-sections for multiple 32 nm devices [138].

Parametric Variation Impact on Upset Reversal

Shrinking device sizes have significantly impacted the challenges associated with circuit performance. The soft error rate of circuits has increased due to decreased storage charge and increased operating speeds [3]. Charge sharing has become a sizeable issue due to its prevalence in advanced technologies and its propensity to increase the susceptibility of many circuits to SE radiation [26], [85]-[87]. Additionally, process variations have increased as device sizes have decreased [22]-[25]. These variations cause challenges for circuit performance [25] and impact the single event response of circuits [95], [97]-[99]. Since upset reversal depends strongly on the effects of shrinking

device sizes, an analysis of the potential impact of process variation provides valuable information that can be used during circuit design.

In order to determine the impact of parameter shifts on upset reversal, simulations were conducted to analyze the impact of process variation on the reversal-charge values. The reversal charge value refers to the higher charge threshold at which a flip-flop will not show an upset (or the amount of charge required so that upset *does not* occur). A Monte Carlo approach was selected for the simulations since that approach captures the extremities of circuit performance. In a reliability situation, it is important to know how a circuit will perform under all, not just typical, circumstances. A Monte Carlo simulation set was performed on each of the junctions that demonstrated the upset reversal mechanism. After every simulation, each parameter value, the upset response, and the injected charge value were recorded in order to analyze the relationship between parameter values and SE response. Each simulation set confirmed that upset reversal occurred regardless of the parameter variation. However, the reversal charge value shifted with the varying parameters. The shifting of the reversal charge values affects which single events (due to their associated LET value) trigger the upset reversal mechanism and can thus impact the overall single event sensitivity of the circuit.

For the flip-flop example, the nominal charge for SET reversal for a strike on the drain of N_INV0 is 96 fC. However, the range of SET reversal charges over the Monte Carlo simulation set begins at 76 fC and ends at 116 fC. Fig. 71 shows the spectrum of the SET reversal-charge values. The process variations cause a shift of +/- 20% in the reversal-charge values.

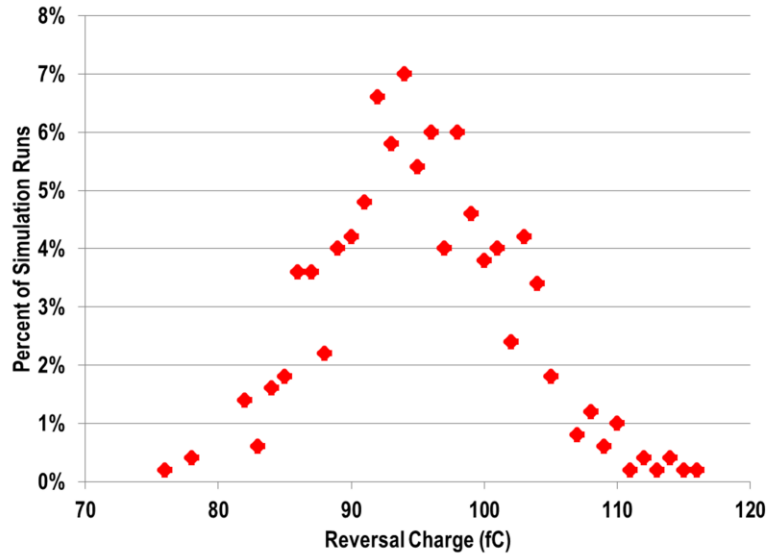

Fig. 71. The spectrum of the reversal charge values for a single event hit on the N_INV0.

The range of reversal-charge values indicates that process variation impacts upset reversal, but does not indicate which parameters are the most impactful. In order to determine which parameters exercise the most influence, the reversal charge was correlated to the specific parameter values (for all varying parameters) for each simulation in the simulation set. Since multiple parameters have varying values, the correlation is a manner of examining the simulation data from the perspective of a single parameter. The effect of the other varying parameters can be seen in the range of upset reversal charges for a specific parameter value. In the analysis, a greater correlation coefficient implies a stronger relationship between the reversal charge and a parameter. A strong relationship indicates that the variation of the parameter affects the onset of upset reversal. Several parameters show a significant correlation coefficient to the onset of upset reversal. The most strongly correlated parameters are TOXE, the electrical gate oxide thickness, VTHO, the threshold voltage, XW, width variation due to masking and etching, and XL, length variation due to masking and etching, for the PMOS transistors.

Oxide thickness varies with wafer furnace position, process temperature, and atmospheric pressure [139]. Such variations lead to changes from run-to-run, die-to-die, and within-die in the oxide thickness [140]. TOXE is the BSIM4 model transistor parameter that represents the electrical gate oxide thickness. The simulations show that when TOXE increases, the reversal charge decreases. Fig. 72, through a correlation scatter plot, shows the relationship between the upset-reversal charge and the PMOS transistor TOXE value, which is presented as a percentage of the nominal value. Increases in TOXE values decrease the nodal capacitances in the flip-flop. The decreased TOXE values also affect the threshold voltage, and subsequently the transistor currents and gate delays, to alter the reversal charge requirements.

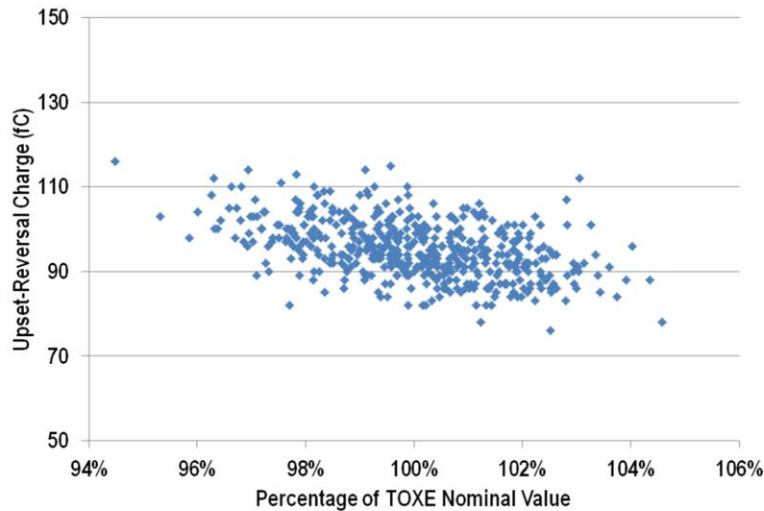

Fig. 72. A scatter plot showing the correlation between the electrical gate oxide thickness and the upset-reversal charge.

Masking and etching issues lead to variations in the channel. In SPICE, variations in the channel width are represented by the parameter XW (for NMOS transistors in this case). Since it represents the variation in the channel width (instead of the actual channel

width), XW must be added to the drawn channel width to get the effective channel width. The magnitude of the nominal value of XW is approximately 5.7% of the drawn channel width for N_INV0 in the 65 nm CMOS process. Thus the variance of the nominal XW magnitude over the Monte Carlo simulations represents approximately -2% to 14% of the drawn channel width. Variations in XW affect the onset of upset reversal. Fig. 73 shows that the reversal charge decreases as XW increases. Increases in XW increases the effective channel width and subsequently affects individual transistor currents and gate delays. The increase in the restoring transistor current and decrease in gate delays increases reversal charge requirements. Therefore as XW increases, the upset reversal charge increases.

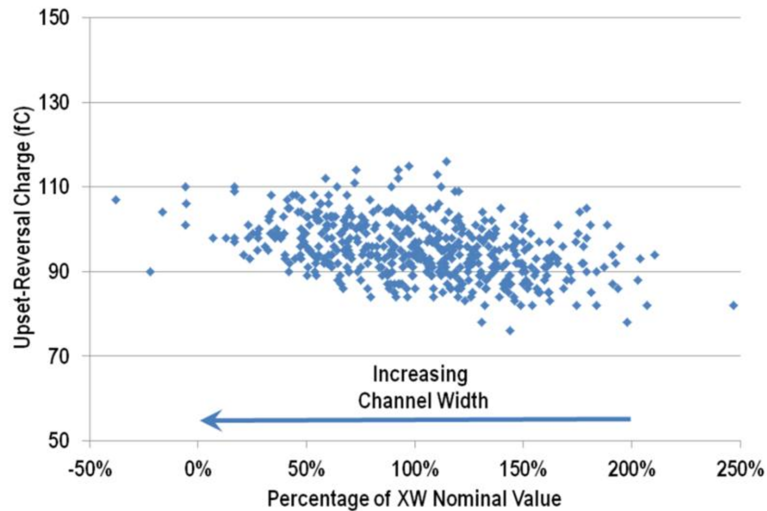

Fig. 73. A scatter plot showing the correlation between the channel width variation and the upset-reversal charge.

Similarly, shifts in the parameter XL, which is channel length variation due to masking and etching, impact the upset-reversal value. The effective channel length is determined by adding the variation, XL, to the drawn length. The magnitude of the

nominal value of XL, for PMOS transistors, is approximately 8.5% of the drawn channel length. Therefore, the range of XL magnitudes over the Monte Carlo simulations is -2% to 26% of the drawn value. As XL increases, the effective channel length increases. While channel length is a factor in both nodal capacitance and drain current, the effect on drain current is the dominant effect. Increased channel length decreases the current through the PMOS transistors that provide current reinforcing the upset NODE 0 value. The decrease in reinforcing current increases the ability of the collected charge to pull the value at NODE 0 back to the original low value. Thus an increase in XL lowers the upset-reversal charge values, as shown in Fig. 74.

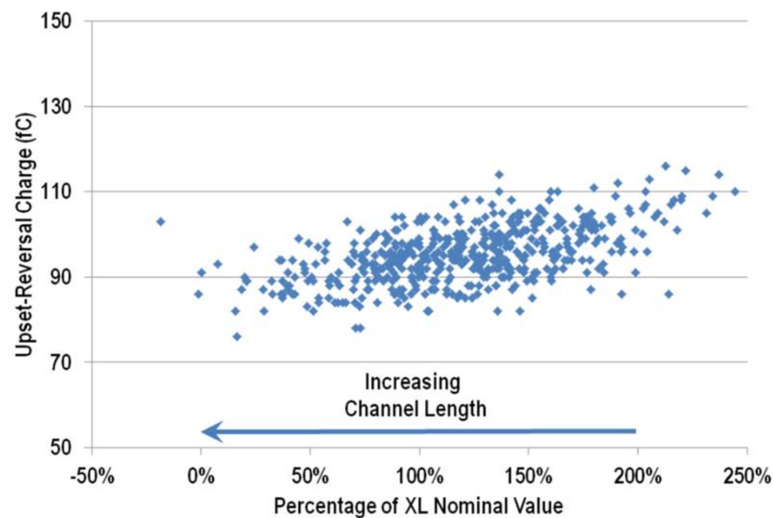

Fig. 74. A scatter plot showing the correlation between the channel length variation and the upset-reversal charge.

Threshold voltage variations result from oxide thickness and dopant fluctuation issues [4]. The variations impact the flip-flop reversal charge by affecting the current provided by the PMOS transistors in the tri-state inverter INV1 and the restoring current

drive at the hit node. As the magnitude of the threshold voltage (for a PMOS transistor) increases, the reversal charge value decreases. When the magnitude of threshold voltage increases, the current supplied by the transistor is lower. Since PMOS transistors provide restoring current, lower current increases the ability of the collected charge to pull the upset nodal voltage back to LOW. Therefore an increase in threshold voltage magnitude results in a lower reversal-charge value, as shown in Fig. 75.

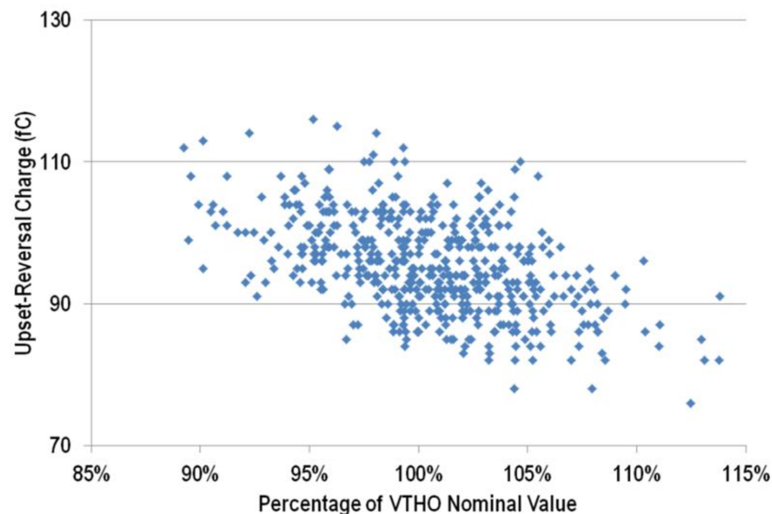

Fig. 75. A scatter plot showing the correlation between the threshold voltage and the upset-reversal charge.

Process variations impact the onset of upset reversal by affecting nodal capacitance and restoring current. This indicates that several factors can impact the onset of upset reversal because several factors affect nodal capacitance and restoring current. Table VIII shows the correlation coefficient between VTHO, TOXE, XL, and XW, and the upset-reversal charge values. Since no single parameter is solely responsible for the change in upset-reversal values, the correlation coefficients are significant, but none of

them dominates the mechanism. It is interesting to note the holistic impact of the parameter variations.

TABLE VIII.
THE CORRELATION COEFFICIENTS OF THE HIGHEST-IMPACTING TRANSISTOR PARAMETERS

TOXE	XW	VTHO	XL
-0.452	0.405	0.491	-0.549

As device sizes shrink, circuit reliability has encountered significant challenges. Single events have caused an increased number of soft errors, charge sharing has contributed to amplified SE sensitivity, and process variations progressively impact circuit performance and radiation response. The interaction between transistor-level process-variations and the upset-reversal mechanism has been analyzed. Process variations are shown to change the onset of upset reversal for a master-slave flip-flop. Analysis of the interactions between the process variation and upset reversal provides a more accurate description of the radiation-response mechanisms anticipated in advanced sub-micron circuits

Error Source Analysis

During a simulation or experimental analysis, a thorough description of the error sources adds to the efficacy of the analysis. In the analysis of the impact of process parameter variations on the single event upset response of sub-100 nm latches, there are five main sources of error. These include the manufacturer modeling error, the BSIM4 quantization error, the numerical error, the circuit modeling error, and the Monte-Carlo sampling error. The manufacturer modeling error, E_{TM}, describes the difference between the BSIM4 transistor model of transistor behavior and the actual behavior of the transistor. Asenov, et al., analyzes the compact modeling (CM) parameter generation for the BSIM4 model and the PSP model [141]. The work particularly considers the statistical variation found in integrated circuits and provides an estimate of the error between actual transistor behavior and the model representation of transistor behavior. Table IX lists the statistical parameter extraction errors for BSIM4 models as a function of the number of parameters that were used to capture the intrinsic statistical variation in an actual transistor [141].

TABLE IX.
STATISTICAL PARAMETER EXTRACTION ERRORS FOR BSIM [141].

Number of Parameters	Average RMS fitting error (%)	Maximum RMS fitting error (%)	Standard Deviation
1	16.8	30.1	4.3
2	10.5	22.5	3.5
3	8.5	21.5	4.1
4	3.99	9.75	1.4
5	2.85	6.75	1.15
6	1.56	3.6	0.6
7	1.16	2.8	0.45

Other sources of error include the quantization error. Quantization error results from the inability to represent analog parameters in a quantized digital format [142]. Quantization error is at most one least significant bit (LSB) if the mantissa is chopped and is at most one-half of an LSB if the mantissa is rounded [142]. Numerical Error results from the use of a computer. A computer uses finite precision to perform operations on floating-point values. The amount of error associated with numerical error is at most one LSB [142]. Since the calculations used in the analysis used double-precision, the error is 2^{-64}, or approximately $5.42*10^{-20}$. Since the error from both the quantization error and the numerical error are several orders of magnitude less than the manufacturer modeling error, the manufacturer modeling error will dominate the three error sources.

Circuit modeling error, E_{CM}, represents the error incurred by the SPICE netlist used to model an integrated circuit during simulation. Circuit modeling error derives from several sources. One source is the non-idealities that occur in a physical circuit. The

netlist can only imitate actual circuit performance to the extent that the inherent imperfections in the circuit are included. If parasitic extraction is performed on a circuit layout, the SPICE netlist can include many of the circuit non-idealities. This work does not include layout parasitics, such as line–to-substrate capacitance, line-to-line coupling capacitance, trace resistance, and inherent inductance. Other factors also contribute to the accuracy of the circuit model. These include the step size during a transient simulation, the accuracy of the single event model, and the simulation settings on numerical accuracy (simulation tool numerical error).

The Monte-Carlo sampling error, E_S, derives from the use of Monte Carlo simulations to represent the overall behavior of transistors over the entire range of parameter variations. In essence, the simulations are samples taken of a larger population and are, as such, subject to sampling error [143]. The sample sizes, in the analysis, are the number of samples in each parameter segment. Since the number of samples in each segment varies with the parameter values, the smallest number of samples will be selected as the measure of error in order to show the maximum error. The root-mean-square (RMS) error between the sample mean and the population mean is $1/\sqrt{n}$ where n is the number of samples [143]. Equation (1) describes the Monte-Carlo sampling error.

$$E_S = \sqrt{\frac{(E_{TM}^2 + E_{CM}^2)}{n}} \quad (1)$$

Since the total RMS error, E_{TOTAL}, is equal to the square root of the sum of the squares of the contributing error source, the total amount of error arising from the parameter analysis can be calculated [144]. Equations (2) and (3) describe the total error.

$$E_{TOTAL} = \sqrt{E_{TM}^2 + E_{CM}^2 + E_S^2} \quad (2)$$

$$E_{TOTAL} = \sqrt{(E_{TM}^2 + E_{CM}^2)\left(\frac{n+1}{n}\right)} \quad (3)$$

Given numerical error component values, the total error can be obtained. A numerical approximate of the total error can be assessed if the values provided by Asenov, et al., are used for the manufacturer modeling error, if the circuit modeling error is estimated at half of the manufacturer modeling error, and if the smallest number of samples per segment for the simulation data presented in this document, four, is used for n (since the smallest number of samples would represents the largest sampling error). Table X shows the estimate. If four parameters were used to develop the BSIM4 models used in the parameter analysis, the total RMS error is less than 5%.

TABLE X.
PARAMETER ANALYSIS ERROR QUANTIFICATION

Number of Parameters [138]	Average Modeling RMS Error (%) [138]	Circuit Modeling RMS Error (%)	Sampling RMS Error (%)	Total RMS error (%)
1	16.8	8.4	9.39	21
2	10.5	5.25	5.87	13.125
3	8.5	4.25	4.75	10.625
4	3.99	1.995	2.23	4.9875
5	2.85	1.425	1.59	3.5625
6	1.56	0.78	0.87	1.95
7	1.16	0.58	0.65	1.45

CHAPTER VII

CONCLUSIONS

Thorough comprehension of the impact of process variations on the single event upset response of integrated circuits is required for full understanding of SEU response. The anticipated increase in the effect of process variations with decreasing device size along with the expected escalation in the influence of single events on circuit performance makes the analysis of their interaction vital. An approach to study and quantify the effect of process variations on the SEU response has been demonstrated. The impact of process variations on the SEU response of sub-100 nm memory cells has been presented and discussed.

The analysis exploits the manufacturer-provided description of process variation included in the process design kit for each technology. Monte Carlo simulations are conducted and specific information is extracted. The extracted information allows the SRAM upset response to be correlated to specific transistor parameter shifts while maintaining the required integrity of transistor parameter relationships. The quantification of the relationship between varying transistor parameters and the likelihood of single event upset provides the circuit designer with both trending and numerical information about the sensitivity of his circuit design. If a designer is able to determine that process variations may decrease the critical charge of his circuit below

acceptable levels, he may employ hardening techniques to counter the impact of process variations.

Interdie process variation impact on SRAM single event upset response was examined for 90 nm and 65 nm SRAM cells. The impact of the transistor parameters on upset probability was examined over a range of injected charge values. Several parameters were indicated to have a significant impact on the single event response of the SRAM cells. These include the oxide thickness (TOXE), the channel width (XW) and length (XL) variations, and the threshold voltage (VTHO). For instance, the range of threshold voltage values corresponds to a peak-to-peak swing in the possible upset probabilities of 73.9% around the upset probability value that corresponds to the nominal threshold voltage value. A survey of the intradie process variation impact on the SEU response for a 65 nm 6T SRAM cell was also conducted. The channel width variation and threshold voltage were shown to have the greatest impact on SEU response. Knowledge of the most impactful parameters provides a circuit designer with beneficial information that can be used to harden sensitive nodes.

The impact of process variations, via their impact on transistor parameters, on the SEU response of flip-flops was analyzed for 65 nm and 45 nm D-flip-flops. The analysis, which included the effect of charge-sharing, indicated that the same set of parameters, TOXE, VTHO, XL, and XW, have significant impact on the SEU response. Also, the impact of process variation increased with the decrease in device size.

Experimental tests were conducted in order to verify the impact of parameter variation on upset response. A shift in threshold voltage was imposed using negative bias

temperature instability. Three flip-flops designs, a DICE flip-flop and two D flip-flops, fabricated in a 40 nm bulk CMOS process were subjected to heavy–ions before and after temperature and voltage stressing. The data showed that the sensitivity of all three flip-flop designs increased with the NBTI-induced change in threshold voltage.

In advanced technologies, the upset response of circuits can change with increasing LET. While the previously summarized research studied the effect of process variations on the onset of SEU, the analysis of SEU upset response continued by studying upset reversal, a mechanism that effectively reverses single event upset given sufficient injected charge. Upset reversal, which showed sensitivity to VTHO, TOXE, XL, and XW, may serve as a mitigation technique in advanced technologies since it exploits their inherent sensitivity to charge sharing.

As technologies progress, the impact of process variations is anticipated to grown more severe. Additionally, charge sharing is expected to increase in effect with decreasing device size. Combined with the intensified effect of single events in advanced technologies, the single event upset response of circuits may grow more severe and complex. Multiple upset onset and reversal charge thresholds may exist. Analysis, which to this point has typically examined the critical charge threshold, will need to be performed to determine the impact of process and parameter variation on each of the charge thresholds. Also, the conducted investigation was limited to sub-100 nm memory cells. Similar investigations should analyze the effect of process variations on combinational logic. As circuit speed increases, SEU occurring in combinational logic will increase in importance to chip performance.

The exploration of the relationship between single event upset response and process-induced transistor parameter variations is vital to the full understanding of integrated circuit single event sensitivity. A method for the quantification of those relationships has been presented and applied to memory cells targeted to 90 nm, 65 nm, and 45 nm. The results show that parameter variation has a significant impact on SEU response and that the impact is likely to increase with technology advancements. The investigation of the effect of process variations on single event upset response of sub-100 nm memory cells provides key insight into the complex field of radiation response.

REFERENCES

[1] E. E. Conrad, “Radiation Effects Research in the 60’s,” IEEE Transactions on Nuclear Science, vol. 41 (6), pp. 2648-2659, December 1994.

[2] W. G. Magnuson, “Circuit Analysis and Simulation Programs – An Overview,” IEEE Transactions on Nuclear Science, vol. 29 (1), pp. 567-572, February 1982.

[3] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, J. A. Felix, “Current and Future Challenges in Radiation Effects on CMOS Electronics,” IEEE Transactions on Nuclear Science, vol. 57, no. 4, August 2010.

[4] A. Asenov, S. Kaya, A. R. Brown, “Intrinsic parameter fluctuations in decananometer MOSFETS introduced by gate line edge roughness,” IEEE Transactions on Electron Devices, vol. 50, no. 5, pp. 1254-1260, May, 2003.

[5] P. A. Stolk, F. P. Widdershoven, D. B. M. Klaasen, “Modeling Statistical Dopant Fluctuations in MOS Transistors,” IEEE Transactions on Electron Devices, vol. 45, no. 9, pp. 1960-1971, Sept. 1998.

[6] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, V. De, “Parameter variations and impact on circuits and microarchitecture,” Proceedings of the 2003 Design Automation Conference, pp.338-342, 2003.

[7] K. J. Kuhn, “Process Technology Variation,” IEEE Transactions on Electron Devices, vol. 58 (8), pp. 2197-2208, August, 2011.

[8] Y. Wang, U. Bhattacharya, F. Hamzaoglu, P. Kolar, Y-G. Ng, L. Wei, Y. Zhang, K. Zhang, M. Bohr, “A 4.0 GHz 291 Mb Voltage-Scalable SRAM Design in a 32nm High-k + Metal-Gate CMOS Technology with Integrated Power Management,” IEEE Journal of Solid-State Circuits, vol. 45 (1), January 2010.

[9] J. M. Steigerwald, “Chemical mechanical polish: The enabling technology,” IEEE 2008 International Electron Devices Meeting Technical Digest, pp. 37-40, December 2008.

[10] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, M. Hirose, “Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current,” IEEE Transactions on Electron Devices, vol. 48 (2), pp. 259-264, February 2001.

[11] K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra, A. Nishida, S. Kamohara, T. Hiramoto, “Understanding Random Threshold Voltage Fluctuation by Comparing Multiple Fabs and Technologies,” IEEE 2007 International Electron Devices Meeting Technical Digest, pp. 467-470, December 2007.

[12] A. Asenov, “Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 µm MOSFET’s: A 3-D ‘Atomistic’ Simulation Study,” IEEE Transaction on Electron Devices, vol. 45(12), pp. 2505-2513, December 1998.

[13] I. Ahsa, N. Zamdmer, O. Glushchenkov, R. Logan, E. J. Nowak, H. Kimura, J. Zimmerman, G. Berg, J. Herman, E. Maciejewski, A. Chan, A. Azuma, S. Deshpande, B. Diraoui, G. Freeman, A. Gabor, M. Bribelyuk, S. Huang, M. Kumar, K. Miyamoto, D. Mocuta, A. Mahorowala, E. Leobandung, H. Utomo, B. Walsh, “RTA-Driven Intra-Die Variations in Stage Delay, and Parametric Sensitivities for 65 nm Technology”, 2006 Symposium on VLSI Technology Digest of Technical Papers, pp. 170-171, June 2006.

[14] T. Tanaka, T. Usuki, T. Futatsugi, Y. Momiyama, T. Sugii, “Vth Fluctuation Induced by Statistical Variation of Pocket Dopant Profile,” 2000 International Electon Devices Meeting Technical Digest, pp. 271-274, December 2000.

[15] D. M. Fleetwood, M. P. Rodgers, L. Tsetseris, X. J. Zhou, I. Batyrev, S. Wang, R. D. Scrimpf, S. T. Pantelides, “Effects of Device Aging on Microelectronics Radiation Response and Reliability,” 2006 25th International Conference on Microelectronics, pp. 84-91, May 2006.

[16] C. Schlunder, W. Heinrigs, W. Gustin, H. Reisinger, “On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs,” 2006 IEEE International Integrated Reliability Workshop Final Report, pp. 1-4, 2006.

[17] J. G. Massey, “NBTI: What We Know and What We Need to Know – A Tutorial Addressing the Current Understanding and Challenges for the Future,” 2004 IEEE International Integrated Reliability Workshop Final Report, pp. 199-211, 2004.

[18] A. T. Krishnan, V. Reddy, S. Chakravarthi, J. Rodriquez, S. John, S. Krishnan, “NBTI Impact on Transistor & Circuit: Models, Mechanisms & Scaling Effects,” IEEE International Electron Devices Meeting 2003, pp. 14.5.1-14.5.4, 2003.

[19] A. H. Johnston, “Radiation Effects in Advanced Microelectronics Technologies,” IEEE Transactions on Nuclear Science, vol. 45, no. 3, pp. 1339-1354, June 1998.

[20] X. Tang, V. K. De, and J. D Meindl, “Intrinsic MOSFET Parameter Fluctuations Due to Random Dopant Placement,” IEEE Transactions on VLSI Systems, vol. 4, 1997.

[21] V. K. De, X. Tang, and J. D. Meindl, “Random MOSFET Parameter fluctuation limits to gigascale integration (GSI),” Symposium on VLSI Technology, 1996 Digest of Technical Papers, pp. 198-199, 1996.

[22] A. A. Mutlu, N. G. Gunther, and M. Rahman, “Concurrent Optimization of Process Dependent Variations on Difference Circuit Performance Measures,” Proceedings of the 2003 International Symposium on Circuits and Systems, vol. 4, pp. 692-695, 2003.

[23] P. Cox, P. Yang, S. S. Mahant-Shetti, P. Chatterjee, “Statistical Modeling for Efficient Parametric Yield Estimation of MOS VLSI Circuits,” IEEE Transactions on Electron Devices, vol. 32, No. 2, pp. 471-478, 1985.

[24] A. A. Mutlu, M. Rahman, “Statistical Methods for the Estimation of Process Variation Effects on Circuit Operation,” IEEE Transactions on Electronics Packaging Manufacturing, vol. 28, no. 4, pp. 364-375, October 2005.

[25] O. S. Unsal, J. W. Tschanz, K. Bowman, V. De, X. Vera, A. Gonzalex, O. Ergin, “Impact of Parameter Variations on Circuits and Microarchitecture,” IEEE Micro, vol. 26, no. 6, pp. 30-39, 2006.

[26] S. G. Duvall, “Statistical Circuit Modeling and Optimization,” 2000 5th International Workshop on Statistical Metrology, pp. 56-63, 2000.

[27] R. C. Baumann, “Radiation-Induced Soft Errors in Advanced Semiconductor Technologies,” IEEE Transactions on Device and Materials Reliability, vol. 5, no. 3, September 2005.

[28] G. E. Moore, “Cramming more components onto integrated circuits,” Electronics, vol. 38 (8), April 1965.

[29] P. Bondyopadhyay, “Moore’s Law Governs the Silicon Revolution,” Proceedings of the IEEE, vol. 86 (1), pp. 78-81, January 1998.

[30] ITRS, “International Technology Roadmap for Semiconductors 2010 Update Overview,” 2010 [Online]. Available: http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/2010_Update_Overview.pdf.

[31] W. Maly, “Computer-Aided Design for VLSI Circuit Manufacturability,” Proceedings of the IEEE, vol. 78 (2), pp. 356-392, February 1990.

[32] BSIM4 MOSFET Users Manual [Online]. Available: https://www.device.eecs.berkeley.edu/~bsim3/bsim4.html.

[33] N. D. Arora, E. Rios, Cheng-Liang Huag, “Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance,” IEEE Transactions on Electron Devices, vol. 42, no. 5, pp. 935-943, May 1995.

[34] P. Habas, J. V. Faricelli, “Investigation of the Physical Modeling of the Gate-Depletion Effect,” IEEE Transaction on Electron Devices, vol. 39 (6), pp. 1496-1500, June 1992.

[35] C-L. Huang, N. D. Arora, “Measurements and Modeling of MOSFET I-V Characteristics with Polysilicon Depletion Effect,” IEEE Transactions on Electron Devices, vol. 40 (12), pp. 2330-2337, December 1993

[36] W. Shockley, “Problems Related to p-n Junctions in Silicon,” Solid-State Electronics, vol. 2 (1), pp. 35-60, January 1960.

[37] B. Hoenseisen, C. A. Mead, “Fundamental Limitations in Microelectronics – I. MOS Technology,” Solid-State Electronics, vol. 15 (7), pp. 819-829, July 1972.

[38] J.Shyu, G. C. Temes, F. Krummenacher, “Random error effects in matched MOS capacitors and current sources,” IEEE Journal of Solid-State Circuits, vol. 19, no. 6, pp. 948-956, Dec. 1984.

[39] S. Borkar, “Designing Reliable Systems from Unreliable Components: The Challenges of Transistor Variability and Degradation,” IEEE Micro, vol. 25, no. 6, pp. 10-16, Nov.-Dec., 2005.

[40] X. Tang, V. K. De, and J. D. Meindle, “Effects of random MOSFET parameter fluctuations on total power consumption,” International Symposium on Low Power Electronics and Design, pp. 233-236, 1996.

[41] T. Mizuno, J. Okamura, A. Toriumi, “Experimental Study of Threshold Voltage Fluctuations Using an 8k MOSFET’s Array,” 1993 Symposium on VLSI Technology Digest of Technical Papers, pp. 41-42, 1993.

[42] T.Mizuno, M. Iwase, H. Niiyama, T. Shibata, K. Fujisaki, T. Nakasugi, A. Toriumi, and Y. Ushiku, “Performance Fluctuations of 0.10µm ULSIs,” 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 13-14, 1994.

[43] K. Nichinohara, N. Shigyo, T. Wada, “Effect on Microscopic Fluctuations in Dopant Distributions on MOSFET Threshold Voltage,” IEEE Transactions on Electron Devices, vol. 39, no. 3, pp. 634-639, March 1992.

[44] R. W. Keyes, “Physical Limits in Digital Electronics,” Proceedings of the IEEE, vol. 63, no. 5, pp. 740-767, May, 1975.

[45] T. Hagiwara, K. Yamaguchi, S. Asai, “Threshold Voltage Deviation in Very Small MOS Transistors Due to Local Impurity Fluctuations,” 1982 Symposium on VLSI Technology Digest of Technical Papers, pp. 46-47, 1982.

[46] D. Burnett, K. Erington, C. Subramanian, K. Baker, “Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits,” 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 15-16, 1994.

[47] P. Andrei, “Automated design of random dopant fluctuation resistant MOSFETs,” 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, pp. 404-407, 2008.

[48] V. Varadarajan, L. Smith, T-J. King Liu, “FinFET Design for Tolerance to Statistical Dopant Fluctuations,” IEEE Transactions on Nanotechnology, vol. 8 (3), pp. 375-378, May 2009.

[49] P. Andrei and L. Oniciuc, “Suppressing random dopant-induced fluctuations of threshold voltages in semiconductor devices,” Journal of Applied Physics, vol. 104 (10), pp. 104508 – 10458-10, 2008.

[50] K. A. Bownan, S. G. Duvall, J. D. Meindle, “Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution for Gigascale Interaction,” IEEE Journal of Solid-State Circuits, vol. 37, no. 2, pp. 183-190, Feb. 2002.

[51] M. Eisele, J. Berthold, D. Schmitt-Landsiedel, R. Mahnkopf, “The Impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 5, no. 4, pp. 360-368, Dec. 1997.

[52] ITRS, “The 2009 International Technology Roadmap for Semiconductors,” 2009 [Online]. Available: http://www.itrs.net/Links/2009ITRS/Home2009.htm

[53] ITRS, “The 2001 International Technology Roadmap for Semiconductors,” 2001 [Online]. Available: http://www.itrs.net/Links/2001ITRS/Home.htm

[54] ITRS, “The 2003 International Technology Roadmap for Semiconductors,” 2003 [Online]. Available: http://www.itrs.net/Links/2003ITRS/Home2003.htm

[55] Johnson, Colin R. “IBM Warns of Design Rule Explosion Beyond 22-nm”, EE *Times*, March 2010. http://www.eetimes.com/electronics-news/4088244/IBM-warns-of-design-rule-explosion-beyond-22-nm

[56] Goering, Richard. “Hope seen for taming IC process variability at next design node,” EE *Times*, April 2006.

[57] L. W. Massengill, “SEU modeling and prediction techniques,” in *IEEE Nuclear Space Radiation Effects Conf. Short Course Text*, 1993.

[58] P. E. Dodd, L. W. Massengill, “Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics,” IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 583-602, June 2003.

[59] D. R. Alexander, “Transient Ionizing Radiation Effects in Devices and Circuits,” IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 565-582, June, 2003.

[60] E. W. Enlow, D. R. Alexander, “Photocurrent Modeling of Modern Microcircuit PN Junction,” IEEE Transactions on Nuclear Science, vol. 35 (6), pp. 1467-1474 , December 1988.

[61] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, T. Turflinger, P. E. Dodd, G. Vizkelethyd, “Heavy Ion-Induced Digital Single-Event Transients in Deep Submicron Processes,” IEEE Transactions on Nuclear Science, vol. 51(6), pp. 3480-3485, December 2004.

[62] J. T. Wallmark and S. M. Marcus, “Minimum Size and Maximum Packing Density of Nonredundant Semiconductor Devices,” Proceedings of the IRE, vol. 50, no. 3, pp. 286-298, March 1962.

[63] D. Binder, E. C. Smith, and A. B. Holman, “Satellite Anomalies from Galactic Cosmic Rays,” IEEE Transactions on Nuclear Science, vol. 22, no. 6, pp. 2675-2680, December 1975.

[64] T. C. May and M. H. Woods, “A New Physical Mechanism for Soft Errors in Dynamic Memories, “ Proceedings of 1978 IEEE International Reliability Physics Symposium, pp.33-40, April 1978.

[65] T. C. May and M. H. Woods, “Alpha-Particle-Induced Soft Errors in Dynamic Memories,” IEEE Transactions on Electron Devices, vol. 26, 1979.

[66] J. C. Pickel and J. T. Blandford, Jr., “Cosmic Ray Induced Errors in MOS Memory Cells,” IEEE Transactions on Nuclear Science, vol. 25, no. 6, pp. 1166-1171, 1978.

[67] D. S. Yaney, J. T. Nelson, and L. L. Vanskiki, “Alpha-Particle Tracks in Silicon and their Effect on Dynamic MOS RAM Reliability,” IEEE Transactions on Electron Devices, vol, 26, no. 1, pp. 10-16, 1979.

[68] C. S. Guenzer, E. A. Wolicki, and R. G. Allas, “Single Event Upset of Dynamic RAMS by Neutrons and Protons,” IEEE Transactions on Nuclear Science, vol. 26, pp. 5048-5052, 1979.

[69] R. C. Wyatt, P. J. McNulty, P. Toumbas, P. L. Rothwell, and R. C. Filz, “Soft Errors Induced by Energetic Protons,” IEEE Transactions on Nuclear Science, vol. 26, pp. 4905-4910, 1979.

[70] W. A. Kolasinski, J. B. Blake, J. K Anthony, W. E. Price, and E. C. Smith, “Simulation of Cosmic-Ray Induced Soft Errors and Latchup in Integrated-Circuit Computer Memories,” IEEE Transactions on Nuclear Science, vol. 26, pp. 5087-5091, 1979.

[71] J. R. Srour, “Radiation Effects R & D in the 1970s: A Retrospective View,” IEEE Transactions on Nuclear Science, vol. 41, no. 6, pp. 2660-2665, December 1994.

[72] C. Slayman, “Soft Errors-Past History and Recent Discoveries,” IEEE 2010 International Integrated Reliability Workshop Final Report, pp. 25-30, 2010.

[73] J. F. Ziegler, H. W. Curtis, H. P. Muhlfeld, C. J. Montrose, B. Chin, M. Nicewicz, C. A. Russell, W. Y. Wang, L. B. Freeman, P. Hosier, L. E. LaFave, J. L. Walsh, J. M. Orro, G. J. Unger, J. M. Ross, T. J. O’Gorman, B. Messina, T. D. Sullivan, A. J. Sykes, H. Yourke, T. A. Enger, V. Tolat, T. S. Scott, A. H. Taber, R. J. Sussman, W. A. Klein, C. W. Wahaus, “IBM Experiments in Soft Fails in Computer Electronics (1978-1994),” IBM Journal of Research and Development, vol. 40 (1), pp. 3-18, January 1996.

[74] T. C. May, “Soft Errors in VLSI: Present and Future,” IEEE Transactions on Components, Hybrid, and Manufacturing Technology, vol. 2 (4), pp. 377-387, December 1979.

[75] C. Lage, D. Burnett, T. McNelly, K. Baker, A. Bormann, D. Dreier, V. Soorholtz, “Soft Error Rate and Stored Charge Requirement in Advanced High-Density SRAMs,” 1993 International Electron Devices Meeting Technical Digest, pp. 821-824, 1993.

[76] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, G. L. Hash, “Neutron-Induced Latchup in SRAMs at Ground Level,” Proceedings of the 2003 IEEE International Reliability Physics Symposium, pp. 51-55, 2003.

[77] P. D. Bradley, E. Normand, “Single Event Upsets in Implantable Cardioverter Defibrillators,” IEEE Transactions on Nuclear Science, vol. 45 (6), pp. 2929-2940, December 1998.

[78] D. Lyons, “Sun Screen,” Forbes Magazine, November 13, 2000. [Online], Available: http://www.forbes.com/forbes/2000/1113/6613068a.html.

[79] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, G. L. Hash, “Neutron-Induced Soft Errors, Latchup, and Comparison of SET Test Methods for SRAM Technologies,” Digest of the 2002 International Electron Devices Meeting, pp. 333-336, 2002.

[80] N. Cohen, T. S. Sriram, M. Leland, D. Moyer, S. Butler, R. Flatley, “Soft Error Considerations for Deep-Submicron CMOS Circuit Applications,” 1999 International Electron Devices Meeting Technical Digest, pp. 315-318, 1999.

[81] R. C. Baumann, E. B. Smith, “Neutron-Induced Boron Fission as a Major Source of Soft Errors in Deep Submicron SRAM Devices,” 2000 IEEE International Reliability Physics Symposium Proceedings, pp. 1520157, 2000.

[82] International Technology Roadmap for Semiconductors 2009 Edition. [Online]. http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_Design.pdf.

[83] R. Ronen, A. Mendelson, K. Lai, S.-L. Lu, F. Pollack, J. P. Shen, “Coming Challenges in Microarchitecture and Architecture,” Proceedings of the IEEE, vol. 89 (3), pp. 325-340, March 2001.

[84] R. Baumann, “Soft errors in advanced computer systems,” IEEE Design and Test of Computers, vol. 22 (3), pp. 258-266, May-June, 2005.

[85] O. A. Amusan, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, J. D. Black, M. P. Baze, L. W. Massengill, “Single Event Upsets in a 130nm Hardened Latch Design Due to Charge Sharing,” Proceedings of the 45th Annual IEEE International Reliability Physics Symposium, pp. 306-311, 2007.

[86] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, R. D. Schrimpf, “Charge Collection and Charge Sharing in a 130nm CMOS Technology,” IEEE Transactions on Nuclear Science, vol. 53, no. 6, pp. 3253-3258, December 2006.

[87] O. A. Amusan, L. W. Massengill, M. P. Baze, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, J. D. Black, "Single Event Upsets in Deep-Submicrometer Technologies Due to Charge Sharing," IEEE Transactions on Device and Materials Reliability, Vol. 8, No. 3, pp. 582-589, September 2008.

[88] O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, J. R. Ahlbin, R. A. Reed, M. W. McCurdy, "Mitigation Techniques for Single Event Induced Charge Sharing in a 90 nm Bulk CMOS Process," Proceedings of the 2008 IEEE International Reliability Physics Symposium, pp. 468-472, 2008.

[89] T. D. Loveless, S. Jagannathan, T. Reece, J. Chetia, B. L. Bhuva, M. W. McCurdy, L. W. Massengill, S.-J. Wen, R. Wong, D. Rennie, "Neutron- and Proton-Induced Single Event Upsets for D- and DICE-Flip/Flop Designs at a 40nm Technology Node," IEEE Transactions on Nuclear Science, vol. 58, no. 3, pp. 1008-1014, June 2011.

[90] A. M. Francis, D. Dimitrov, J. Kauppila, A. Sternberg, M. Alles, J. Holmes, H. A. Mantooth, "Significance of Strike Model in Circuit-Level Prediction of Charge Sharing Upsets," IEEE Transactions on Nuclear Science, vol. 56 (6), pp. 3109-3114, December 2009.

[91] J. R. Ahlbin, M. J. Gadlage, D. R. Ball, A. W. Witulsi, B. L. Bhuva, R. A. Reed, G. Vizkelethy, L. W. Massengill, "The Effect of Layout Topology on Single-Event Transient Pulse Quenching in a 65 nm Bulk CMOS Pocess," IEEE Transactions on Nuclear Science, vol. 57 (6), pp. 3380-3385, Dec., 2010.

[92] J. R. Ahlbin, L. W. Massengill, B. L. Bhuva, B. Narasimham, M. J. Gadlage, P. H. Eaton, "Single-Event Transient Pulse Quenching in Advanced CMOS Logic Circuits, IEEE Transactions on Nuclear Science, vol. 56 (6), pp. 3050-3056, December 2009.

[93] R. K. Lawrence and A. T. Kelly, "Single Event Effect Induced Multiple-Cell Upsets in a Commercial 90 nm CMOS Digital Technology," IEEE Transactions on Nuclear Science, vol. 55 (6), pp. 3367-3374, December 2008.

[94] J. D. Black, D. R. Ball, W. H. Robinson, D. M. Fleetwood, R. D. Schrimpf, R. A. Reed, D. A. Black, K. M. Warren, A. D. Tipton, P. E. Dodd, N. F. Haddad, m. A. Zapsos, H. S. Kim, M. Friendlich, "Characterizing SRAM Single Event Upset in Terms of Single and Multiple Node Charge Collection," IEEE Transactions on Nuclear Science, vol. 55 (6), pp. 2943-2947, December 2008.

[95] T. D. Loveless, M. L. Alles, D. R. Ball, K. M. Warren, L. W. Massengill, "Parametric Variability Affecting 45 nm SOI SRAM Single Event Upset Cross-Sections," IEEE Transactions on Nuclear Science, vol. 57 (6), pp. 3228-3233, December 2010.

[96] A. V. Kauppila, B. L. Bhuva, J. S. Kauppila, L. W. Massengill, W. T. Holman, "Impact of Process Variations on SRAM Single Event Upsets," IEEE Transactions on Nuclear Science, vol. 58 (3), pp. 834-839, June 2011.

[97] H. K. Peng, C. H. P. Wen, J. Bhadra, “On soft error rate analysis of scaled CMOS designs – a statistical perspective,” IEEE/ACM International Conference on Computer-Aided Design – Digest of Technical Papers, pp. 157-163, 2009.

[98] A. Balasubramanian, P. R. Fleming, B. L. Bhuva, O. A. Amusan, L. W. Massengill, “Effects of Random Dopant Fluctuations (RDF) on the single event vulnerability of 90 and 65 nm CMOS Technologies,” IEEE Transactions on Nuclear Science, vol. 54 (6), pp. 2400-2406, Dec. 2007.

[99] A. Balasubramanian, P. R. Fleming, B. L. Bhuva, A. L. Sternberg, L. W. Massengill, “Implications of Dopant-Fluctuation-Induced V_t variations on the Radiation Hardness of Submicrometer CMOS SRAMs,” IEEE Transactions on Device and Materials Reliability, vol. 8, no. 1, pp. 135-144, March 2008.

[100] A. V. Kauppila, B. L. Bhuva, L. W. Massengill, W. T. Holman, D. R. Ball, “Impact of Process Variations on Charge-Sharing Induced Upset Reversal in a 65 nm Flip-Flop,” 2011 RADECS Conference Proceedings, 2011.

[101] S. E. Armstrong, B. D. Olson, W. T. Holman, J. Warner, D. McMorrow, L. W. Massengill, “Demonstration of a Differential Layout Solution for Improved ASET Tolerance in CMOS A/MS Circuits,” IEEE Transactions on Nuclear Science, vol. 57 (6), pp. 3615-3519, December 2010.

[102] A. T. Kelly, P. R. Fleming, W. T. Holman, A. F. Witulski, B. L. Bhuva, L. W. Massengill, “Differential Analog Layout for Improved ASET Tolerance,” IEEE Transactions on Nuclear Science, vol. 54 (6), pp. 2053-2059, December 2007.

[103] L. W. Massengill, M. L. Alles, S. E. Kerns, K. L. Jones, “Effects of Process Parameter Distributions and Ion Strike Locations on SEU Cross-Section Data,” IEEE Transactions on Nuclear Science, vol. 40, no. 6, pp. 1804-1811, December 1993.

[104] E. L. Petersen, J. C. Pickel, J. H. Adams, Jr., E. C. Smith, “Rate Prediction for Single Event Effects – a Critique,” IEEE Transactions on Nuclear Science, vol. 39, no. 6, pp. 1577-1599, December 1992.

[105] L.W. Massengill, D.V. Kems, S.E. Kems, and M.L.Alles, "Single-Event Charge Enhancement in SO1 Devices," IEEE Electron Device Letters, vol. EDL-11, no. 2, pp. 98-99 (1990).

[106] S.E. Kerns, L.W. Massengill, D.V. Kems, Jr., M.L. Alles, T.W. Houston, H. Lu, L.R. Hite, "Model for CMOS/SOI Single-Event Vulnerability," IEEE *Trans. on Nuclear Science,* vol. NS-36, no. 6, pp. 2305-2310 (1989).

[107] J.C. Pickel and E.L. Petersen, "Rate Prediction for Single Event Effects -- A Critique," presented at the 1992 Nuclear and Space Radiation Effects Conference, New Orleans, LA, July, 1992.

[108] L.W. Massengill, M.L. Alles, and S.E. Kerns, "SEU Characterization of Modem, Hardened Technologies," presented at the 1992 SEU Symposium, Los Angeles, CA, April, 1992.

[109] R A. Kohler, R. Koga, “SEU characterization of hardened CMOS SRAMs using statistical analysis of feedback delay in memory cells,” IEEE Transactions on Nuclear Science, vol.36 (6), pp. 2318-2323, December 1989.

[110] P. S. Winokur, F. W. Sexton, D. M. Fleetwood, M. D. Terry, M. R. Shaneyfelt, P. V. Dressendorfer, J. R. Schwank, “Implementing QML For Radiation Hardness Assurance,” IEEE Transactions on Nuclear Science, vol. 37 (6), pp. 1794-1805, December 1990.

[111] P. E. Dodd, “Device Simulation of Charge Collection and Single-Event Upset,” IEEE Transactions on Nuclear Science, vol. 43 (2), pp. 561-575, April 1996.

[112] J. S. Kauppila, A. L. Sternberg, M. L. Alles, A. M. Francis, J. Holmes, O. A. Amusan, L. W. Massengill, “A bias dependent single-event compact model implemented into BSIM4 and a 90 nm CMOS process design kit,” IEEE Transactions on Nuclear Science, vol. 56, no. 1, pp. 3152-3157, Dec. 2009.

[113] T. Calin, M. Nicolaidis, R. Velazco, “Upset hardened memory design for submicron CMOS technology,” IEEE Transactions on Nuclear Science, vol. 43 (6), pp. 2874-2878, December 1996.

[114] [Commercially Available CMOS 65 nm Process] Model Reference Guide, July 2008.

[115] S. M. Jahinuzzaman, M. Sharifkhani, and M. Sachdev, “An Analytical Model for Soft Error Critical Charge of Nanometric SRAMs,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 17 (9), pp. 1187-1195, September 2009.

[116] M. Bagatin, S. Gerardin, A. Paccagnella, and F. Faccio, “Impact of NBTI Aging on the Single-Event Upset of SRAM Cells,” IEEE Transactions on Nuclear Science, vol 57, no. 6, pp. 3245-3250, December, 2010.

[117] C. Schlunder, “Device reliability challenges for modern semiconductor circuit design – A review,” Advances in Radio Science, pp. 201-211, 2009.

[118] D. K. Schroder, J. A. Babcock, “Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing,” Journal of Applied Physics, vol. 94(1), pp. 1-18, July 2003.

[119] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, S. T. Pantelides, “Hydrogen-Related Instabilities in MOS Devices Under Bias Temperature Stress,” IEEE Transactions on Device and Materials Reliability, vol. 7 (4), pp. 502-508, December 2007.

[120] C. Schlunder, R. Brederlow, B. Ankele, W. Gustin, K. Goser, R. Thewes, "Effects on inhomogeneous negative bias temperature stress on p-channel MOSFETs of analog and RF circuits," Microelectronics Reliability, vol. 45 (1), pp. 39-46, January 2005.

[121] C. Schlunder, R. Brederlow, P. Wieczorek, C. Dahl, J. Holz, M. Rohner, S. Kessel, V. Herold, K. Goser, W. Weber, R. Thewes, "Trapping mechanisms in negative bias temperature stressed p-MOSFETs," Microelectronics Reliability, vol. 39 (6-7), pp. 821-826, June-July 1999.

[122] R. D. Scrimpf, K. M. Warren, R. A. Weller, R. A. Reed, L. W. Massengill, M. L. Alles, D. M. Fleetwood, X. J. Zhou, L. Tsetseris, S. T. Pantelides, "Reliability and Radiation Effects in IC Technologies," 2008 International Reliability Physics Symposium Proceedings, pp. 97-106, 2008.

[123] S. R. Pantelides, L. Tsetseris, M. J. Beck, S. N. Rashkeev, G. Hadjisavvas, I. G. Batyrev, B. R. Tuttle, A. G. Marinopoulos, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, "Performance, Reliability, Radiation Effects, and Aging Issues in Microelectronics – From Atomic-Scale Physics to Engineering-Level Modeling," Proceedings of the European Solid State Device Research Conference 2009, pp. 76-83, 2009.

[124] B. E. Deal, M. Sklar, A. S. Grove, E. H. Snow, "Characteristics of the Surface-State Charge (QSS) of Thermally Oxidized Silicon," Journal of the Electrochemical Society: Solid State Science, pp. 266-274, March 1967.

[125] K. O. Jeppson, C. M. Svensson, "Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices," Journal of Applied Physics, vol. 48 (5), pp. 2004-2014, May 1977.

[126] X. J. Zhou, D. M. Fleetwood, J. A. Felix, E. P. Gusev, C. D'Emic, "Bias-temperature instabilities and radiation effects in MOS devices," IEEE Transactions on Nuclear Science, vol. 52 (6), pp. 2231-2238, December 2005.

[127] K. Zhao, J. H. Stathis, B. P. Linder, E. Cartier, A. Kerber, "PBTI under dynamic stress: From a single defect point of view, " 2011 IEEE International Reliability Physics Symposium, pp. 4A.3.1-4A.3.9, 2011.

[128] D. Rossi, M. Omana, C. Metra, A. Paccagnella, "Impact of Aging Phenomena on Soft Error Susceptibility," 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems, pp. 18-24, 2011.

[129] W. Wang, Z. Wei, S. Yang, Y. Cao, "An Efficient Method to Identify Critical Gates under Circuit Aging," 2007 IEEE/ACM International Conference on Computer-Aided Design, pp. 735-740, 2007.

[130] G. La Rosa, Wee Loon Ng, S. Rauch, R. Wong, J. Sudijono, "Impact of NBTI Induced Statistical Variation to SRAM Cell Stability," 44th Annual IEEE International Reliability Physics Symposium Proceedings, pp. 274-282, 2006.

[131] P. Marshall, M. Carts, S. Currie, R. Reed, B. Randall, K. Fritz, K. Kennedy, M. Berg, R. Krithivasan, C. Siedleck, R. Ladbury, C. Marshall, J. Cressler, Niu Guofu, K. LaBel, B. Gilbert, "Autonomous bit error rate testing at multi-gbit/s rates implemented in a 5AM SiGe circuit for radiation effects self test (CREST)," IEEE Transactions on Nuclear Science, vol. 52 (6), pp. 2446-2454, December 2005.

[132] Lawrence Berkeley National Laboratory 88-inch Cyclotron, 2011 [Online]. Available: http://user88.lbl.gov.

[133] J. S. Kauppila, T. D. Haeffner, D. R. Ball, A. V. Kauppila, T. D. loveless, S. Jagannathan, A. L. Sternberg, B. L. Bhuva, L. W. Massengill, "Circuit-Level Layout-Aware Single-Event Sensitive-Area Analysis of 40-nm Bulk CMOS Flip-Flops Using Compact Modeling," IEEE Transactions on Nuclear Science, vol. 58 (6), pp. 2680-2686, December 2011.

[134] CMOS 10SF (CMS 10SF) Technology Design Manual, February 4, 2009.

[135] A. V. Kauppila, B. L. Bhuva, L. W. Massengill, W. T. Holman, D. R. Ball, "Impact of Process Variations and Charge Sharing on the Single-Event-Upset Response of Flip-Flops," IEEE Transactions on Nuclear Science, vol. 58 (6), pp. 2658-2663, December 2011.

[136] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. D. Scrimpg, J. K. Want, B. Bartz, E. Pitta, M. Buer, "Single-Event Charge Collection and Upset in 40-nm Dual- and Triple-Well Bulk CMOS SRAMs," IEEE Transactions on Nuclear Science, vol. 58 (6), pp. 2761-2767, December 2011.

[137] N. Seifert, V. Ambrose, B. Gill, Q. Shi, R. Allmon, C. Recchia, S. Mukherjee, N. Nassif, J. Krause, J. Pickholtz, A. Balasubramanian, "On the Radiation-Induced Soft Error Performance of Hardened Sequential Elements in Advanced Bulk CMOS Technologies," 2010 IEEE International Reliability Physics Symposium, pp. 188-197, 2010.

[138] N. Seifert, B. Gill, J. A. Pellish, P. W. Marshall, K. A. LaBel, "The Susceptibility of 45 and 32 nm Bulk CMOS Latches to Low-Energy Protons," IEEE Transactions on Nuclear Science, vol. 58 (6), pp. 2711-2718, December 2011.

[139] K. Saki, S. Kawase, J. Shiozawa, A. Yamamoto, and Y. Mikata, "Novel approach for precise control of oxide thickness," 2001 IEEE International Semiconductor Manufacturing Symposium, pp. 451-454, 2001.

[140] C. Zhuo, K. Chopra, D. Sylvester, D. Blaauw, "Process Variation and Temperature-Aware Full Chip Oxide Breakdown Reliability Analysis," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 9, pp. 1321-1334, September 2011.

[141] A. Asenov, B. Cheng, D. Dideban, U. Kovac, N. Moezi, C. Millar, G. Roy, A. R. Brown, S. Roy, "Modeling and simulation of transistor and circuit variability and reliability," 2010 IEEE Custom Integrated Circuits Conference, pp. 1-8, 2010.

[142] R. L. Burden and J. D. Faires, “Mathematical Preliminaries” in *Numerical Analysis*, 7th ed. Pacific Grove, CA: Brooks/Cole, 2001, pp. 1-46.

[143]. H. Stark and J. W. Woods, “Random Vectors and Parameter Estimation” in *Probability and Random Processes with Applications to Signal Processing*, 3rd ed. Upper Saddle River, NJ: Prentice Hall, 2002, pp. 244-303.

[144] G. R. Cooper and C. D. McGillen, “Several Random Variables” in *Probabilistic Methods of Signal and System Analysis*, 3rd ed. New York, NY: Oxford University Press, Inc., 1999, pp. 120-158.