

**IMPACT OF WELL STRUCTURE ON SE RESPONSE IN 90-nm BULK CMOS**

By

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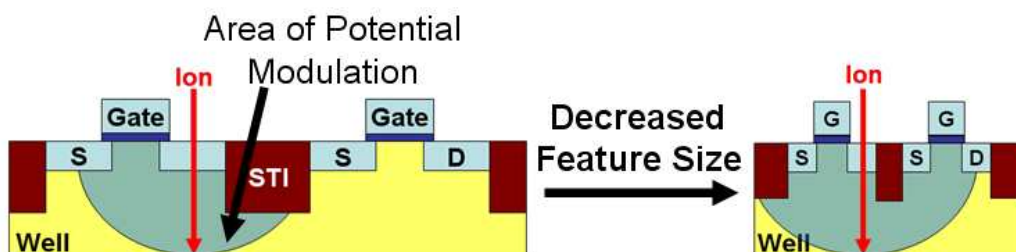
## Chapter I

### INTRODUCTION

#### Section 1.1 Overview

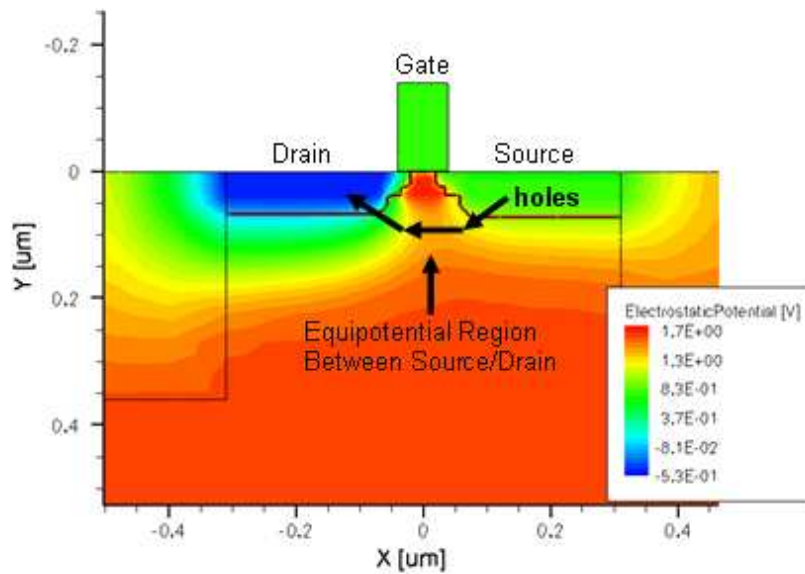
A single event (SE) occurs when an ionizing particle traverses through a silicon volume creating excess charge along its path. Classically, excess charge drifts and diffuses to the source/drain junctions of MOSFETs in proximity to the ion strike location, possibly leading to single event upsets (SEU) in memories and single transients (SET) in combinational logic circuits depending on the amount of charge collected by the MOSFET junctions. This charge collection process can be affected by the MOSFET well engineering and sub-threshold leakage mitigation implants.

The charge deposited by an SE may cause the well potential to modulate in the proximity of the ion strike location, referred to as well potential modulation (WPM) and is illustrated in Fig. 1. This well potential modulation can activate the parasitic bipolar inherent to the MOSFET structure leading to additional charge collection that would not be collected by drift and diffusion processes alone. Decreased feature sizes lead to increased transistor density, WPM can envelope multiple transistors causing parasitic bipolar charge collection at multiple nodes; one mechanism of “charge sharing” among multiple MOSFETs in sub-100nm technology nodes [1].



**Fig. 1. Illustration of well modulation collapse (WPM). A SE can cause the well potential to modulate in the proximity of the ion strike, shown as the shaded round area in the well below the MOSFET. As transistor density increase, WPM collapse can affect multiple devices.**

As technology nodes progress to smaller feature size a punchthrough condition is more likely to occur, which is the merging of the source and drain depletion regions in the substrate below the channel region controlled by the MOSFET gate as shown in Fig. 2. When punchthrough occurs, a nearly equipotential region forms between the source and drain. This equipotential region has much lower potential barrier across the source/drain-body junctions. This allows electrons to easily flow from the drain to the source in the substrate. The anti-punchthrough (APT) implants are used to prevent the merging of the source and drain depletion regions, accomplished by increasing the substrate ion species concentration (doping) in the region where punchthrough occurs. There are various methods for creating APT implants in sub-100nm technologies and can affect the SE charge collection process.



**Fig. 2. Merging of the source and drain depletion regions in the substrate of a PFET, referred to as punch through. When punch through occurs, an equipotential region forms between the source and drain.**

The focus of this thesis is to further understand how process engineering factors, such as well depth and doping, affect WPM-induced multiple node charge collection and how APT implants affect single device charge collection. Variations in contact spacing, well doping concentration, well depth, presence of a P+ buried layer, transistor density are applied to a 90nm

bulk CMOS technology are applied using technology computer aided (TCAD) simulations to obtain trends for WPM spatial extent and duration. TCAD simulations are used to explore the effects of different APT implants, such as blanket and pocket implants, to analyze the affected SE charge collection mechanisms.

## Section 1.2 Overview of previous work

Previous works have introduced the importance of understanding SE charge sharing among multiple MOSFETs. Charge sharing can occur because of the direct collection of excess charge by multiple MOSFETs (Fig. 3) and the activation of the inherent bipolar by SE well potential modulation (Fig. 4). It has been shown through experiments that charge sharing is of real concern for sub-100nm technology nodes [2]. Charge sharing can affect combinational logic circuits through “pulse quenching,” where the original SET produced by a struck transistor is shortened by charge collected by nearby MOSFETs along the signal path [3]. Multiple bit SEUs can occur in memory arrays, such as a SRAM bank, can occur because of charge being shared among multiple circuit nodes, increasing single event error rates [4], [5]. Even in radiation tolerant circuit designs like DICE memory circuits which are immune to single node upsets, charge sharing can affect multiple nodes if care nodal separation is used during physical layout of the circuit [6]. Well potential collapse has been shown to be one of the mechanisms behind charge sharing by activating the bipolar in multiple MOSFETs [7-9]. To fully understand the charge sharing phenomenon, it is important to understand what parameters affect WPM.

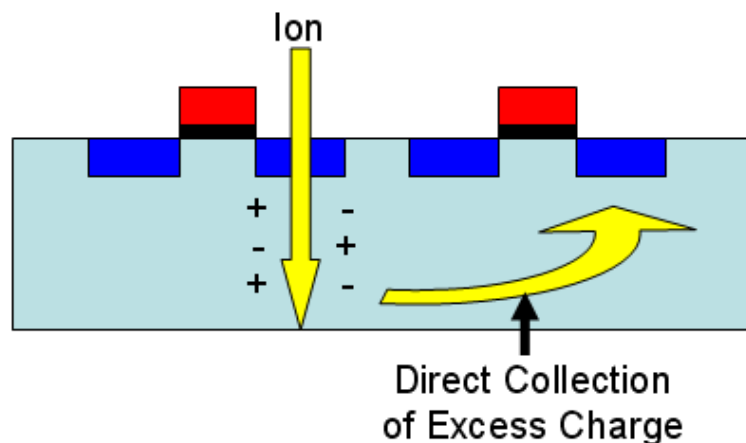
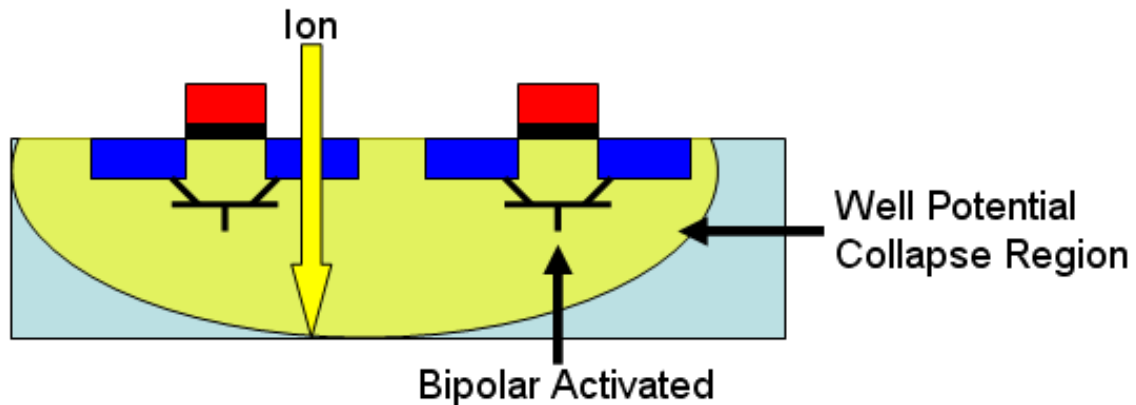


Fig. 3. Illustration of charge sharing by direct collection of SE deposited charge.



**Fig. 4. Illustration of WPC inducing charge collection by activating the parasitic bipolar of multiple MOSFETs.**

As technology scaling progresses, punchthrough has become a major concern as it can result in higher static power consumption in MOSFETs. Overtime, this as lead to the creation of blanket, gate aligned, and pocket APT implants, illustrated in Fig. 5 [10]. Blanket implants were the first attempt at controlling punchthrough, but as technology scaling progressed blanket implants created high source/drain-body junction capacitances leading to higher dynamic power consumption and slower switching speeds and could interfere with voltage-threshold implants due to following annealing steps in the process. To overcome to drawback of blanket implants, pocket implant techniques were created by using high angle ion implantation. Using the high angle implants, it was possible to place the pocket implants directly in the region of the punchthrough path while maintaining lower source/drain-body junction capacitances and reduce the chance of the pocket implant from interfering with the voltage threshold implant. For emerging technology generations, it is almost guaranteed that pocket implants are used in controlling punchthrough.

The SE charge collection process has been extensively studied for single MOSFET ion strikes. Technology scaling reduces transistor drive currents thus leading to smaller amounts of charge needed to cause SEUs; the lowest amount of charge to cause an upset in a circuit is known as  $Q_{crit}$ . Also, sub-100nm technology nodes have ushered in the need of APT implants to reduce sub-threshold currents. To the author's knowledge, there have been no studies on the effects of various APT implants on SE charge collection.



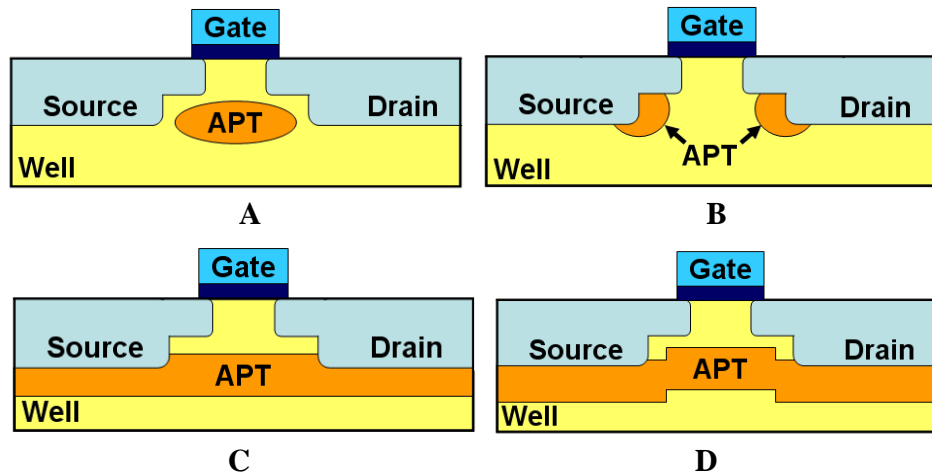


Fig. 5. Various APT implants. A) Gate aligned. B) Pocket Halo C) Standard Blanket D) Step Blanket

### Section 1.3 Thesis overview

This work aims to characterize the spatial temporal trends of WPM across various parameters and the effects of different APT implants on single MOSFET SE charge collection through the use of TCAD simulations. To date, WPM effects have been characterized with respect to single or two MOSFETs, but no study has been performed on the characteristics of WPM itself. Also, the design for a novel circuit is introduced that can be used to experimentally characterize SE WPM collapse. With the availability of various APT implants, it is important to understand how these implants can affect the SE charge collection process and how implants can be implemented to improve radiation hardness. The previous literature on these topics is discussed in Chapters 3 and 4.

Chapter 2 covers the basic 90nm bulk CMOS 3D TCAD model structure and associated compact models used for simulations used in the WPM and APT implant studies. Well potential collapse spatial and temporal characterization is contained in chapter 3. This chapter characterizes WPM collapse across a wide spread of various parameters to capture the global nature of WPM. In Chapter 4, the WPM measurement circuit is introduced with simulations as a proof of concept. Chapter 5 explores the effects of various APT implants on charge collection process. In addition, the effects of masking are covered to help improve radiation hardened processes that contain APT implants.

## Chapter II

### MOSFET SIMULATION MODELS

#### Section 2.1 Overview

This chapter covers the basic MOSFET models used in later 3D TCAD simulations. The TCAD transistors are based on calibrated to current-voltage curves obtained from the IBM 9SF 90nm bulk CMOS technology node. The baseline transistor and well doping parameters are presented for reference in future sections.

#### Section 2.2 3D TCAD MOSFET models

Previously calibrated full 3D TCAD device models were used as baseline structures for all simulations. Calibration details are thoroughly covered in [11]. The well structure and STI depth are based on 130nm technology node specifications, as 130 nm and 90 nm well structures are expected to be similar. Model creation and heavy ion simulation are performed with Synopsys Sentaurus tools, specifically the models are built with Structure Editor and Mesh then bias and heavy ions simulations are performed by SDevice [12]. Simulations were performed on the ACCRE computing cluster at Vanderbilt University [13]. This section covers current-voltage characteristics of the models and doping concentrations of the MOSFETs and well structures.

The nFET size used in all simulations has an actual channel length of 80nm and width of 280nm. The current versus voltage curves are shown Fig. 6 for nFET TCAD models and match curves obtained from the IBM PDK. In Fig. 7, the basic nFET, p-well, p+ buried layer, and p-substrate are shown. All doping implants are created using Gaussian profiles shown in Fig. 8.

The actual length used in pFET simulations is 80nm. Two pFET widths are used, 280nm and 840nm. Current versus voltage sweeps are for a pFET with 280nm width are shown in Fig. 9. The basic pFET, n-well, p+ buried layer, and p-substrate are displayed in Fig. 10. Gaussian doping profiles versus depth are contained in Fig. 11.

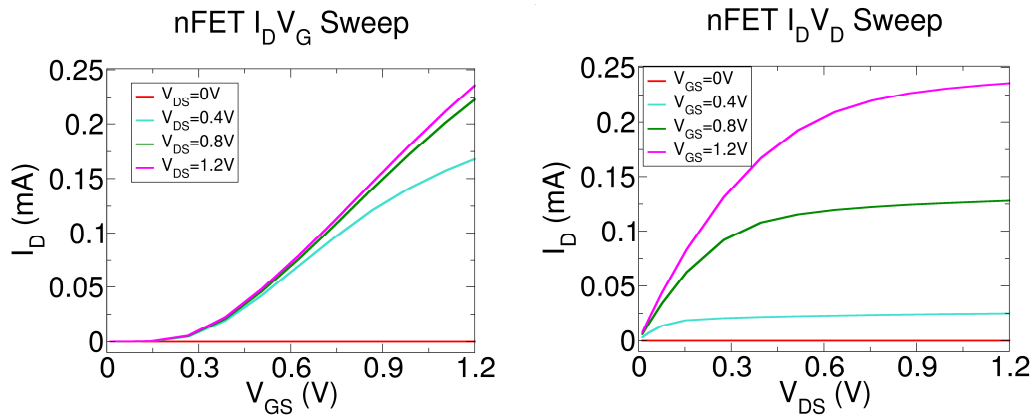


Fig. 6. Current versus voltage sweeps for a nFET with  $L=80\text{nm}$  and  $W=280\text{nm}$ .

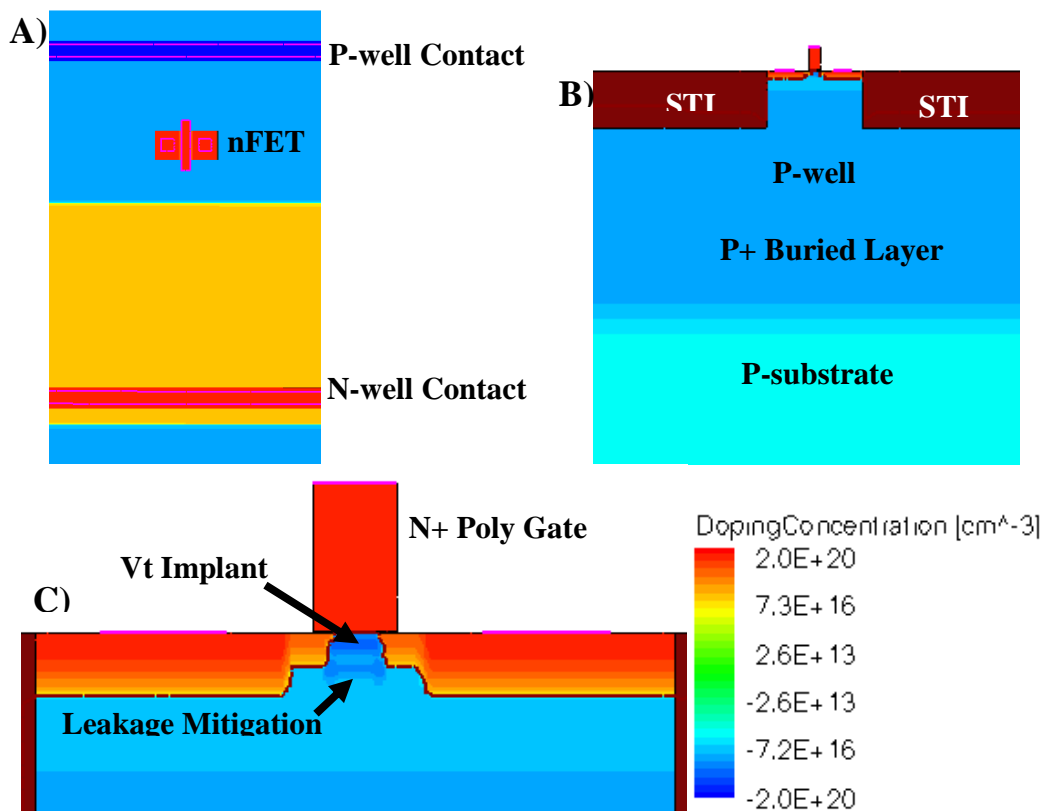


Fig. 7. nFET 3D TCAD structure. A) overhead view of nFET and wells. B) Side view of nFET showing the P-well, P+ buried layer, and P-substrate. C) Close-up view of nFET.

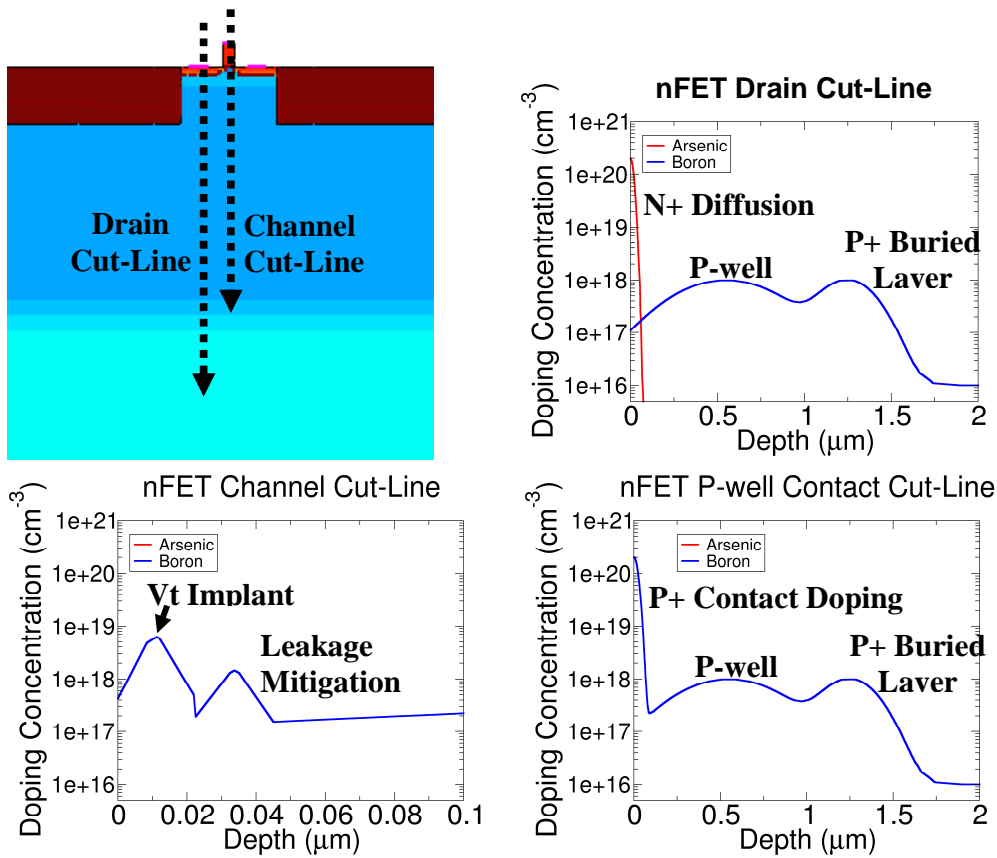


Fig. 8. 1D cut-line showing the doping concentration versus depths at various locations of the nFET structure.

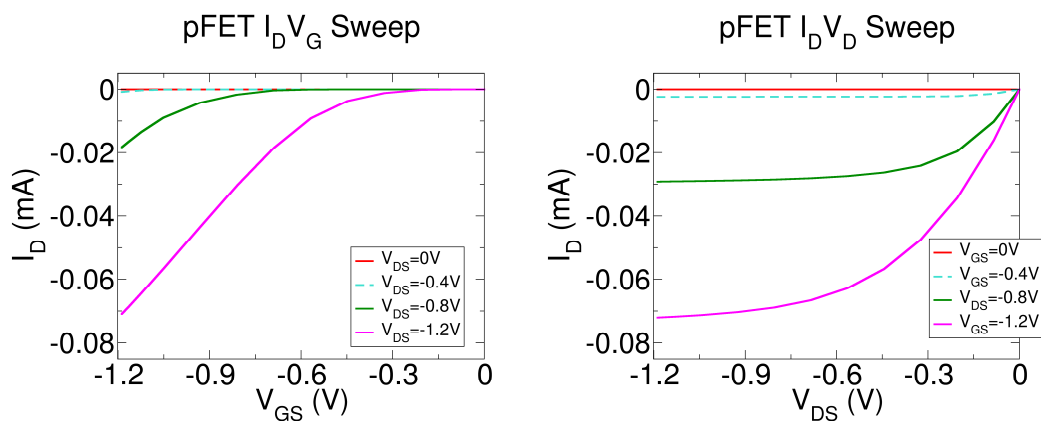


Fig. 9. Current versus voltage sweeps for a pFET with  $L=80\text{nm}$  and  $W=280\text{nm}$ .

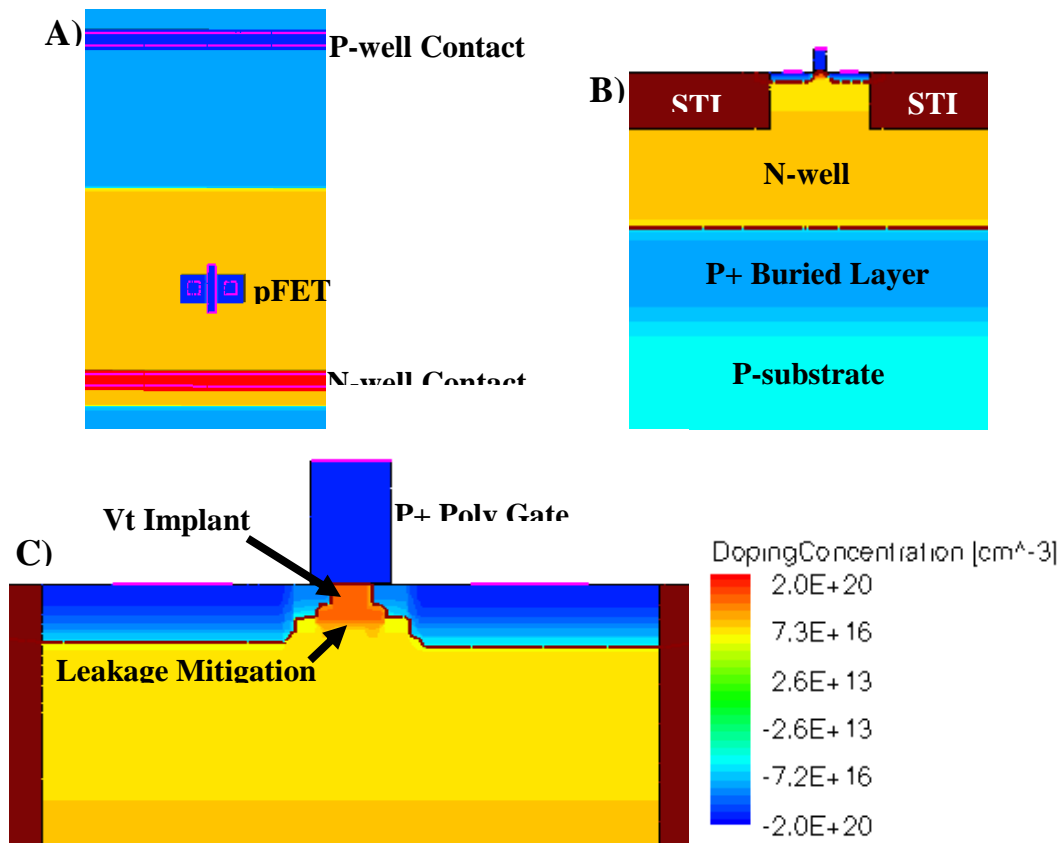


Fig. 10. pFET 3D TCAD structure. A) overhead view of pFET and wells. B) Side view of pFET showing the N-well, P+ buried layer, and P-substrate. C) Close-up view of pFET.

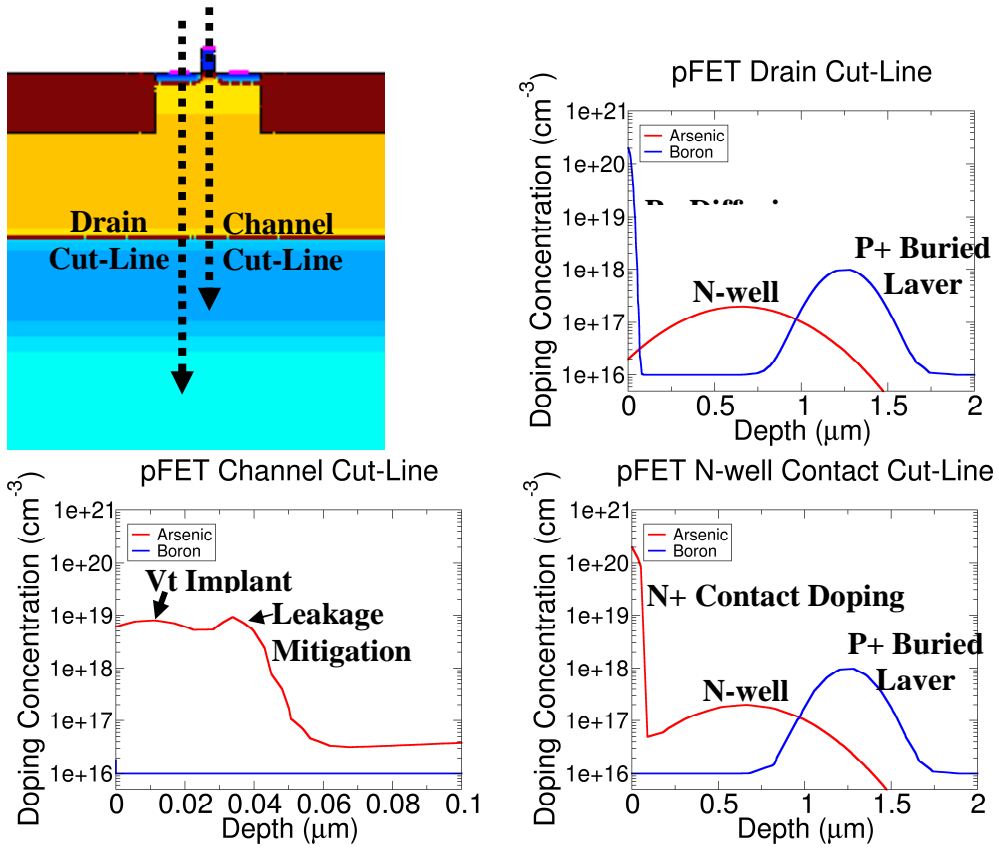


Fig. 11. 1D cut-line showing the doping concentration versus depths at various locations of the pFET structure.

2D Cut-Line

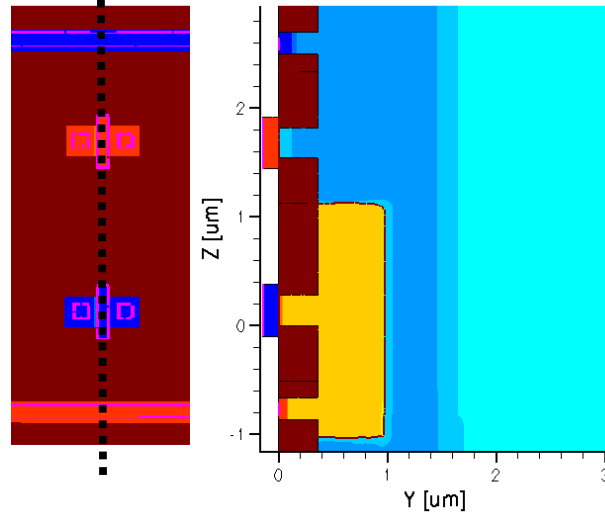


Fig. 12. 2D Plot of the side of both nFET and pFET to show well dimensions.

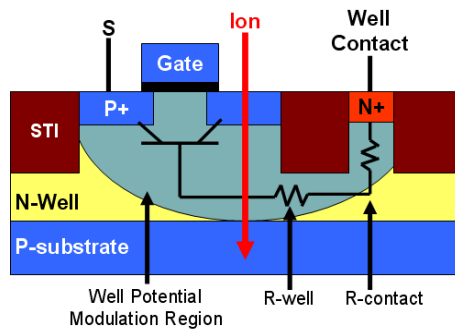
## Chapter III

### WELL STRUCTURE EFFECTS ON WPM RESPONSE

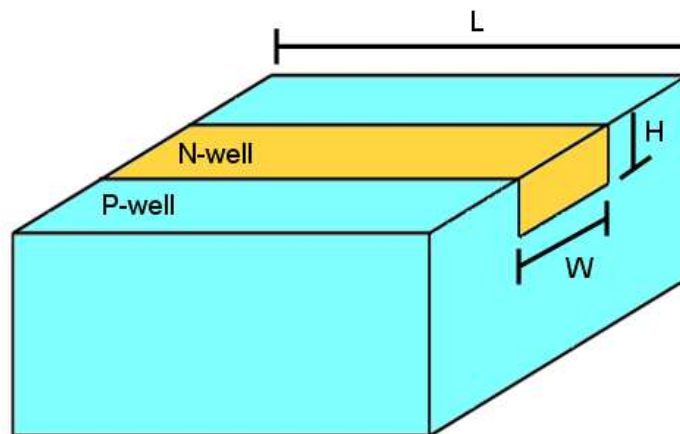
#### Section 3.1 Overview

The main focus of study for well potential modulation in previous works focus on WPM effects on a single transistor, sometimes multiple transistors [2], [4], [5], [7], [8], [14-17]. Amusan showed in two photon absorption laser experiments that WPM triggers the bipolar of PFET devices in 90nm bulk CMOS [2]. WPM can affect SET pulse shapes shown by DasGupta [15]. Black, Gasiot, and Olson show that WPM is directly linked to multiple cell upsets in SRAM arrays [4], [17], [18]. These works explain that WPM induces SE bipolar charge collection on multiple devices. TCAD simulations show that for the 90nm technology node that WPM can spatially encompass tens of transistors for a 5 MeV-cm<sup>2</sup>/mg ion strike, inducing bipolar charge collection at multiple nodes. This chapter shows that WPM spatial extent and duration are affected by layout and technology process parameters. Mainly, these factors affect the lateral resistance path from the transistor to the well contact (R-well) and the vertical resistance path through the STI connecting to the well contact metallization (R-contact), shown in Fig. 13. Fig. 14 shows how the lateral resistance, R-well, of the N-well can be estimated to the N-well contacts. A similar approach can be used to calculate the vertical resistance from the bulk of the well through the STI to the well contact, R-contact. Technology process parameters such as well doping concentration and well depth can affect the well resistance and change the rate at which charge is removed from the well, thus affecting WPM. WPM manifests differently in N-well and P-well structures due to the more confined geometry of the N-well versus P-well in dual well Bulk CMOS. To further understand multiple node charge collection, it is important to exercise various technology and structural parameters over a range of values to capture the spatial and temporal aspects of WPM. The following chapter will focus on characterizing WPM over various factors divided into the following sections: well spacing, well doping, well depth, presence of the P+ buried layer, transistor density, LET dependence, and WPM in p-wells.





**Fig. 13. Well resistances that affect SE parasitic bipolar current of a device. Well layout and technology process parameters can affect these resistances. Also, these resistances can affect the spatial and temporal characteristics of WPM.**



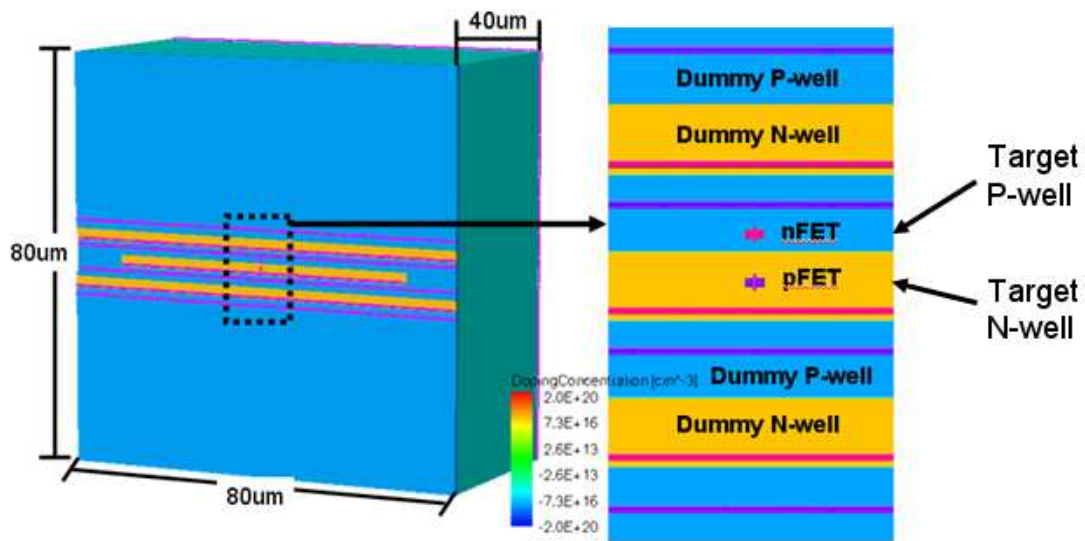
$$R_{\text{well}} = \rho * L / (W*H)$$

**Fig. 14. Illustration showing how to estimate the resistance of the N-well.**

### Section 3.2 Simulation Setup

To properly capture the physical behavior of a typical well in a CMOS logic application during a single event transient, a large and complex 3D TCAD structure is used for mixed-mode simulations, depicted in Fig. 15. This model uses the TCAD models described in the introductory modeling section for the transistors; the baseline well parameters, such as well doping, well depth, and P+ buried layer, are based on the same 90nm TCAD model. The nFET and pFET W/L

values are 280nm/80nm in all simulations. The nFET and pFET are electrically isolated and only share connections through the supply rails; both transistors are unloaded and have their respective gates biased so the transistor is off (no channel inversion), for example nFET gate and source is connected to ground and the drain is connected to VDD as shown in Fig. 16. The voltage sources and electrical connections to the TCAD structure are made in the SPICE portion of the mixed-mode simulation. Multiple dummy wells are used to surround the central target P-well and N-well containing the nFET and pFET transistors. The central target N-well does not laterally extend across the entire structure; this is done to avoid WPM interaction with the non-realistic simulation boundary. Ion strikes are centered on the drain of the device in the target well.



**Fig. 15. 3D TCAD simulation structure. A large structure with multiple wells is used to accurately capture the WPC response of the P-well and N-well containing the nFET and pFET.**

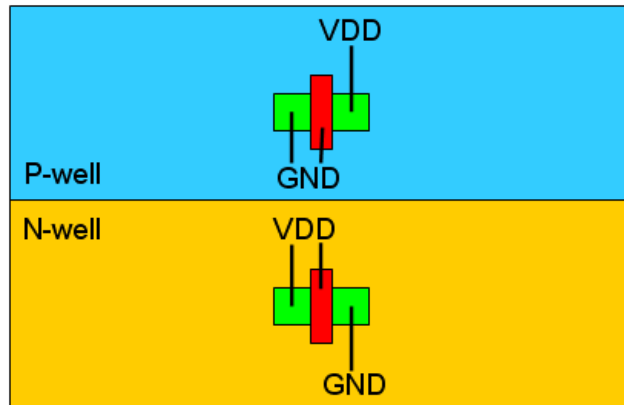


Fig. 16. SPICE voltage source connections to TCAD MOSFETs.

### Section 3.3 Well Contact Spacing Effects on WPM in N-well Structures

One method for increasing transistor density in CMOS designs is to increase well contact spacing (reducing well contact density) and leaving more active area for transistors in the cell layout, a technique commonly used in SRAM arrays. Well contact spacing affects the length lateral well resistance path (R-well), shown in Fig. 13. To examine well contact spacing effects on WPM spatial extent and duration, simulation structures are simulated using three different contacting schemes, shown in Fig. 17. Again, ion strikes are simulated in the drain of the pFET. Before extensively examining WPM results, a new method will be introduced for plotting WPM spatial extent and duration. Then, results are examined showing the effect of contact spacing on WPM spatial extent and duration.

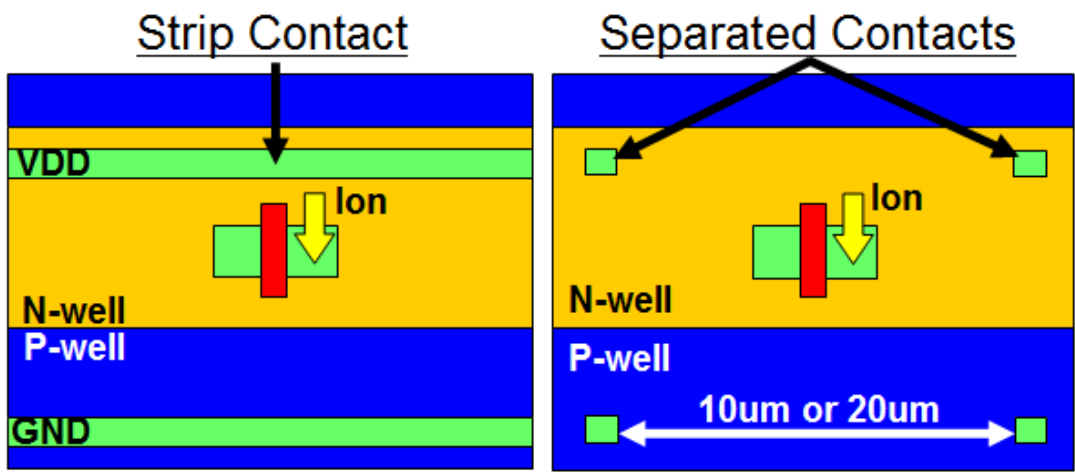


Fig. 17. Well contacting schemes simulated. Strip contacts provide least amount of well resistance compared to the 10um and 20um spaced contacts.

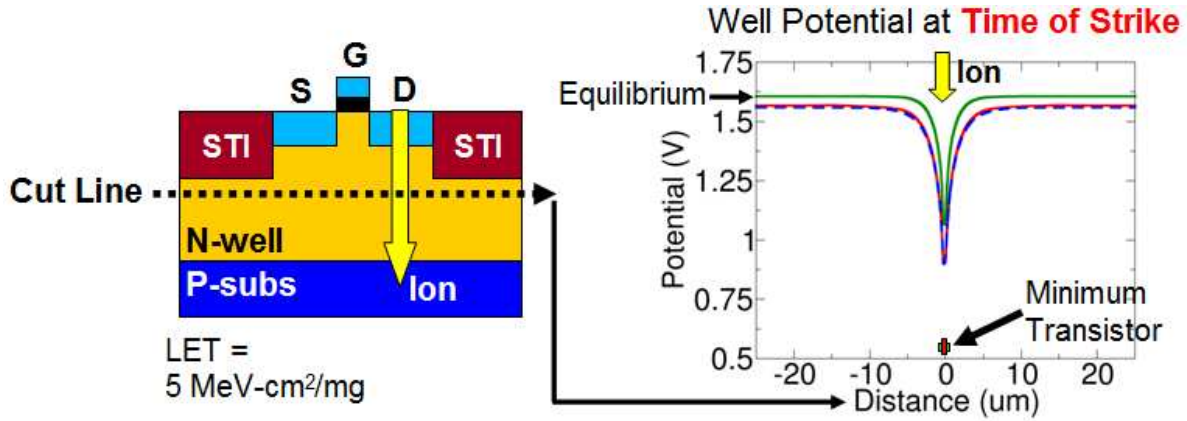
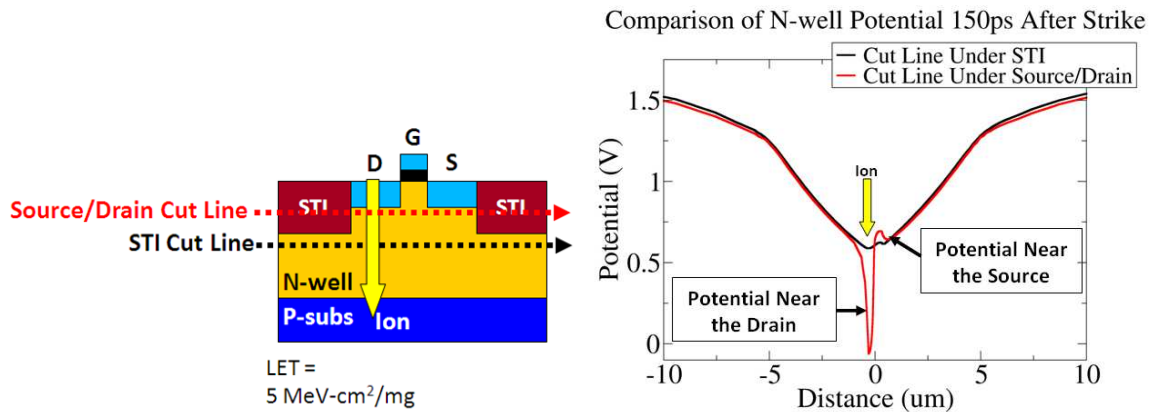


Fig. 18. Plot showing potential along the N-well 20nm below the STI. The ion strike occurs at the center of the well (Distance = 0) and the potential vs. the distance plot from the strike shows the WPM voltage drop along the well. This shows the potential that can affect devices along the well.



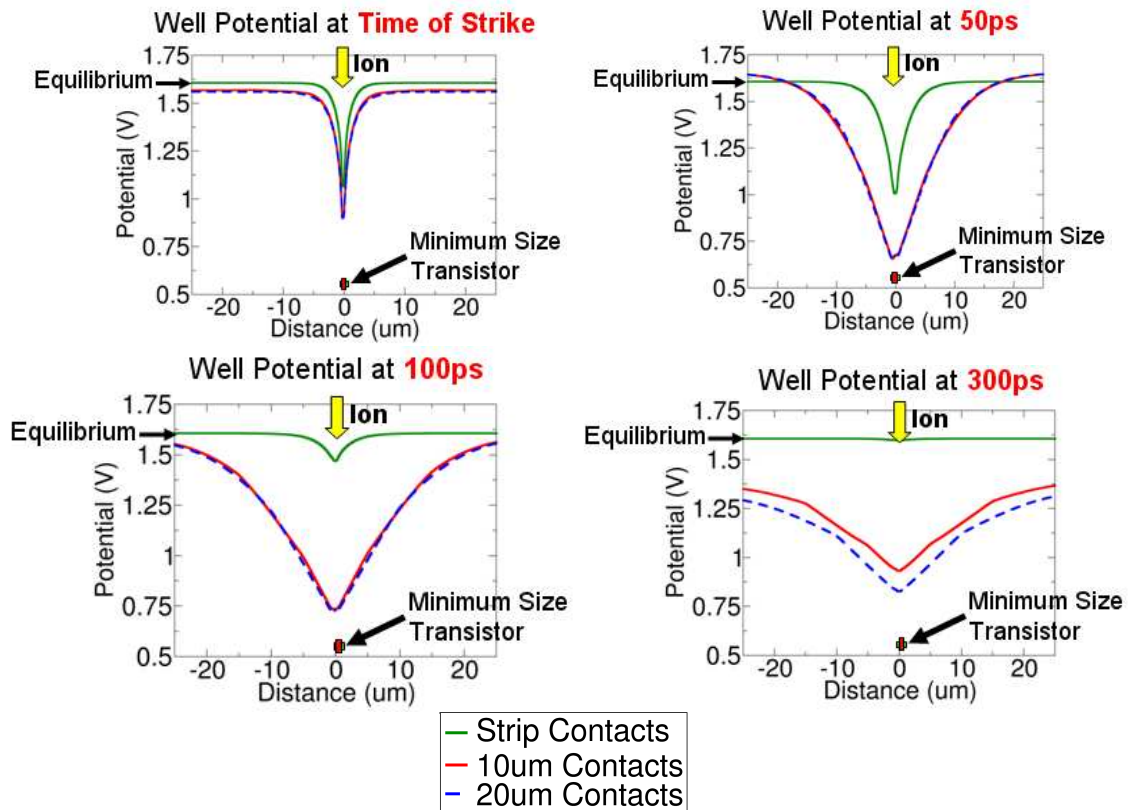
**Fig. 19 Potential cut-line along the n-well. Cut-lines are taken below the source/drain diffusions and STI. The potential cut-line through the STI provides a good estimate of the potential seen closer to the transistor.**

In the following discussion, simulation results are examined and a new way of visualizing WPM spatial extent and duration is introduced using the three well contacting schemes. This new WPM spatial extent and duration plot is used as the method for comparison for the remaining sections of this chapter. First, Fig. 18 shows that the well potential is evaluated by taking a 1D cut-line 20nm below the STI. In Fig. 19 two potential cut-lines are shown at different depths in the well; this plot shows that using the potential cut-line below the STI provides a meaningful estimation of the potential seen near the transistor. The potential near the drain is lower because of the depletion region being pushed out during the SE. While the potential near the source is higher because of the injection of holes. At equilibrium, the cut-line below the drain and source of the device will not be a straight line due to the drain depletion region extending into the substrate. Source charge injection occurs in a PMOS transistor when the potential of the N-well becomes lower than the potential applied to the source. To gain a better grasp of how WPM manifests over time, Fig. 20 shows 1D potential plots versus distance from a 5 MeV-cm<sup>2</sup>/mg ion strike in the N-well at progressive times during the strike. Initially after the strike, the WPM collapse area is confined to the immediate area of the strike. Shortly after the strike, charge is able to drift and diffuse from the strike location toward the well contacts, generating a larger potential gradient in the well. The metric used to characterize the extent of WPM is related to the area in the well where the potential modulation from equilibrium is equal to or greater than the zero-bias built-in potential (VJ0) across source-body junction,

approximately 0.6V; potential modulation greater than  $V_{J0}$  completely forward biases the emitter of the parasitic MOSFET bipolar and produces the largest amount of source injected current. The  $V_{J0}$  region versus time plot is created by calculating the distance over which well potential modulation exceeds the source-body built-in potential at that point in time; transistors within this calculated distance will experience the maximum amount of source injected current compared to other transistors in the WPM affected area. By graphing the distance of well potential modulation greater than the built-in voltage ( $V_{J0}$ ) (assumed to be 0.6V for these plots, but actual is 0.88V, all presented trends would still hold if 0.88V is used) versus time after the strike, comparisons can be made WPM spatial extent and duration can be made for different well structures, illustrated in Fig. 21. The vertical axis ( $V_{J0}$  distance) allows for a comparison of the WPM spatial extent while the horizontal axis allows for a comparison of the WPM duration. It is clear from Fig. 21 that the WPM in the well with the strip contacts is much more localized and recovers to equilibrium much faster than either the 10 or 20 micron spaced contact variants.

Now, comparisons of WPM spatial extent and duration can easily be extracted from the different contacting schemes. Previously, only strip, 10 $\mu\text{m}$ , and 20 $\mu\text{m}$  contact spacing WPM results were shown for simplicity. Simulation results for strip, 1 $\mu\text{m}$ , 2 $\mu\text{m}$ , 4 $\mu\text{m}$ , 8 $\mu\text{m}$ , 10 $\mu\text{m}$ , and 20 $\mu\text{m}$  contact spacing are shown in Fig. 22.

As contact spacing increases, the maximum WPM spatial extent increases. This trend can be seen in Fig. 22 by comparing the maximum  $V_{J0}$  distance for the various contact schemes, with the strip contact having the smallest and the 20 $\mu\text{m}$  having the largest  $V_{J0}$  distance. By increasing the contact spacing, resistance to well contacts becomes larger limiting SE restoration current to the well. Current paths to the well contacts determine the rate at which charge is removed from the well after the SE. If the charge is not removed promptly from the well after the SE, the charge will begin to drift and diffuse throughout the well to reach a state of equilibrium until sufficient charge is removed from the well to begin recovery of the potential or recombination occurs. When contact spacing is increased, charge is able to stay in the well longer and spread farther in the well. Comparing the strip and 1 $\mu\text{m}$  contact schemes, the strip contact is able to remove charge from the well much faster than the 1 $\mu\text{m}$  contacts leading to less charge spreading through the well, in turn smaller WPM spatial extent.



**Fig. 20.** 1D potential cut line 20nm below STI for an N-well strike at different times after the strike. Strip contacting (green) WPM spatial extent and duration are significantly smaller compared to the 10um (red) and 20um (blue dashed) separated contacts.

An interesting trend in the VJ0 distance is seen in Fig. 22b; the maximum VJ0 distance appears to saturate as the contact spacing becomes greater than 8um. As contacting spacing increases, WPM area becomes more of a function of the lateral well resistance than the vertical resistance through the STI to the well contact. This effect can be explained by examining at the formula for resistivity in relation to the dimensions of then well,  $R = \rho * \text{Length} / \text{Area}$ , illustrated in Fig. 14,  $\rho$  = resistivity of the well and will be considered constant for this thought experiment. The opening in the STI for the separated contacts has a much smaller area than the lateral opening on the well under the STI; for these simulations the lateral well resistance and vertical resistance through the STI are in series. As the separation of the contacts increases, the length of the lateral distance of the well increases thus increasing the lateral well resistance. The lateral well resistance will begin to become comparable (at some point greater) than the vertical STI

well resistance; when this occurs, the WPM area will become a function of the larger lateral resistance of the well, and thus WPM area saturates for very large well contact distances. It is hypothesized that the small increase in WPM VJ0 distance seen in Fig. 22b (for the 20um separation compared to the 10um) appears to saturate because of the increase in lateral well resistance to the contacts. These results show that WPM area and duration are a function of well contacting densities, but if the well contacting densities are very small, WPM area will appear to saturate due to increases in lateral well resistance.

Another concern as contact spacing increases is the increases in WPM duration. As explained earlier before in the section, resistance to the well contacts increase as contact spacing increases, so charge removal from the well is slow. This will increase the duration of the WPM compared to the more densely contacted (strip) case.

These results show that contact spacing can have a major affect on WPM spatial extent and duration. For very large contact spacing WPM can reach widths that can encompass tens of transistors for 90nm. As scaling in creases, transistor densities increase leading to an even greater number of transistors being affect by WPM compared to 90nm.



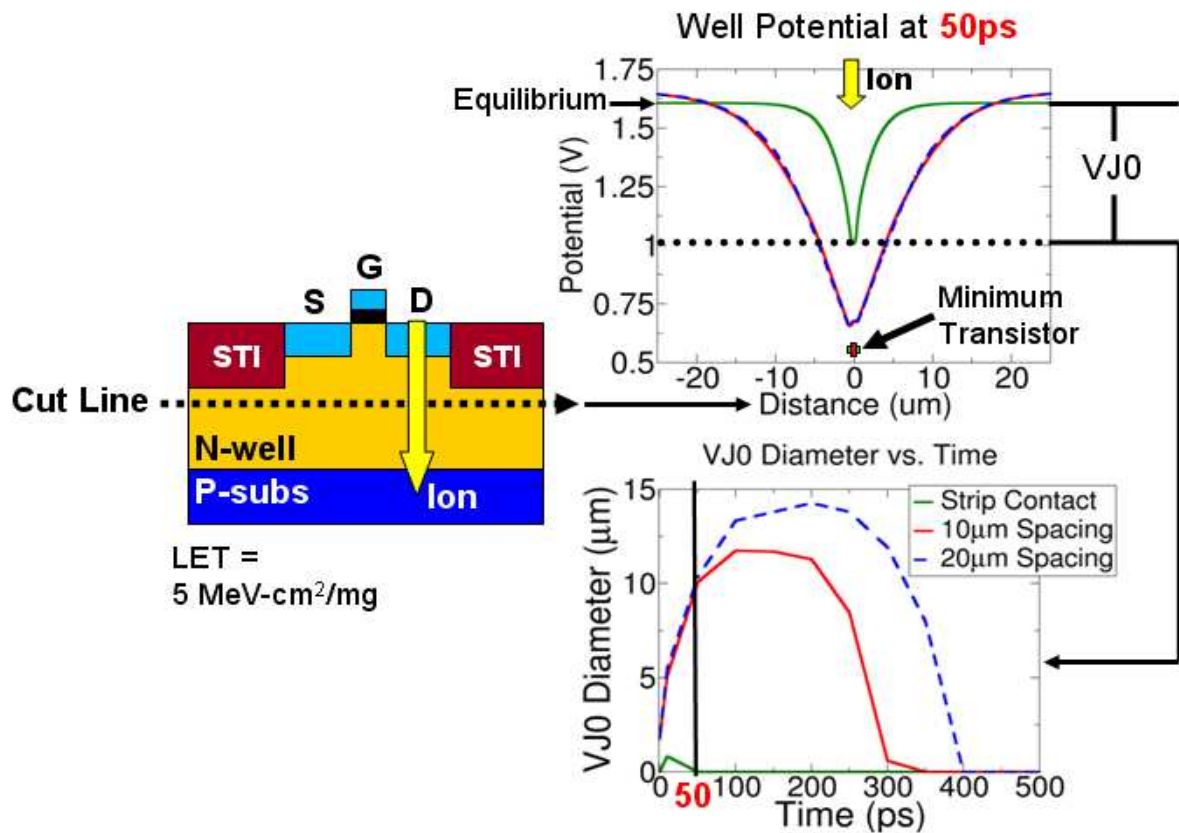


Fig. 21. Illustration of how WPM built-in voltage (VJ0) distance vs. time is generated. The VJ0 Distance is calculated as the distance over which potential modulation in the well exceeds built-in potential of the source-body junction at that point in time.

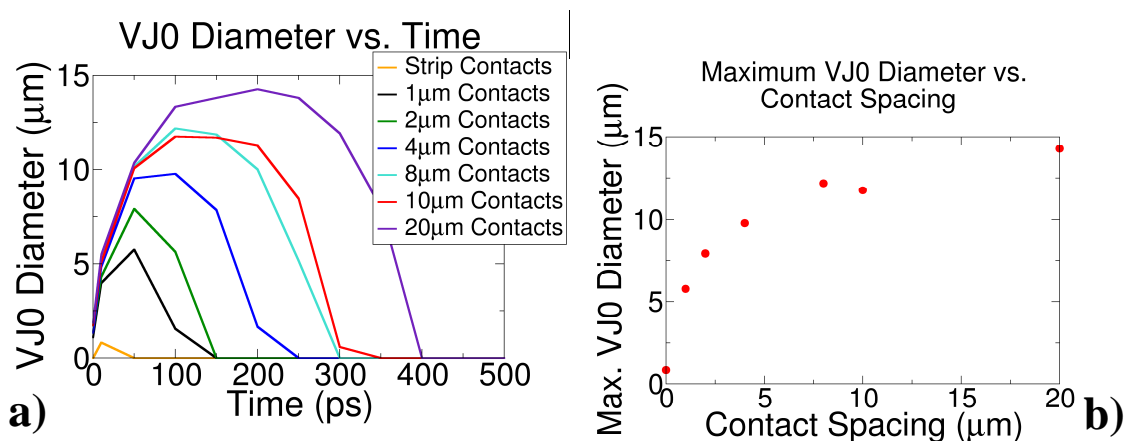


Fig. 22. a) VJ0 distance versus time for various contacting densities. LET value is  $5\text{MeV-cm}^2/\text{mg}$ . b) Maximum VJ0 distance versus contact spacing. VJ0 distance saturates when contact spacing becomes greater than  $8\mu\text{m}$ .

### Section 3.4 Well Doping Concentration Effects on WPM in N-well Structures

Well doping concentration has a direct effect on the conductivity of the well, affecting both the lateral resistance of the well and the vertical resistance through the STI to the substrate supply rail. Increasing the well doping concentration reduces the well resistance and decreases WPM area and duration. Fig. 23 illustrates that increasing the peak N-well doping concentration by an order of magnitude produces approximately order of magnitude decrease in WPM distance and duration. As technology scaling trends continue to reduce transistor size, N-well doping concentration can be expected to increase, but the maximum level of N-well increase is governed by the tolerated amount of drain/source-body junction capacitance. Also, well doping concentration may not be able to continue to increase with technology scaling as well doping will begin to interfere with channel implants [19]. As well doping concentrations begin to saturate between technology generations, WPM area and duration may become a more constant value in future technologies.

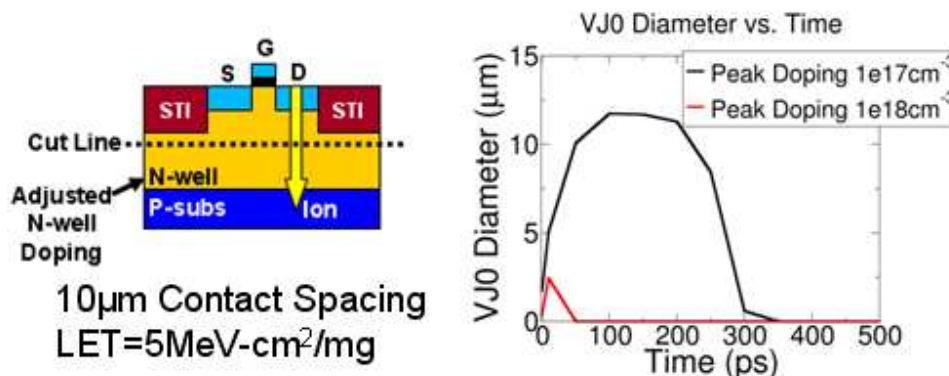


Fig. 23. VJ0 distance vs. time for  $1e17cm^{-3}$  (black) and  $1e18cm^{-3}$  (red) peak N-well doping concentrations. An order of magnitude increase in peak N-well doping concentration can produce almost an order of magnitude decrease in WPM distance and duration.

### Section 3.5 Well Depth Effects on WPM in N-well Structures

Changing the N-well depth has a major effect on the lateral well resistance under the STI to the contacts. To change the well depth, the peak well implantation depth below the silicon surfaced is placed at a different depth and the spreading distance of the well implant is changed

from the peak doping concentration location. To achieve the 0.6 $\mu\text{m}$  and 1.2 $\mu\text{m}$  well depths for this section, Fig. 24 shows the how the peak and roll off of the Gaussian well implants. Fig. 25 shows that for the 0.6 $\mu\text{m}$  well depth the WPM distance becomes almost of factor of 2 smaller compared to the 1.2 $\mu\text{m}$  depth. The factor that decreases the WPM distance is the change in amount of deposited charge due to the different well depths; the 0.6 $\mu\text{m}$  well depth collects about half the amount of charge as the 1.2 $\mu\text{m}$  well, thus showing less charge is deposited in the 0.6 $\mu\text{m}$  deep well. The smaller amount of charge collected in the 0.6 $\mu\text{m}$  deep well leads to smaller WPM spatial extent than the 1.2 $\mu\text{m}$  deep well. Reducing the well depth decreases the well volume under the STI increasing the lateral well resistance to the well contacts. The increased lateral well resistance to the contacts of the 0.6 $\mu\text{m}$  well depth increases the duration of WPM since removal of charge from the well takes more time than the 1.2 $\mu\text{m}$  well depth structure. The trend to decrease N-well depths as process technologies progress is rooted in decreasing latch-up vulnerability, but decreasing N-well depth is constrained by the same factors as increasing the N-well doping: higher source/body junction capacitances and increased well doping interaction with channel implants [20]. Thus, as technology scaling continues, WPM spatial extent will become smaller, but the WPM duration will increase.

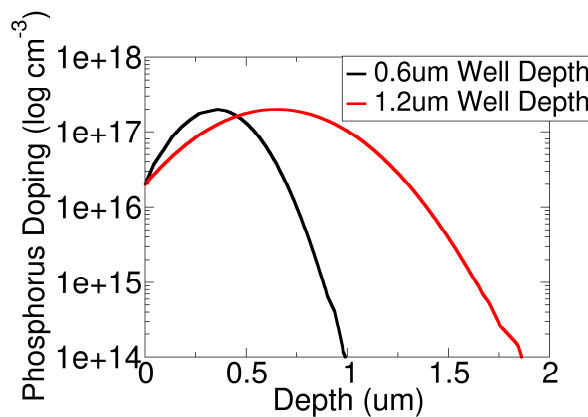


Fig. 24. N-well doping concentrations for 0.6 $\mu\text{m}$  and 1.2 $\mu\text{m}$  well depths.

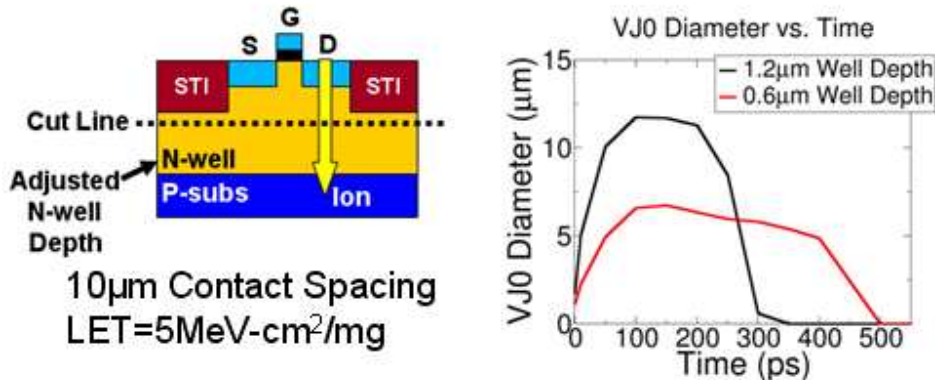


Fig. 25. VJ0 distance vs. time for 1.2um (black) and 0.6um (red) N-well depths. A factor of 2 decrease in N-well depth produces almost factor of 2 decrease in WPM distance.

### Section 3.6 P+ Buried Layer Effects on WPM in N-well Structures

Deep p+ implants are used to help reduce the substrate resistive path from the p-well to the n-well improving SE latch-up performance; the location of the p+ buried layer is below the n-well and p-well implants shown in Fig. 26 [21]. The presence of the p+ buried layer does not have a large effect on the n-well resistance compared to the previously discussed factors. Instead, the p+ buried layer limits the n-well substrate charge collection by reducing the n-well depletion region depth into the p-substrate. By reducing the n-well collected charge from the substrate by using a p+ buried layer, only the charge deposited in n-well region and the small depletion region into the substrate needs to be removed from the n-well (although in practice there is charge injected by the PMOS source as well). Thus, the presence of the P+ buried layer has less charge that needs to be removed from the n-well allowing for a smaller WPM distance and duration compared to having no P+ buried implant as seen in Fig. 26. Calculations show that the presence of the p+ buried layer can reduce the n-well depletion depth by a factor of three; simulation results show that the presence of the p+ buried layer reduced the amount charge collected by the well contacts is reduced by a factor of three showing a strong correlation to depletion region depth. The p+ buried layer can provide multiple benefits, SEL mitigation and reduction of SE bipolar multi-node charge collection.

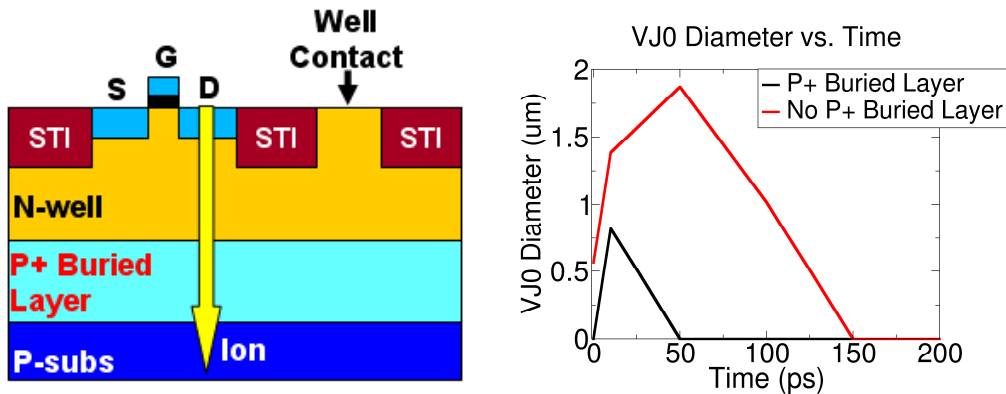


Fig. 26. WPM Distance vs. Time for the well structures with and without a P+ buried layer. Presence of the P+ buried layer reduces substrate charge collection to the N-well reducing WPM distance and time.

### Section 3.7 Effect of multiple transistors on WPM

In actual circuit designs there will be multiple transistors present in well; previous simulations used a single transistor in the well to reduce simulation time and resources. The sources of other transistors help to reduce WPM [4], by injection of charge carriers. The effect of multiple transistors is examined in this section using two simulation structures containing one transistor and five transistors, shown in Fig. 27. The five transistor structure uses five pFETs with W/L of 280nm/80nm with 150nm spacing between each transistor. All pFETs are electrically connected to be in the off state, the drain is connected to ground and the gate and source are connected to VDD. These structures provide insight into the interaction of multiple transistors and WPM by showing that the introduction of multiple sources help to maintain well potential and additional source and drain diffusions increase well capacitance.

As Black predicted, the sources of additional transistors in the five transistor simulation reduce the WPM distance compared to the single transistor simulation, seen in Fig. 28 [4]. When the well collapses near the pFETs adjacent to the struck device, the parasitic bipolar of the pFETs are triggered and holes are injected into the well from the source. Some of these injected holes escape being collected by the drain of the pFET and remain in the well, thus increasing the well potential. It can be said that the source-body junction is trying to pin the potential near the pFET to VDD minus the potential across the source-body junction; the sources act as pseudo contacts to help maintain the potential in that region.

Another trend is seen in Fig. 28, the rate of expansion and contraction of the VJ0 distance are different for the one and five transistor simulations. A simple explanation for this is related to the resistor-capacitance (RC) time constant of the well. The initial hypothesis is that the additional drain/source diffusions of the five transistor simulation increase the capacitance portion of the well RC time constant (similar to changing the resistance of the well) compared to the one transistor simulation. As the potential in the well changes near the transistors, their depletion regions are modulated and the charge distribution of the well is changed in the regions near the transistors. In effect, this capacitance modulation slows down the WPM response of the five transistor case compared to the one transistor simulation while restricting the maximum spatial extent of the WPM. This slower response can cause the WPM to occur for a longer period of time in the well before the well potential completely recovers.

As technology scaling continues, transistor densities will increase, hence the density of source/drain diffusions in wells increases. This helps to restrict the maximum WPM spatial extent by acting as pseudo well contacts. As the source/drain diffusion density increases, the recovery time of the WPM is elongated causing the parasitic bipolar of transistors in the area of the WPM to be activated for a longer period of time increasing charge collected by the affected transistors.

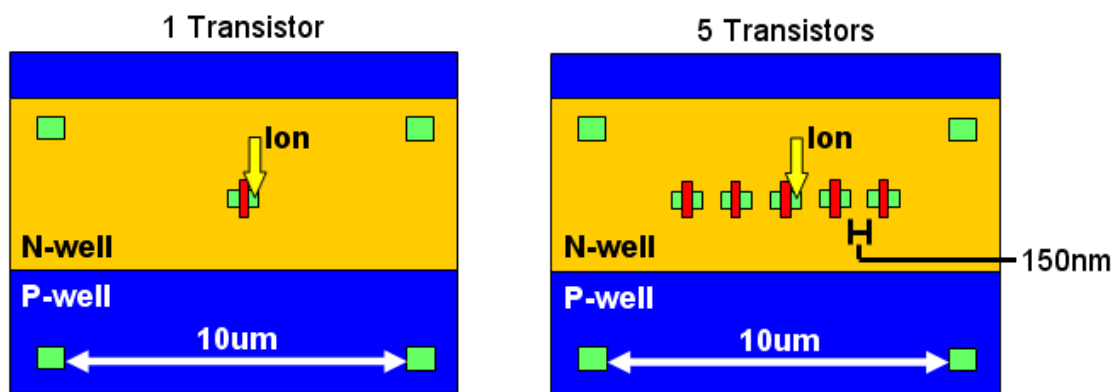
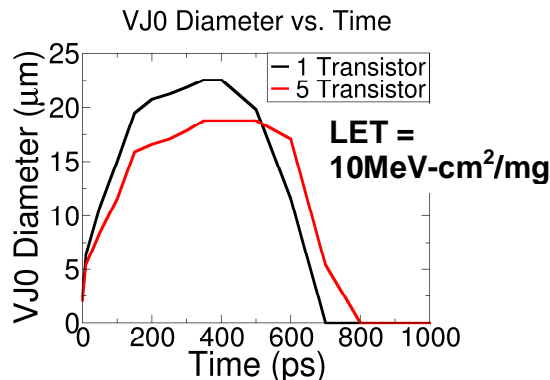


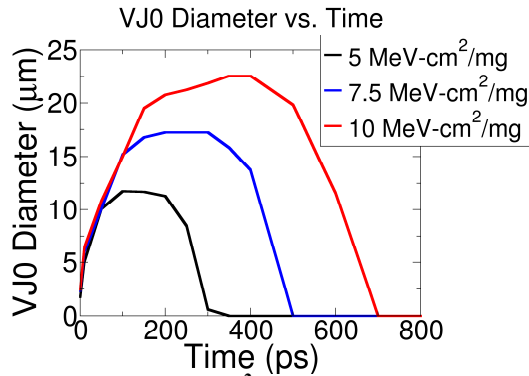
Fig. 27. Illustration of 1 and 5 transistor simulations. The transistors are spaced 150nm apart in the 5 transistor simulation.



**Fig. 28. VJ0 versus time plots for 1 and 5 transistor n-well strikes for a LET value of 10 MeV-cm<sup>2</sup>/mg. The 5 transistor simulation has a smaller maximum VJ0 diameter than the 1 transistor simulation. There is a delay in the rise and fall of the VJ0 diameter for the 5 transistor simulation.**

### Section 3.8 WPM LET dependence

So far, in this chapter we have seen how WPM is affected by resistive changes in the charge collection path and changes to the charge collection volume of the n-well. Next, WPM will be examined by changing the particle LET value, thus varying the charge deposited in the n-well. In Fig. 29, it can be seen that a factor of 2 increase in LET leads to a factor of 2 in the WPM distance and duration. As seen in section 1.3, WPM is a function of the resistive path to the well contacts. Thus, the distance and duration of WPM is dependent on how quickly charge can be removed from the well. More charge that is deposited in the well requires more time to remove, allowing more time for charge that is not removed by the well contacts to drift and diffuse over a larger area. For a given contact density, WPM distance and duration are a function of the deposited charge and restoring current to the well. As the LET of the incident particle becomes greater than 10 MeV-cm<sup>2</sup>/mg, higher charge densities may cause Auger and concentration-dependent SRH recombination to play a greater role, thus the WPM distance and duration may not be linearly promotional to LET of the ion for values greater than 10 MeV-cm<sup>2</sup>/mg.

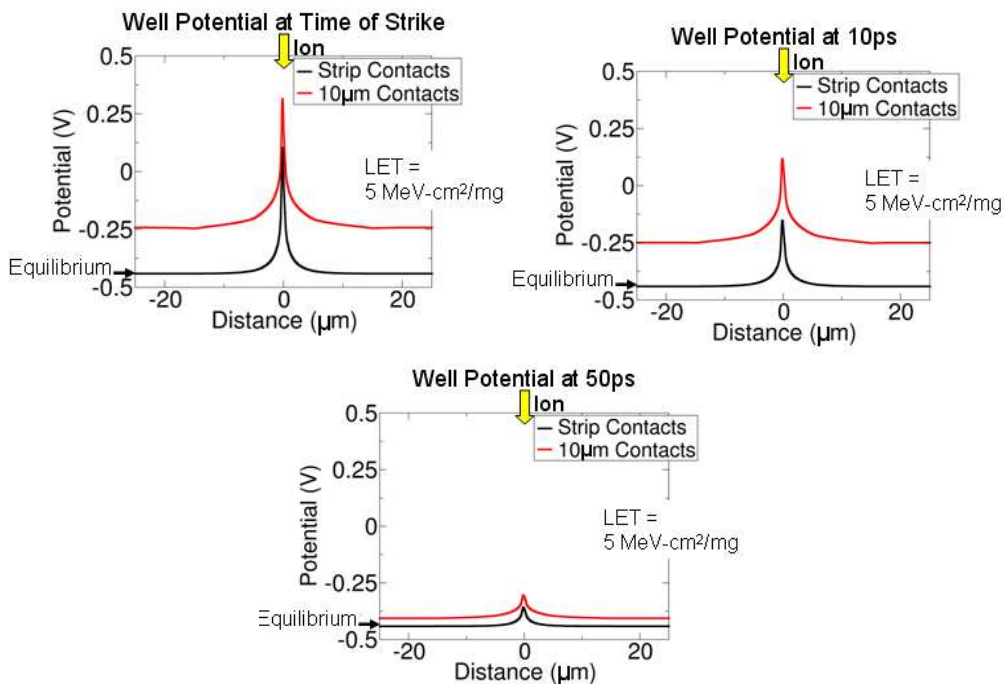
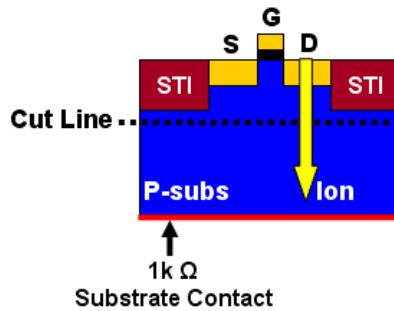


**Fig. 29. VJ0 diameter vs. time for 5 and 10 MeV-cm<sup>2</sup>/mg LET values for 10um separated contacts, 1.2um well depth, and P+buried layer. A factor of 2 increase in LET causes a factor of 2 increase in WPC diameter and duration.**

### Section 3.9 WPM in P-well in Dual Well CMOS

The severity of WPM collapse in p-wells for dual well bulk CMOS process is much less than in n-well structures. Fig. 30 shows 1D potential cut lines versus time for a 5 MeV-cm<sup>2</sup>/mg strike for strip and 10um spaced contacts; during the strike, the potential does vary from equilibrium 0.75V for a short distance from the strike, but shortly after the strike the potential modulation recovers very quickly to equilibrium values for both contact schemes. This fast rate of recovery is attributed to the backside substrate contact and contacts in other p-wells in the structure. All of these contacts are able to create multi low resistance paths for charge to be removed from the structure resulting in small WPM area and duration. Thus, SE bipolar-induced charge collection from well potential modulation is not a major concern for nFET transistors, especially for multiple nodes [8]. Less stringent local contacting schemes can be used for p-well structures with no increase in bipolar multiple node charge collection.





**Fig. 30. 1D potential cut lines vs. time for a 5 MeV-cm<sup>2</sup>/mg ion strike in a p-well. For p-well strikes in dual well CMOS, the WPM is small and short even for spaced contacts, compared to N-well strikes. Approximately 50ps after the strike, the potential for the strip contact (black) and 10µm spaced contact (red) has completely recovered to equilibrium values.**

### **Section 3.10 Conclusion**

Contact spacing TCAD simulations shows that for the 90nm technology node that WPM can spatially encompass tens of transistors, inducing bipolar charge collection at multiple nodes. Contact spacing is an important parameter in controlling WPM spatial extent and duration. Increased contact spacing will increase WPM spatial extent. At very large contact spacing, the spatial extent of WPM appears to saturate. For these 90nm simulations WPM can encompass more than 10 transistors; this means that multiple circuit nodes can be affected by SE bipolar charge collection. Also, as contact spacing increases, the WPM duration increases extending the duration of SE bipolar charge collection.

The other parameters described in this section relate to factors controlled in the process: well doping concentration, well depth, the presence of a p+ buried layer, and transistor density. As technology scaling progresses, well doping concentration tends to increase causing decreases in WPM spatial extent and duration, but doping concentrations can only be increased to a certain value before introducing detrimental effects. Well depth tends to decrease as technologies are scaled which can decrease WPM spatial extent and increase WPM duration. Transistor density increases from technology scaling help to reduce WPM spatial extent while the added capacitance from diffusions can cause slight increases in WPM duration. Overall, as technology scaling continues WPM duration and spatial extent should decrease if the above simulated trends are accurate and scaling guidelines don't change significantly in future technology regimes.

## Well Potential Modulation Expansion

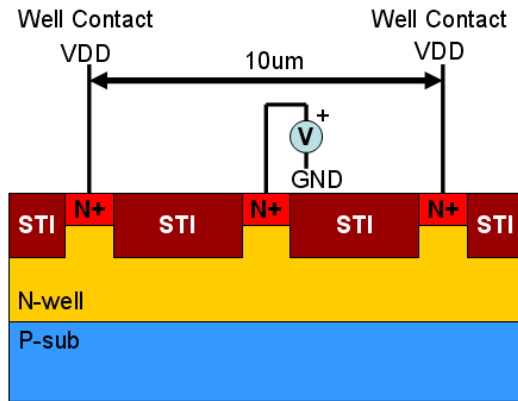
### Chapter IV

#### Section 4.1 Overview

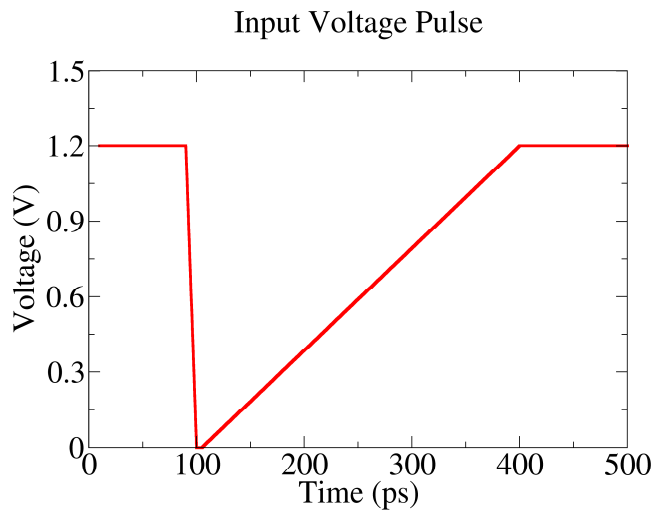
In Chapter 3, for various structures we saw WPM expanding across very large distances in very short time periods on the order of hundreds of picoseconds. This section proposes the mechanism through which WPM expansions occurs is due to simple electrical transmission of the SE generated potential modulation in the N-well after the ion strikes occurs. The SE generates a potential pulse in the N-well at the strike location; this pulse then travels along the N-well similar to any other electrical signal in a conductive medium. To support this hypothesis, a potential pulse is generated with a voltage or current source to decouple the charge deposition affect that occurs during an ion strike from the resulting potential in the well. It is shown that the voltage and current course pulse widths produce responses identical to the potential variation generated by a heavy ion.

#### Section 4.2 Simulation Setup

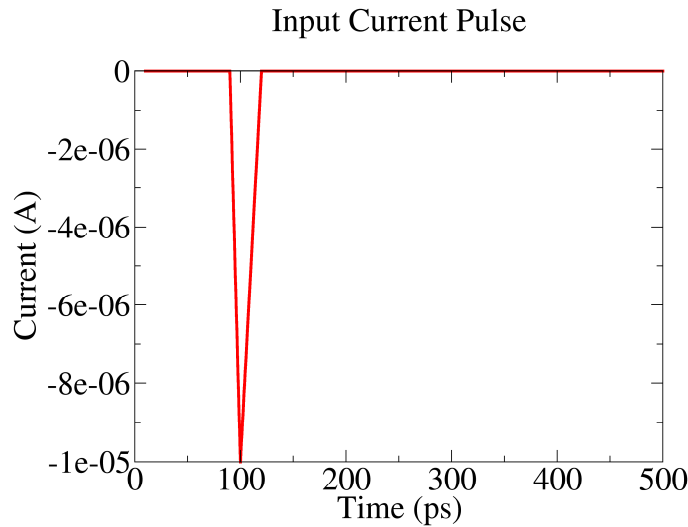
To study SE potential modulation expansion (potential propagation), it is important to decouple the charge deposition of the ion strike from resulting the potential modulation in the N-well. Using the 10um contact spacing structure from chapter 3, the pFET is removed from the 3D structure and is replaced with an N+ implant to provide proper conductivity to the N-well at that point, shown in Fig. . Either a voltage or current source is connected to the central N-well contact in Fig. . The variable voltage source has a waveform with a 10ps fall time (from 1.2V to 0V) and rise time of 400ps that emulates the heavy ion strike generated potential pulse shown in Fig. 32. The variable current pulse mimics the charge deposition of the heavy ion deposited charge, with a 10ps fall time and 20ps rise time as seen in Fig. 33.



**Fig. 31.** Simulation structure used with voltage and current sources. 10um spaced contact structure used from chapter 3 with the pFET device replaced with a N-well contact.



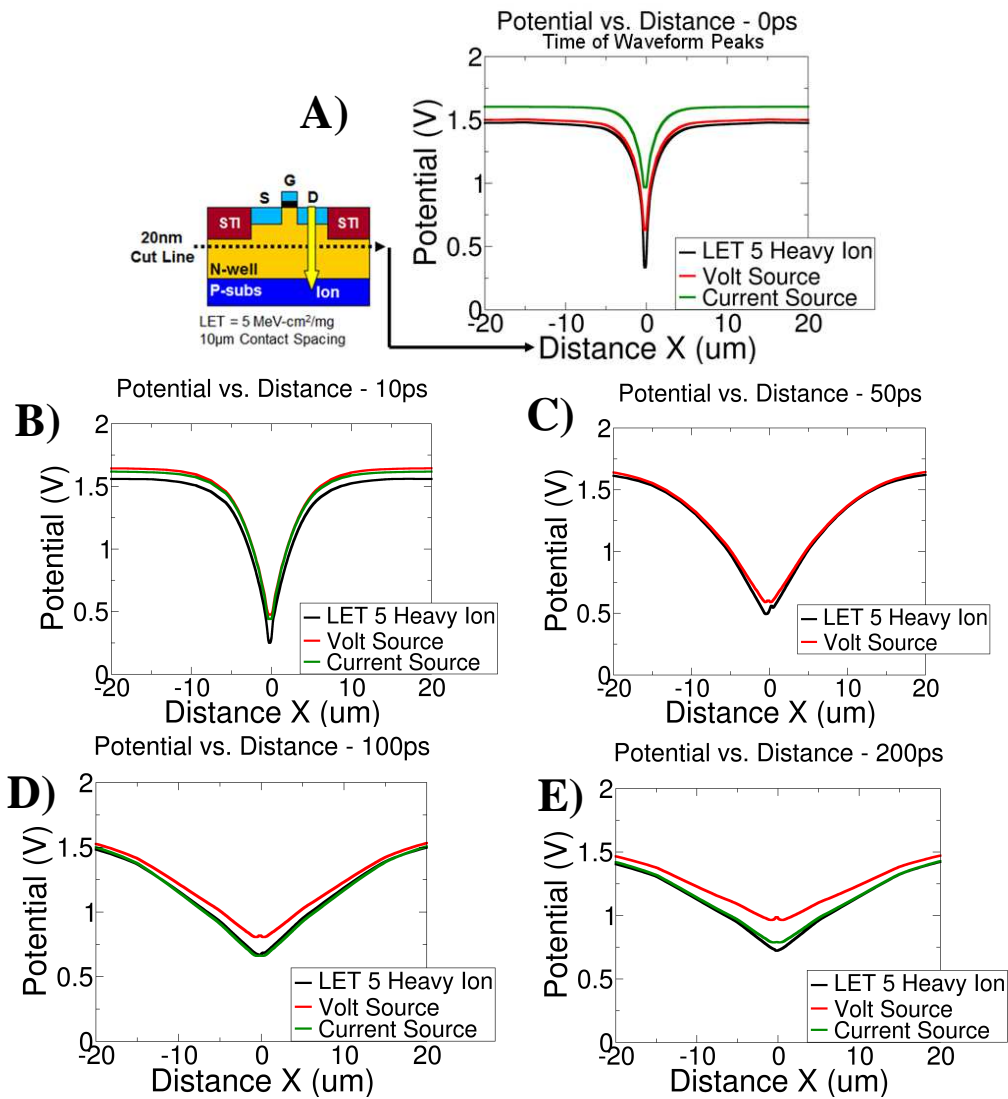
**Fig. 32.** Variable voltage source waveform. Shape tries to imitate the potential variation of the heavy-ion strike, 10ps fall time and 400ps rise time.



**Fig. 33. Variable current source waveform. Shape mimics the heavy ion charge deposition rate, 10ps fall time and 20ps rise time.**

### **Section 4.3 Well Potential Modulation Expansion of Heavy Ion, Voltage, and Current Sources Results**

Regardless of how the potential modulation is injected into the N-well, we see that expansion of potential modulation is extremely similar (if not exactly the same) for the heavy ion, voltage and current sources. To analyze the response of the three sources, 1-D cut-lines are taken 20nm below the STI (similar to chapter 3) and plotted at various times during the recovery after the peak of the all source waveforms in Fig. 34; 0ps in the Fig. 34 A) corresponds to 100ps in Fig. 32 and Fig. 33. In Fig. 34 A), at the peaks of all sources there are differences in the initial potential plots, as should be expected due to the differences in the sources. It is important to note, the 0ps plot occurs after initial injection of signals into the N-well, in other words all three sources have begun generation ~10ps before the 0ps plot shown. From 10ps to 200ps, we see the potential expansion of all three sources is basically identical. This is a very interesting and important result showing that the well potential expansion may not be a function of the deposited charge of the heavy ion strike, but a function of the potential pulse generated by the ion strike in the N-well.



**Fig. 34. 1-D potential cut-lines along the N-well 20nm below the STI at various times after peak signal generation for heavy ion, voltage, and current sources.**

#### **Section 4.4 Proposed Mechanisms of Potential Modulation Expansion**

The results from section 4.3 indicate that the SE WPM expansion may not be directly coupled to the deposited charge of the heavy ion strike. For instance, looking at the case of the voltage source, we see we have the same potential expansion as the heavy ion strike. This would imply the potential expansion is a function of well characteristics and not the source which generates the potential modulation, leading one to suspect that SE well potential modulation is simple electrical transmission of a potential pulse generated at the strike location. It is important to note, that excess generated electrons generated by the ion strike do not disperse farther than roughly 2 $\mu$ m from the strike location, so expansion of excess charge from the strike location is not responsible for WPM expansion. The WPM expansion is controlled by two different mechanisms: the resistive characteristics of the well and the generated potential pulse width.

WPM expansion can be related to the analogy of a voltage pulse traveling through a transmission line. When a voltage pulse travels through a transmission line, it does not change the carrier concentration in the medium as it electrically propagates, similar to the WPM expansion. How the voltage pulse travels down the medium is determined by the resistive-capacitive (RC) characteristics of the wire and not the signal itself. If the WPM expansion is solely determined by the characteristics of the well, then what source generates the potential pulse in the well does not matter to first order. Thinking of the N-well as transmission line, changing the resistance of the N-well will affect how the WPM expansion occurs and is not dependent on the source that generates the potential pulse.

The WPM expansion is determined by the potential pulse length generated by the heavy ion strike. The potential pulse length injected in the N-well is determined by how quickly the potential is able to recover in the immediate area of the strike. The affects of the recovery time of WPM can be seen in chapter 3 simulations. The most interesting of which is the presence of the p+ buried layer and LET dependence. The p+ buried layer and LET dependence do not directly affect the resistivity of the N-well to first order, but affects the N-well collection volume. The more charge deposited in the N-well collection volume, the longer it takes for the potential to recover in the at the immediate strike location. The longer the generated potential pulse, the further WPM expansion occurs. When the potential begins to return to its equilibrium value, the generated potential pulse will become attenuated by the RC characteristics of the well before further WPM expansion occurs.

#### **Section 4.5 Future Work**

To fully prove that WPM expansion is simply electrical propagation of an electrical pulse, more simulation and analysis will need to be conducted. First, more time slices will need to be created to see how the initial voltage pulse evolves for the heavy ion, voltage, and current sources. This involves taking a time slice every pico-second 20ps before after peak deposition for all three sources. Another interesting simulation would involve using the voltage source; the voltage source input would have a fall time of 10ps and remain at 0V until the well equalizes. This would allow us to analyze the actual transmission line behavior of the N-well and allow for an estimation of the RC time constant of the well. Lastly, voltage pulse simulations of the all the variants in chapter 3 should be performed to prove the electrical signal propagation theory holds for all cases.

#### **Section 4.6 Conclusion**

WPM expansion is proposed to be the electrical signal propagation of potential pulse generated by a SE. Comparing the heavy ion, voltage, and current sources provides a promising indication of the proposed mechanism. Using the voltage and current sources indicate that WPM expansion is independent of the excess carriers deposited by the heavy ion, but a function of the potential response caused by the generation of the excess carriers. After the generation of potential pulse at the strike location, WPM expansion is appears to be dictated by the RC characteristics of the well as the potential pulse propagates.



## Chapter V

### WPM MEASUREMENT CIRCUIT

#### Section 5.1 Overview

This chapter covers a novel circuit design that can be used to measure the extent of WPM. To date, WPM has not been experimentally quantified in bulk CMOS designs. Simulations show that this concept can feasibly measure the maximum spatial extent of well collapse. The various components of the circuit are covered along with design considerations.

#### Section 5.2 Application of substrate contacts for well potential measurement

The heart of the WPM measurement circuit involves using substrate contacts to sense voltage at different physical locations in the well. In 90nm bulk CMOS simulations, the substrate contact can be used as a voltage sensor contact, demonstrated in Fig. . The spacing between the substrate voltage sensor contact and the edge of the pFET in Fig. a is 140nm. For a 10MeV-cm<sup>2</sup>/mg ion strike, the voltage substrate sensor contact is able to monitor the potential at that point in the well over time, the red curve in Fig. b; this voltage sensor substrate contact is connected to the input of a buffer and is able to change the output state of the buffer (blue curve). Using a substrate contact for voltage sensing provides a usable signal for particle LET values as low as 1 MeV-cm<sup>2</sup>/mg for a buffer. The only concern is to select a method of detecting the voltage signal at the substrate contact that is fast and sensitive to the change that occurs at that point in the well.

#### Section 5.3 Voltage sensing circuitry

Section 4.2 shows that a buffer can produce a digital signal from voltage signal produced by a substrate voltage sensor contact. One can use an array of buffers connected to substrate sensor contacts to measure the spatial extent of WPM, illustrated in Fig. 36. When the potential of the well varies by more than switching threshold voltage of the buffers in the region of a substrate voltage sensor contact, the output of the buffer

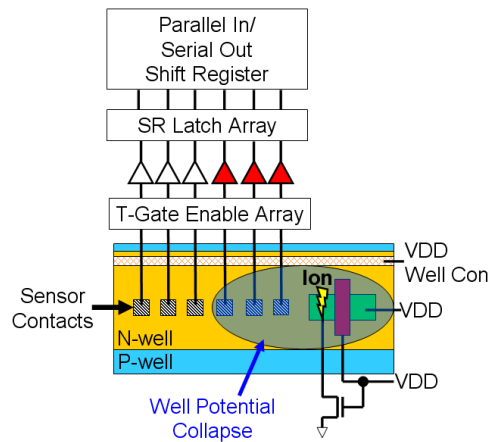


will change state, setting the SR latch connected to the buffer. Then, the output of the SR latch array is loaded into the parallel in/serial out shift register to be transmitted off chip. Serially shifting the data off chip greatly reduces the number of out pins. This method does not completely capture all the voltage and timing characteristics of WPM, but using TCAD simulations in conjunction with this method should allow for a full analysis of WPM. As is, this measurement circuit can be used to for qualitative analysis of various well contacting schemes and transistor densities.

An alternative to using buffers as the voltage sensing circuitry would be differential amplifiers. Using an array of differential amplifiers as comparators, it would be possible to change the reference voltage of the differential amplifiers; this can find the exact well potential at the substrate voltage sensor contacts, rather than relying on just the buffers' single threshold switching point voltage. Of course, there are drawbacks to using differential amplifiers: design complexity and speed. Differential amplifiers are much larger than the buffer and require more area and time to layout. Also, a differential amplifier will be slower than a buffer. With proper circuit design, differential amplifiers maybe able to provide a more accurate analysis of WPM than buffers.

#### **Section 5.4 Design considerations**

The main issue with connecting the substrate voltage sensor contact to a probe pad to directly measure the potential off chip is the large of capacitance inherent to the pad. This large capacitance would affect the WPM completely skewing the results. If it is possible the capacitive loading on the voltage sensor substrate contacts must be kept at a minimum. An array of transmission gates can be used to select which substrate contact is sampled at a particular point in time, shown in Fig. 37. The t-gates are able to disconnect the capacitance of the voltage sensor circuitry (the buffers in Fig. 37) from the well, thus reducing the capacitive loading that can affect the WPM. The loading capacitance associated with voltage sensor circuitry is usually gate capacitance and be on the order of 1fF for 90nm bulk CMOS; capacitive loading of an off t-gate can be an order of magnitude lower than the gate capacitance. For sensitive measurements where the WPM is sensitive to capacitance, it is important to reduce capacitive loading on the substrate voltage sensor contacts.



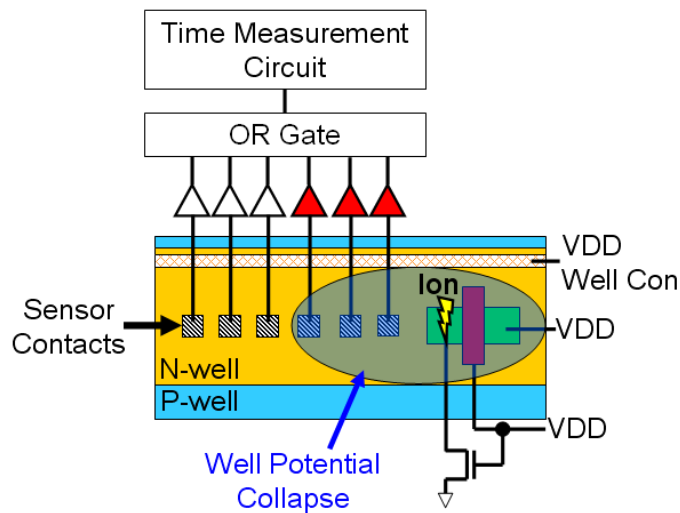
**Fig. 37. An array of transmission gates (t-gates) can be used to select which substrate contact is sampled at a given point in time. The transmission gates can disconnect the capacitance of specific buffers, thus reducing the amount of affecting the WPM.**

## Section 5.5 Implementations and Future Work

This circuit has been constructed in AMI 0.5um and TSMC 90nm bulk CMOS technologies nodes. Unfortunately, when constructing the circuit in 90nm at the schematic level the p-well and n-well sensory circuits were wired incorrectly and the circuit would not operate so no test data could be gathered on the circuit. The 0.5um circuit is schematically operational, but no has been obtained at this time. Currently, we are waiting for test time to become available at the Naval Research Laboratory (NRL). Space has been reserved to implement this circuit in TSMC 28nm Bulk CMOS.

Another test is in the design phase for future designs that would allow us to capture the maximum duration of the WPM. Fig. 38 shows an example of using a time measurement circuit (similar to the SET measurement circuit in [22]) to measure the maximum duration of WPM. Using the substrate sensor contacts connected to buffers, the output of the buffers are connected to an OR gate (or similar OR structure) and connected to a time measurement circuit. During the WPM, the sensor contacts located within WPM area will cause a pulse to be sent through the time measurement circuit. The pulse duration will coincide with the time it takes for all of the

potential to be restored at all the contacts in the WPM area. The pulse is stored in a series of latches that can be serially shifted off chip and analyzed to get the duration in pico-seconds.



**Fig. 38. Illustration of a circuit to measure the WPM maximum duration. The time measurement circuit uses a similar design that is used in [20].**

The above circuits have focused on structures for laser experiments. To capture the WPM spatial extent during broad-beam heavy ions test, the test structure needs to have a larger target well area and more complex detection circuitry with an area much smaller than the target well area or at least less vulnerable than the target well area. Fig. 39 shows that using multiple rows of n-wells and p-wells, substrate sensor contact buffers from the different n-wells can be connected to an OR gate to simultaneously detect WPM in all of the wells simultaneously, while reducing the amount of latch circuitry required to capture the well modulation.

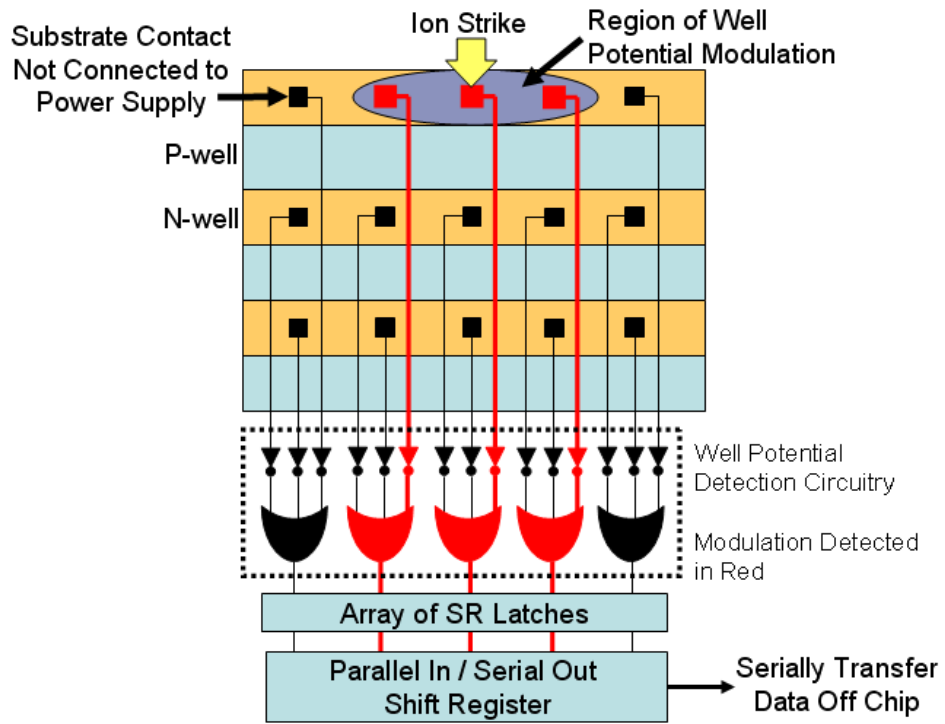


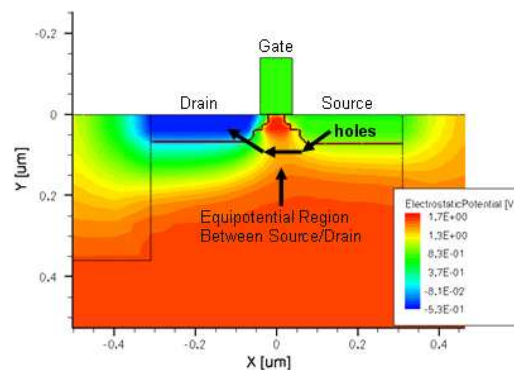
Fig. 39. Illustration of WPM spatial extent measurement circuit for broad-beam heavy ion testing.

## Chapter VI

### SE RESPONSE OF ANTI-PUNCH-THROUGH IMPANTS

#### Section 6.1 Overview

As technology scaling progresses, leakage current in the substrate region between the source and drain of MOSFET transistors can increase from one technology node to the next. This increase in leakage current is directly affected by decreasing channel lengths. A current path is formed in the substrate below the control of the transistor's gate when the source and drain depletion regions merge (known as punch through), shown in Fig. 40.



**Fig. 40. Illustration of punch through in a PFET. Merging of the source and drain depletion regions in the substrate current leakage path.**

To mitigate punch-through leakage current, anti-punch-through (APT) implants are created by increasing the substrate doping concentration between the source and drain to prevent the merging of the two depletion regions. Various techniques are used to create APT implants: gate aligned, pocket halo, standard blanket, and step blanket implants as seen in Fig. 41.

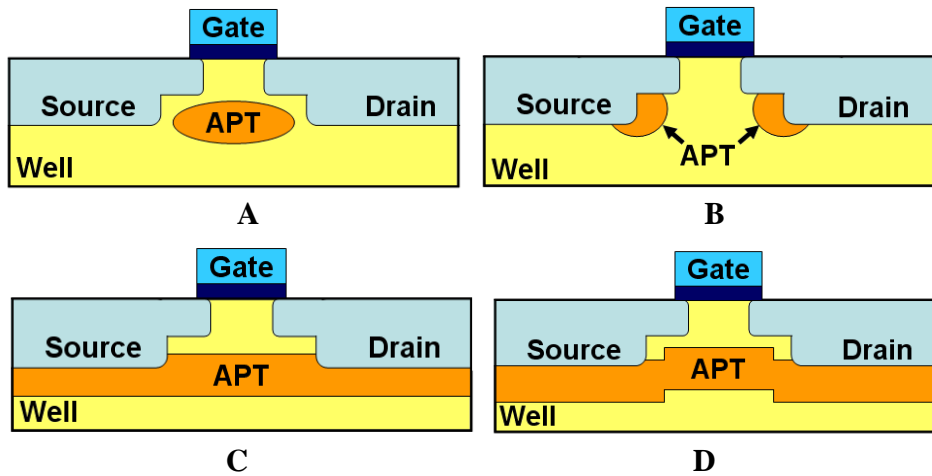


Fig. 41. Various APT implants. A) Gate aligned. B) Pocket Halo C) Standard Blanket D) Step Blanket

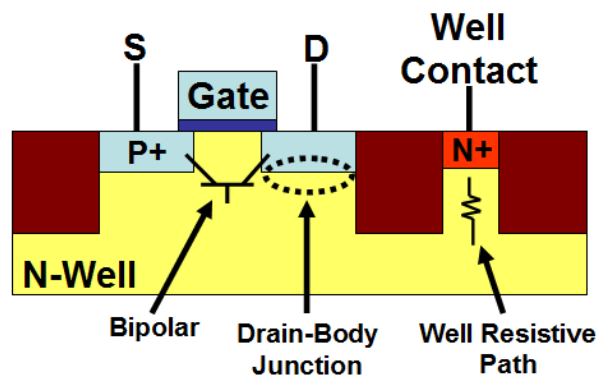


Fig. 42. SE mechanisms that can be affected by APT implants: bipolar induced current, drain-body junction recovery, and resistive path to well contact.

The type of APT implant used can have an affect on one or more SE recovery mechanisms. Fig. 42 illustrates the three mechanisms APT implants can affected, drain-body junction recovery, bipolar induced current, and the resistive path to the well contact. These implants can have an affect on the charge collected deposited by a single event, dependent on the LET of the incident particle and restoring current at the struck node. In this chapter, after examination of TCAD simulations of various implants, the SE mechanisms affected by APT implants are explained.



Lastly, by making alterations to the APT masking layer, the well potential recovery can be decreased leading to improved SE pulse width response.

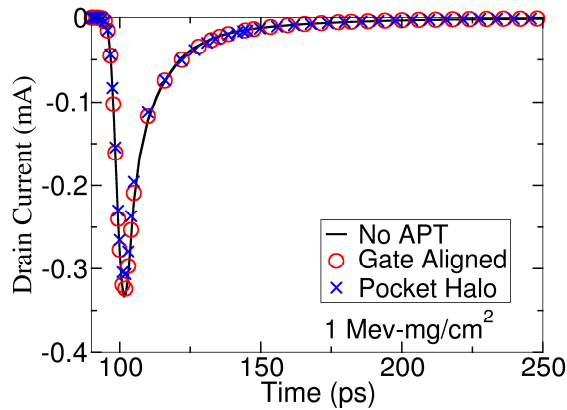
## **Section 6.2 Simulation Structures**

The results presented in this chapter use the 90nm models described previously as the baseline structure (referred to as No-APT transistor) for the TCAD structure and APT implants are added to the baseline structure. The results presented use APT implants to further reduce the subthreshold leakage current from baseline structure. This was done to ensure that the only variation between the different APT implants and the baseline structure was the APT implant. Hence APT variations could be analyzed for their effects on SE charge collection. The transistors are simulated with no load on the drain of the device, unless stated otherwise. No load condition is chosen so only the APT implants will affect the charge collection process. Also, for the different implants various ion energies are used to further characterize the response. Using the standard 90nm model as described, it is possible fully understand the affect the APT implants have on the SE response in CMOS transistors.

## **Section 6.3 Gate Area Implants**

Gate aligned and pocket halo implants are often used in modern processes due to lower penalties to source and drain diffusion capacitances compared to other implant types; these implants affect a small area of the transistor and have a small affect on the SE charge collection when compared to the baseline transistor. Fig. 43 shows there is no difference in drain currents during a single event between the transistor with gate aligned implants and the baseline transistor with no implants; the SE drain current shown is a strike through the drain of a pMOSFET transistor. The same response is seen for higher ion energies. Since these gate area implants (gate aligned and pocket implants) do not interact with a large area of the drain and source depletion regions, they do not change the drain-body response. In addition, the distance between the source and drain below the low doped diffusions, where the gate area implants are placed, is approximately 100nm; this distance is small enough that doping concentrations higher than those generally used for APT implants will not affect the SE bipolar response. The same response is seen in nMOSFET transistor with gate area implants versus the baseline transistor with no APT

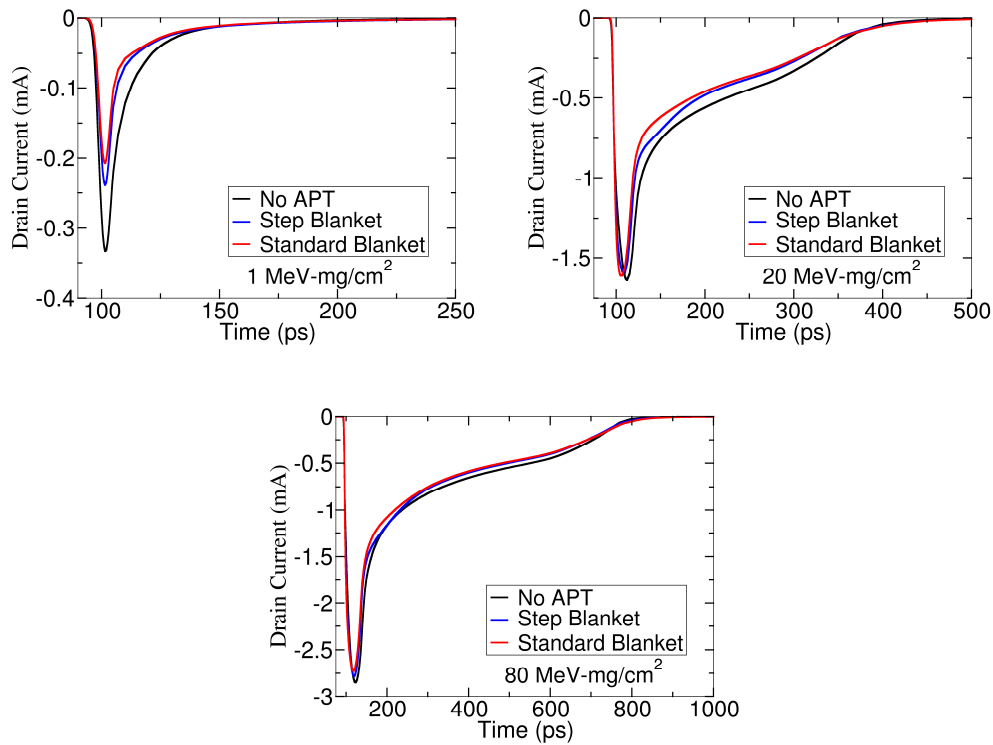
implant. After examining these results, it is easily seen that gate aligned and pocket halo implants do not significantly contribute to the SE response of the transistor.



**Fig. 43. pMOSFET drain currents resulting from a 1 MeV-mg/cm<sup>2</sup> strike. There is no significant difference in the currents among the 3 different transistor PT implants.**

### Section 6.4 Blanket Implants

Blanket APT implants are generally found in technology nodes larger than 100nm due mainly to the increased source and drain junction capacitances compared to the previously described gate area implants. Using the same masking layer used to create the wells, blanket implants can cover the entire well in the area of the substrate beneath the transistors; this allows the blanket implant to have a much larger affect on the SE response of the transistors when compared to gate area implants. For SE strikes in the drain of pMOSFET transistors with no load, Fig. 44 and Table 1 show the difference in drain currents and collected charge for various ion energies. The difference in collected charge of the transistors with blanket implants compared to the baseline transistor is much higher for lower ion energies. This is mainly due to drain-body junction recovery in the different transistors. The following section will discuss the how the blanket implants affect charge collection by affecting the recovery of the drain-body junction and bipolar induced current.



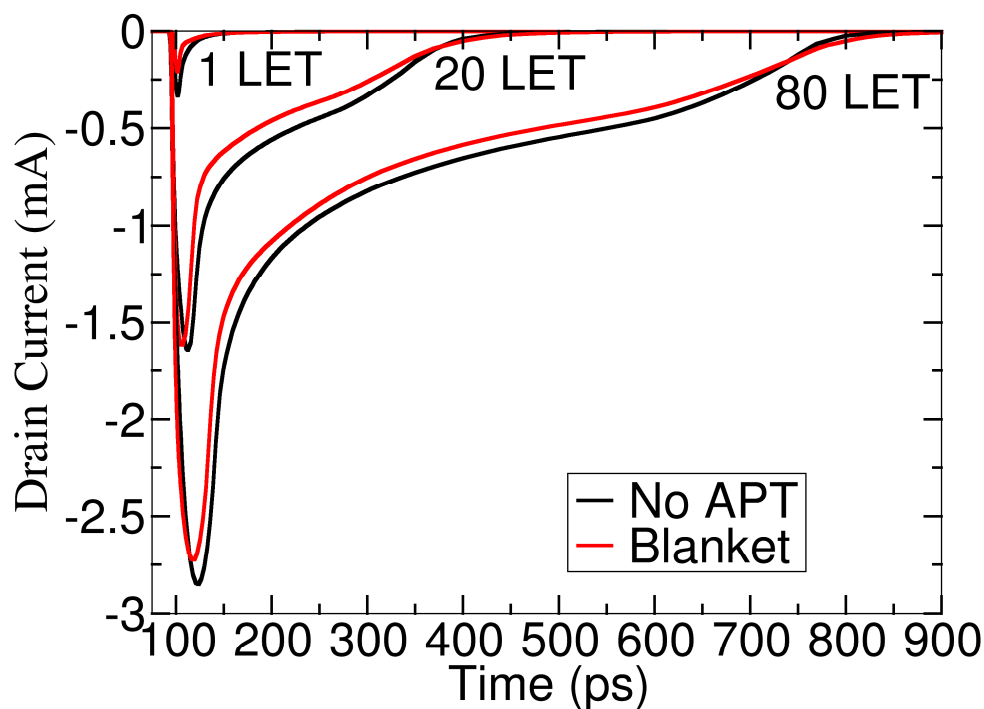
**Fig. 44. pMOSFET SE drain currents. Shown are strikes for 1, 20 , and 80 MeV-mg/cm<sup>2</sup>. For higher ion energies, the affect blanket implants have on the SE response becomes less compared to a transistor with no APT.**

**Table 1. pMOSFET total collected SE charge. As ion energies increase the difference in collected charge for a transistor with blanket implants become less compared to a transistor with no APT implant.**

LET	Collected charge (fC)		% difference
	Blanket	No APT	
1	3.074	4.73	35
10	51.25	64.92	21
20	128.84	152.09	15
80	474.4	515.19	8

For the drain-body junction to recover from a single event, the charge deposited in the depletion region must return to concentrations levels comparable to that of the doping concentrations in those regions [23]; this allows for the potentials and electric fields to be returned to their pre-strike equilibrium conditions. The higher doping concentration and smaller depletion region caused by the blanket implants allow for faster recovery of the junction when

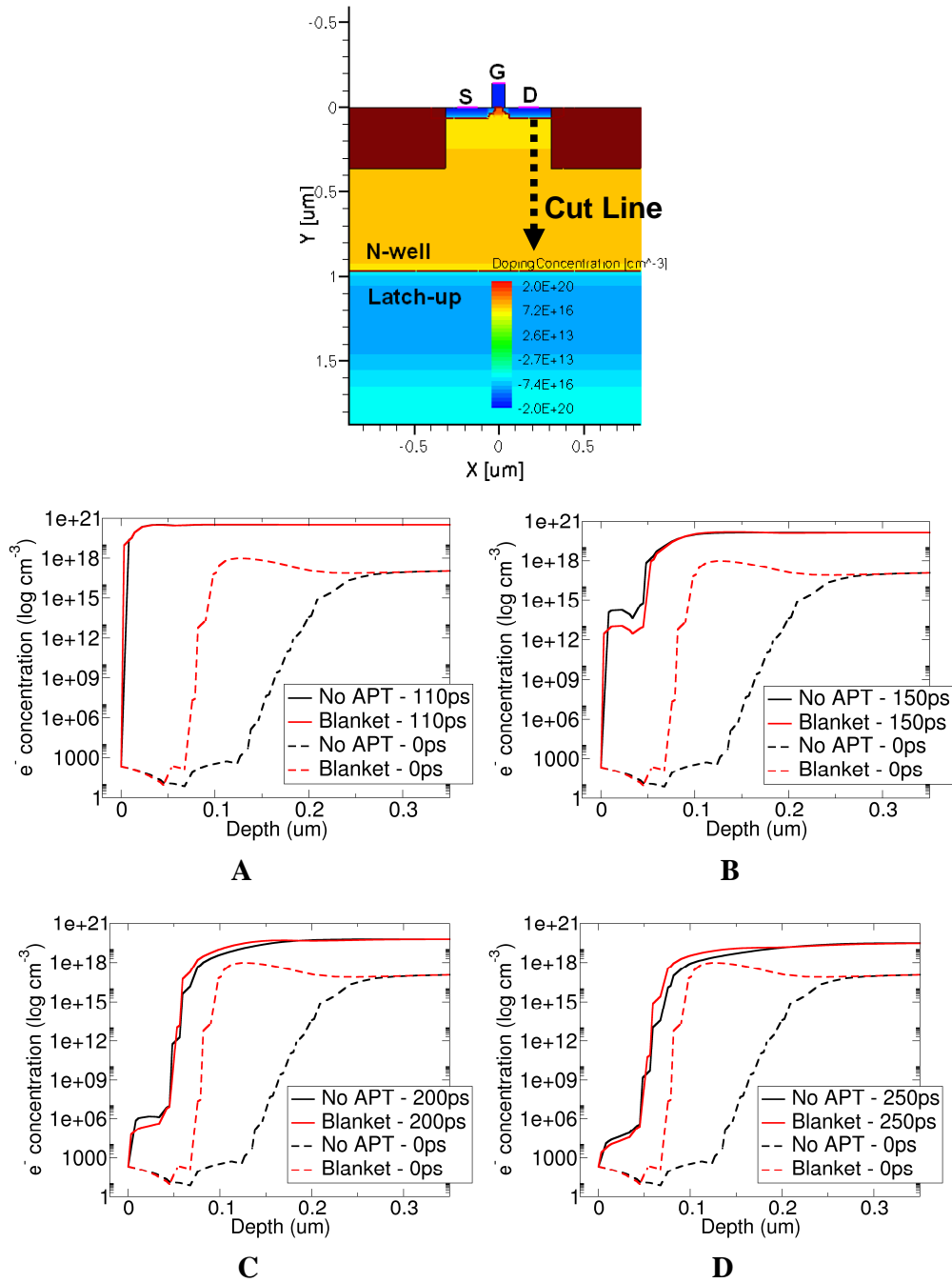
compared to the baseline transistor. Fig. 45 shows currents for pMOSFET strikes with no load for various ion energies on the standard blanket APT implant and baseline transistor. A transistor with a blanket implant produces a lower drain current, for almost the entire duration of SE, when



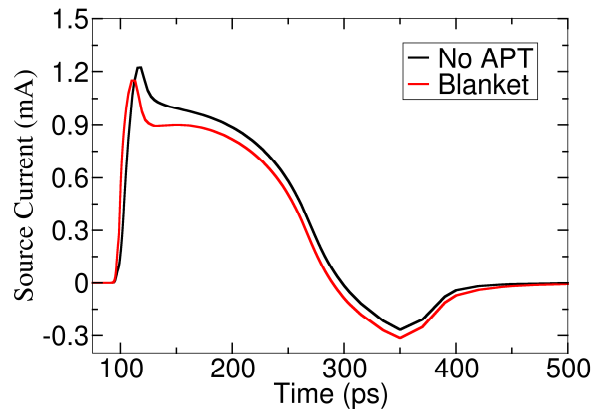
**Fig. 45. Drain currents for SE strikes of pMOSFETs with no load. Blanket implants allow for slightly faster recovery of the junction resulting in less drain current. LET units in MeV-cm<sup>2</sup>/mg.**

compared to a transistor with no APT. This attributed to the higher doping concentrations of the blanket APT near the drain junction. Fig. 46 shows the electron concentration at different times after the SE occurs. The electron concentration shortly after the strike more closely resembles the pre-strike electron concentration in the transistor with the blanket implant than the transistor with no APT; this allows the transistor with the APT implant to recover more quickly than the no

APT baseline transistor. The blanket implants become less effective for higher energy ions because the blanket implants can only become effective when deposited excess carriers equal doping concentrations in the depletion region. As the drain-body junction recovers, the potential near the device returns to the pre-strike equilibrium potential, thus the source injected current becomes smaller. Since the transistor with the blanket implant recovers more quickly than the baseline transistor with no APT, the source injected current for the transistor with the blanket implant will be less, shown in Fig. 47. Lower source injected current into the drain of the transistor decreases the amount of charge collected by the drain. A similar response is seen for nMOSFETs, but a significant decrease in drain collected charge is only seen for ion energies less than  $5 \text{ MeV}\cdot\text{mg}/\text{cm}^2$ ; in these simulations, the source-body junction is more perturbed and more bipolar induced current is created by the confined n-well that contains the pMOSFET transistors, compared to the nMOSFETs contained in a large p-well and p-substrate. Combining the faster drain-body junction recovery and the decrease in bipolar injected current compared to the baseline transistor with no APT, transistors with blanket implants can collect up to 30% less charge for low ion energies.



**Fig. 46.** 1D cut lines through the drain of a pMOSFET showing the electron concentration during an 80 MeV-mg/cm<sup>2</sup> strike. A is at 110ps, B is at 150ps, C is at 200ps, D is at 250ps. The electron concentration of the transistor with the APT implant is much closer to the pre-strike electron concentration.



**Fig. 47. pFET source injected currents from a 20 MeV-mg/cm<sup>2</sup> SE. Due to the faster recovery of the junction for the transistor with the blanket APT there is a lower source injected current.**

### **Section 6.5 Altering APT Implant Masking Layer to Increase Conductivity to the Well Contact**

The previous results were obtained by creating the APT implants in the area solely beneath the transistor. This was done to capture how the APT affects the transistor locally. By altering the masking layer of an APT implant, the APT implant can increase the doping concentration in the substrate in the region beneath the well contact, seen in Fig. 48; this can increase the conductivity to the well contact, thus decreasing the amount of time for the potential of a well to recover after a single event. Decreasing the well recovery time will decrease the SE bipolar action leading to less collected charge and smaller SET pulse widths [14]. Fig. 49 shows for a pMOSFET strike by 40 MeV-mg/cm<sup>2</sup> ion in an inverter that an additional decrease in pulse width is possible for blanket implants. This reduction in SET pulse width is possible with any type of APT implant if the masking layer allows the APT ion implantation to be deposited in this region.

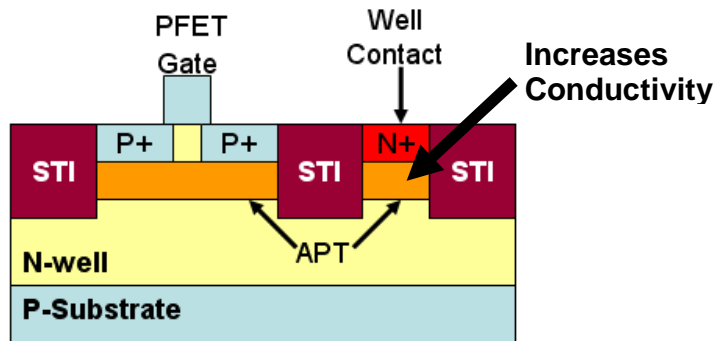


Fig. 48. Adjusting the APT implant masking layer can allow increased doping in the substrate below the well contact, increasing conductivity in the region

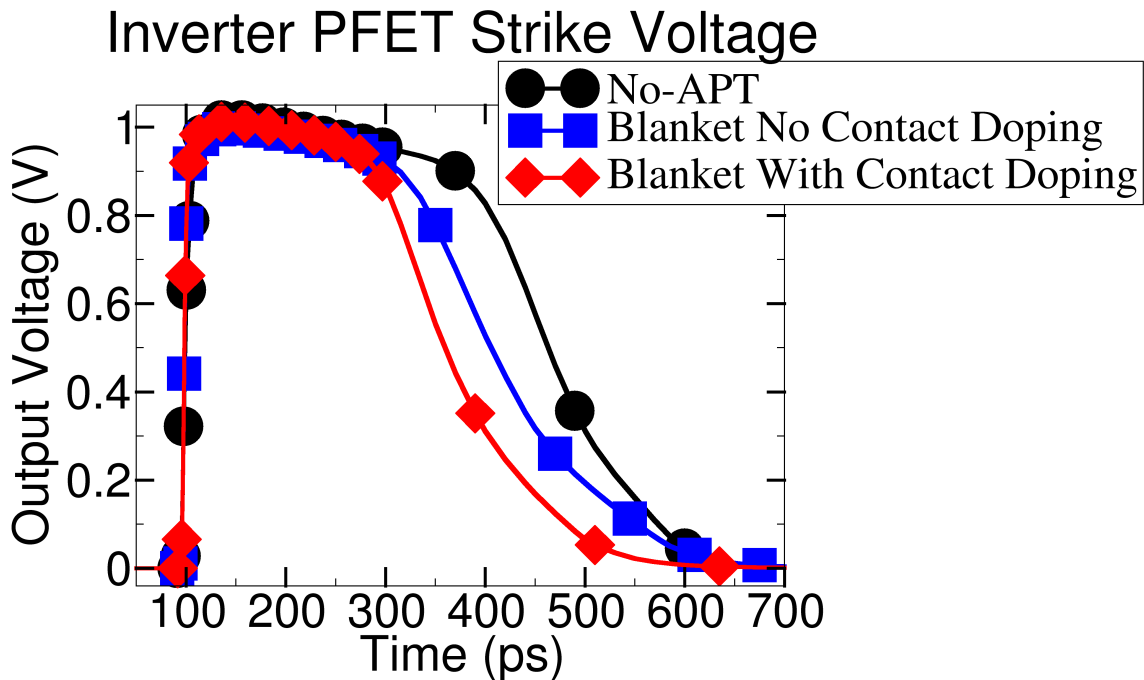


Fig. 49. pMOSFET strike voltage transients in an inverter from a 40 MeV-mg/cm<sup>2</sup> ion. By depositing the APT implant in the region below the well contact, a noticeable decrease can be obtained in SET pulse widths.

### Section 6.6 Conclusion

It is shown that APT implants can have a limited effect on SE charge collection. Gate area implants, like pocket halo implants, have no effect on the SE bipolar charge collection. Blanket implants can larger impact on drift collected charge for LET values lower than 20 MeV-



$\text{cm}^2/\text{mg}$ . The blanket implants reduce the depth of the drain/source-body junction depletion regions thus reducing the amount of prompt drift collected charge when compared to a MOSFET with no APT implant. For LET values higher than  $20 \text{ MeV}\text{-cm}^2/\text{mg}$  the excess carrier concentration exceeds the doping concentration of the blanket implant degrading its ability to shield charge from being collected by the drain. Thus, blanket implants may be more beneficial for radiation applications than gate area implants.

As technology scaling progresses, it is important to reduce parasitic capacitances from source/drain junctions. Simulations show that blanket implants can increase junction capacitances by a factor of 6, possibly more, compared to gate area implants. This is due to blanket implants constricting the depletion region to a smaller area under the source/drain diffusions than the gate area implants. If speed and power are a higher priority than radiation hardness, gate area implants will be more favorable than blanket implants

By utilizing the APT implant masking layer, it is possible to improve conductivity to the well contact in the highly resistive region under the well contact. This can reduce SE bipolar charge collection and reduce WPM spatial extent and duration.

## Chapter VII

### CONCLUSION

Though the SE charge track does not change size as technologies scale, WPM spatial extent and duration will change as technology process evolve. WPM is one of the mechanisms behind the charge sharing process. It is important to understand WPM to fully understand pulse quenching and multiple-bit upsets. This work has shown that WPM response can be influenced by contact spacing and various technology parameters. Ultimately, any increases in resistance to the restoring current path to well supply rail will increase WPM spatial extent and duration.

To reduce WPM spatial extent and duration it is important to maintain a high conductivity to the well supply rail. Circuit and layout designers can greatly reduce WPM effects by using strip contacts as opposed to spaced contacts. Of course the use of strip contacts has a very large area penalty, but offers the needed reduction in WPM effects needed for radiation tolerant designs. Process engineers can design a process with a high well conductivity to decrease WPM effects. Higher well conductivity can be achieved by increasing well doping concentrations. Reducing the well depth can reduce WPM spatial extent, but can increase the WPM duration of the affected area. The p+ buried layer can reduce the amount of charge collected by the n-well from the substrate reducing WPM effects. One goal of technology scaling is to increase transistor density; as transistor densities increase, the higher concentration of transistors can limit WPM spatial extent while added diffusion capacitance can delay the spread of the WPM. Designers have many options to reduce the WPM spatial extent and duration at various levels of CMOS designs.

APT implants are another form of well engineering focused on reducing subthreshold leakage and parasitic capacitances. Gate area implants are more prevalent in new technology nodes and have no affect on SE charge collection. Older technologies use blanket implants. Blanket implants can affect SE charge collection by reducing the depth of the depletion region into the substrate. Also, by utilizing the APT implant layer, it is possible to increase the conductivity of the well to the well contact, reducing WPM effects.

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