RELIABILITY AND IRRADIATION EFFECTS OF 4H-SiC MOS DEVICES

By

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This is my favorite part to write. To all of those, who are happy to see this happen, Cheers!

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To my grandparents.

TABLE OF CONTENTS

Page

LIST OF FIGURES

Figure Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

In recent years, SiC MOS devices have received much attention in high-power, high frequency and radiation-hardened applications. Owing to the compatibility with Si technology, SiC has inherent advantages over many other advanced materials. The 4H-SiC polytype is of particular interest because of its wider band gap, greater breakdown field, and enhanced bulk electron mobility [1],[2],[3],[4]. Although 4H-SiC offers advantages of high electric breakdown field, high thermal conductivity, and high-saturated electron drift velocity, limitations to oxide reliability and channel mobility are blocking the way to commercialization of MOS devices [5],[6]. In this work, we investigate various reliability issues for 4H-SiC MOS capacitors and MOSFETs. Devices are characterized electrically and then subjected to electric stress at various temperatures. Bias-temperature instabilities are characterized. Devices are irradiated and annealed to evaluate their potential for application in a space environment. 1/*f* noise measurements are employed to help understand the defects that affect the reliability and radiation response of SiC MOS devices.

SiC Polytypes

With respect to device processing and especially compatibility with Si MOS manufacturing, SiC technology is currently the most mature among all the wide-band gap semiconductor materials, like GaN, and diamond. Cree launched the industry's first commercial SiC high-power MOSFET in 2011 [7]. SiC has several polytypes determined by the Si-C bi-layer sequence in the crystal structure, with significantly different electronic properties, as summarized in Table 1.1 [8],[9]. Among these polytypes, 3C-SiC does not have a proper technology for the growth of the bulk crystals. Up to now, it is quite challenging to make available large 3C-SiC seeds and stabilize the crystal for the high temperatures involved in the physical vapor transport (PVT) [10]. Between 4H-SiC and 6H-SiC, the most important difference is that 4H-SiC has an electron mobility that is approximately double that of 6H-SiC. In addition, the 4H-SiC polytype is favored

because of its wider band gap in present technology development. At room temperature, the theoretical barrier of electron injection from SiO_2 for 4H-SiC is 2.7 eV. The strong temperature dependence of Fowler-Nordheim (FN) current in 4H-SiC could be a concern for applications at very high temperature [11]. As temperature is increased to 325 ℃, the effective barrier height for electron injection decreases to be ~2.1 eV. The reduction of effective barrier height with temperature raises concerns about the long-term reliability of gate oxides in SiC devices that are used in high temperature applications [11].

However, the energy band diagram (Fig. 1) is considered optimal since the conduction band offset is equal to the valence band offset [1],[11],[12]. Due to this property, the leakage current in the SiC MOS structures is acceptably low, even at elevated temperatures [13].

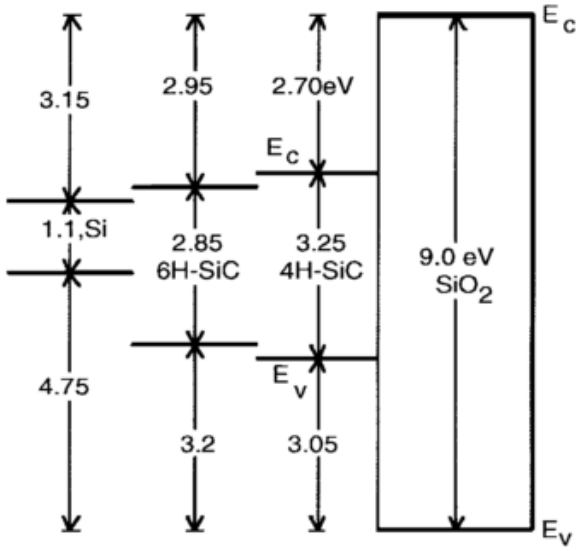


Fig. 1 Energy band diagrams of Si, 6H-SiC, 4H-SiC, and SiO_2 illustrating barrier heights for F-N electron injection from semiconductor into the gate oxide (after [1],[11]).

Table 1.1

Property	*Si*	*4H-SiC*	*6H-SiC*	*3C-SiC*
Band gap (eV)	1.1	3.26	3.0	2.2
Critical Field (MV cm^{-1})	0.3	2.0	2.4	3
Saturation carrier velocity ($\times 10^7$ cm s^{-1})	1.0	2.0	2.0	2.5
Electron mobility (cm^2 V^{-1} s^{-1})	1350	850	370	1000
Thermal conductivity (W cm^{-1} s^{-1})	1.5	4.5	4.5	4.9

Oxidization of SiC

The fact that SiC can be converted to SiO_2 under the influence of oxidizing agents is a unique advantage of SiC. As compared with most other compound semiconductors, SiC can be oxidized to form stoichiometric SiO_2. The process of oxidation is very similar to the oxidation of Si. However, the oxidation of SiC is more complicated, since it requires the removal of C in the form of CO, shown in the reaction below:

$$SiC + 1.5\ O_2 = SiO_2 + CO$$

The oxidation of Si at the interface of SiO_2/SiC is shown in Fig. 2 [14]. Starting with a locally abrupt SiO_2/SiC interface in Fig. 2a, the new O atom arrives, removes a C atom and then forms two Si-O-Si bridges, as shown in Fig. 2c. The energy barriers for these processes are expected to be large, due to the slow rate-limiting oxidation of SiC, compared to Si.

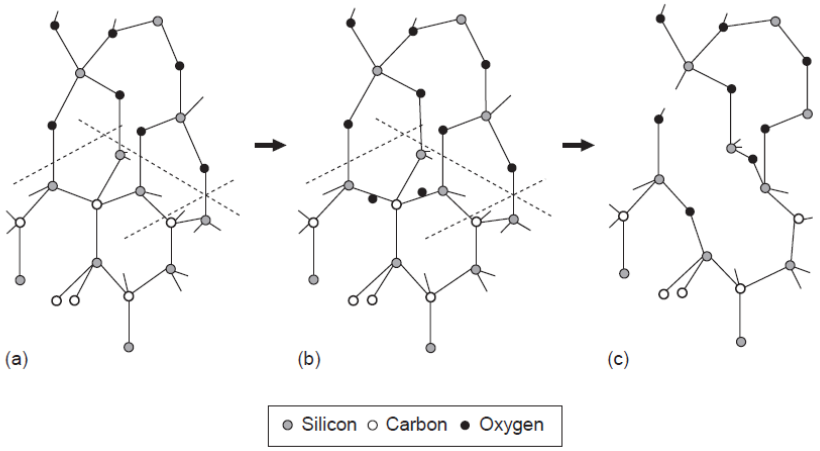


Fig. 2. Atomic-scale steps for oxidation of SiC: (a) an initially abrupt interface region, (b) two O atoms arrive at the interface as shown, and (c) a C atom is ejected and two Si-O-Si bridges are formed (after [14]).

Passivation of 4H-SiC/SiO_2 interfaces

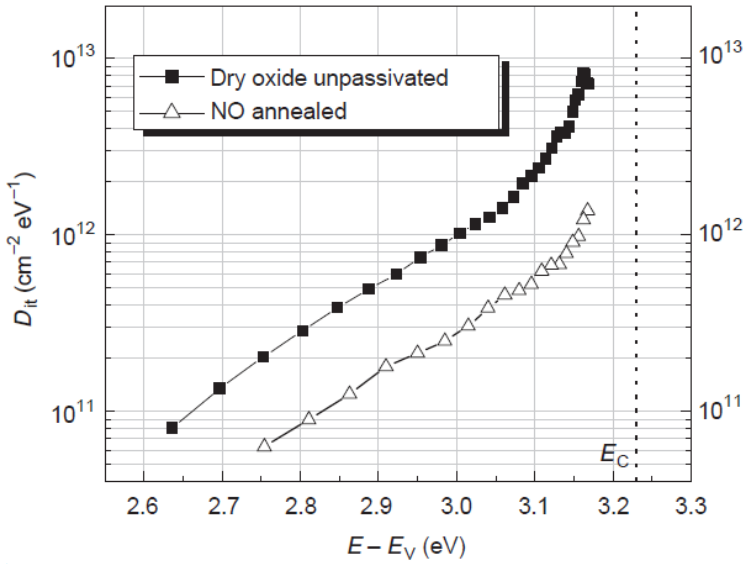
Various attempts have been made to passivate the traps at the 4H-SiC/SiO_2 interface, including a broad exploration of various oxidation and post-oxidation annealing procedures, like wet oxidation [15], re-oxidation [16], and post-oxidation anneals in different ambients, like H_2 [17], NO [18] and N_2O [19]. To date, the most effective method among the passivation schemes involves nitridation processing [20]. The effects

of hydrogen on the 4H-SiC/SiO_2 interfaces have also been investigated, as hydrogen annealing is an important passivation technique for traditional Si MOS technologies.

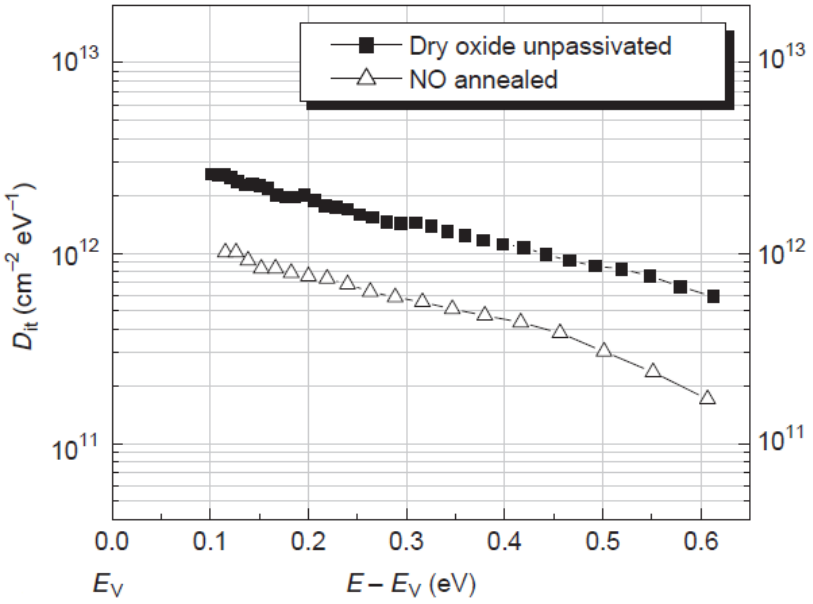
Effects of nitric oxide annealing on SiC/SiO_2 interface traps

Post-oxidation annealing in NO was reported by Chung et al. [21], who found that an order of magnitude reduction in interface trap density can be achieved. D_{it} profiles near the band edge are plotted in Figs. 3(a) and (b), showing a significant reduction of traps for post-oxidation NO treatment [22],[23]. The D_{it} profiles in Fig. 3(a) and (b) were obtained via high-low *C-V* measurement at room temperature on *n*-type and *p*-type 4H-SiC capacitors. Traps located in the oxide and at the SiO_2/SiC interface can degrade the transistor mobility significantly, relative to its bulk value [20]. A substantial improvement of the inversion channel mobility was reported in [22],[24]-[26] for lateral n-channel MOSFETs fabricated with standard thermal oxidation techniques following the passivation anneals. A reduction in D_{it} with NO post-oxidation annealing is observed for several different types of oxidation methods [23].

The mechanisms for nitridation passivation involve [27]: (1) creation of strong Si ≡N bonds that passivate dangling Si bonds and replace Si-O bonds, and (2) removal of carbon clusters. Based on the quantitative observation of C-C graphitization and the presence of complex compounds CO_xSi_y at the interface, the density of structural defects near or at the interface of SiC/SiO_2 is significantly reduced by NO treatment.



(a)



(b)

Fig. 3. The profile of D_{it} (a) near the valence band for *n*-type and (b) near the conduction band for *p*-type 4H-SiC (after [21]).

Effects of hydrogen annealing on SiC/SiO$_2$ interface traps

Hydrogen passivation of interface traps via various device-processing techniques has been well known for Si technology [28],[29]. However, under conditions that lead to interface trap reduction in Si MOS devices, hydrogen annealing is not as effective at SiO_2/4H-SiC interfaces [30]. High temperature annealing in hydrogen has been reported to be more effective for interface passivation via atomic hydrogen than with molecular hydrogen [29],[30]. H_2 can be cracked into atomic H after passing through a transition metal layer, such as Pt. The atomic H terminates the dangling bonds of Si and C atoms on the SiC interface. The treatment of nitridation followed by hydrogenation yields complementary passivation and a remarkable reduction of D_{it} [32]. Unfortunately, some of these techniques are not easily incorporated into a full MOS device processing sequence.

Overview of the thesis

This PhD dissertation research reports the results of characterizing and identifying the defects responsible for the post-rad degradation and long-term reliability issues in 4H-SiC MOSFETs. The research effort described in this thesis is organized as follows: 1) Chapter I provides the introduction and motivation for this work. 2) Chapter II describes the background for this work. 3) Chapter III details the experimental set-up and device information, including SiC *n*- and *p*-substrate capacitors and SiC *n*MOSFETs. 4) Chapter IV describes the combined radiation response and reliability of optimized SiC MOS devices. A 10-keV X-ray irradiator was used as the radiation source. 5) Chapter V summarizes the bias temperature instabilities in SiC MOS *n*- and *p*-substrate capacitors and *n*MOSFETs. 6) Chapter VI investigates the 1/*f* noise of SiC nMOSFETs as a function of gate voltage, temperature, with irradiation and after irradiation. The temperature dependence of threshold voltage is also studied using TCAD simulation. 7) Chapter VII provides the summary and conclusions of this work.

CHAPTER II

BACKGROUND

Radiation response of 4H-SiC MOSFETs

For MOS devices, the oxide is the most sensitive part for ionizing radiation. During exposure to ionizing radiation, electron-hole pairs are generated [33],[34],[35]. A percentage of the generated electrons and holes recombine quickly. The electric field in the oxide can separate the remaining carriers, driving electrons and holes in opposite directions. Most of the electrons will be swept out due to their relatively high mobility in SiO_2. Holes, on the other hand, transport much more slowly through SiO_2. Over a period of time, the holes can migrate to the SiO_2/Si interface under positive bias and then either recombine with injected electrons from the silicon or be trapped forming a positive oxide-trap charge. The hydrogen ions can react with Si-H bonds at the SiO_2/Si interface to form interface traps. The process is schematically shown in Fig. 4 [34]. Radiation-induced oxide trapped charge and interface traps are a significant concern for MOS transistors, particularly because they affect the operation parameters of the devices.

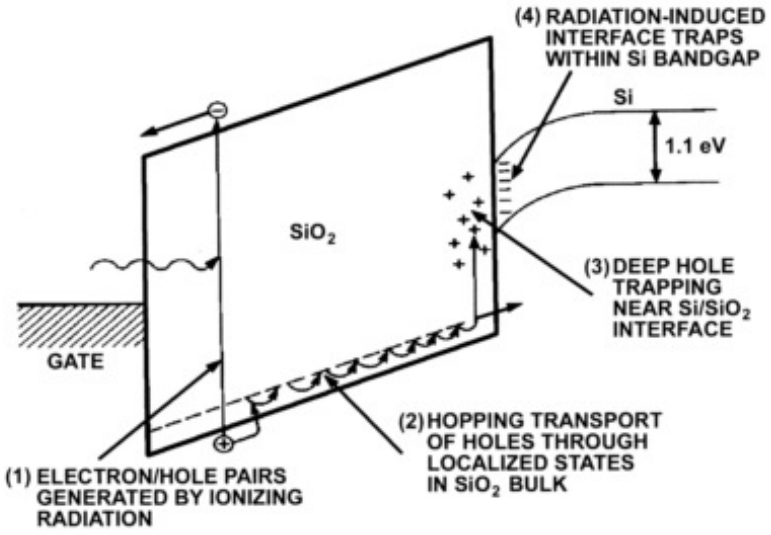


Fig. 4. Schematic energy band diagram for a *n*MOS structure under positive bias, indicating physical processes underlying radiation response (after [34]).

The interface traps for Si MOS devices are assumed to be charge neutral when the Fermi level is at midgap [36]. In this case the midgap voltage shift (ΔV_{mg}) is presumed to be entirely due to the trapped oxide charges. The interface traps change the slope of the capacitance-voltage characteristics or current-voltage characteristics. In the upper half of the silicon band gap, interface traps are acceptor-like, while in the lower half of the silicon band gap (below midgap) they are donor-like. Interface traps usually shift threshold voltage positively in *n*-channel MOSFETs and negatively in *p*-channel MOSFETs. Oxide-trap charges shift threshold voltage negatively for both *n*- and *p*-channel MOSFETs.

The radiation response of 4H-SiC MOSFETs with nitrided oxides has been investigated in preliminary studies [37],[38],[39]. The performance/reliability trade-off [40],[6] for 4H-SiC devices is typically more severe than for Si-based MOS technologies. For example, the radiation-induced oxide trap density for passivated and unpassivated SiO_2/SiC gate oxides are compared with a buried oxide from SOI technology in Fig. 5 [34]. At 1 Mrad(SiO_2), the charge trapping in both SiO_2/SiC structures is much larger than that in the SOI buried oxides.

A detailed study on nitride and non-nitrided SiC MOS devices was performed by Dixit in [38]. At ~10 Mrad(SiO_2) the midgap voltage shift for SiC MOS capacitors with nitrided oxides is observed to be ~ −10 V in Fig. 6. Even at 10 Mrad(SiO_2), the charge trapping does not appear to saturate. It is possible that the absence of charge compensation via interface trap build-up shows up as an enhanced midgap voltage shift [38]. In Fig. 7, the midgap voltage shift is plotted as a function of total dose for devices biased at ± 0.8 MV/cm during irradiation. Higher shifts are observed at positive gate bias as the holes are pushed toward the oxide/SiC interface. Both 3C- and 4H-SiC substrate devices, with SiO_2 gate dielectrics, were examined for charge trapping properties after irradiation. 3C-SiC devices exhibited more charge trapping than 4H-SiC due to the greater nitrogen content at the interface. No significant generation of interface traps was observed for devices studied in [37].

Before this work, the combined radiation response and reliability of SiC MOS devices had not been studied in detail. To understand the long-term performance of these

devices in space, we evaluated their combined reliability and radiation responses. We will show results from our work on this combined response in chapter III.

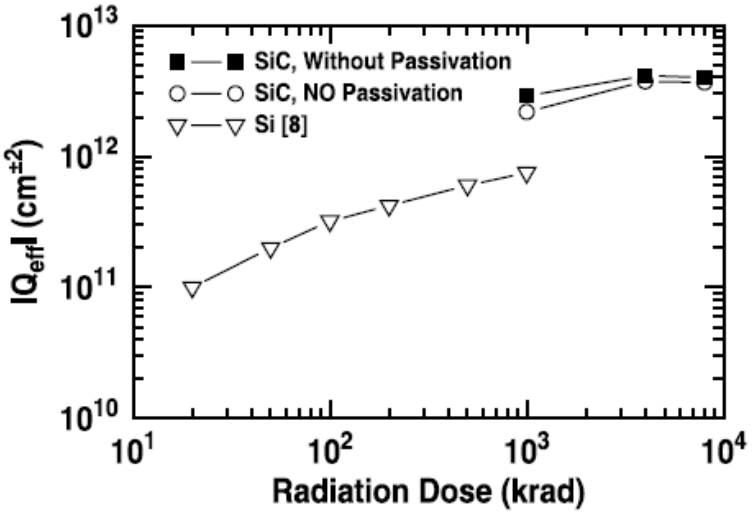


Fig. 5. Measured effective oxide trap charge Q_{eff} of both passivated and unpassivated SiO_2/SiC, compared to values for Si SOI technology, as a function of radiation dose (after [34]).

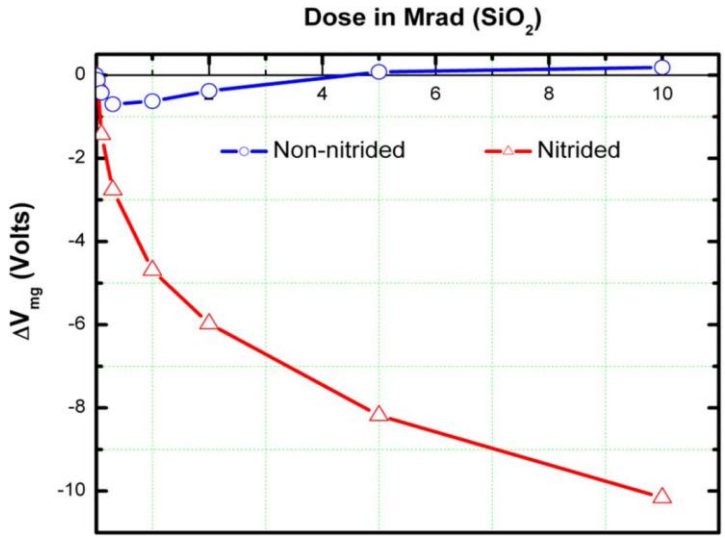


Fig. 6. Midgap voltage shift as a function of dose in Mrad(SiO_2) for nitrided and non-nitrided samples positively biased at 1.5 MV/cm (after [38]).

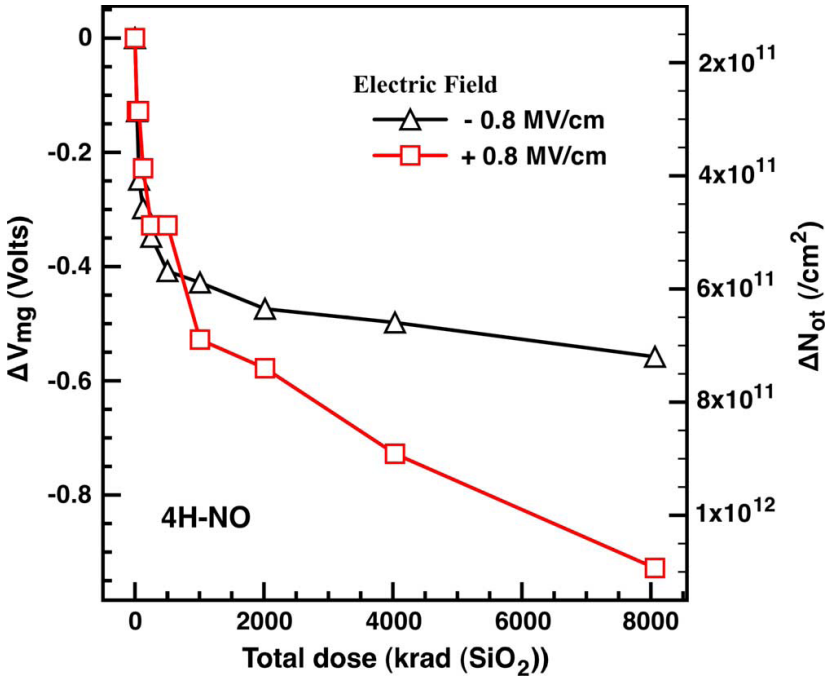


Fig. 7. Midgap voltage shift as a function of X-ray dose for 4H-SiC MOS capacitors with oxides grown in NO (after [37]).

Bias temperature instabilities for 4H-SiC MOS devices

Bias temperature instabilities (BTIs) are a long-term reliability issue for modern MOS devices with low operation voltage [41]. BTIs are associated with the generation of oxide and interface trap charge at the Si/dielectric interface, when biases are applied to the gate for a long time and/or at elevated temperatures [42]. The typical temperature during stress ranges from 50 ℃ to 300 ℃ with oxide electric fields below 6 MV/cm [43]. It is believed for the case of the Si/SiO_2 system that the release of hydrogen from passivated interfacial Si dangling bonds under BTI stress can lead to interface-trap buildup and oxide-trap charge [44] at low applied electric fields. At higher stressing fields, charge trapping can dominate the observed BTI for Si MOS devices [45],[46]. Many factors can impact NBTI sensitivity, such as chemical species (hydrogen, nitrogen, water, and boron), which could be introduced into the devices during the processing, temperature, the processing of the oxide layer, etc. Most of the effects modify either the reaction dynamics or influence the rate of BTIs. Moreover, as discussed before, in the case of SiC/SiO_2, hydrogen processing is less effective in reducing the interface trap

density than it is for the Si/SiO_2 interface [17]. Because of these reasons, the mechanisms of BTI in SiC MOS devices can differ significantly from those in Si MOS devices.

Both 6H-SiC MOS capacitors [47] and 4H-SiC capacitors [48] have been characterized to find evidence of NBTI for *n*-type substrates. Dangling bonds at the interface of SiO_2/SiC are energetically deep and these states contribute to the fixed charges. At temperatures above 600 K, additional negative/positive fixed charges are generated in an *p*- and *n*-substrate SiC/SiO_2 MOS capacitors by the degradation process [47] in Fig. 8. Also, a dramatic decrease in threshold voltage V_T instability following a NO anneal suggests that the oxide and interface traps may be indistinguishable for some measurements. Fig. 9 shows a linear-with-log-stress-time extrapolation of bias-stress-induced threshold-voltage instability data versus stress time to early times and zero instability for a SiC *n*MOSFET. It is consistent with electrons tunneling into and out of oxide traps spatially distributed into the oxide from the SiC/SiO_2 interface [49].

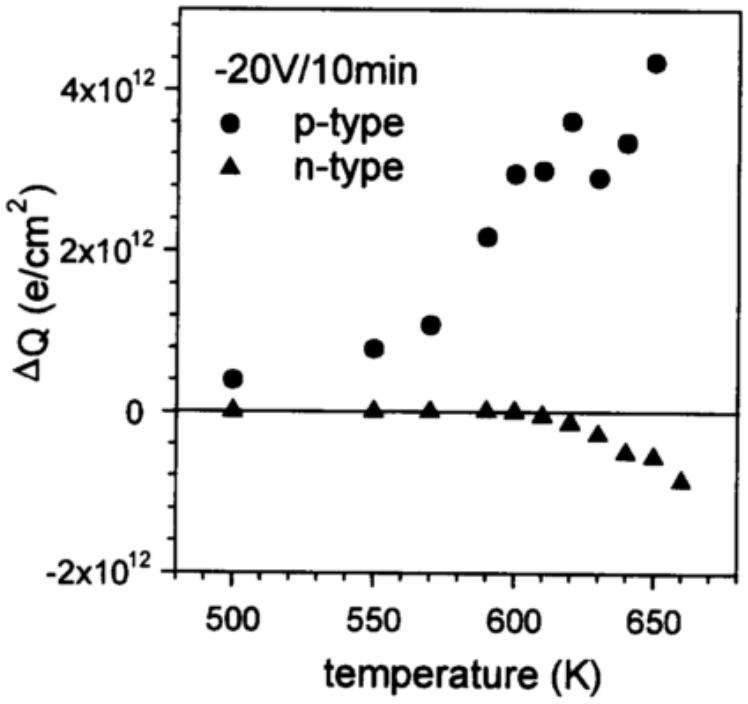


Fig. 8. Comparison of the generated charges for an *n* and *p*-type substrate SiC MOS capacitor as a function of temperature (*T*) (after [43]).

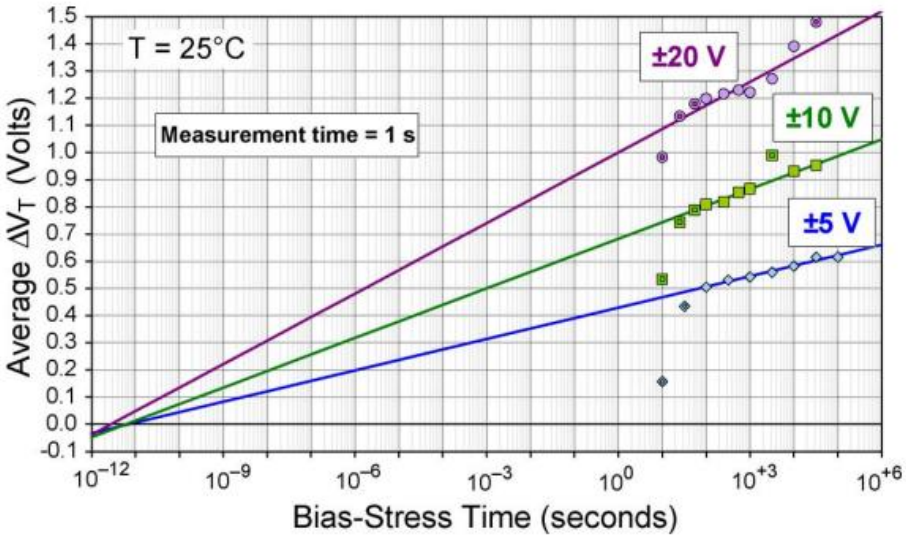


Fig. 9. The bias-stress-induced threshold voltage instability versus individual stress time as a function of biases during stress for a linear SiC *n*MOSFET (after [49]).

1/f noise measurements for 4H-SiC devices

Low frequency noise measurements have been employed as a sensitive probe of the impurities and defects in MOS structures [46],[47],[52],[33]. It has been widely accepted that 1/*f* noise is associated with the capture and emission of charge carriers from trap sites in the oxide, at or near the Si/SiO_2 interface. Fluctuations in the oxide-trap charge couple to the channel, directly through fluctuations in the inversion layer charge density, and indirectly through fluctuations in scattering associated with fluctuations in trap occupancy. The other mechanism, carrier-mobility fluctuations are described as fluctuations in carrier mobility due to phonon scattering. In this thesis, we generally use carrier-number fluctuation models to characterize MOS 1/*f* noise, assuming that any scattering due to trapped carriers produces a less significant fluctuation in mobility. The dependence of the excess noise on frequency, drain voltage, and gate voltage in MOSFETs typically follows [52]:

$$S_{vd}(f, V_d, V_g) = \frac{K}{f^a} \frac{V_d^2}{(V_g - V_t)^b} \qquad (1)$$

$$K = S_{Vd} f (V_g - V_{th})^2 V_d^{-2} \qquad (2)$$

where K is the normalized noise magnitude, and α and β are phenomenological fitting parameters that reflect the observed frequency dependence and gate-voltage dependence, respectively. In this model, the traps that exchange directly charges with the conducting channel are assumed to exist uniformly in the energy band gap. For a MOS transistor operated in strong inversion, the fluctuations in the trapped charge will result in a fluctuation in the effective gate voltage. For a fixed $V_{d,}$ β equals 2 and α equals 1 for purely number fluctuation noise with a uniform distribution of defects within the band gap. If not, $D_t(E_f)$ is considered to be non-uniform within the bandgap [51][52][33].

Previous work related temperature dependence to the nature and energy structure of the defects that cause the noise [53]. The frequency and temperature dependence of the noise are related via

$$a(w,T) = 1 - \frac{1}{\ln(wt_0)}\left(\frac{\partial \ln S(w,T)}{\partial \ln T} - 1\right) \qquad (3)$$

Here the frequency exponent α is defined as $\alpha = -\frac{\partial lnS}{\partial f}$. The conditions [53],[54] for Eq. (4) to be valid are:

1. The noise is due to random processes with thermally activated characteristic times. The distribution of activation energies $D(E_0)$ varies slowly over any interval, $\Delta E \cong kT$.
2. The attempt frequency $f_0 = 1/\tau_0$ is much larger than the frequency at which the noise is measured.
3. The total noise is independent of temperature. No new defects are created or existing defects annealed during the noise measurements.

In particular, if the $1/f$ noise is due to a thermally activated random process with a distribution of activation energies, and $D(E_0)$ varies slowly over any range $\Delta E \sim k_B T$, the energy distribution of defects that cause the noise can be related to the noise power spectral density:

$$D(E_0) \mu \frac{w}{k_B T} S(w,T) \qquad (4)$$

where $\omega = 2\pi f$. The activation energy of the defect, $E_0 \approx -k_B T ln(\omega\tau_0)$, where τ_0 is the characteristic time for the defect.

It was shown by past work that the the 1/*f* noise of most bulk MOS and buried oxide transistors satisfies the Dutta-Horn criteria in Fig. 10 [54]. This enables the use of the equations above in extracting useful information about the defect energy levels and distributions from noise measurements as a function of temperature for those particular devices.

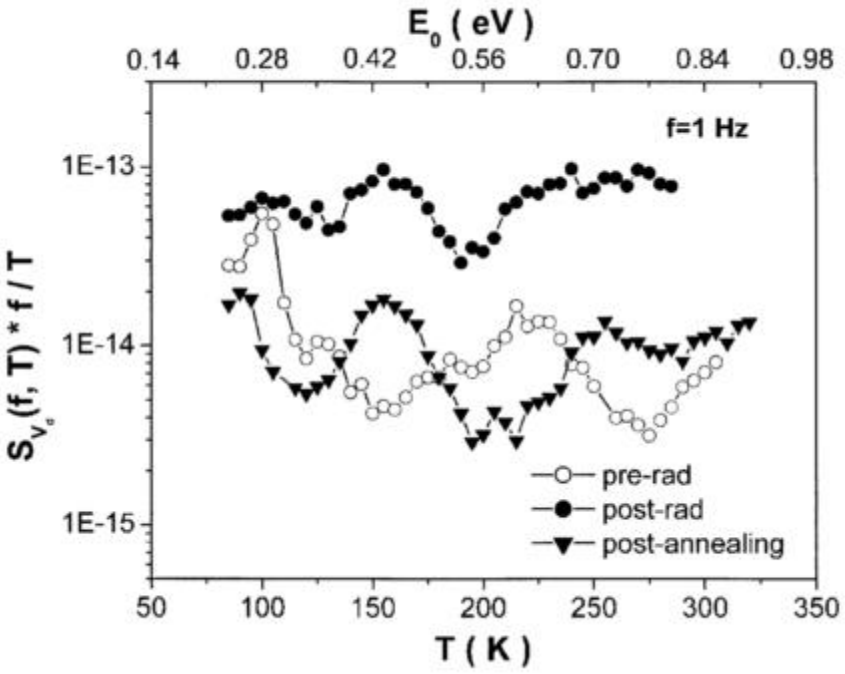


Fig. 10. $S_v f/T$ as a function of T and E_0 for the MOSFET. The energy scale inferred from the Dutta-Horn model is on the upper x-axis (after [54]).

The temperature dependence of 4H-SiC MOS devices will be described in chapter V. Only a limited number of studies of the 1/*f* noise of 4H-SiC devices have been performed before [51],[52],[57],[58]. Previous work on 4H-SiC junction field effect transistors has shown that the noise is determined by carrier number fluctuations at the SiC/SiO_2 interface [51],[57],[59]. As seen in Fig. 11, the gate voltage dependence $V_g - V_t$ of SiC MOS devices exhibits a slope of ~0.5 instead of 2 over the entire range. Such a dependence of β value is usually explained by the energy distribution of the density of localized states that $D_t(E_f)$ increases towards the conduction band edge. This result is consistent with previous results using capacitance-voltage methods to analyze interface-trap energy distributions in [21],[22],[25]. In this work, low frequency noise

measurements are employed as a sensitive probe of impurities and defects that affect the reliability issues and radiation response for 4H-SiC MOS devices.

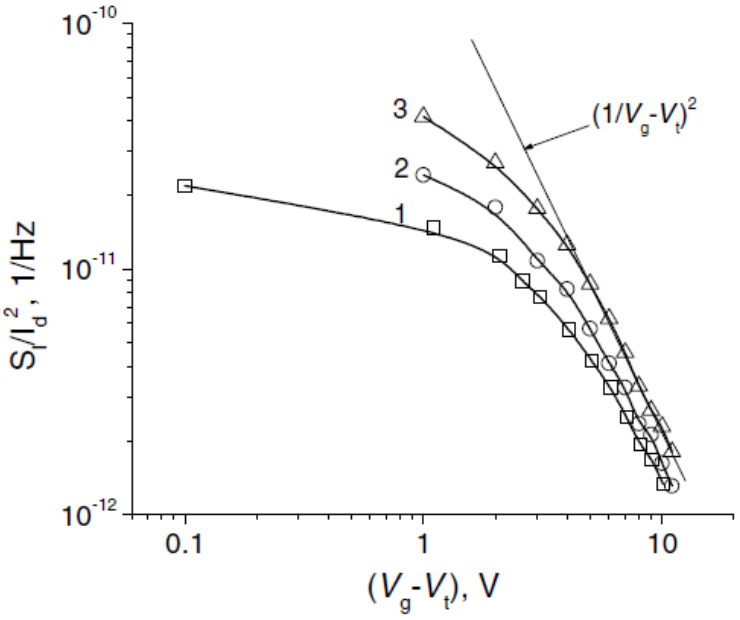


Fig. 11. Gate voltage V_g-V_t dependence of low-frequency noise at constant drain voltage V_d = 0.1 V for three devices after NO treatment. The dashed line shows the dependence $S_I/I_d^2 \sim (V_g\text{-}V_t)^{-2}$ (after [56]).

CHAPTER III

DEVICES AND EXPERIMENTAL DETAILS

This chapter describes the SiC *n*- and *p*-substrate MOS capacitors and SiC *n*MOSFETs used in this study, the different measurement techniques used to characterize these devices, and the experimental conditions to which they were subjected.

Devices

SiC *n*MOS and *p*MOS capacitors

Both *n*- and *p*-substrate MOS capacitors were fabricated at Cree, Inc., on 4H-SiC epitaxial layers, as shown schematically in Fig. 12. An *n*-type SiC epitaxial layer, doped with nitrogen, is grown on a heavily doped p-type substrate for n-substrate MOS capacitors, and a *p*-type epitaxial layer, doped with aluminum, is grown on a heavily doped substrate (also *n*-type) for *p*-substrate MOS capacitors, both with a Ni backside contact. Each epitaxial layer had a doping density of 6×10^{15} cm^{-3} and a thickness of ~10 μm. The gate is B-doped poly-crystalline Si, with an Al gate contact. The gate oxide is SiO_2, with thicknesses of 55 nm and 67.5 nm for the *p*- and *n*-substrate capacitors, respectively. All devices received a standard post-oxidation NO anneal at 1175 ℃ for 2 h [25],[26]. Additional details of the device processing are provided elsewhere [60].

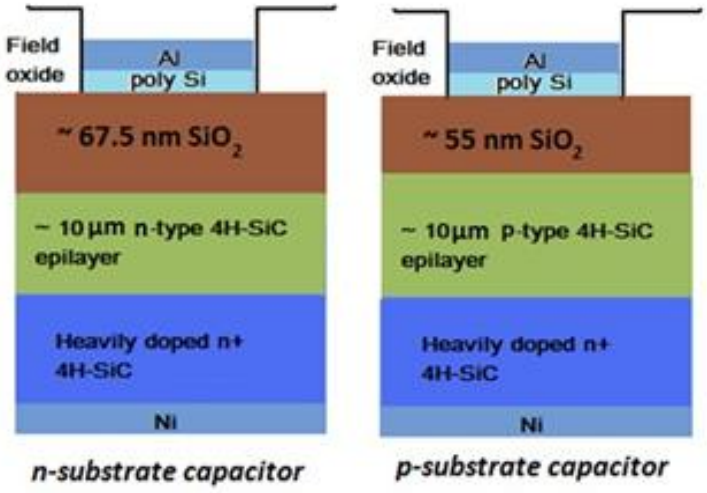


Fig. 12. Schematic cross-section of the *n*- and *p*-substrate capacitors (after [61]).

SiC *n*MOSFET

The SiC *n*MOSFETs were fabricated at Cree, Inc., on 4H-SiC epitaxial layers, as shown schematically in Fig. 13. A *p*-type SiC epitaxial layer, doped with aluminum, is grown on a heavily doped *n*-type substrate with a Ni backside contact. The epitaxial layer has a doping density of 6×10^{15} cm^{-3} and a thickness of ~10 μm. The gate is B-doped poly-crystalline Si, with an Al gate contact. The gate oxide is thermally grown SiO_2 in dry O_2 conditions with a thickness of 55 nm. All devices received a standard post-oxidation NO anneal at 1175 ℃ for 2 hours. The channel width and length are 400 μm × 400 μm. Additional details of the device processing are provided elsewhere [60].

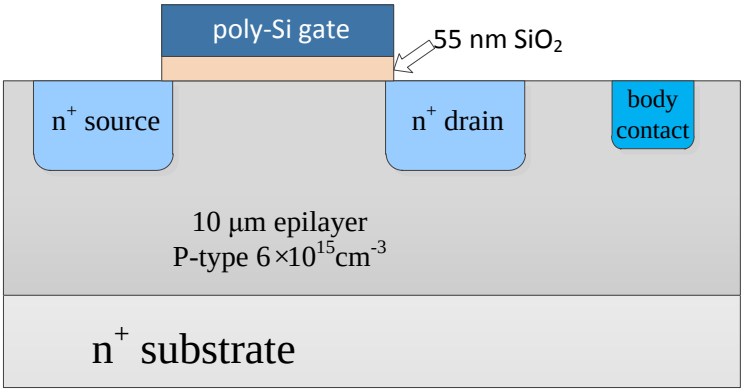


Fig. 13. Schematic cross-section of a lateral 4H-SiC *n*MOSFET with B doped poly-Si gate as used in the experiments (after [61]).

Experimental Setup and Measurement Techniques

Irradiation

Irradiation experiments were performed at the wafer level with a 10-keV ARACOR X-ray irradiator (shown in Fig. 14) at room temperature. For the SiC *n*- and *p*-substrate MOS capacitors, the gates were biased at 0 V (oxide electric field E_{ox} ~ -0.1 MV/cm), ±10 V (E_{ox} ~ 1.6 MV/cm and -1.0 MV/cm), and 20 V (E_{ox} ~ 3.1 MV/cm) for *n*-substrate capacitors, and 0 V (E_{ox} ~ -0.5 MV/cm), ± 8.5 V (E_{ox} ~ 1.6 MV/cm and -1.1 MV/cm), and 17 V (E_{ox} ~ 3.1 MV/cm) for *p*-substrate capacitors. These calculations of electric field include the differing pre-irradiation flatband voltage V_{fb} values shown in the following Figs. 16(a) and 2(b), where V_{fb} ~ −3.0 V for *p*-substrate capacitors and ~ −0.6

V for *n*-substrate capacitors. The calculations are confirmed with TCAD calculations by the same MOS structure. Device responses to biased annealing after radiation were evaluated at 150 ℃. For the SiC *n*MOSFETs, the irradiations were performed with an applied gate bias of 8.5 V, resulting in an electric field of + 1.6 MV/cm across the gate oxide. Devices were also annealed at the same bias after radiation at 120 ℃ for times up to 667 hours.

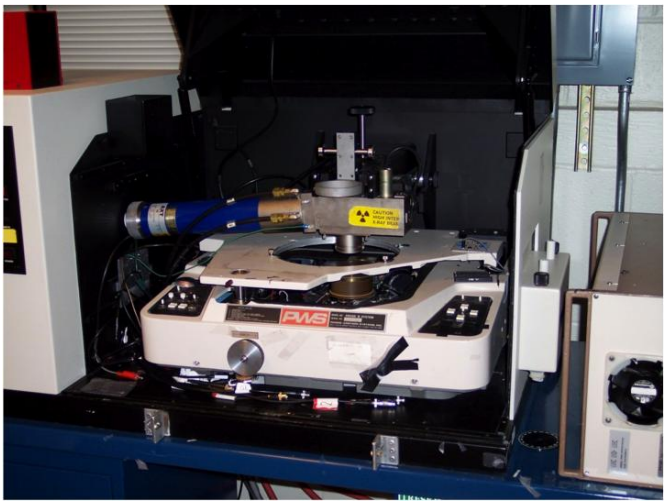


Fig. 14. 10-keV X-ray irradiator as used in the experiments.

Noise measurements

Excess noise measurements were performed when transistors were operating in strong version in the linear regime. A schematic diagram for the 1/*f* noise measurement is shown in Fig. 15. The two voltages V_A and V_B were supplied by a HP 4140B constant voltage supply. The resistor R_B in the circuit was chosen to be 400 kΩ and connected to the MOSFET drain. Both the source and drain of the MOSFET were grounded. The drain voltage noise was amplified using a low-noise amplifier. The power spectral density was calculated by a spectrum analyzer after amplifying the drain noise. The frequency span of the noise measurement extended from 1-500 Hz. During the noise measurements, the drain voltage V_D was held at a constant 1 V and the gate voltages V_g-V_t were varied during the measurements.

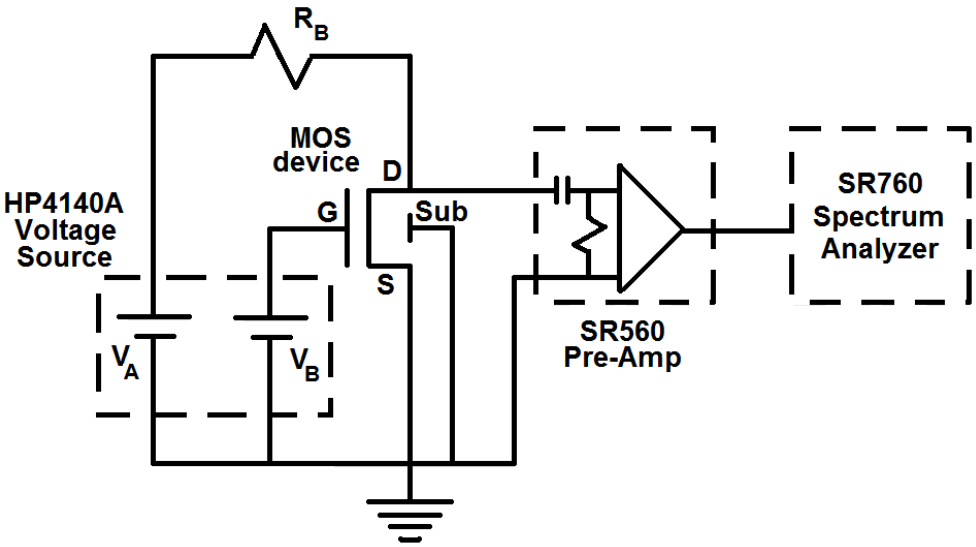


Fig. 15. Schematic diagram of 1/*f* noise measurement circuit (after [51]).

CHAPTER IV

EFFECTS OF BIAS ON THE IRRADIATION AND ANNEALING RESPONSES OF 4H-SIC MOS DEVICES

Introduction

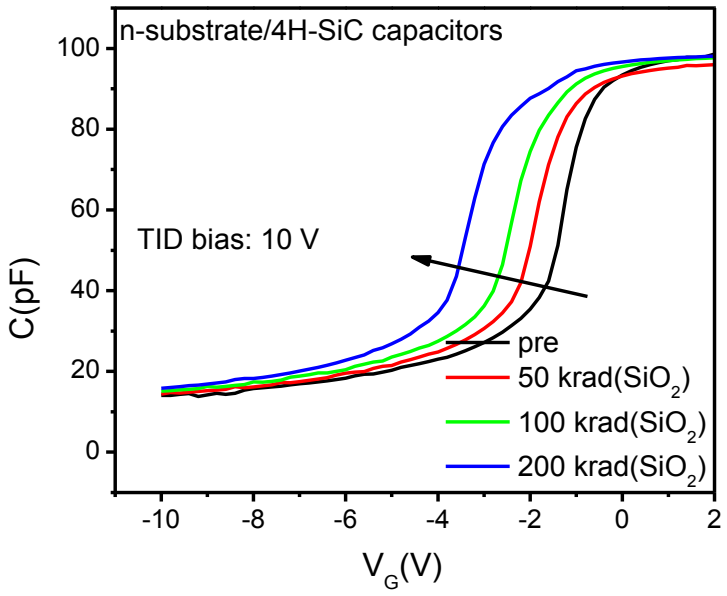
In this work, we evaluate the 10-keV X-ray irradiation and annealing responses for SiC MOS devices under varying gate bias conditions. These devices exhibit a much lower oxide-trap charge trapping efficiency than 4H-SiC MOS devices with nitrided oxides evaluated previously in [37],[38]. The worst-case combined response is positive bias during irradiation followed by negative bias during annealing. Moreover, the net positive oxide-trap charge for *p*-substrate devices irradiated with 0 V or negative bias increases significantly when positive gate bias is applied during post-irradiation annealing at elevated temperature. We attribute this increase in midgap voltage shift to the motion of trapped holes from shallow traps in the oxide bulk to trap locations closer to the SiC/SiO_2 interface. The absence of electrons in deeply depleted *p*-substrate devices provides additional stability for these trapped charges, as compared with accumulated *n*-substrate devices that are irradiated and annealed under similar bias conditions.

Experimental results and discussion

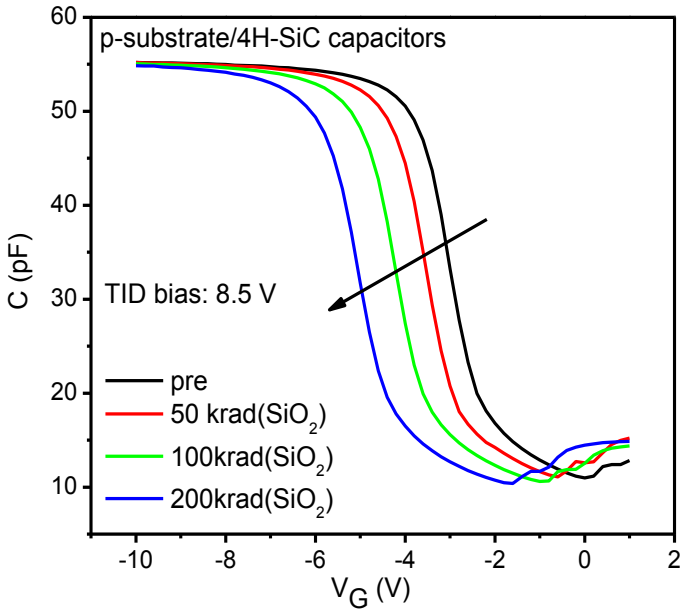
A. Total dose results for *n*- and *p*-substrate capacitors

High-frequency (100 kHz) capacitance-voltage (*C*-*V*) measurements were performed at room temperature with a HP4284A precision LCR meter. At least 5 devices were measured for each case shown here. Fig. 15 shows the capacitance *C* as a function of gate voltage V_G for (a) n-substrate capacitors and (b) p-substrate capacitors with increasing total dose. The irradiation bias is +10 V and +8.5 V, respectively. A midgap voltage shift (ΔV_{mg}) of ~ −1.2 V is observed for both n- and p-substrate capacitors after a total dose of ~100 krad(SiO_2). For SiC, both oxide-trap charge and deeper interface traps (with energies more than 0.6 eV below the conduction band edge) can contribute to midgap voltage shifts [4],[62]. The absence of any significant change in the stretch-out of

the curves during irradiation here and in previous work on SiO_2 on SiC devices suggests that oxide-trap charge tends to dominate SiC radiation response[37],[38],[39].



(a)

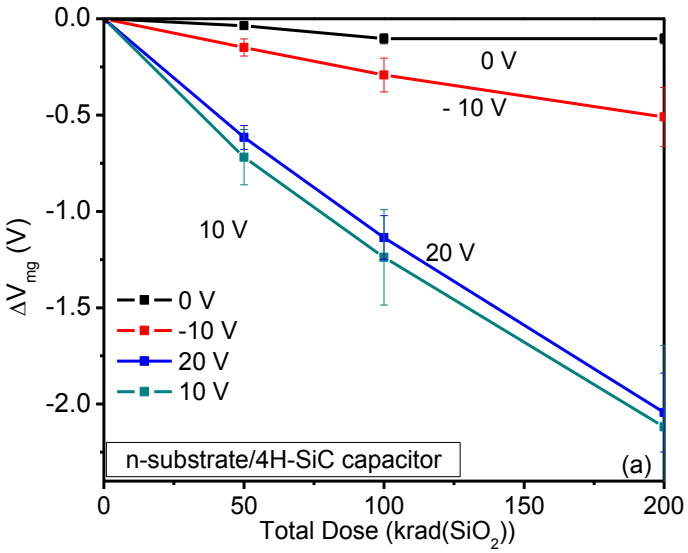


(b)

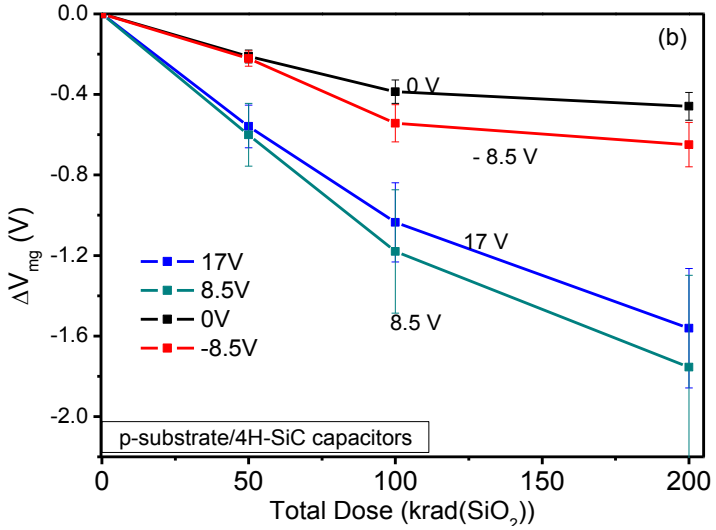
Fig. 16. Capacitance C as a function of gate voltage V_G with varying total dose (a) n-substrate 4H-SiC capacitors with 67.5 nm nitrided oxides and (b) p-substrate 4H-SiC capacitors with 55 nm nitrided oxides (after [61]).

Fig. 17 shows ΔV_{mg} as a function of total dose for (a) *n*-substrate capacitors with 67.5 nm oxides and (b) *p*-substrate capacitors with 55 nm oxides. These results are generally consistent with total ionizing dose effects on Si/SiO_2 devices, with radiation-induced-hole trapping dominating the device radiation response [34],[37],[38],[63],[64]. The midgap voltage shifts negatively for both *n*- and *p*- substrate MOS devices, with larger shifts under positive bias than for either negative bias or zero bias. The enhanced charge trapping at positive bias is due primarily to the transport of radiation-induced holes toward the SiC/SiO_2 interface, and the resulting hole trapping at O vacancies [4],[64].

The values of ΔV_{mg} are generally larger for the *n*-substrate capacitors (67.5 nm oxides) in Fig. 17(a) than for the *p*-substrate capacitors (55 nm oxides) in Fig. 17(b). The differences in mean values of ΔV_{mg} are slightly less (~17%) than one would expect from the typical oxide-thickness squared scaling of hole trapping in SiO_2, in the absence of any other differences in processing [34],[64]. However, we note that these differences are well within the device-to-device variation in midgap voltage shifts for the groups of devices. We compare these results to previous work on SiC MOS devices in the next section. The slight decrease in midgap voltage shift as the bias is increased from 10 V to 20 V bias for the n-substrate capacitors and from 8.5 V to 17 V for the *p*-substrate capacitors is most likely due to a reduction in the effective hole capture cross section with increasing applied electric field [34],[64],[35],[65],[66].



(a)



(b)

Fig. 17. Midgap voltage shift (ΔV_{mg}) as a function of total dose at varying gate biases for (a) n-substrate 4H-SiC capacitors with 67.5 nm nitrided oxides and (b) p-substrate 4H-SiC capacitors with 55 nm nitrided oxides (after [61]).

B. Combined effects of irradiation and annealing

Fig. 18 shows the post-irradiation annealing response of *p*-substrate 4H-SiC MOS capacitors that are subjected to negative bias annealing after the zero bias, negative bias, and positive bias irradiation sequences of Fig. 16 (b) after X-ray irradiation to 200 krad(SiO_2). Each value of the midgap voltage shift was taken after a single period of post-irradiation annealing for 20 minutes at the listed temperature. Quite similar enhancement of degradation with elevated temperature annealing is observed for all irradiation bias conditions. Irradiation under positive bias and annealing at negative bias leads to the greatest charge trapping during this combined irradiation and annealing test sequence. The increased degradation after irradiation occurs primarily because of the detrapping of compensating electrons from N-related defects and O vacancies in the near-interfacial SiO_2, as has been observed previously for both SiO_2 [67],[68],[69],[70] and high-k oxide/oxynitride dielectrics on Si [37],[69].

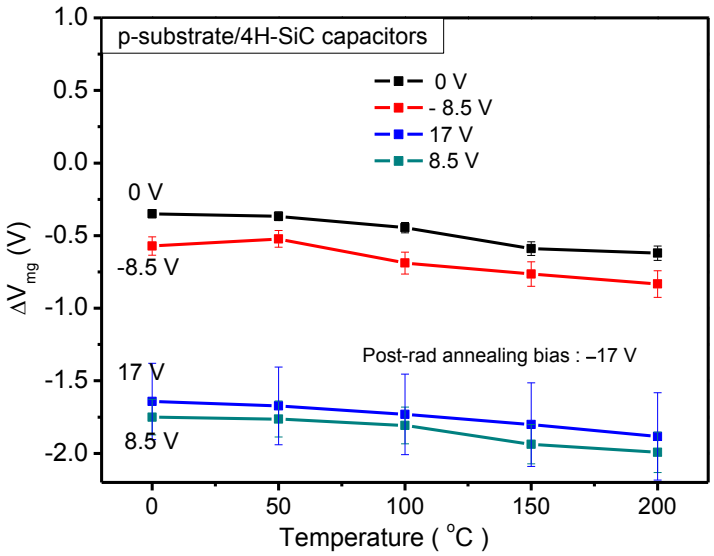


Fig. 18. Midgap voltage shift (ΔV_{mg}) as a function of temperature and gate bias during x-ray irradiation to 200 krad(SiO_2) for p-substrate 4H-SiC MOS capacitors. The gate bias for post-irradiation annealing is − 17 V in all cases. For each temperature, the stress time for a new device was 20 min. This was not a cumulative exposure of a single device to a series of anneals (after [61]).

Fig. 19 compares the separate and combined effects of negative bias stress for *p*-substrate 4H-SiC MOS capacitors, with and without prior radiation exposure. The relatively small increases in ΔV_{mg} for negative stress on unirradiated devices are due to negative-bias-temperature instabilities in these devices [72],[73] The dashed line is the sum of the shift observed with negative bias on the unirradiated devices (approximately − 0.25 V in about one day of stressing at 150 ℃) and the shift observed for 200 krad(SiO_2) irradiation under positive bias (− 16 V). The midgap voltage shifts for devices that are first irradiated and then subjected to negative bias annealing for up to three hours (approximately − 2.7 V) exceed the sums of the separate irradiation and stress results by ~ 70%. This shows a strong interaction between the applied negative field and the radiation-induced defects, as has also been observed for high-k oxides on Si [37],[69].

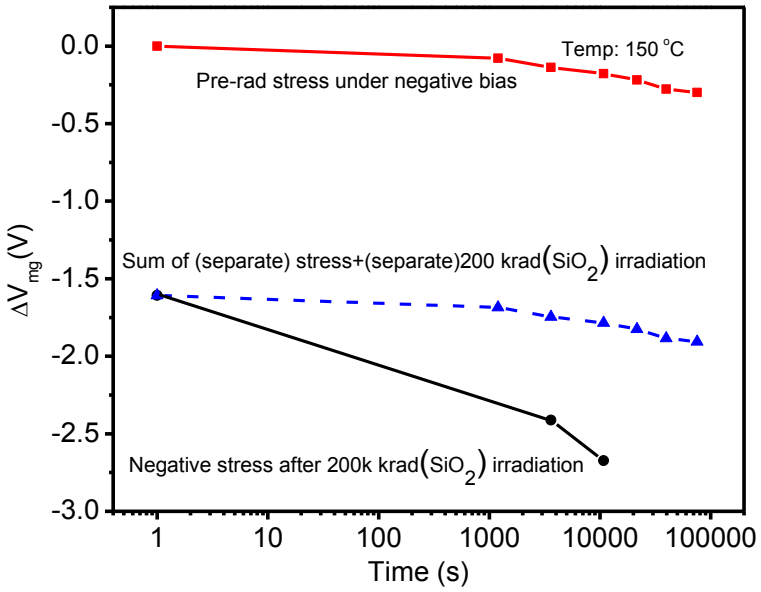


Fig. 19. Comparison of the separate and combined effects of radiation exposure and negative bias annealing for p-substrate 4H-SiC MOS capacitors. ΔV_{mg} is plotted as a function of stress time for irradiated and unirradiated devices. The irradiation bias is 8.5 V; the gate bias for negative stressing is −17 V and the stress temperature is 150 ℃ (after [61]).

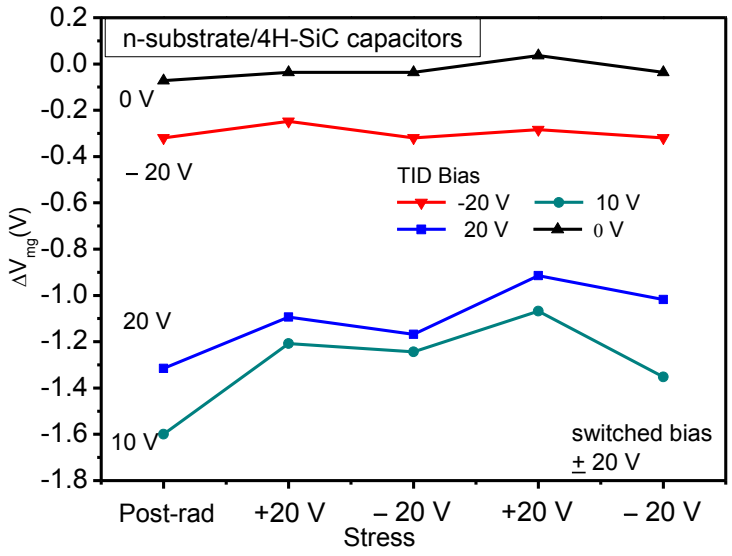
C. Switched-bias annealing studies

To explore the mechanisms that lead to the enhanced degradation in Fig. 15, the post-irradiation annealing bias was switched between −20 V and 20 V on *n*-substrate capacitors, and between −17 V and 17 V on *p*-substrate capacitors. All of the stress experiments were done at 150 ℃, and all measurements were performed at room temperature. The first pair of negative and positive stresses was performed for 20 min, and the second pair of stresses was performed for 60 min. Fig. 20(a) shows switched bias annealing results for *n*-substrate 4H-SiC MOS capacitors, irradiated with the same bias conditions as in Fig. 16(a). The value of ΔV_{mg} increases in magnitude for negative bias annealing and decreases in magnitude for positive bias annealing. The reversibility of the midgap voltage shifts for devices irradiated under positive bias is greater than for devices irradiated under negative or zero bias. During positive-bias annealing, the neutralization of radiation-induced positive oxide-trap charge dominates the device response. During negative-bias annealing, electrons in border traps that were captured during irradiation

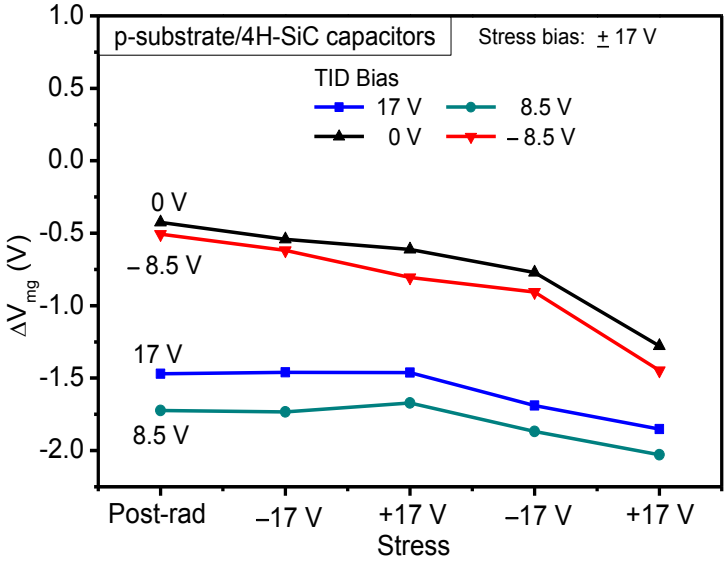
are now pushed out of the SiO_2 and into the SiC. In response to repeated bias changes during annealing, a portion of the electrons can tunnel back and forth to the *n*-type SiC [37],[68],[69]. The switching behavior in the SiC/SiO_2 system is similar to the effects observed for oxides on Si [67–70].

Fig. 20(b) shows the switched bias annealing response for *p*-substrate 4H-SiC MOS capacitors, irradiated under conditions similar to those in Fig. 16(b). Increases in ΔV_{mg} are found for both positive and negative bias annealing after irradiation under all four bias conditions. In contrast with the results of Fig. 17(a), this behavior (particular for devices irradiated at 0 V or negative bias) is not typically observed for irradiated and annealed SiO_2 oxides on Si [31],[61],[65]-[68].

During negative-bias annealing at longer times in Fig. 17(b), detrapping of compensating electrons or hole trapping due to negative bias-temperature instabilities may contribute to the observed shifts in *p*-type SiC [72]. During positive bias annealing, the midgap voltage shifts in these soft oxides can be enhanced by redistribution of trapped positive charge within the oxide [74],[75]. The degradation is especially enhanced for the 60 min, + 17 V stress of devices irradiated at negative or 0 V bias. This increase is likely due to the drift of positive charge from shallow defects (e.g., E_δ' centers [75]) in the oxide bulk towards the SiC/SiO_2 interface. The absence of electrons in these depleted *p*-substrate devices [72] provides additional stability at these trap locations, as compared with accumulated *n*-substrate devices that are irradiated and annealed at similar biases. Similar behavior is not observed for Si devices owing to the much smaller band gap, and the relative ease in forming an inversion layer at similar biases and temperatures. The resulting midgap voltage shifts more than double for the 0 V and negative bias irradiations that are followed by elevated-temperature switched-bias stresses. This is an interesting result that would be useful to study with techniques (e.g., thermally stimulated current [63],[76]) that are more sensitive to trapped charge location and energy than are midgap voltage measurements.



(a)



(b)

Fig. 20. Midgap voltage shift (ΔV_{mg}) as a function of gate bias after total dose irradiation for (a) *n*-substrate 4H-SiC MOS capacitors with 67.5 nm oxides, with the post-irradiation bias switched between −20 V and 20 V and (b) *p*-substrate 4H-SiC MOS capacitors with 55 nm oxides, with the post-irradiation bias switched between −17 V and 17 V. All of the stress measurements were done at 150 ℃, and all measurements were performed at room temperature. The first pair of negative and positive stresses was performed for 20 min, and the second pair of stresses was performed for 60 min (after [61]).

Charge trapping efficiency

We now compare the radiation results observed for the nitrided oxides on 4H-SiC of this study to those employed in previous work. A convenient method to compare the defect densities of devices with different oxide thicknesses is the effective oxide-trap charge trapping efficiency [31],[75], $f_{ot} = -(\varepsilon_{ox}\ \Delta V_{mg})/(q\kappa_g\ f_y\ t_{ox}^2 D)$. Here ε_{ox} is the dielectric constant of SiO_2, $-q$ is the electron charge, κ_g is the number of electron-hole pairs generated per unit dose per unit volume in the dielectric layer, f_y is the charge yield, t_{ox} is the SiO_2 dielectric thickness, and D is the dose. The average charge trapping efficiency under worst-case bias conditions for the nitrided oxides of Figs. 13 and 14 in this work is ~10%. For both the 34 nm nitrided oxides on 4H-SiC evaluated by Dixit et al. in [38] and the 25 nm nitrided oxides on 4H-SiC evaluated by Arora et al. in [37], f_{ot} is ~30%. Hence, the density of radiation-induced oxide-trap charge is ~3 times lower in the devices used here than in previous work [32],[33], emphasizing the relatively high quality of these devices. We also note that the *C-V* curves in Fig. 12 do not show the "ledge" exhibited in previous work by Dixit et al., which is consistent with a comparatively smaller density of both oxide and interface traps for the devices of Fig. 12 than in [38].

Summary and conclusions

We have investigated SiC MOS radiation effects and annealing as a function of applied gate bias. The combined effects of irradiation and negative bias annealing on *p*-MOS SiC capacitors are greater than the linear combination of both types of stress. Switching the bias between irradiation and annealing can lead to enhanced midgap voltage shifts due to the removal of compensating electrons from the SiO_2 and/or the injection of holes from the SiC under negative bias, or the drift of trapped holes from the bulk of the oxide to the SiO_2/SiC interface under positive bias. These results show that combined radiation and reliability stresses are needed to qualify SiC devices for use in relatively high total-ionizing dose applications.

CHAPTER V

BIAS TEMPERATURE INSTABILITIES IN 4H-SIC MOS DEVICES

Introduction

This chapter presents results on the bias temperature instabilities (BTIs) of unirradiated SiC *n*- and *p*-substrate capacitors and unirradiated SiC *n*MOSFETs under a range of stress conditions. For SiC *n*MOSFETs, threshold voltage decreases due to NBTI under negative bias at elevated-temperature when the surface is accumulated. Similar results observed for SiC *n*MOS and *p*MOS capacitors correlate strongly with the additional ionization of deep dopants in SiC at elevated temperatures. Devices stressed when the surface is inverted do not exhibit significant threshold voltage shift. The charge that leads to BTI lies in deep interface traps that are 0.6 eV away from the SiC conduction or valence bands and O vacancies in the SiO_2.

Experimental results and discussion

A. SiC *n*- and *p*-substrate capacitors

Figure 21 shows *C*-*V* curves measured at room temperature before and after stress for the *n*- and *p*-substrate capacitors. The *C*-*V* curves shift positively after 20 min of stress at 20 V applied to the gate for the *n*-substrate capacitor, and negatively for the *p*-substrate capacitor stressed for 20 min with −17 V applied to the gate. For *n*-substrate capacitors under positive bias, negative oxide-trapped charge and electrons in deeper interface traps (energies more than 0.6 eV below the conduction band edge) can each lead to a positive midgap voltage shifts in SiC MOS capacitors [62]. Interface traps in shallower levels would lead instead to stretchout in the *C*-*V* curve; no significant stretchout is observed in these devices under these stressing conditions. Some of the defects likely are process-induced; others may be created during the BT stressing. Similarly, in Fig. 21(b), for *p*-substrate capacitors stressed at negative bias, negative midgap voltage shifts are observed. These negative shifts are consistent with positive oxide-trapped charge and/or holes in deeper interface traps (energies more than 0.6 eV

above the valence band edge) [75],[78],[79],[80].Again, no significant increase in *C-V* stretchout is observed.

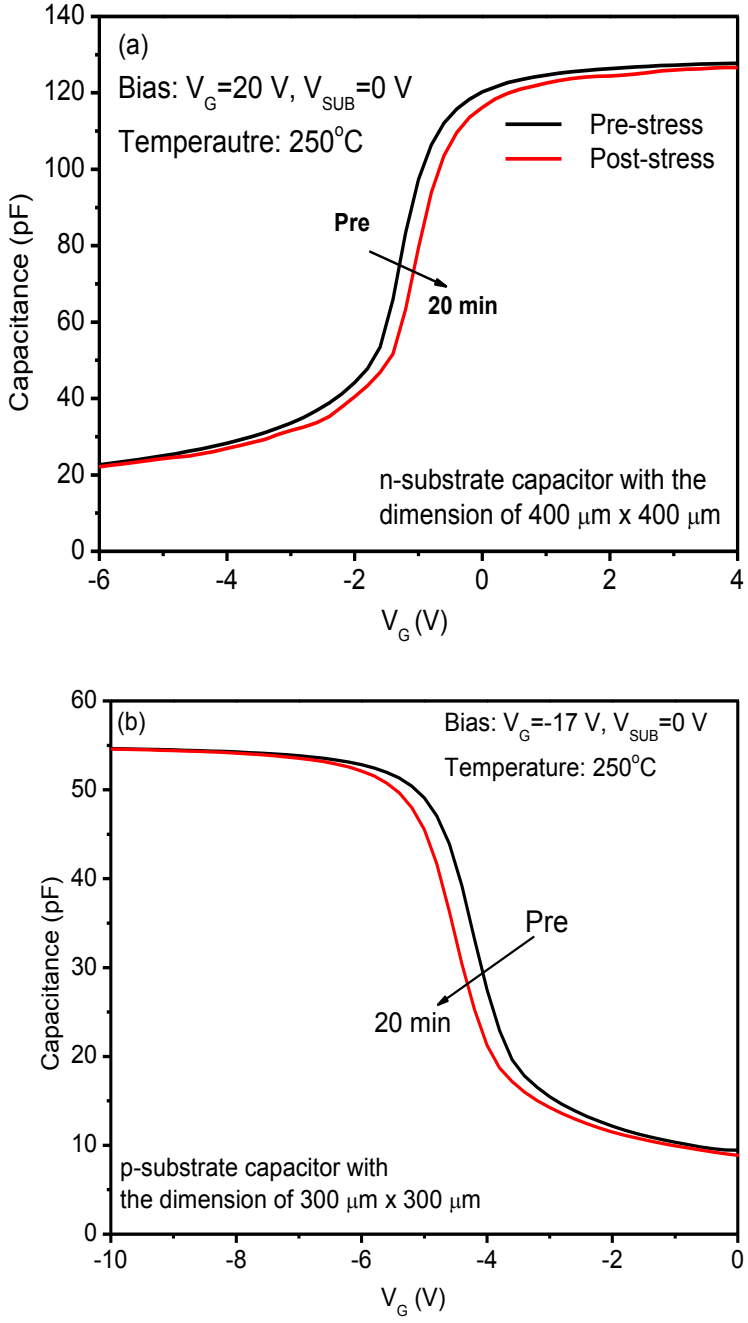


Fig. 21. Capacitance as a function of gate voltage measured at room temperature for (a) an *n*-substrate/4H-SiC capacitor, stressed with a gate voltage of 20 V at a temperature of 250 ℃, and (b) a *p*-substrate/4H-SiC capacitor, stressed by the gate voltage of −17 V at a temperature of 250 ℃ (after [81]).

Figure 22 shows *C-V* curves as a function of stressing time for a *p*-substrate capacitor; the gate voltage is −17 V and the stressing temperature is 150 ℃. The curves shift monotonically to more negative values, again consistent with hole trapping. Figure 23 shows the midgap voltage shift (ΔV_{mg}) as a function of stress time for *n*-substrate (Fig. 23(a)) and *p*-substrate (Fig. 23(b)) capacitors at biases of ± 17 V on the gate and a temperature of 150 ℃. In each case, the trapping shows a monotonic increase in the magnitude of the midgap voltage shifts at early stress times, with saturation at longer times. This saturation represents the filling of process and stress-induced interface and near-interfacial oxide (border) traps in these devices [26],[75].

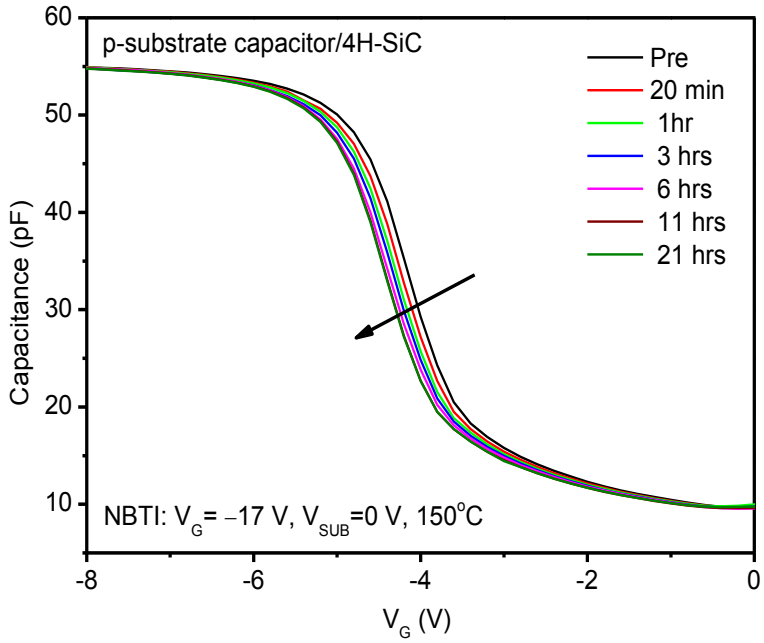


Fig. 22. Capacitance as a function of gate voltage and stress time for a 300 μm×300 μm p-substrate 4H-SiC capacitor. The stressing bias is −17 V on the gate and the temperature is 150 ℃ (after [81]).

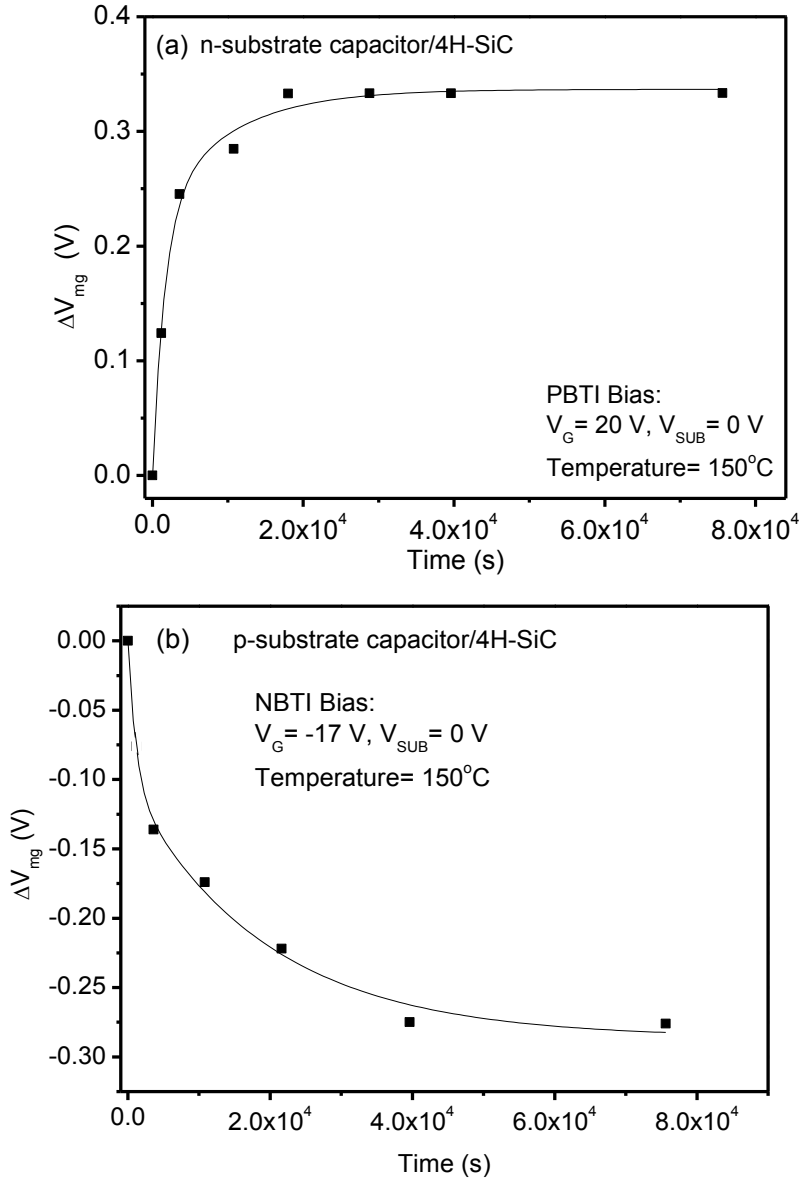


Fig. 23. Midgap voltage shift (ΔV_{mg}) as a function of stress time for (a) *n*-substrate SiC capacitors stressed at 150 ℃ and a gate bias of ± 20 V, and (b) *p*-substrate 4H-SiC capacitors stressed at 150 ℃ and a gate bias of ± 17 V. The lines are guides to the eye (after [81]).

The magnitudes and the time dependencies of the BTI responses in Fig. 23 differ significantly from what are typically observed for thin SiO_2 gate oxides on Si [37],[44],[71],[78]. In particular, the shifts are larger than observed on highly scaled Si devices, and do not follow a power-law time dependence, as commonly observed in Si

[45],[79],[82]. These differences occur primarily for four reasons. (1) Oxides on SiC are thicker and grown at higher temperatures than the ultrathin nitrided SiO_2 and/or high-K gate dielectrics used in Si-based integrated circuit technologies. This results in larger trap densities at and near the SiC/SiO_2 interface for these devices than for the Si/SiO_2 interface of typical Si-based MOS devices and integrated circuits [45],[78],[82],[83]. (2) For Si-based MOS transistors, the time constants to fill interface traps are much shorter than the time scales of BTI stressing conditions. For SiC MOS capacitors, part of the observed time dependence for NBTI/PBTI is associated with the filling of interface trap levels that are away from the band edges and quite slow to populate [62],[79]. (3) As we discuss further below, SiC has deep donor and acceptor levels, which can be ionized more completely during the bias-temperature stress than during typical room-temperature *C-V* measurements [49],[72],[84],[85]. This can increase the number of carriers available to be trapped at elevated temperature relative to room temperature. (4) For Si MOS technologies, hydrogen is known to play an important role in both the passivation of process-induced interface traps and the creation of defects during bias-temperature stress [14],[44],[86] . Hydrogen reactions at the SiC interface are typically not as effective in passivating interface traps as at the Si/SiO_2 interface [14],[25],[26],[31],[32],[87],[88], so the role of hydrogen in BTI on SiC is less clear. Excess nitrogen associated with the NO nitridation treatments used to reduce interface-trap densities in these SiC devices [25],[26],[31],[89] likely will introduce a relatively small but finite density of N-related trap levels in the near-interfacial SiO_2. These may behave similarly to N-related defects in near-interfacial SiO_2 on Si, where N-related centers are observed to function as both electron traps and hole traps [83],[90]. Moreover, nitrogen has been demonstrated to increase NBTI in oxides on Si [83],[91]. However, the overall effects of NO processing on these devices are quite favorable, since oxides that are not treated with nitrogen typically show much inferior characteristics to NO annealed devices [25],[26],[49]. So we emphasize that, if N-related defects play a significant role in the observed response, it is the excess nitrogen concentration above and beyond the levels required to passivate the process-induced defects that are likely contributing to the BTIs.

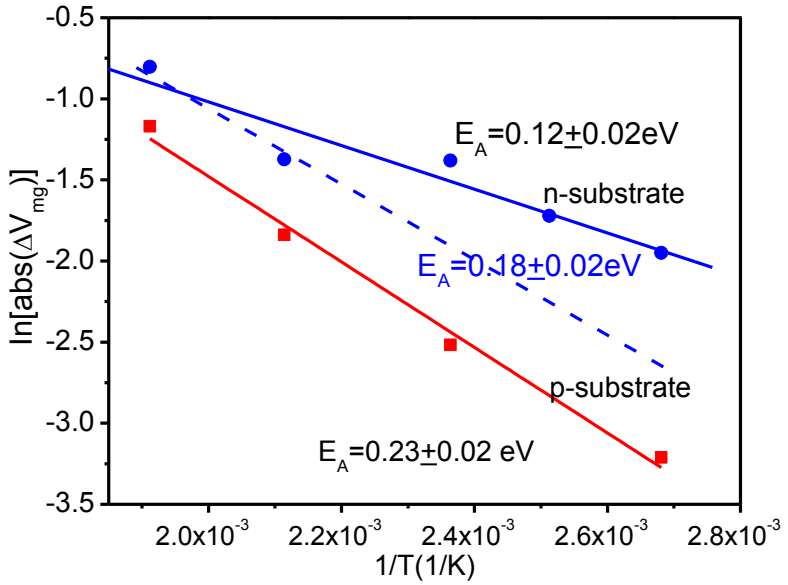


Fig. 24. Midgap voltage shift as a function of stressing temperature for *n*- and *p*-substrate/4H-SiC capacitors stressed in accumulation for 20 minutes at 20 V (n-substrate capacitors) and -17 V (p-substrate capacitors) on the gates. The effective activation energies are 0.23 ± 0.02 eV and from 0.12 ± 0.02 eV to 0.18 ± 0.02 eV for *p*- and *n*-substrate capacitors, respectively. The standard deviation in Arrhenius slope is ± 0.02 eV in each case (after [73]).

Figure 24 shows the midgap voltage shifts as a function of stressing temperature for *n*- and *p*-substrate SiC MOS capacitors stressed for 20 minutes at +20 V and −17 V on the gates, respectively. The best fit, effective activation energies of the resulting BTI are 0.12 ± 0.02 eV (for positive threshold voltage shifts), although at higher temperatures the value may increase by as much as ~ 50% (as shown by the dotted blue line in Fig. 23), and 0.23 ± 0.02 eV (for negative threshold voltage shifts) for the *n*- and *p*-substrate capacitors [72]. The activation energies for the *n*-substrate SiC capacitors in Fig. 24 are somewhat lower than those typically measured for SiO_2 on Si devices, but the *p*-substrate devices show effective activation energies similar to those reported for SiO_2 on Si [44],[78],[79],[82].

We have postulated previously that the ionization of deeper donor and acceptor levels may play a significant role in the increased charge trapping that leads to the observed midgap voltage shifts of SiC devices subjected to bias-temperature stress [72].

Figure 25 shows the band diagram for 4H-SiC capacitors in accumulation (positive bias on *n*-substrate/4H-SiC capacitor and negative bias on *p*-substrate/4H-SiC capacitor). For *n*-substrate/4H-SiC capacitors, nitrogen doping introduces donor traps with multiple activation energies. Shallow donors have an activation energy of ~ 0.045-0.065 eV, with deeper traps showing an activation energy of ~ 0.105-0.125 eV [72],[84]. These energies are remarkably similar to the effective activation energy for *n*-substrate capacitors in Fig. 23(a), especially from room temperature through ~ 250 ℃. At higher temperatures, the activation energy may increase. Moreover, there is an acceptor level at ~ 0.22 eV for aluminum doped *p*-type 4H-SiC [85], similar to the effective activation energy of the *p*-substrate capacitors in Fig. 23(b). The similarities among these dopant ionization levels and the effective activation energies in Fig. 24 strongly suggest that the presence of additional carriers at elevated temperatures due to the ionization of deep dopants in SiC may enhance the observed charge trapping during bias-temperature stress [72]. The carrier tunneling rates in SiC will like increase at elevated temperatures, owing to barrier lowering, which may become rate-limiting for BTI in SiC at higher temperatures [72].

Fig. 26 shows the percentage of ionized dopant atoms in SiC for *n* and *p*-substrate capacitors as a function of dopant density (recall that these capacitors are nominally doped at ~ 6×10^{15} cm^{-3}). At room temperature, fewer than 50% of the *p*-substrate dopants are ionized in the capacitors we have evaluated, so it is quite plausible that the availability of extra carriers that originate from the deep Al dopant level can lead to additional charge trapping during higher temperature stresses in the *p*-substrate capacitors [72]. However, more than 90% of the dopant atoms are ionized for the *n*-substrate capacitors at room temperature, so additional factors must be considered for the *n*-substrate devices. For example, Chatterjee et al. have suggested that the NO anneal may lead to a significant increase in the effective N-doping of the SiC channel [92]. This may decrease the fraction of ionized N dopants at 25 ℃, consistent with the possibility that dopant-ionization is rate-limiting for BTI in *n*-type SiC over a similar range of temperatures. There may also be deeper levels (~ 130 to 360 meV below the conduction band) associated with O donors that are introduced at the SiC/SiO_2 interface during the NO anneal [92]. So a significant role for O vacancies and/or dopant activation, especially

at higher temperatures, is possible for the *n*-substrate capacitors; however, it is also possible that trap creation or carrier capture is rate limiting in these devices.

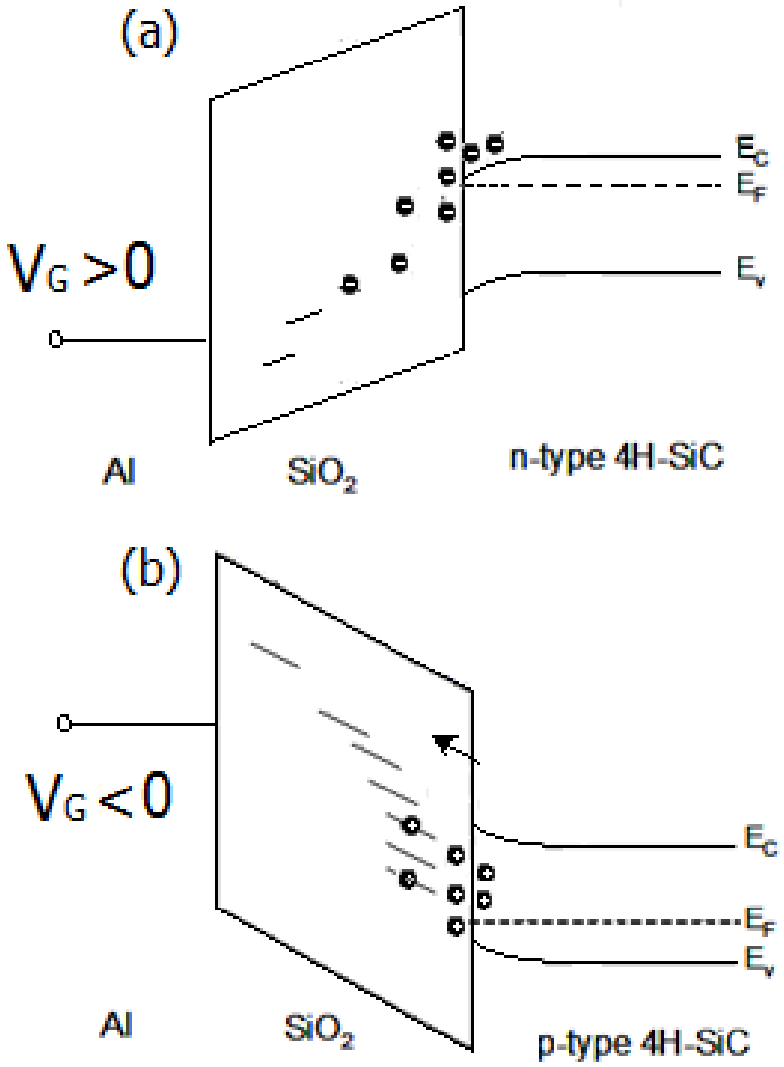


Fig. 25. Schematic band diagrams for (a) *n*-substrate/4H-SiC capacitors under positive bias, and (b) *p*-substrate/4H-SiC capacitors under negative bias, where charge trapped in the bulk of SiO_2 and at the SiO_2/SiC interface (electrons in (a) and holes in (b)) (after [81]).

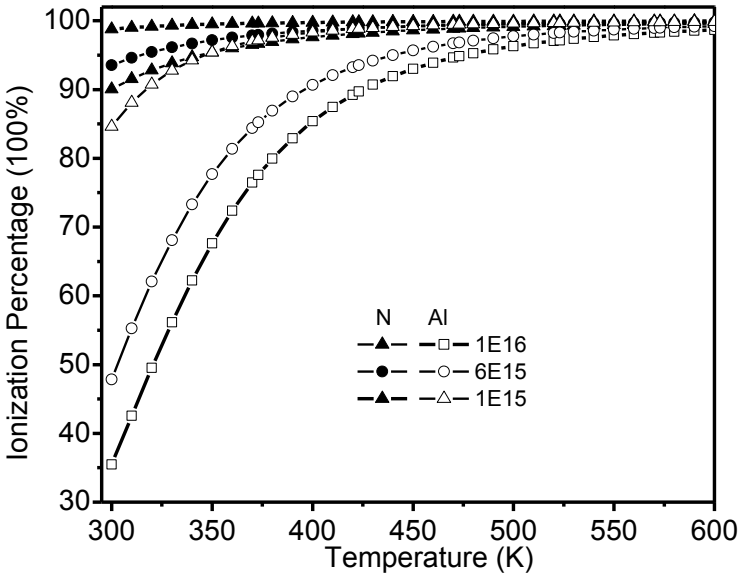


Fig. 26. Calculated dopant ionization percentage in nitrogen and aluminum doped 4H-SiC MOS capacitors with doping concentrations of 1×10^{16}, 6×10^{15} (this work), and 1×10^{15} cm^{-3}. The solid symbols are for nitrogen doping and the open symbols are for aluminum doping (after [81]).

The different activation energies between the *n*- and *p*-substrate capacitors also are likely to be influenced by other factors as well. These include (1) different generation and transport rates of electrons and holes in *n*- and *p*-doped SiC, which will affect the time it takes to populate deeper interface traps [93][94], (2) a slightly lower barrier for electrons (2.7 eV) than holes (3.05 eV) to be emitted from the SiC into the SiO_2 [1],[95], and (3) as shown by previous radiation effects and high-field stressing studies [14],[26],[37],[38],[61],[73] and confirmed in the switched-bias stress experiments below, the enhanced stability of trapped holes in these materials, relative to trapped electrons. It is also likely that the NO anneal has introduced N related defects with different energy levels for these SiC MOS capacitors, as compared to Si MOS capacitors [24],[31],[88],[90],[96]. In any case, because of the low activation energies, one still requires kinetic factors (e.g., differences in carrier generation rates in Si and SiC) to account for differences in charge trapping that are caused by changes in ionization rates of dopants with these energies at room temperature. For example, the excess charge could result from carriers emitted from dopant atoms in configurations that lead to deeper

ionization levels that are located near the interface, with the carriers being quickly captured in deep interface traps. Additional work is required to determine whether this is the case. One would likely not observe similar effects in Si devices because of the much narrower band gap and shallower dopant levels.

As is the case for BTI in Si devices, the effective activation energies in Figs. 23(a) and (b) may not represent a single physical process, but may instead denote a combination of factors, as demonstrated in reaction-diffusion models developed by Ogawa et al. [42], Alam et al. [79], and Tsetseris et al. [44], for example, which show similarly low activation energies in NBTI studies on Si MOS devices. It is unlikely that hydrogen transport and reactions play the significant role in these SiC MOS devices that they do in Si [14],[23],[24],[32],[42],[44],[87],[88]. In any case, it is clear that processes with such low effective activation energies cannot be the only rate limiting steps in the charge trapping processes. Otherwise, the trapping would be instantaneous at these temperatures, and/or the extra carriers available at elevated temperature would simply return to their original locations on the dopant atoms.

Figure 27 shows the midgap voltage shifts (ΔV_{mg}) as a function of switched stressing biases for (a) *n*-substrate and (b) *p*-substrate capacitors; the temperature is 150 ℃ during the bias-temperature (BT) stress. The characterization was performed at room temperature. For the *n*-substrate capacitor in Fig. 27(a), the midgap voltage shifts positively after 20 minutes of positive bias-temperature (PBT) stress and then recovers somewhat during the next 20 minutes of negative bias-temperature (NBT) stress, with similar responses for a second cycle of switched-bias stresses of 60 minutes each. During the first 20-minute PBT stress, there is a positive V_{mg} shift. If all of the midgap voltage shifts were due to shallow interface trap charge buildup, one might expect the shift to recover more completely after the subsequent NBT stress. But charge trapped in defects in the SiO_2 is slower to recover, reinforcing the role of oxide traps and/or deep interface traps in the observed PBTI for *n*-substrate capacitors.

For the *p*-substrate capacitors in Fig. 27(b), there is significantly less recovery during the first period of PBT stress following the initial NBT stress, while a small, additional increase in midgap voltage shift is observed in the second period of PBT stress that follows the second NBT stress. This response indicates that trapped holes are more

stable than trapped electrons in these devices. The slight increase in the magnitude of the midgap voltage shift during the second period of PBT stress in Fig. 27(b) may result from the bias-induced motion of trapped positive charge in the SiO_2 layer from trapping sites within the oxide to sites at or closer to the Si/SiO_2 interface. The trapped charge is likely to comprise mostly trapped holes. In oxides in Si, many of these holes would be neutralized via electron compensation [75], but the charge generation rates in SiC are significantly less than in Si [49],[93], so fewer electrons are available to compensate the trapped holes in SiC MOS capacitors than in Si MOS capacitors. We note that smaller shifts but significantly more reversibility is typically observed for Si MOS capacitors subjected to similar switched-bias stressing conditions [37],[69]. A significant role for O vacancies in this process has been demonstrated for SiC/SiO_2 structures [61],[72],[95] in addition to Si/SiO_2 structures. It is also possible that some of the trapped positive charge is in the form of H^+ [95],[97]. Other mobile ions could also be the agents. If that is the case in these oxides on SiC, then the results of Fig. 27(b) suggest that the H^+ in the SiO_2 can move closer to the SiO_2/SiC interface during the application of PBT stress, but there must not be a significant amount of interface trap formation, or the midgap voltage shift would be positive instead of negative, under positive bias. Trapping of H^+ at defects in the near-interfacial SiO_2 regions of oxides with high O vacancy densities has been observed in Si MOS devices [97], so this interpretation of the results is also consistent with Fig. 27(b).

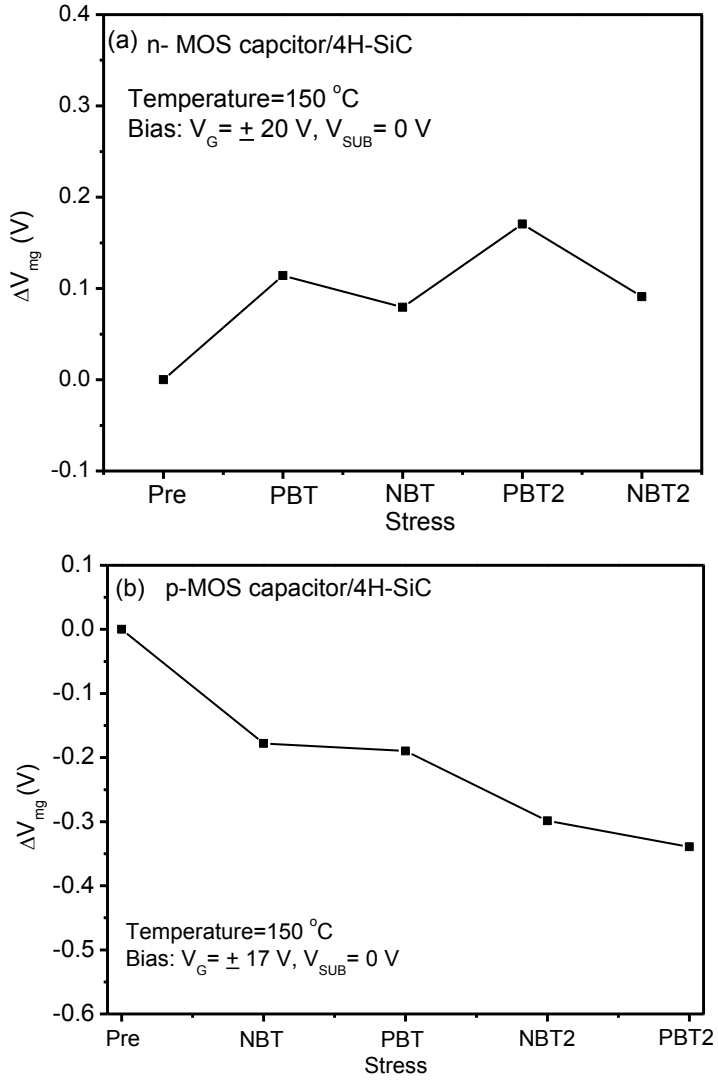


Fig. 27. Midgap voltage shift (ΔV_{mg}) as a function of switched bias stress for (a) *n*-substrate 4H-SiC capacitors at a gate bias of ± 17 V and (b) *p*-substrate 4H-SiC capacitors at a gate bias of ± 20 V at the temperature of 150 ℃. The stress times for the biases are 20 min for the first set of biases and 60 min for the second set of biases in each case (after [73]).

B. 4H-SiC nMOSFETs

Figure 28 shows I_D-V_G curves measured at room temperature as a function of time for *n*MOSFETs stressed in inversion at 3 MV/cm at 150 ℃. The curves do not exhibit any significant shift with stressing time; the threshold voltage shift (ΔV_{th}) is less than 1 mV. Even if we increase the stress temperature up to 250 °C, the magnitude of ΔV_{th} is

only ~ 4 mV after 20 hour stress (Fig. 29). This shows the relative stability of these 4H SiC devices under inversion bias at elevated temperatures.

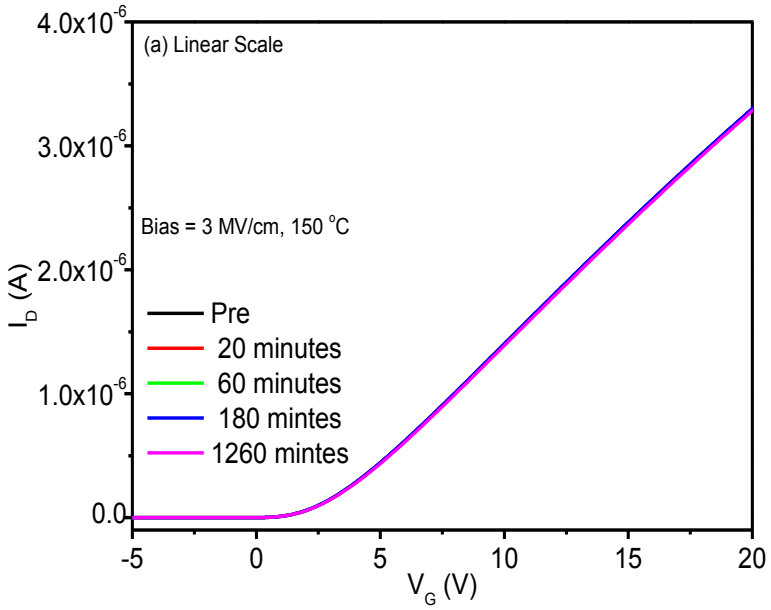


Fig. 28. Drain current as a function of gate voltage (I_D-V_G) and stress time for 4H-SiC nMOSFETs. The stress bias is +3 MV/cm and the temperature is 150 ℃ (after [73]).

Fig. 30 shows I_D-V_G curves measured at room temperature as a function of time for *n*MOSFETs stressed under accumulation bias at −3 MV/cm at 150 °C. At this stress bias, the curves shift monotonically negatively with stress time due to hole trapping. The corresponding threshold voltage shift is shown as a function of stressing time in Fig. 31. The magnitude of the midgap voltage increases monotonically at early stress times, with saturation at longer times. These negative shifts are caused primarily by the ionization of deeper acceptor levels [62] in these SiC MOSFETs, as we discuss in detail elsewhere [72]. We now provide a brief summary of several converging lines of evidence from capacitor and transistor experiments that support this interpretation of the result.

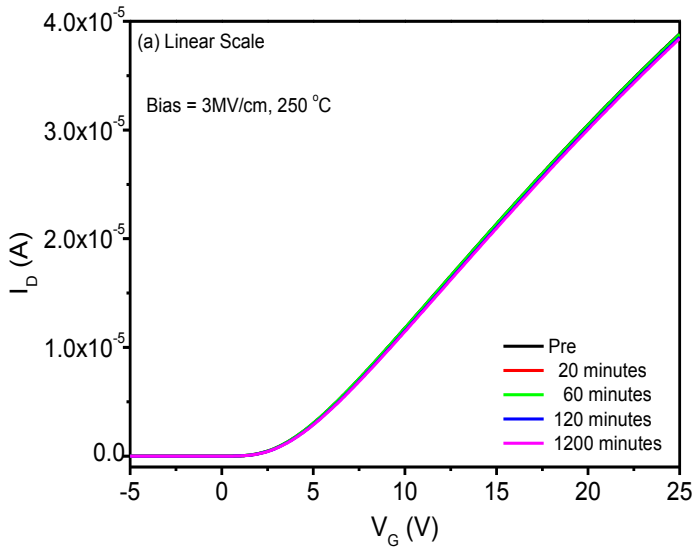


Fig. 29. Drain current as a function of gate voltage (I_D-V_G) and stress time for 4H-SiC nMOSFETs. The stress bias is +3 MV/cm and the temperature is 250 ℃ (after [73]).

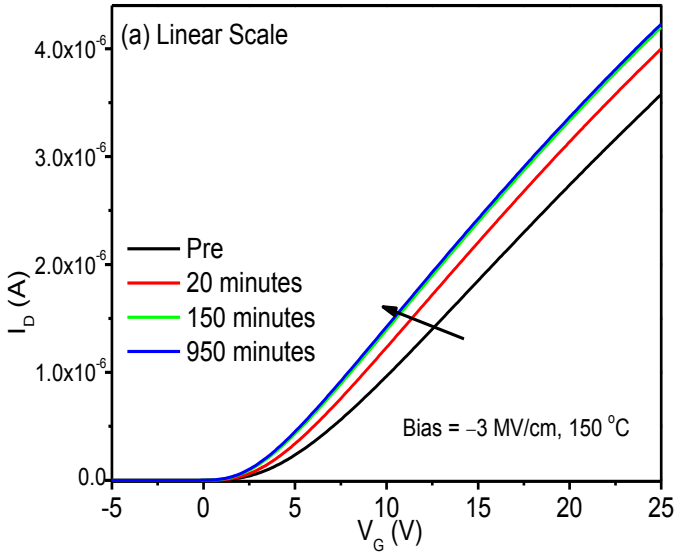


Fig. 30. Drain current as a function of gate voltage (I_D-V_G) and stress time for 4H-SiC nMOSFETs. The stress bias is –3 MV/cm and the temperature is 150 °C (after [73]).

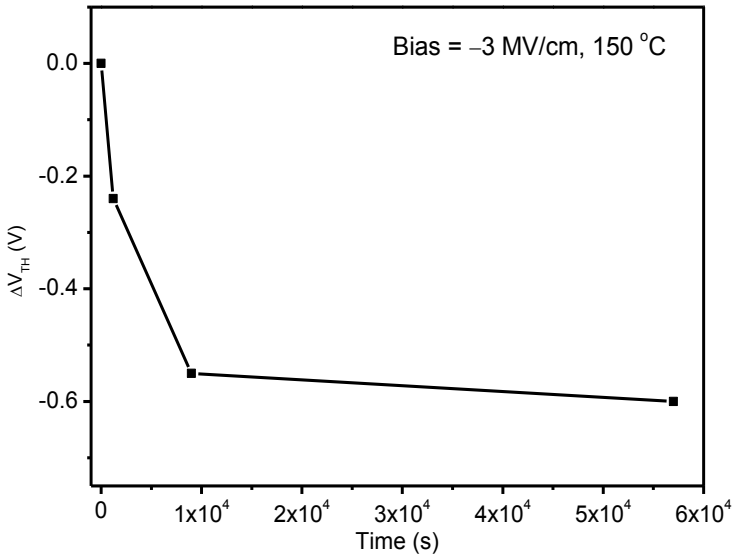


Fig. 31. Threshold voltage shifts (ΔV_{th}) as a function of stress time for the 4H-SiC nMOSFETs of Fig. 27 (after [73]).

Fig. 32 shows bias-temperature stress experiments on *p*-substrate capacitors processed in the same lot as the *n*MOSFETs. These results show that the effective activation energy for these devices (~ 0.23 ± 0.02 eV) virtually coincides with the known ionization energies of the Al dopants in 4H-SiC, 0.20 to 0.22 eV [72],[96],[97]. These ionization energies are larger than respective energies in Si. Whereas dopants in Si are fully ionized at room temperature, the deeper dopants in SiC are only partially ionized [72],[100].

A simple calculation shows that, of the ~ 6×10^{15} cm^{-3} Al acceptors, assuming an ionization energy of ~ 0.20 eV, only ~ 50 % are ionized at room temperature [72]. At the elevated temperatures of the BT stress, additional carriers are released from the dopants under these accumulation stress-bias conditions. The excess carriers are available to tunnel into border traps [101] and increase the midgap voltage shift. This mechanism is significant and apparently rate-limiting in SiC MOS devices under these stressing conditions because SiC at or a few hundred ℃ above room temperature has more defects and fewer carriers, as compared with Si. Thus, the availability of carriers has significantly more effect on NBTI in SiC MOS capacitors than on similarly biased Si MOS capacitors. In support of this interpretation, we note than no significant PBTI is observed for transistors biased in inversion in Fig. 28, 29, under conditions that are higher in

temperature and longer in time to those shown for devices in accumulation in Figs. 30. This is because it is very difficult for inversion layers to form in 4H-SiC capacitors, owing to its wide band gap, at temperatures even as high as a few hundred ℃ [62],[101],[93]. Similarly, interface trap levels that are away from the band edges are quite slow to populate in SiC MOS devices [62],[93]. Hence, carrier availability can affect BTI due to both interface and oxide trap charge effects in SiC MOS devices much more significantly than in Si MOS devices.

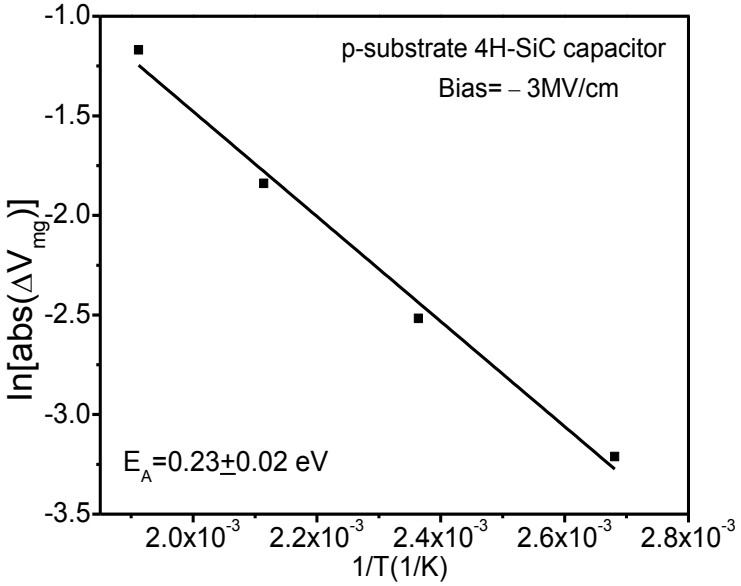


Figure 32. Logarithm of the absolute value of the midgap voltage shift as a function of the reciprocal of the temperature for *p*-substrate/4H-SiC MOS capacitors stressed for 20 minutes at –3 MV/cm (after [81]).

In addition to differences in dopant ionization and carrier density, there are other differences between Si MOS and SiC MOS devices that must be considered. The gate oxides on SiC are thicker and grown at higher temperatures than the ultrathin nitrided SiO_2 and/or high-K gate dielectrics used in Si-based integrated circuit technologies [37], [71],[76]. For Si MOS technologies, hydrogen is known to play an important role in both the passivation of process-induced interface traps and the creation of defects during bias-temperature stress [14],[44],[86]. Hydrogen reactions at the SiC interface are typically not as effective in passivating interface traps as at the Si/SiO_2 interface [19],[22],[30], so the role of hydrogen in BTI on SiC is less clear. Excess nitrogen associated with the NO

nitridation treatments used to reduce interface-trap densities in these SiC devices [20],[23],[24],[31] may also introduce a relatively small but finite density of N-related trap levels in the near-interfacial SiO_2. N-related centers are observed to function as both electron traps and hole traps [80],[90]. Moreover, nitrogen has been demonstrated to increase NBTI in oxides on Si [80],[102]. However, NO processing typically has been found to improve the characteristics to NO annealed devices [23],[24],[49],[103]. So we emphasize that, if N-related defects play a significant role in the observed response, it is the excess nitrogen concentration above and beyond the levels required to passivate the process-induced defects that are likely contributing to the BTIs. Further, holes trapped by N-related defects typically are re-emitted when the temperature is raised past 125 ℃ [26]. So it seems more likely that O vacancies may play a role in the hole trapping in these devices (20), similar to what is found for Si MOS devices stressed at similar temperatures but higher electric fields (e.g., > 5 MV/cm) [45],[80],[104].

Fig. 33 shows the values of ΔV_{TH} as a function of switched stressing biases for 4H-SiC based *n*MOSFETs. The characterization was performed at room temperature before and after BT stressing at 150 ^{o}C. The V_{TH} shifts negatively after the first 20-minute negative-bias stress, and then recovers somewhat during the next 20-minute positive-bias stress. In contrast, an additional increase in V_{TH} shift is observed in the second period (60 minutes) of positive-bias stress that follows the second negative-bias stress (60 minutes). Smaller shifts but significantly more reversibility is typically observed for Si MOS capacitors subjected to similar switched-bias stressing conditions [37],[69]. For the SiC MOS devices of Fig. 33, the majority of trapped holes remain in interface and/or oxide traps despite the reverse bias stress, showing that hole traps are more stable than electron traps in these devices [72]. The significant increase in the magnitude of the midgap voltage shift during the second period of PBT stress may result from the bias-induced motion of trapped positive charge in the SiO_2 layer from trapping sites within the oxide to sites at or closer to the SiC/SiO_2 interface. The trapped charge is likely to comprise mostly trapped holes. In oxides in Si, many of these holes would be neutralized via electron compensation [69],[75], but charge generation rates in SiC are significantly less than in Si [62],[93], so fewer electrons are available to compensate the trapped holes in SiC MOS capacitors than Si MOS capacitors. It is also possible that some of the trapped

positive charge is in the form of H^+ [95],[96]. Positive charged mobile ions have not been ruled out as the agents too. If H^+ is the agent in these oxides on SiC, then the results of Fig. 33 suggest that the H^+ in the SiO_2 can move closer to the SiO_2/SiC interface during the application of PBT stress. These H^+ cannot easily enter the SiC or be compensated by the lower density of electrons that are present in deep depletion under positive bias for *p*-type substrates, in constrast to the higher density of electrons that are present in accumulation for *n*-type substrates. However, there must not be a significant amount of interface trap formation, or the midgap voltage shift would be positive instead of negative, under positive bias. Trapping of H^+ at defects in the near-interfacial SiO_2 regions of oxides with high O vacancy densities has been observed in Si MOS devices [97], so this interpretation of the results is also consistent with Fig. 33.

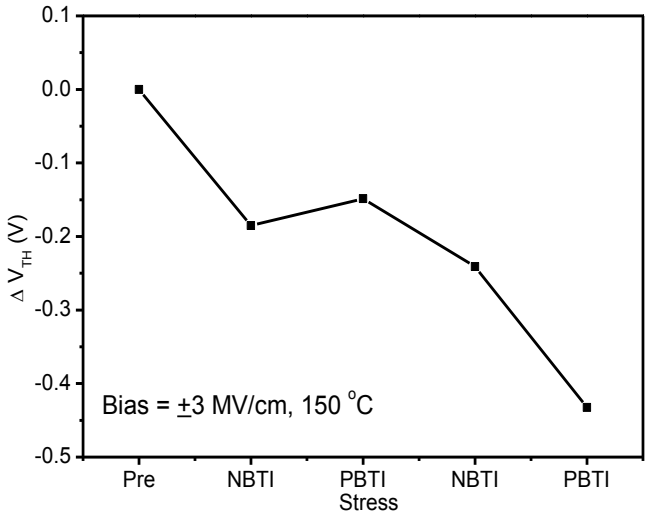


Fig. 33. ΔV_{TH} as a function of switched-bias stress for 4H-SiC nMOSFETs. The electric field during the stress was ± 3 MV/cm; the temperature was 150 ℃; the stress times were 20 min. for the first pair of stresses, and 60 min. for the second pair (after [73]).

Conclusion

We have performed a detailed experimental study of bias-temperature-instabilities in 4H-SiC based metal-oxide-semiconductor (MOS) transistors before and after total ionizing dose irradiation. For unirradiated devices, the threshold voltage shifts negatively under negative bias due primarily to hole trapping at or near the SiC-SiO_2 interface. The *p*-type dopants are only partially ionized at room temperature, while at elevated

temperatures, further ionization leads to additional carriers that are available for trapping by interface and oxide defects. The effective activation energy between room temperature and ~250 ℃ for NBTI is 0.12 ± 0.02 eV for the *n*-substrate capacitors and 0.23 ± 0.02 eV for PBTI for the *p*-substrate capacitors. O vacancies are found to play a significant role in this degradation, but a supporting role for deep interface traps and N-related defects is also possible. The low effective activation energies are comparable to results observed for Si MOS capacitors, but the mechanisms responsible for the BTIs in SiC MOS devices appear to be different in origin from those in Si MOS devices. The magnitudes and the time dependencies of the BTI responses observed in these SiC-based MOS structures differ significantly from what are typically observed for Si-based MOS devices with ultra-thin gate oxides. Shifts are larger for SiC-based devices than for Si-based devices, and do not follow a simple power-law time dependence, as commonly observed in Si-based MOS devices. Switched-bias stress experiments reveal a complex interplay among charge trapping and redistribution effects that warrant follow-on studies.

CHAPTER VI

TEMPERATURE DEPENDENCE AND POST-IRRADIATION ANNEALING RESPONSE OF THE 1/*f* NOISE OF 4H-SIC MOSFETS

Introduction

In this chapter, detailed studies of the temperature and voltage dependences of the low-frequency noise of 4H-SiC MOSFETs (shown in Fig. 13) and TCAD simulations show that the noise is caused primarily by interface traps. First-principles calculations identify these traps as carbon vacancy clusters and nitrogen dopant atoms at or near the SiC/SiO_2 interface.

The defects that cause low-frequency noise are often difficult to identify [105], complicating efforts to improve device performance and reliability. Oxygen vacancies in the near-interfacial SiO_2 (border traps) are the most common defect responsible for 1/*f* noise in Si MOS devices [33]. 4H-SiC MOSFETs are promising candidates for high-temperature and high-power electronics applications due to the wide band gap of SiC and breakdown voltage. Defects at or near the SiC/SiO_2 interface degrade the transistor mobility significantly, relative to its bulk value [1].

In this Chapter, we evaluate the charge trapping properties and low-frequency noise of 4H-SiC MOSFETs as a function of voltage, measuring temperature, and irradiation and post-irradiation annealing responses. The magnitude of the 1/*f* noise decreases significantly with increasing temperature. We find that the magnitude of the 1/*f* noise decreases significantly with increasing temperature. No significant change in the magnitude or frequency dependence of the noise is observed after irradiation or post-irradiation annealing. TCAD and density functional theory (DFT) calculations assist the characterization of the density, energy distribution, and microscopic nature of the defects in these devices. There are two significant findings: (1) The results strongly suggest that the 1/*f* noise in 4H-SiC MOSFETs is caused primarily by slow interface and border traps, and is not strongly affected by bulk oxide trap charge. (2) A dominant defect responsible for low-frequency noise and interface traps in 4H-SiC MOSFETs is newly identified via DFT calculations as a carbon vacancy cluster at the SiC/SiO_2 interface. Additional

contributions to the noise from N dopants at or near the Si/SiO_2 interface are likely at low temperature. Hence, the location and nature of performance-limiting defects differ significantly for 4H-SiC and Si MOSFETs.

Experimental details

A. 1/f Noise measurements

Low frequency noise measurements were performed as a function of frequency, gate and drain voltage, and temperature, using the experimental configuration described in chapter III. The dependence of the excess noise on frequency, drain voltage, and gate voltage in MOSFETs typically follows [52]. Other background information has been provided in chapter I. The input-referred gate-voltage noise-power spectral density, $S_{Vd} = S_{Vg} V_d^2 / (V_g - V_t)^2$, measured in the linear mode of device operation, can be described with a number fluctuation model [33],[52],[77],[106]:

$$S_{Vg}(f, V_g, T) \approx (V_g - V_t)^{\beta} \frac{q^2}{C_{ox}^2} \frac{k_B T D_t(E_f)}{LWf^{\alpha} ln(\tau_1 / \tau_2)} \qquad (5)$$

Here C_{ox} is the capacitance per unit area, k_B is the Boltzmann constant, $D_t(E_f)$ is the effective areal trap density, T is the temperature, and τ_1 and τ_2 are high and low frequency "cutoff" times for the noise measurements ($\tau_1/\tau_2 \sim 10^5$ for the test conditions here), and α and β are empirical factors that denote the frequency and gate-voltage dependence. Values of α are the same whether one characterized the noise via S_{Vd} or S_{Vg}; however, the value of β are different. For example, for a uniform energy distribution of traps, $\beta = 2$ when number fluctuation noise is parameterized via S_{Vd}, but $\beta = 0$ for the input-referred noise, since the V^2 voltage dependence is already incorporated in its formulation [33],[52],[77],[106].

B. Irradiation and annealing response

Devices were irradiated at the wafer level with 10-keV x-rays at a dose rate of 31.5 krad(SiO_2)/min at room temperature, with an applied gate bias of 8.5 V, resulting in an electric field of +1.6 MV/cm across the gate oxide. Devices were also annealed at the

same bias after radiation at 120 ℃ for times up to 667 hours. Details were provided in chapter Ⅲ.

Experimental results and discussion

A. Gate-voltage dependence

Fig. 34 shows S_{Vg} as a function of frequency f, and Fig. 35 shows S_{Vg} at f =10 Hz as a function of gate voltage. For number fluctuation noise with a uniform density of traps, all of the data in Fig. 35 would lie on a single curve, and β would equal zero in Fig. 34. Instead, β is 1.2 ±0.1. The β value indicates the slope of *Sv* VS f to be ~ 0.7-0.9, close to the result of 0.5 shown in Fig. 11 with a differenct definition by Eq. (5). These results demonstrate that the defect energy distribution $D_t(E_f)$ increases significantly as the Fermi level moves toward the conduction band edge [52],[107], a result that is consistent with prior measurements of the interface-trap energy distribution of 4H-SiC MOS devices [108].

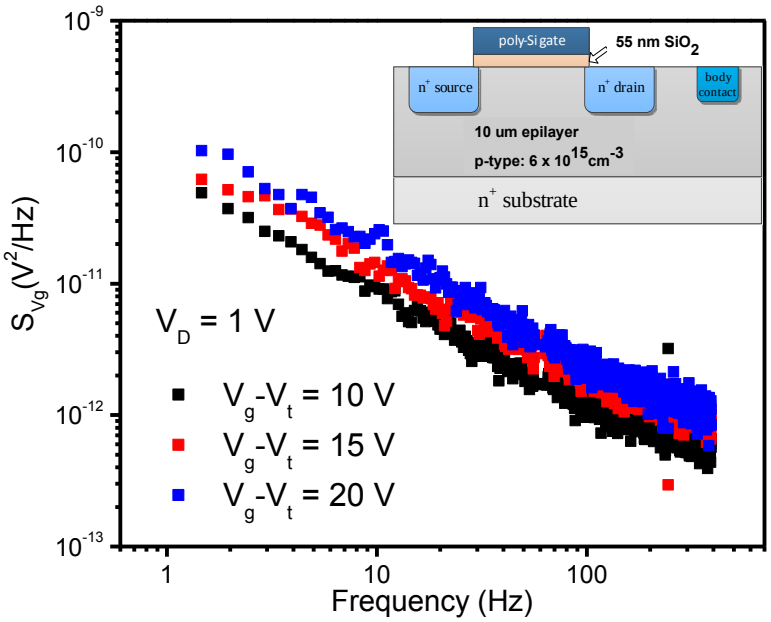


Fig. 34. Excess gate-voltage noise power spectral density S_{Vg} as a function of f for V_d = 1.0 V at V_g-V_t = 10 V, 15 V, and 20 V (after [109]).

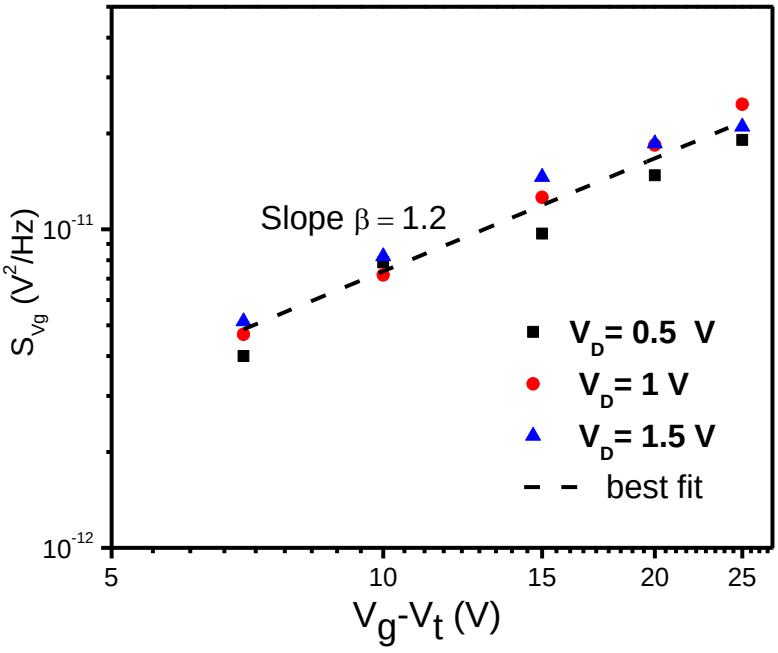


Fig. 35. Excess gate-voltage noise power spectral density S_{Vg} at f = 10 Hz as a function of V_g-V_t for V_d = 0.5 V, 1.0 V, and 1.5 V. The value of the gate voltage dependence parameter β = 1.2 ± 0.1 in the figure is estimated from best fit slopes to the lines. After [109].

B. Temperature dependence

The drain current I_D versus gate voltage V_G is shown as a function of measurement temperature T at 85 K, 300 K, and 420 K in Fig. 36. The threshold voltage shifts negatively and the drain current increases monotonically with increasing temperature, due to a decrease in interface-trap density, as we discuss in detail below.

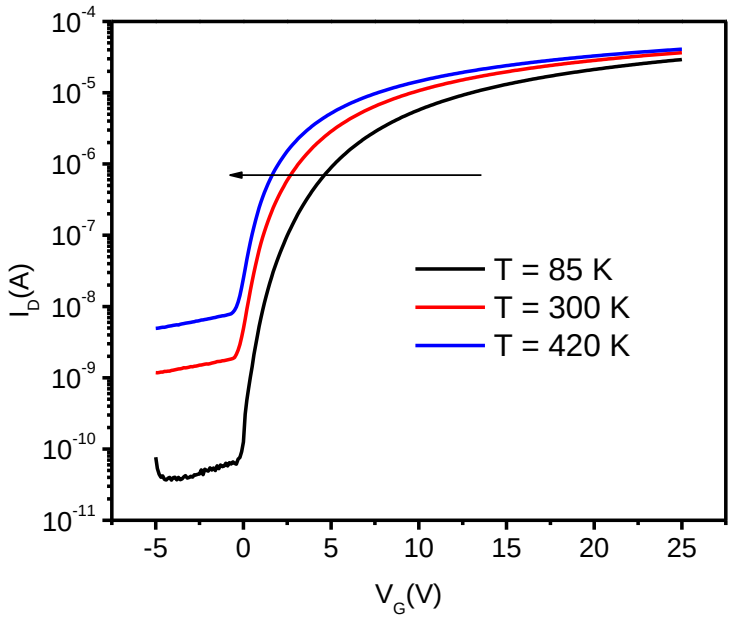


Fig.36. Drain current I_D-gate voltage V_G characteristics at varying temperature (after [109]).

We have measured the temperature dependence of the noise at fixed values of $V_g - V_t$ (10 V) and V_d (1 V). The threshold voltage of these devices varies significantly with temperature, consistent with previous work [56],[109],[110],[111],[112]. Fig. 37 shows the excess gate-voltage noise power spectral density S_{vg} as a function of frequency f at four temperatures. At each temperature, the noise was measured with the gate bias $V_g - V_t$ = 10 V, and a constant drain-source voltage V_{ds} = 1 V. The noise power spectral density decreases significantly as the temperature increases.

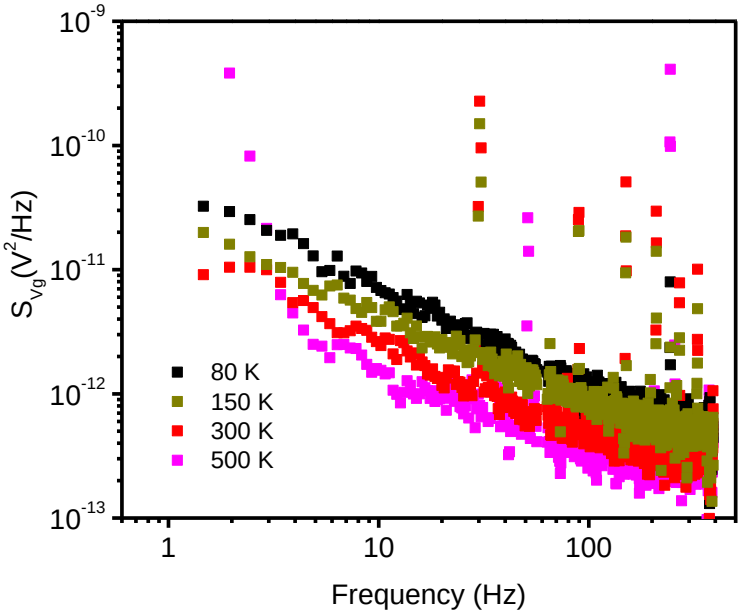


Fig. 37. Excess gate-voltage noise power spectral density S_{Vd} as a function of frequency f at 85 K, 150K, 300 K and 500 K (after [109]).

The nature of the traps that lead to 1/f noise in 4H-SiC MOSFETs is not well known [108]. Via first-principles density functional theory (DFT) [113] calculations using a hybrid exchange-correlation functional [114], we found that Si-Si bonds, which contribute significantly to Si MOS noise [115], do not exhibit appropriate energy levels in the near-interfacial SiO_2 layers of 4H-SiC MOSFETs. This is the case even if we strain them (by compressing the Si-Si bond length to 2.36 Å or stretching it to 3.03 Å) or consider clusters up to four Si-Si bonds. Instead, we found that carbon vacancy clusters on the SiC side of the interface have the necessary shallow levels. Fig. 38(a) shows defect levels of carbon vacancy (V_C) clusters that consist of one to four V_C's. The 2 V_C, 3 V_C, and 4 V_C clusters have energy levels at or near the bottom of the SiC conduction band. Although it is often believed that the SiC/SiO_2 interface contains excess carbon [12],[32], carbon vacancy clusters can form as carbon atoms at the oxidizing interface react with oxygen to form CO or CO_2 during the oxidation process. In addition to carbon vacancy clusters, incompletely ionized N dopants at the SiC/SiO_2 interface from post-oxidation NO processing, which exhibit an activation energy of ~0.10-0.12 eV [116],[118], may also contribute to fluctuations in carrier number at low temperatures.

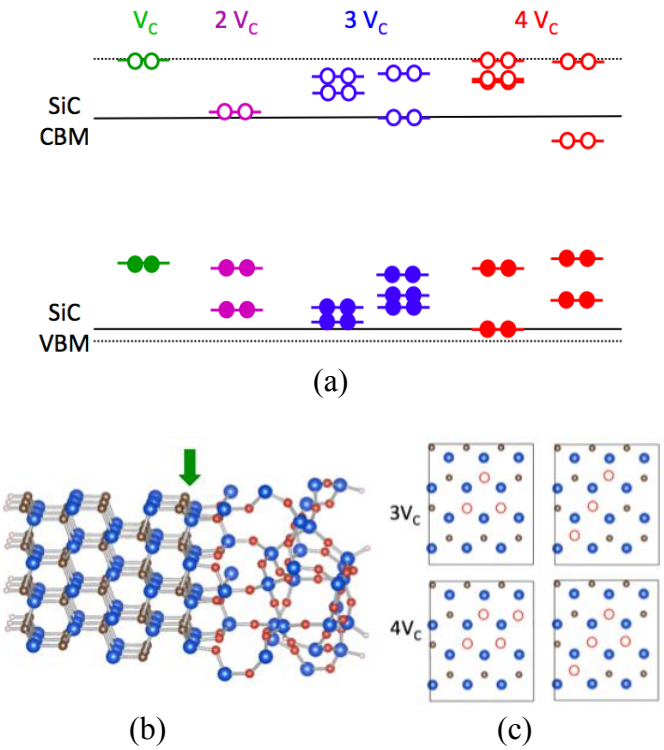


Fig. 38. (a) Defect levels of carbon vacancy clusters on the SiC side of the SiC/SiO_2 interface. The dotted black lines represent the positions of the SiC conduction and valence bands, obtained from the interface model shown in (b). The solid black lines represent the band positions after correcting for the quantum confinement effect due to the finite slab thickness. (c) Locations of removed carbon atoms are shown for the first SiC layer (green arrow in (b)) for the clusters of 3 and 4 carbon vacancies in (a) (after [109]).

Fig. 39 shows the excess gate-input-referred noise power spectral density S_{Vg} at ~10 Hz as a function of temperature. The magnitude of the 1/*f* noise decreases by ~77% as the temperature increases from 85 K to 510 K. Using Eq. (5), the effective density of traps $D_t(E_f)$ is estimated to be 2.3×10^{13} $eV^{-1}cm^{-2}$ at T = 85 K, decreasing to 3.2×10^{12} $eV^{-1}cm^{-2}$ at 300 K [109], and finally to 1×10^{12} $eV^{-1}cm^{-2}$ at 510 K. Qualitatively, the decrease in noise with increasing temperature is consistent with the decrease in density of interface traps and increase in percentage of ionized N dopant atoms associated with NO annealing [109],[117],[118]. The results and analysis of Figs. 34-39 strongly confirm that the low-frequency noise of 4H-SiC MOSFETs is dominated by slow interface and border traps

[109]. We now discuss the dependence of noise magnitude on temperature more quantitatively.

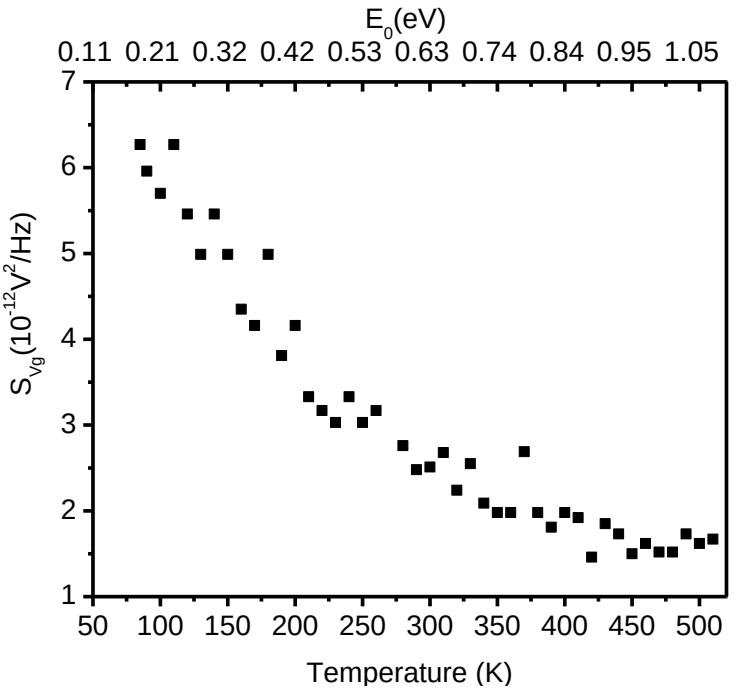


Fig. 39. Excess gate-voltage noise power spectral density S_{Vg} at ~10 Hz as a function of temperature from 85 K to 510 K (after [109]).

C. Energy distributions for noise

For comparison of these results with other technologies, the Hooge number α_H can be expressed in terms of S_v and the normalized noise magnitude K [52],[53] as Eq. (2) and (4):

$$K = S_{Vd} f (V_g - V_{th})^2 V_d^{-2} \qquad (2)$$

$$\alpha_H = \frac{KLWC_{ox}}{q\left(V_g - V_t\right)} \qquad (4)$$

At f = ~10 Hz, $V_g - V_t$ = 10 V. At room temperature, α_H is ~ 5×10^{-3} for the devices of Fig. 39. This result agrees to within a factor of ~2 with the value of α_H (~ 2.4×10^{-3}) obtained for 4H-SiC devices in [56]).

It is useful to check whether the temperature dependence of the noise in these devices can be described by the model of Dutta and Horn, which is a method to evaluate

the role of thermally-activated random processes in determining the temperature dependence of the noise [50],[51]. The frequency dependence of the noise is characterized through the slope of the plot of S_V as a function of f: $\alpha = -\frac{\partial lnS}{\partial lnf}$. For a process in which the temperature dependence of the noise is determined primarily by thermally activated capture and emission, and/or scattering processes, the frequency and temperature dependence of the noise magnitudes are coupled via the relation (Eq. (3)):

$$\alpha(\omega,T) = 1 - \frac{1}{ln(\omega\tau_0)}\left(\frac{\partial lnS(\omega,T)}{\partial lnT} - 1\right) \qquad (3)$$

where $\omega \equiv 2\pi f$ and $\tau_0 \approx 1 \times 10^{-12}$ [54].

Fig. 40 shows the frequency dependence of the noise (α) as a function of T for the data shown in Fig. 38. The overall shape of the measured $\alpha(T)$ curve is qualitatively consistent with the Dutta-Horn model, but there is an offset between the measured frequency dependence and that anticipated from the Dutta-Horn model at temperatures lower than 175 K and higher than 450 K. Similar offsets have been observed for noise measurements on carbon resistors [119] and SOI devices, for example. For these SiC devices, this offset appears to be caused at least partially by the incompletely ionized N dopants at the SiC/SiO_2 interface from post-oxidation NO processing [92], and partially by the decrease in trapped charge density with increasing temperature [72][109]. Despite the presence of this offset, one may infer the shape of the activation energy distribution of defects $D(E_0)$ from $S_v(T)$. The noise $S_v(T)$ is associated with thermally activated transition between defect states. The activation energy E_0 of a defect reconfiguration can be calculated via [119], as depicted on the top axis in Fig. 39 (Eq. (5)):

$$E_0 = -k_B T ln(\omega\tau_0) \qquad (5)$$

where k_B is Boltzmann's constant, T is the temperature, and $\tau_0 \approx 1 \times 10^{-12}$. In 4H-SiC MOS devices, first principles calculations show carbon vacancy clusters on the SiC side of the SiC/SiO_2 interface have activation energy levels of ~0.1 to 0.2 eV [109], and appear to be a promising candidate defect to account for the low-temperature noise peak at ~0.1 eV.

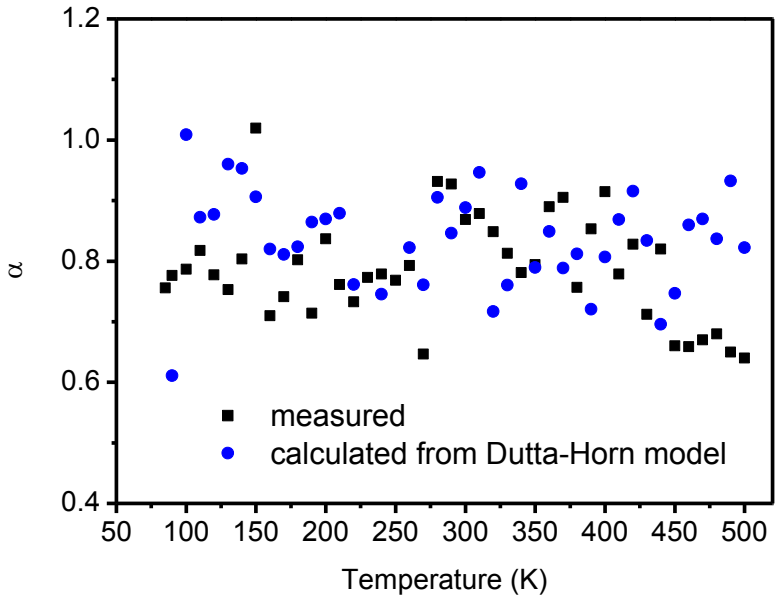


Fig. 40. Frequency dependence α of the noise versus temperature T for the devices of Fig. 38 (after [109]).

Threshold voltage values V_T extracted from I_D-V_G characteristics (Fig. 38) are shown as a function of temperature T in Fig. 41. A strong decrease in magnitude of V_T is observed with increasing T. Technology Computer Aided Design (TCAD) simulations were performed to model the experimental threshold value V_T, including the effects of partial ionization and Fermi-Dirac statistics [72],[121]. The best fit to the experimental data is found for a fixed positive charge density of ~3.4×10^{12} cm^{-2} over the entire temperature range. The slope of the V_T vs. T curve was reproduced well up to ~ 360 K in TCAD simulation with an interface-trap density that reaches a maximum of ~2×10^{13} $cm^{-2}eV^{-1}$ at the conduction band edge, and then decreases approximately exponentially in density as the distance from the band edge increases. The density of interface traps and fixed charge is consistent with the estimated effective density of traps via noise measurements in Fig. 39.

At temperatures above ~360 K, a simple exponential fall-off in trap density no longer matches the experimental results accurately. As seen in Fig. 41, at temperatures above 360 K, the density of interface traps decreases less rapidly than at lower temperatures. Below ~360 K, interface traps dominate the noise. The decrease in noise

occurs because of the reduction in trap density and increase in percentage of ionized N dopant atoms at or near the Si/SiO_2 interface with increasing temperature [107],[118], [119]. Above ~360 K, the noise from interface traps is greatly reduced from levels observed at lower temperatures. So now contributions to the noise from border traps become relatively more significant. Charge exchange between the channel and border traps occurs primarily via tunneling [33],[122],[123], which is less sensitive to temperature changes than is the occupancy of interface traps in these SiC MOS devices. Hence, the best-fit TCAD model in Fig. 41 includes border traps at energies of ~0.76 to 0.96 eV (corresponding to temperatures of 360 K to 460 K) below the conduction band, as illustrated schematically in Fig. 42. The resulting trap distribution exhibits a stretched exponential dependence, which is quite characteristic of low-frequency noise processes in semiconductor devices [124].

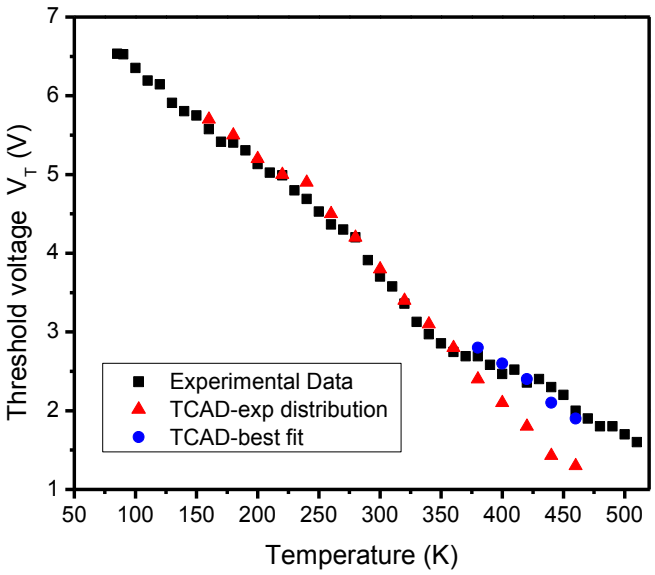


Fig. 41. Experimental and calculated threshold voltage V_T as a function of temperature T; the inset illustrates the change in occupancy of interface traps with T (after [109]).

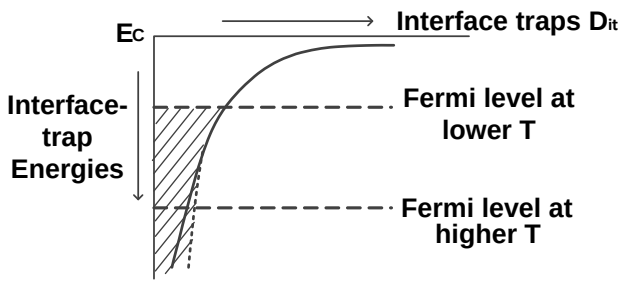


Fig. 42. Change in occupancy of interface traps as a function of temperature *T*. The solid line depicts an exponential reduction in trap density with increasing temperature, and the dotted line indicates a stretched-exponential trap distribution at higher *T*.

D. Irradiation and annealing response

To understand the role of radiation-induced oxide traps on the 1/*f* noise of 4H-SiC MOSFETs, we have measured the noise of the devices at room temperature as a function of X-ray irradiation dose and post-irradiation annealing time. Fig. 43 shows the drain current I_D as a function of gate voltage V_G for a sequence of X-ray irradiations, followed by elevated-temperature annealing, for 4H-SiC *n*MOSFETs with width/length ratio *W/L* = 400 μm/400 μm. The off-state leakage current increases with total dose and decreases with annealing time, and results from leakage currents associated with isolation oxides [31],[58],[64]. These leakage currents do not significantly affect the low-frequency noise. The negative shift in threshold voltage results from oxide-trap charge buildup in the SiO_2 gate dielectric, while annealing for long times leads to enhanced recovery. This is consistent with trends in radiation-induced hole trapping and annealing in previous work on MOS structures on both Si and SiC [31]-[33],[58],[64],[83].

Fig. 44 shows the change in radiation-induced oxide-trap charge density (projected to the SiC/SiO_2 interface) ΔN_{ot} as a function of total ionizing dose, extracted from the results of Fig. 43 via the midgap charge separation technique [83]. The value of ΔN_{ot} is 2.5×10^{12} cm^{-2} after the devices are irradiated to 1 Mrad(SiO_2). This is somewhat less than the process-induced fixed charge inferred from TCAD simulations on unirradiated devices, ~ 3.4×10^{12} cm^{-2}. In Fig. 45, the excess low frequency noise power spectral density S_{Vg} is shown as a function of irradiation dose and elevated-temperature-

annealing time. In contrast to what is typically observed for Si MOSFETs [33],[125],[126], there is no observable increase in S_{vg} after irradiation or change in noise level after very long-time annealing. Consistent with previous work, we assume that the effective density of interface traps D_t that contribute to the low-frequency noise can be estimated by the number fluctuation model [33],[122],[127]. With these assumptions, the value of D_t at room temperature is estimated to be $\sim 2.6\times 10^{12}\,\mathrm{eV^{-1}cm^{-2}}$.

This result is qualitatively consistent with interface and border traps at or near the SiC/SiO_2 interface contributing significantly to the low-frequency noise [109],[123]. Bulk oxide traps in such soft oxides are typically distributed more than 2-3 nm from the SiC interface [74],[128]. Therefore, those oxide traps do not fluctuate with the channel carriers significantly. Second, we note that the density of radiation-induced oxide-traps for the devices of Fig. 44 is much smaller than the interface trap density of the as-processed 4H-SiC devices (calculated above). Both the relatively high density of the interface traps and their proximity to the channel carriers lead to a more significant impact on the low-frequency noise, as compared with radiation-induced oxide-traps.

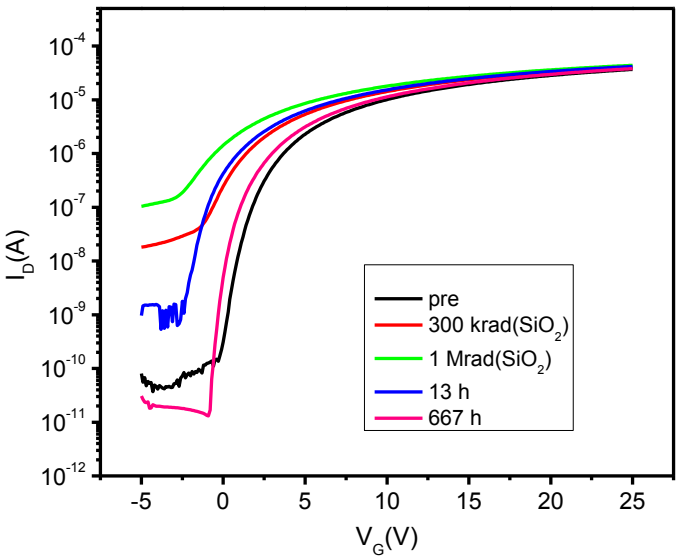


Fig. 43. Drain current I_D as a function of gate voltage V_G at varying total dose and annealing time. Irradiation and annealing biases are + 8.5 V. All of the current-voltage measurements through the irradiation and annealing experiments are performed at room temperature; the post-irradiation annealing is performed at 120 ℃ (after [109]).

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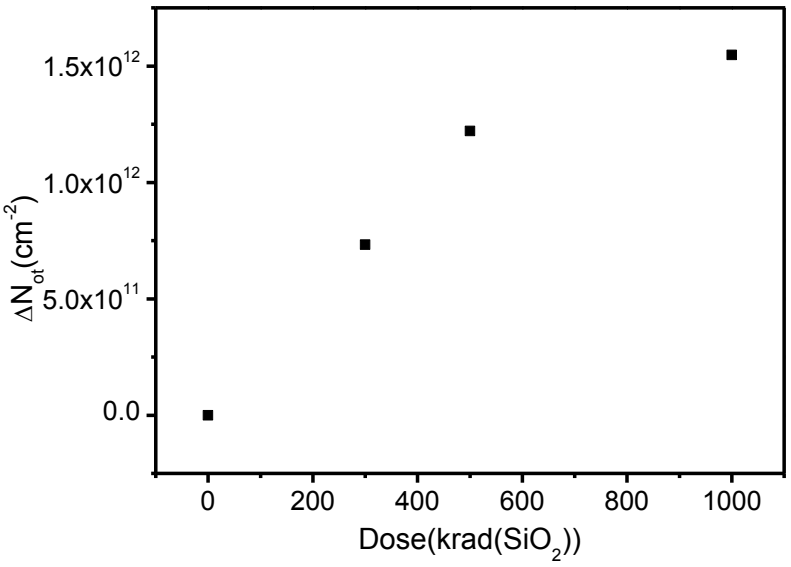

Fig. 44. ΔN_{ot} as a function of total dose for a SiC *n*MOSFET device with W/L = 400 µm/400 µm (after [109]).

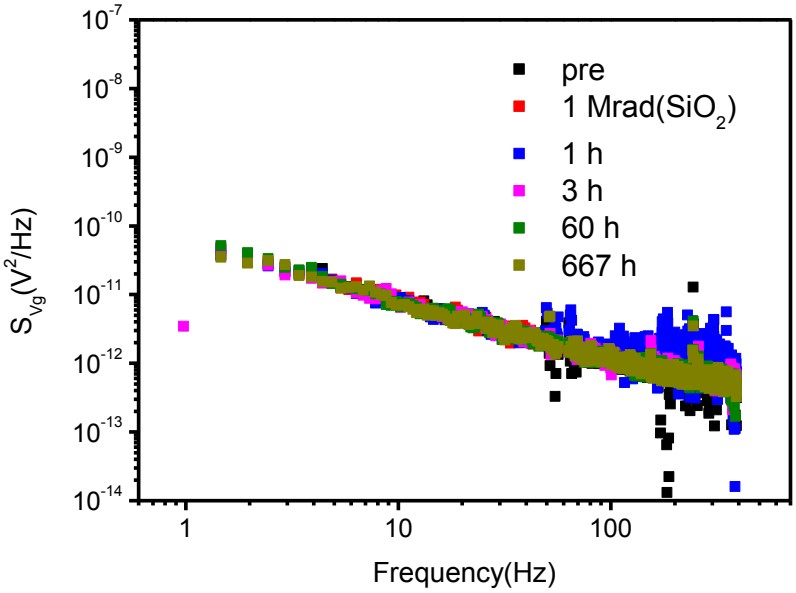

Fig. 45. Excess gate-voltage noise power spectral density S_{vg} as a function of frequency f after 1 Mrad(SiO_2) irradiation and elevated-temperature-annealing time (after [109]).

Summary and conclusions

The low-frequency noise of 4H SiC MOS transistors de-creases dramatically with increasing temperature, due to the decrease in density of interface traps with increasing temperature at temperatures below ~360 K. Above ~360 K, the contributions from border traps become relatively more significant to the noise. There is no observable increase in S_{Vg} after irradiation or change in noise level after 1.0 Mrad(SiO_2) irradiation and very long-time annealing. Due to the relatively low density of bulk oxide traps, as com-pared with densities of slow interface and border traps, the low-frequency noise of 4H-SiC MOSFETs is affected much more strongly by process-induced interface traps than bulk oxide traps, even after devices irradiated to 1.0 Mrad(SiO_2). These results contrast strongly with typical experience on Si/SiO_2 MOSFETs, in which interface traps are fast traps instead of slow traps, and as-processed interface trap densities are typically much lower than in these 4H-SiC MOSFETs.

CHAPTER VIII

CONCLUSIONS

In summary, a detailed experimental study of bias-temperature-instabilities has been performed in 4H-SiC MOS devices before and after total ionizing dose irradiation. For unirradiated devices, the threshold voltage shifts negatively under negative bias due primarily to hole trapping at or near the SiC-SiO_2 interface. The *p*-type dopants are only partially ionized at room temperature, while at elevated temperatures, further ionization leads to additional carriers that are available for trapping by interface and oxide defects. O vacancies are found to play a significant role in this degradation, but a supporting role for deep interface traps and N-related defects is also possible. The low effective activation energies are comparable to results observed for Si MOS capacitors, but the mechanisms responsible for the BTIs in SiC MOS devices appear to be different in origin from those in Si MOS devices. The magnitudes and the time dependencies of the BTI responses observed in these SiC-based MOS structures differ significantly from what are typically observed for Si-based MOS devices with ultra-thin gate oxides. Shifts are larger for SiC-based devices than for Si-based devices, and do not follow simple power-law time dependence, as commonly observed in Si-based MOS devices. Switched-bias stress experiments reveal a complex interplay among charge trapping and redistribution effects that warrant follow-on studies.

The irradiation and annealing responses of SiC MOS devices are investigated at varying bias. Radiation-induced hole trapping dominates the radiation effects of SiC MOS devices. Switching bias between irradiation and annealing can lead to significant enhancement of degradation in SiC MOS devices. The pair of positive/negative gate bias during irradiation/annealing on *p*-substrate capacitors is found to be the worst-case of degradation. After irradiation, the reversibility of charge trapping in switching bias annealing is observed in *n*-substrate capacitors; while the enhanced charge trapping is found in *p*-substrate capacitors. This work confirms the combined radiation and reliability

stresses can be challenging for certain combination of biases during radiation and long-term stress.

The temperature dependence of the low frequency noise of 4H-SiC *n*MOSFETs with nitrided oxides is further reported over the temperature range of 85 K-510 K. The 1/*f* noise decreases significantly with increasing measurement temperature. This decrease in noise results primarily from a decrease in the density of interface traps at increasing temperatures. The 1/*f* noise has also been characterized after total ionizing dose irradiation and post-irradiation annealing. No significant change in the 1/*f* noise is observed after the devices are irradiated to 1 Mrad(SiO_2) and then annealed at elevated temperature under bias. These results indicate that the 1/ *f* noise in 4H-SiC MOSFETs is dominated by the interaction of channel carriers with slow interface traps at temperatures below 360 K and with border traps above 360 K. This result contrasts with most experience with Si/SiO_2-based MOSFETs, and results from the wider band gap and greater density of slow interface traps in SiC/SiO_2-based MOSFETs than in Si/SiO_2-based MOSFETs.

While some of these results are qualitatively similar to effects observed in Si MOS, the mechanisms are much different in SiC MOS devices, resulting from the wider band gap, lack of free carriers, and greater density of slow interface traps in SiC/SiO_2-based MOSFETs than in Si/SiO_2-based MOSFETs. This work also identifies carbon vacancy clusters and/or incompletely ionized N dopants at the SiC/SiO_2 interface from post-oxidation NO processing, which both exhibit an activation energy of ~0.10-0.12 eV, may contribute to the possible degradation at low temperature.

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