RADIATION CHARACTERIZATION OF A RADIATION HARDENED LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) DRIVER AND RECEIVER

By

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CHAPTER I

INTRODUCTION

Low voltage differential signaling (LVDS) is becoming increasingly common in systems where high-speed, low-power data transfer across physical layer interfaces is required. The ever-increasing speed of microprocessor motherboards, optical transmission links, intelligent hubs and routers, etc., is pushing the off-chip data rate into the Gb/s-per-pin range [2]. There currently exist commercial products such as the Intel 925XE Express Chipset with chip to chip communication frequencies greater than 1 Ghz [1]. Additionally, while the reduction of power consumption is of great concern in portable systems, it is also required in other systems to reduce costs related to packaging and additional cooling systems. The LVDS technology was developed to provide a low-power and low-voltage alternative to other high-speed I/O interfaces for point to point data transmission [4] [5].

The desirable operating characteristics of the LVDS technology lend itself to use in a wide variety of electrical systems. One concern for the microelectronics industry is the effect of radiation on these devices. The shrinking of feature sizes necessary to achieve the high-speed and low-voltage characteristics of the LVDS circuits make them increasingly vulnerable to radiation damage due to single event effects (SEE). The increase in military electronics incorporating LVDS devices introduces a need for these devices to survive a military dose rate environment [6]. Unfortunately there is currently a severe lack of radiation effects research on LVDS devices.

In this thesis a LVDS driver and receiver pair was evaluated in the heavy ion and

dose rate radiation environments. Detailed quantitative computer simulations were performed to develop an understanding of the heavy ion and dose rate device response of the LVDS driver and receiver circuits. Existing simulation methodologies used for heavy ion and dose rate radiation simulations were evaluated and improved upon to obtain the most accurate results possible. These simulation results are currently being used to aid in physical radiation test planning for the recently fabricated LVDS devices.

Chapter II introduces the general LVDS driver and receiver operation and process technology which will be useful in later discussions. In Chapter III, an introduction to the dose rate and heavy ion radiation environments is given. In Chapter IV, the heavy ion simulation setup is described, and Chapter V follows with the results. Chapter VI details the setup and results for the dose rate simulations. Chapter VII discusses the simulation results and implications. Chapter VIII concludes this thesis by summarizing the important results of this work.

CHAPTER II

LVDS AND SOI PROCESS TECHNOLOGY BACKGROUND

LVDS technology utilizes differential data transmission and reception. The use of differential signaling has the advantage of being much less susceptible to common mode noise versus single-ended transmission standards [9]. The most popular consumer application for LVDS is data transmission to/from flat-panel displays, but the low-power, high speed aspects of the technology are also ideal for spaceborne and military applications [9].

An LVDS system is typically implemented with a driver and receiver pair as seen in Figure 1. The driver circuit inputs a CMOS logic signal and outputs a differential voltage. The differential voltage swing is small (typically 250-400 mV) to allow for fast switching characteristics [10]. The common mode voltage of the differential signal also varies from approximately 1.05 to 1.45 V to account for common mode noise in the transmission path. This differential voltage is terminated with a 100 ohm load before entering the LVDS receiver circuit. The receiver inputs the differential signal and outputs a CMOS logic signal. LVDS is a standardized technology described in IEEE STD 1596.3 [4].

The operation of a typical LVDS driver can be seen with the help of Figure 2. This figure shows a switch level and transistor level implementation of a typical LVDS driver, which will be used in all subsequent architectural discussions due to the proprietary nature of the specific driver used in this work. The switch level implementation in the left side of the figure shows four switches corresponding to

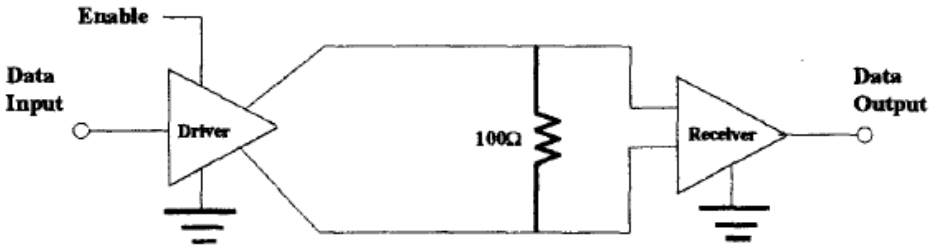

Figure 1: Typical LVDS driver and receiver pair. The differential signal is terminated by a 100 ohm resistor.

the logical value of 'D', 2 resistors and a current source designated by I_b. The bias current I_b changes polarity through the resistors depending on the logical state of 'D' and thus produces the correct output swing which is seen between V_{op} and V_{on}. The values of the two resistors are used to control the common mode voltage of the differential signal produced between V_{op} and V_{on}. The transistor implementation of this circuit which is seen on the right of Figure 2 simply replaces the switches with FETs M1 to M4 and the current sources with FETs M5 and M6. A snapshot of the electrical operation of the driver being tested can be seen in Figure 3. This snapshot was taken in the Cadence IC5.1.41 Spectre simulator under nominal test conditions. More detail on the simulation setup and conditions is given in future chapters.

A typical LVDS receiver at the transistor level is shown in Figure 4 [2]. The differential signal at the input, represented by V_{IN+} and V_{IP-}, is detected by a Schmitt trigger formed by FETs M1 to M6. The Schmitt trigger ensures that there is enough hysteresis (25 mV to 50 mV) necessary to meet the IEEE STD 1596.3 [4]. Full swing CMOS levels are obtained at the output, designated as V_{OUT}, by the inverter represented in FETs M7 and M8. The waveforms that ocur during operation of the receiver being tested can be seen in Figure 5.

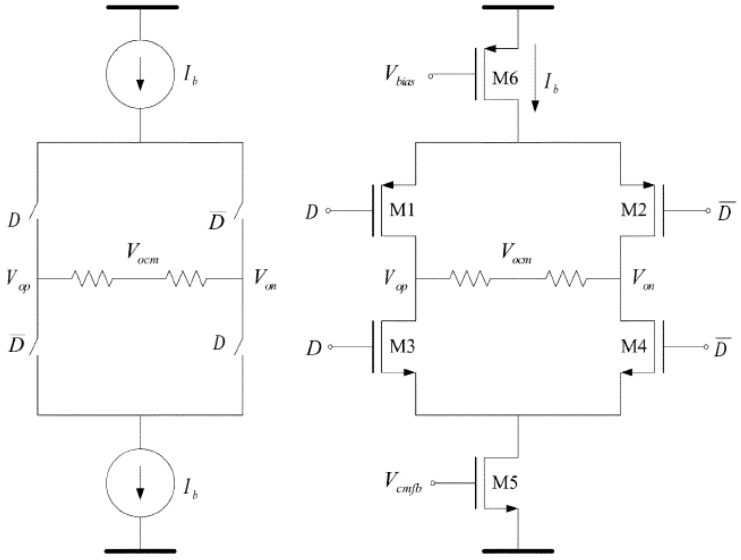

Figure 2: Typical architecture of a LVDS driver circuit. Note that the switch level implementation is shown on the left and the transistor level version is on the right.

The LVDS circuits in this thesis were taken after the final circuit layout was completed and the package defined. Because of this, all parasitic elements associated with the circuit layout have been back annotated into the SPICE level circuit. Also, the package parasitics have been defined using a standard LRC model and similarly annotated into the SPICE circuit. The inclusion of these parasitics increases the simulation time when running the circuit in a SPICE simulator, but significantly improves the accuracy of the resulting simulations. The LVDS SPICE circuits each exist in 2-bit form which taking into account the coupling and other associated effects that may be seen in the when the final device, which exists in 4-bit form, is physically tested. Simulations on the LVDS circuits were performed using the Spectre simulation tool on the Cadence IC5.1.41 Unix platform.

The LVDS driver and receiver circuits studied in this work were designed and fabricated in a proprietary partially depleted (PD) SOI process. This process technology

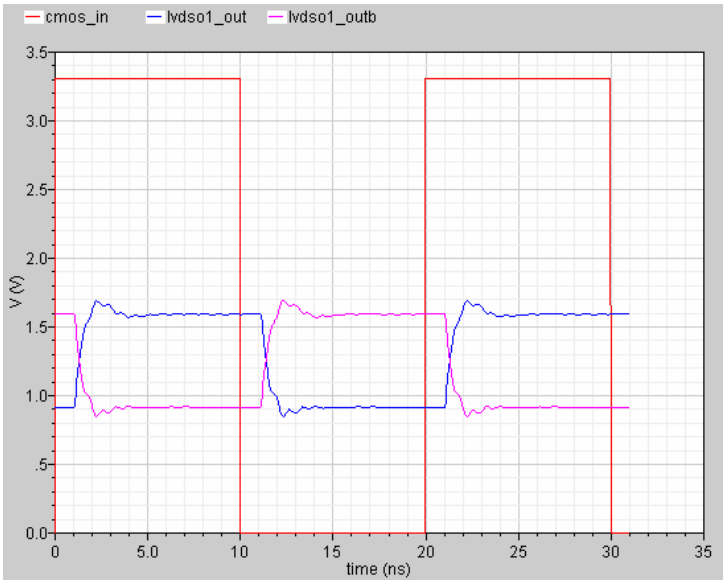

Figure 3: Electrical operation of LVDS driver under test in Spectre simulation environment.

has a significant effect on circuit performance in the heavy ion and dose rate radiation environments as is discussed in the next chapter. A cross-section of a typical PD SOI metal oxide semiconductor field effect transistor (MOSFET) device can be seen in Figure 6. This figure highlights some of the important differences between SOI and the traditional bulk complementary metal oxide semiconductor (CMOS) process. The first difference is the buried oxide (BOX) layer beneath the source, drain and body layers. The BOX layer allows for the transistor to function with a thinner epitaxial Si layer than its bulk counterpart. This thinner Si layer will have important consequences in the response of the transistor to radiation environments. The other side of the BOX layer exists as a mechanical substrate to give the SOI transistor the necessary mechanical support.

SOI devices are also able to incorporate transistor isolation schemes allowing for

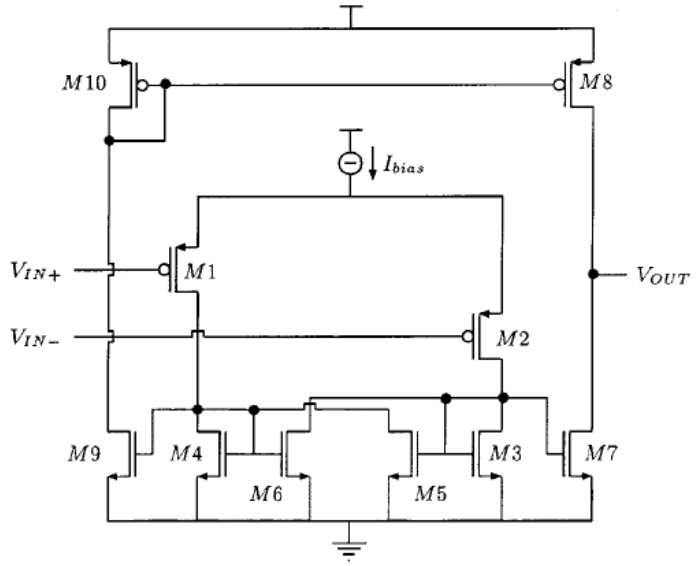

Figure 4: Typical architecture of a LVDS receiver circuit.

complete electrical isolation between adjacent transistors [11]. Bulk technologies typically cannot achieve this complete electrical isolation due to larger Si thickness in the active regions. Failure to achieve electrical isolation between adjacent transistors can lead to the creation of unwanted pnpn and npnp diffusion arrangements which can trigger the destructive latchup phenomenon [12].

A significant drawback to SOI devices is their difficulty to fix the potential of the body region. The body in a SOI device is typically floating, which introduces a parasitic bipolar junction transistor, as seen drawn into Figure 6. If the potential increases in the body of the SOI device, it may turn on the parasitic bipolar device by forward biasing its base emitter junction. This parasitic bipolar effect affects the radiation response being studied in this work and is discussed more in upcoming chapters.

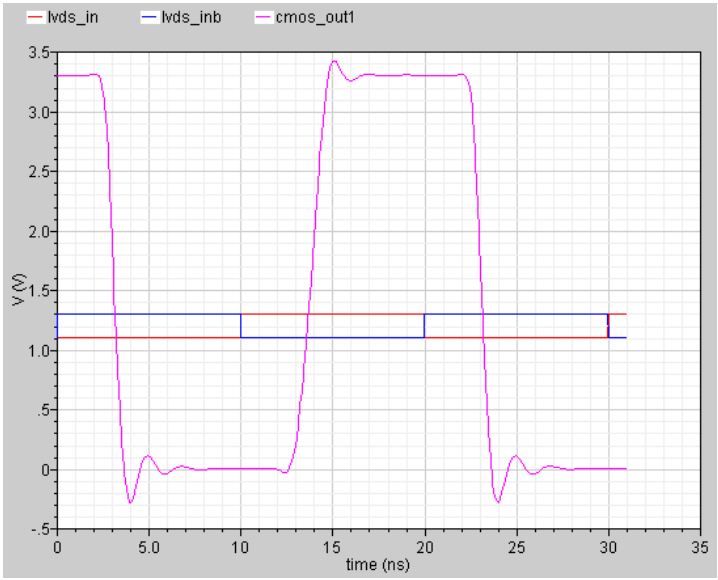

Figure 5: Electrical operation of LVDS receiver under test in Spectre simulation environment.

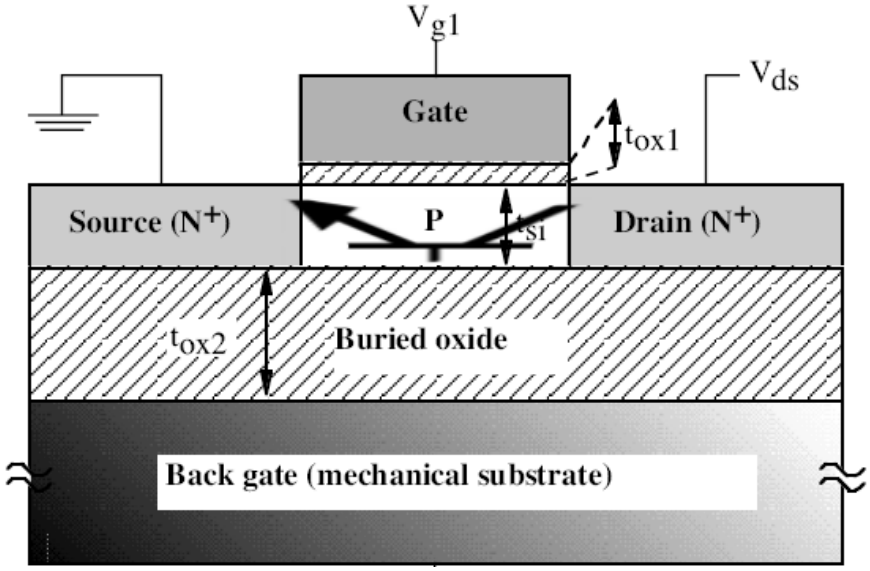

Figure 6: Typical cross-section of a Silicon-On-Insulator MOS Transistor. Note that the parasitic bipolar transistor is superimposed onto the cross-section.

CHAPTER III

SINGLE EVENT EFFECTS AND DOSE RATE RADIATION ENVIRONMENTS

The LVDS circuits discussed in this work were studied in the heavy ion and dose rate radiation environments. These environments have unique effects on both the LVDS driver and receiver circuits. A brief overview of these environments is presented to give the reader background to aid in interpreting simulation results and discussion.

The heavy ion radiation environment discussed in this thesis is part of a broader radiation effect category known as single event effects (SEE). Several types of energetic particles may cause a single event. Alpha particles that come from the radioactive decay of materials used in integrated-circuit packages have been a source of SEEs in the past [8]. Energetic neutrons and protons can produce SEs indirectly through elastic scattering or a nuclear reaction in silicon. Low energy neutrons can also interact with the boron in a semiconductor device to cause an SEE. The heavy ion section of this category are typically generated by solar flares or from deep space and are sometimes referred to as 'cosmic' or 'galactic' ions [13].

When an energetic nuclear particle penetrates any semiconducting material, it loses energy through Rutherford scattering (Coulumbic interactions) with the semiconductor lattice structure [13]. Through predominantly Compton interactions with the nuclei of the crystalline structure, the slowing of the particle as it transfers energy to the lattice leaves an ionization trail of free electron-hole pairs in its wake [13]. These excess charge carriers can deposit charge in unwanted places, often leading to voltage transients on the nodes of the circuit and current transients across device

junctions [13].

The rate of energy loss by the energetic particle due to scattering with the nuclei of the lattice is often expressed as stopping power, or linear energy transfer (LET) [13]. LET has the dimensions of energy per unit length along the path of the particle. The LET of any particle depends on the mass and energy of the particle as well as the density of the target material. Stopping powers and ranges for different ion species have been tabulated and catalogued or can be calculated with the TRIM computer code [14].

Charge deposition by an ion interacting with a semiconductor region can be calculated. On average, 3.6 electron Volts (eV) are needed to create one electron-hole pair in Si for highly energetic incident radiation. If the LET is constant along the path, and the density of the target material is known, the amount of charge created by ionization can be calculated by Equation 1. It should be noted that the energetic particle loses energy as it travels through its target material. Therefore the Equation 1 is valid over an incremental path length where the LET is constant [13]. The simplified equation for Si and its material properties is given by Equation 2 [13].

$$dQ[pC] = L(x)[pC/\mu m] \cdot dX[\mu m] = \frac{LET(x)[MeV/g/cm^2] \cdot p[g/cm^2] \cdot 1.6 \cdot 10^{-5}}{G[eV]} \cdot dX[\mu m] \tag{1}$$

$$L(Si)[pC/\mu m] = 1.035 \cdot 10^{-5} \cdot LET[MeV/g/cm^2] \tag{2}$$

The charge collected by the semiconductor region can vary significantly from the charge deposited by the energetic particle. Charge is typically collected in three ways across a pn junction. Drift depletion region collection occurs due to the E field in the

depletion region separating the electrons and holes to create a current in the direction of the E field. Field funneling occurs when the energetic particle distorts or stretches the depletion region allowing more electrons and holes to be collected by the E field. Diffusion occurs when charges generated within a diffusion length of the junction drift into the depletion region and are collected by the E field. It should be noted that the funneling charge collection component typically does not exist in SOI due to its small epitaxial Si thickness.

Factors such as recombination and charge amplification due to the parasitic bipolar structure found in SOI technologies can alter the charge that is collected and seen by the rest of the circuit. The next chapter will discuss charge collection in greater detail from a modeling standpoint while using Equation 2 to relate LET to deposited charge.

The dose rate radiation environment is typically uniform over the entire circuit [6]. Dose rate irradiations produce photocurrents throughout all pn junctions in every semiconductor device exposed to the radiation. The length of this irradiation typically varies in the range of nano to microseconds. The concentration of photons in the dose rate radiation environment is also variable. Dose rates encountered in the space environment may be small, where the dose rates in the military environments can be significantly larger. This thesis will focus on the military dose rate environment.

The photocurrents produced by a dose rate event are composed of a drift and diffusion component similar to two of the three main heavy ion charge collection components. These two components can be written in equation form as seen in Equation 3 [6]. In SOI, this can be simplified to Equation 4 because the diffusion component is negligible due to SOI's small epitaxial Si thickness [6].

$$I_{ph} = qg_0VD^{'} + f(L_n, L_p, \tau_n, \tau_n) \tag{3}$$

$$I_{ph} = qg_0VD^{'} + qg_0V\beta^*D^{'} = qg_0V(1+\beta^*)D^{'} \tag{4}$$

This chapter introduced the two types of radiation being studied in this work and the basic mechanisms behind their interaction with semiconductor materials. These basic mechanisms can be used with computer simulation tools to determine the effects that these types of radiation can have on semiconductor circuits. The next chapter discusses computer simulation techniques for simulating the circuit response of the LVDS devices during a heavy ion strike.

CHAPTER IV

HEAVY ION SIMULATION SETUP

The simulation of the LVDS driver and receiver during a heavy ion strike was completed using several proven computer aided design (CAD) tools, while adhering to and improving upon previously published simulation methodologies [20][19]. Improvements take advantage of the scalable nature of the transistors in the LVDS circuits and a database implementation scheme to provide very accurate and efficient modeling of the charge collection. The simulation methodology used in this work, as well as the test conditions for the LVDS circuits, will be described in detail in this section.

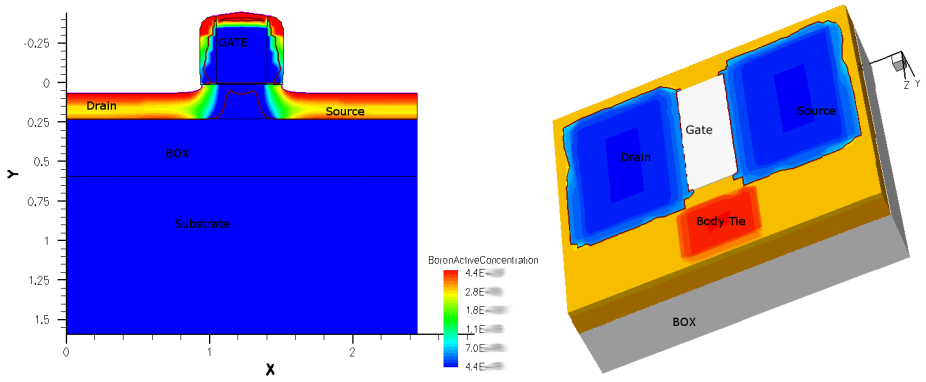

Figure 7: 2D and 3D cross-sections of pmos device generated in ISE Dessis TCAD tool.

The simulation methodology used in this thesis begins with modeling the charge collection profile at the device level and then extending that information to the circuit level to characterize the total circuit response. This is consistent with previous single-event modeling schemes [13]. The methods implemented and number of variables

Table 1: Variables taken into account with heavy ion simulation methodology.

Simulation Variables	**Range of Values**
Device Types	NMOS, PMOS
LET (MeV·cm^2/mg)	4,8,12,24,36,48,60,72,84,96,128
Absolute Value V_{DS}	0.7V, 1.8V, 2.5V, 3.3V
Strike location resolution in X axis (length)	0.1 μm
Strike location resolution in Z axis (width)	0.2 μm

taken into consideration during this charge collection modeling is unique and novel for modeling SEE in a circuit as large as an LVDS driver and receiver. A database was created logging the charge collection profiles of strikes at 11 different LET values ranging from 4 to 128 MeV·cm^2/mg, 85 spatial locations in 0.1μm increments on the length (x) axis of the transistor and 0.2μm along the width (z) axis of the transistor, and with drain source biases of 0.7V, 1.8V, 2.5V, and 3.3V. A flowchart outlining the major steps in this methodology can be seen in Figure 21.

The scalable nature of the technology used to fabricate the LVDS devices under study was used to define the spatial strike locations. Specifically, the fact that all transistors in these circuits shared the same length value and had varied width values was applied. The 0.1μm increment on the x-axis was chosen to allow for multiple strike locations in the drain, gate and source regions along the fixed length. The 0.2μm increment on the z-axis was chosen by striking at increasing z locations, noting where the resulting charge collection began to stabilize, and then dividing by five to allow for five different z-axis strike points. This stabilizing z axis location appeared at a distance of 1.0μm from the gate edge closest to the body tie, resulting in the 0.2μm increment on the z axis. Table 1 defines the different database parameters for which unique charge collection profiles were obtained.

The charge collection modeling began with the creation of 3D Technology CAD

(TCAD) models for the NMOS and PMOS devices in the proprietary process technology. The process technology is a gate array technology with a constant length parameter. Because of this, a single unique TCAD model for each of the NMOS and PMOS structures was sufficient to characterize the charge collection for all of the transistors existing in the LVDS driver and receiver circuits. The NMOS and PMOS TCAD models were created using proprietary doping files, material parameters, and material dimensions. A body contact was placed near the edge of one side of the gate region in order to replicate the technique seen in the physical transistor layout to minimize the effects of the floating body in the SOI transistor. To simplify the modeling, the mechanical substrate was omitted from the modeling and reduced to a electrical contact due to its lack of influence on device response in the heavy ion and dose rate radiation environments. The modeling was also simplified by modeling only one body contact in the device by effectively splitting the transistor in half across the length and height plane. The TCAD device designs were completed using the Synopsys ISE Devise tools [15]. The 2D and 3D cross sections of the device can be seen in Figure 7.

The devices were placed in Silicon measuring 2.2 μm on the x axis and 2.8 μm on the z axis. This choice in Silicon dimensions was justified by simulating the devices placed in Silicon measuring 200 μm on the x axis and 200 μm on the z axis and achieving comparable charge collection results. The larger size of Silicon allows for a more realistic charge collection simulation and a good comparison to determine if any reflections or other non-realistic behavior was occuring at the Silicon boundaries when simulating with the smaller Silicon. Charge collection results in the form of single-event drain current versus time curves can be seen for both sizes of Silicon in

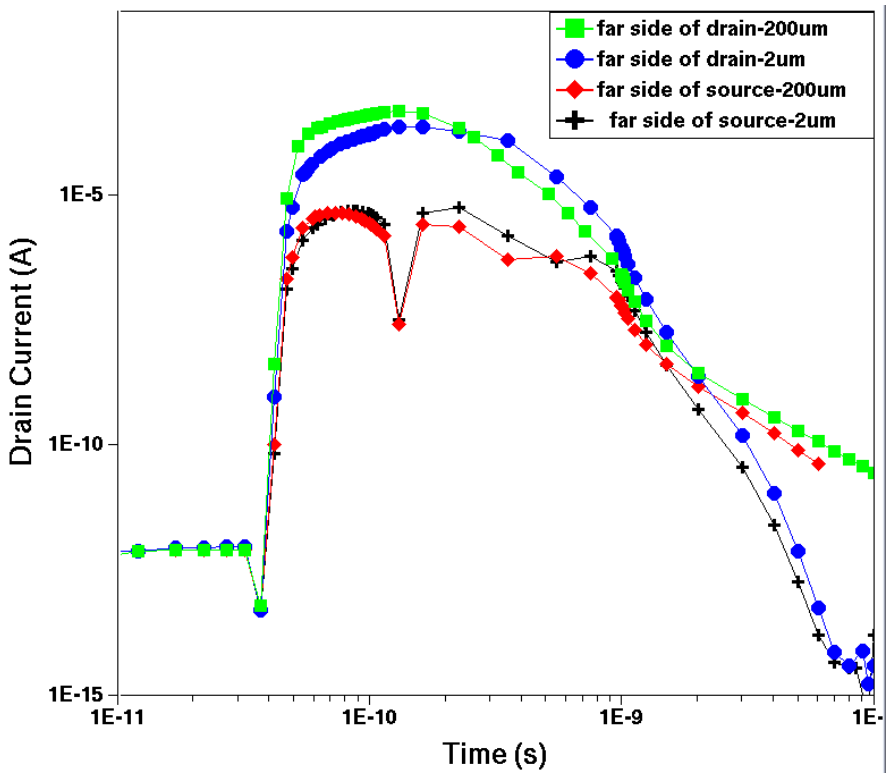

Figure 8: Single-event drain current curves for strikes at the extreme edges of the source and drain regions in the TCAD devices set on different Silicon dimensions. The TCAD devices used in this thesis are labeled as 2 μm in reference to the actual x axis length of Silicon and the more realistic device is labeled as 200 μm in reference to its x axis length of Silicon.

Figure 8. This figure plots the single-event currents of a 128 MeV·cm^2/mg strike at the extreme edges of the source and drain regions in both sizes of Silicon where reflections or other boundary effects would be most prominent. The strike locations on the smaller size of Silicon occur 0.4 μm from its Silicon boundary and the strike locations on the larger size of Silicon occur 99.3 μm from its Silicon boundary. The comparison between these two current responses illustrates that currents in the larger Silicon exhibit very similar behavior until the current begins to decay at roughly 2 ns and 10^{-8} A.

The difference in single-event current decays shown in Figure 8 is believed to be

only marginally important because the operating currents of the transistors in the LVDS circuits exceed this level. SPICE simulations were performed to determine drain to source currents of transistors in the LVDS circuits biased in the saturation region. These saturation currents were found to be in the μA range and higher which is significantly higher than the 10^{-8} A values with which discussed in the previous paragraph. The larger saturation currents mean that if the single-event drain current was competing against a current from a transistor in saturation, the saturation current would dominate, and the single-event current would have little effect on the overall circuit response.

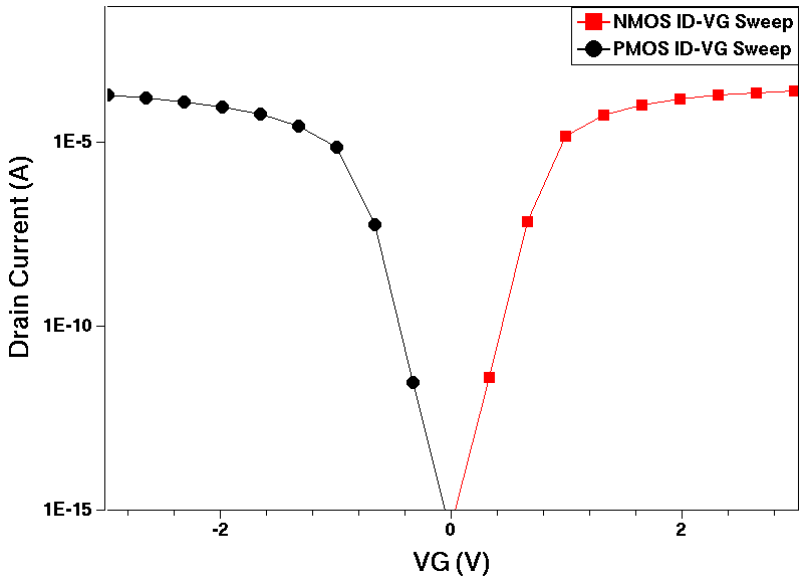

Figure 9: I_D versus V_{GS} curves for 3D TCAD devices generated in TCAD. V_{DS} was fixed at 3.3V for the NMOS device and V_{SD} was fixed at 3.3V for the PMOS device.

A meshing step was then applied to the 3D TCAD devices. This meshing step created mesh points within the devices where various simultaneous equations would be solved by the TCAD simulator. Simultaneous equations such as the Poisson equation are solved in order to calculate the charge density, current, potential, and other

important variables at each mesh point. Over 13000 mesh points were included in each device to achieve results as accurate as reasonably possible. The number of mesh points was chosen by meshing the devices with 80000 mesh points, taking current versus voltage curves on the devices, reducing the number of mesh points and determining the tradeoff between speed and accuracy. It should be noted that the highest concentrations of mesh points were at the pn junction regions and conduction channel regions in the device. Upon settling on an optimum number of mesh points, an I_D versus V_G sweep, with V_{DS} and V_{SD} corresponding to the nominal circuit VDD value, was performed on both the NMOS and PMOS devices as can be seen in Figure 9. This sweep was performed as an additional electrical verification that the devices were operating correctly. All TCAD electrical and radiation simulations were performed using the Synopsys ISE Dessis simulator [15].

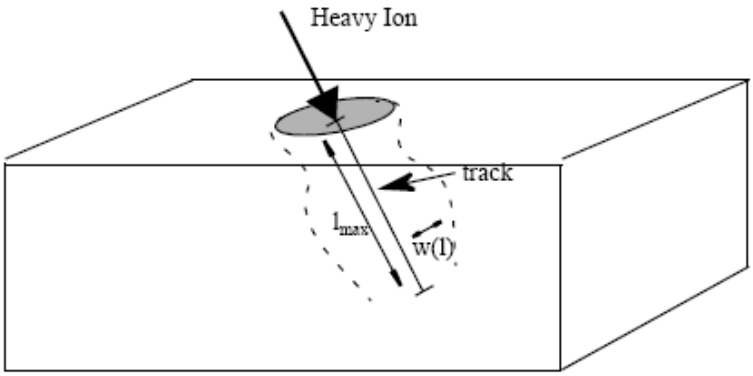

Figure 10: Heavy ion strike as implemented in the ISE Dessis simulator.

Charge collection profiles were obtained via heavy ion simulations in the ISE Dessis simulator. The heavy ion simulation in the Dessis simulator can be understood with the help of Figure 10. This figure shows a heavy ion hitting at a specified angle of incidence traveling a distance of l_{max} with a track radius of W(l). A zero angle of

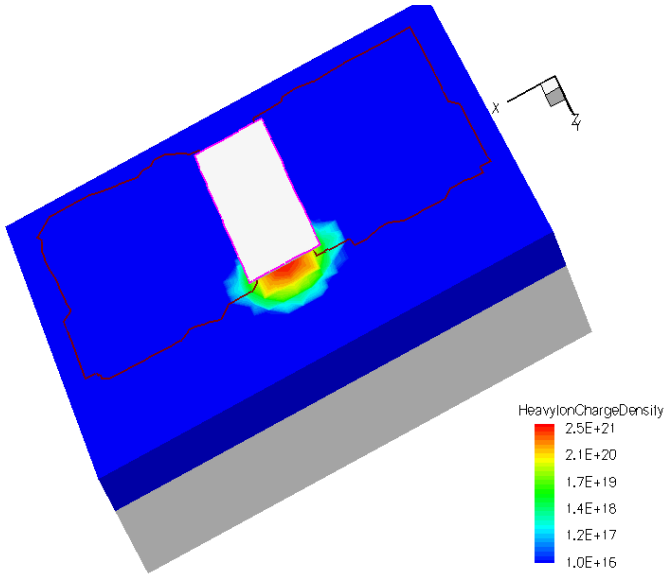

Figure 11: Ion strike in the ISE Dessis simulator at the bottom of the gate near the body contact.

incidence was chosen for these simulations to simplify simulations and produce more easily interpretable results. A traveling distance of 2 μm was chosen to ensure penetration through the epitaxial Si layer. A radius of 50 nm was chosen after discussions with several engineers at ISDE with experience in SEE simulations with the Dessis simulator. The energy of the heavy ion was specified in terms of charge deposition in pC/μm. The appropriate charge density values were obtained using Equation 2, which relates LET to charge in Si assuming a constant LET. A simplification was made in this work to assume a constant LET throughout the epitaxial Si thickness. This simplification ignores effects associated with Bragg peak curves. The Bragg peak curve illustrates how a heavy ion loses energy as a result of increasing penetration depth, which results in non-uniform LET values along the track length of the heavy ion. [16]. A example of the resulting charge deposition in the NMOS TCAD device at a LET value of 128 MeV·cm^2/mg can be seen in Figure 11. This figure shows a

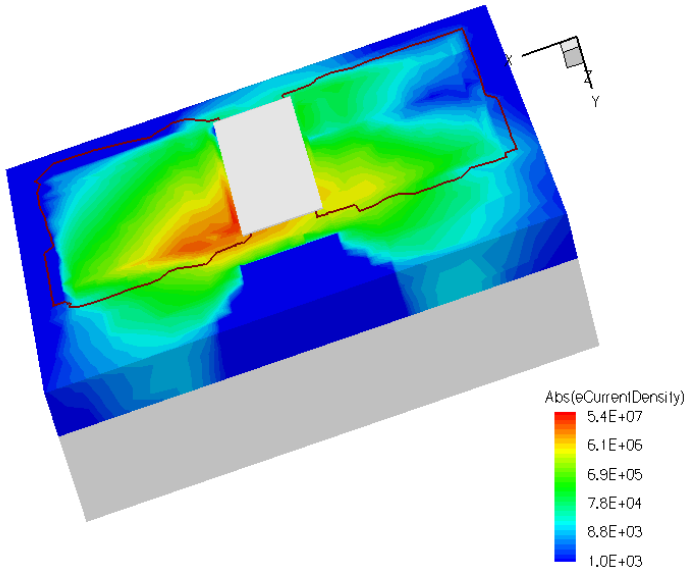

Figure 12: Currents resulting from ion strike in the ISE Dessis simulator at the bottom of the gate near the body contact.

strike at the gate edge near the body contact. A snapshot of the device showing the collected charge shortly after the strike can be seen in Figure 12. It should be noted that some of this charge density can be seen going from the drain to the source and some can be seen entering the body contact.

The parasitic bipolar structure first discussed in chapter II has been shown to significantly affect the collected charge in SOI transistors after a single-event strike [6]. This can be seen in Figure 13 which shows the drain and body currents as a function of distance from the body contact in the width dimension on a SOI transistor. It can be seen that the body current is initially larger than the drain current when near the body contact, but is eventually eclipsed by the drain current as the strikes progress further and further from the body contact. This effect was shown to exist when characterizing the charge collection profiles in the LVDS process technology via TCAD simulation tools as can be seen in Figure 14. This figure shows the drain and

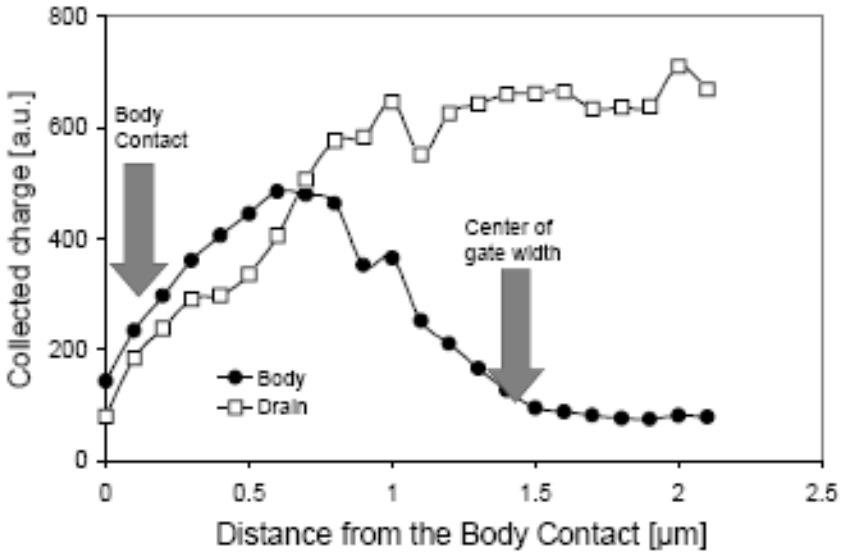

Figure 13: Drain and body currents in SOI FETs shown to vary as strike location varies in distance from body tie.

body currents for a strike near the body contact along the z axis and for a strike away from the body contact near the middle of the transistor along the z axis. The drain current is larger during the strike in the middle of the transistor and smaller during the strike near the body tie. The body current however is significantly smaller during the strike in the middle of the transistor and larger during the strike near the body tie. This behavior agrees with Figure 13.

The charge collection profiles were also shown to vary significantly with strikes at different points along the length dimension of the transistor. Figure 15 shows the charge collection profiles at different strike locations along the length axis (x axis) of the transistor. It can be seen that the largest charges, represented as areas under the curve, occur at values of x=0μm and x=0.1μm. These x axis values correspond to locations on the gate from its center to its edge near the drain. This is to be expected as strikes to these locations can contribute directly to the drift and diffusion charge

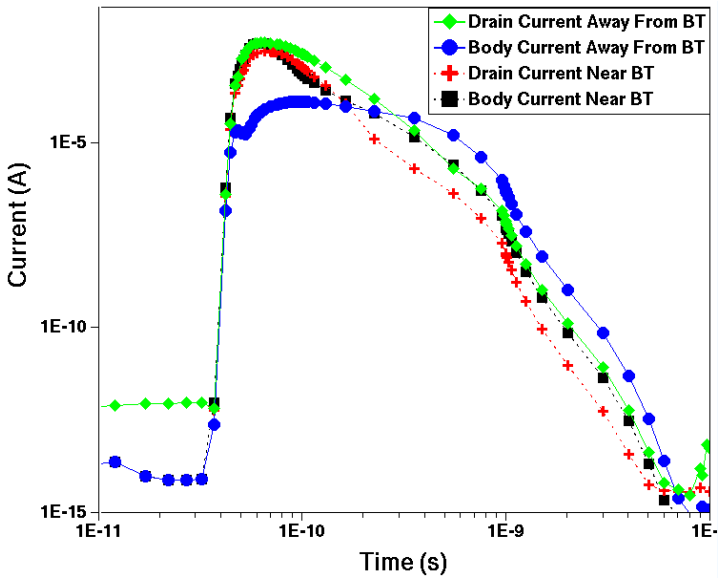

Figure 14: Drain and body currents plotted for a strike in the middle of the gate near the body tie and a strike in the middle of the gate away from the body tie.

collection mechanisms discussed in chapter III.

The charge collection profile in this simulation methodology also takes in to account the voltage bias on the transistor being struck. Four biases are included in the database which relate to possible V_{DS} values that exist at any given state in the circuit. Charge collection profiles for each of these 4 biases are included in Figure 16. Here, it can be seen that the larger biases contribute to more collected charge. The larger biases contribute to a larger E field, which is able to push more of the electron-hole pairs created by the heavy ion strike across from the drain to the source.

The LET value is directly related to the charge deposited in the semiconductor. The larger deposited charge value leads to a larger amount of charge being collected. Charge collection profiles for LET values ranging from 4 to 128 MeV·cm^2/mg can be seen in Figure 17.

The charge collection information obtained by the 3D TCAD heavy ion simulations

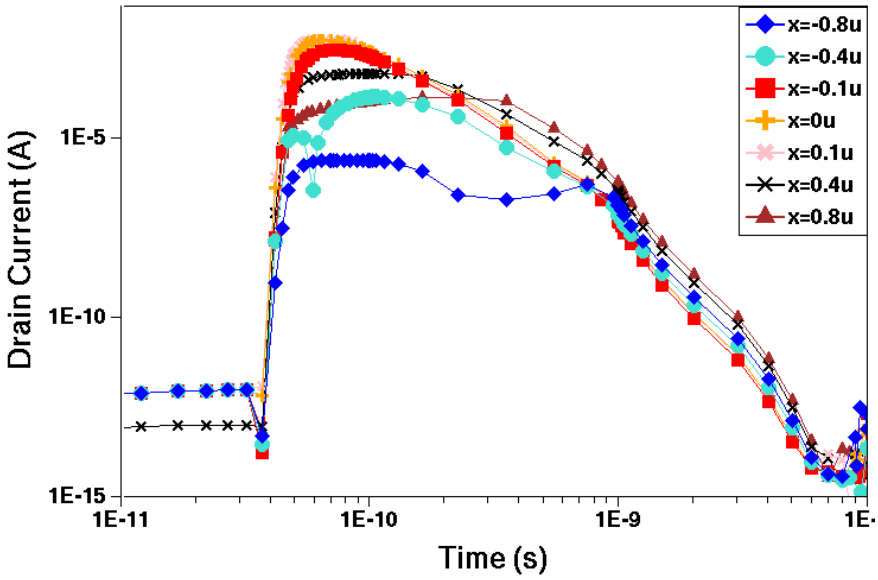

Figure 15: Drain currents plotted for strike along various locations of the "length" dimension of the transistor. Included are strikes on the source, gate and drain regions.

is extended to the circuit level by approximating the device response as a current source in SPICE. This approximation was performed by extracting the drain to body current in the TCAD simulator resulting from the heavy ion strike and fitting the data to a double exponential curve. All TCAD simulations were performed with a 500-ohm load representative of the load an average off-transistor in the circuit would see. This load was determined using SPICE simulations to approximate the lowest drain to source resistance of a transistor biased so that it is conducting current in its saturation region. The double exponential curve is composed of an exponential function accounting for the rise in magnitude of the resulting single-event current and another exponential function modeling the decay in magnitude of this current. These two components of the double exponential function can be seen in Figure 18.

A double exponential current source approximation was made for each possible condition in the characterization database. Accounting for the NMOS and PMOS

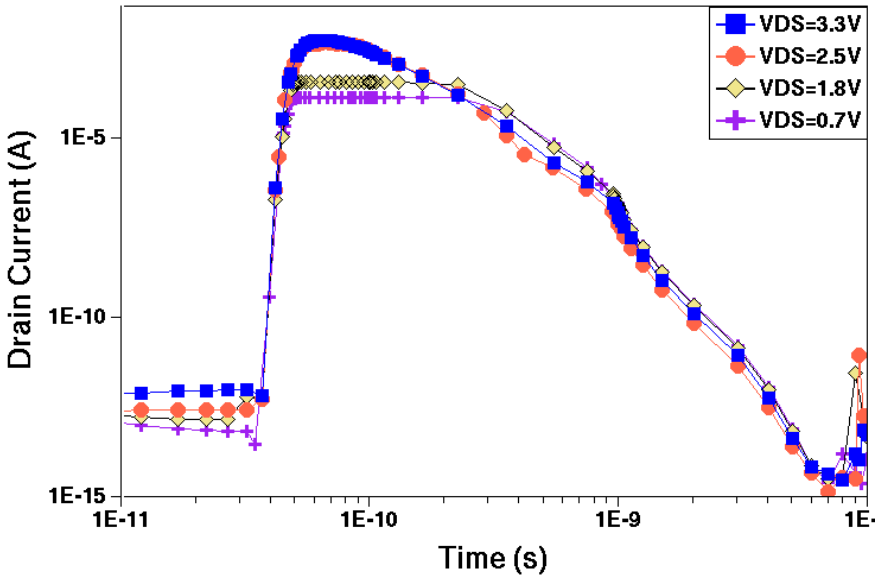

Figure 16: Drain currents plotted for strike at the drain of the transistor at different Vds biases.

device, 4 possible biases, 85 unique strike locations, and 11 LET values yielded 7480 unique double exponential estimates. The double exponential can be expressed with the TD1, TAU1, TD2, TAU2, V1 and V2 parameters in SPICE in accordance with Figure 18. The charge collection information from TCAD simulations was output in a text file containing an array of current vs. time data points. These data points were parsed by a custom Python [17] script to obtain the TD1, TAU1, TD2, TAU2, V1 and V2 parameters. The simplification of the current response to these parameters allowed for storage in a text file for easy access. This approximation has the limitation of assuming that the resulting single-event current is a pure exponential function during its rise and decay. Actual single-event currents are not true exponentials. The significance of this limitation depends, among other things, on how closely the actual current resembles the approximation. The TCAD current responses in this thesis were shown to exhibit an exponential rise very consistent with the approximation.

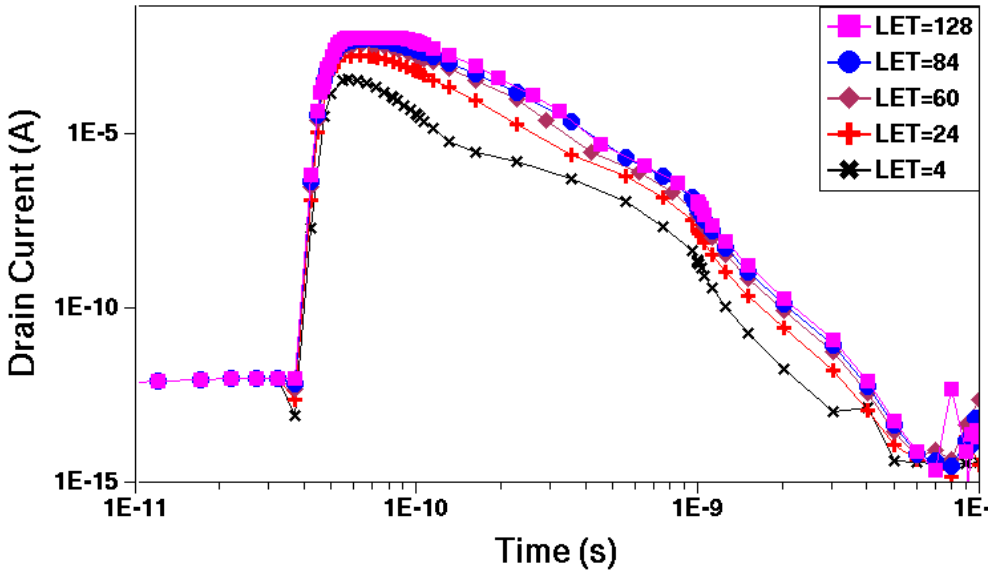

Figure 17: Drain currents plotted for strikes corresponding to different LETs. The units of LET used here are MeV·cm^2/mg

The decaying behavior of the TCAD current responses however was slightly different than a typical exponential decay. The TCAD current responses were seen to decay exponentially for a varying length of time and then begin to decay at a slightly slower exponential rate. This resulted in most of the double exponential approximations being an overestimate during the initial decay of the pulse and an underestimate as time increases and the rate of decay begins to slow. The overestimate had a more significant effect on the results because the initial decay was seen via simulation to have more of an effect on the circuit response than the latter decay. The presence of this latter slower decay, known as the tail of the current response, was shown not to have a significant effect on the circuit due to the low values of currents this was shown to occur at. The transistors in the LVDS circuits had operating currents larger than this tail current, which severely minimizes the effect the tail current would have on the circuit. A comparison between a resulting TCAD currents and its double exponential

TIME	VOLTAGE
0 to ***TD1***	V1
TD1 to ***TD2***	$V1 + (V2 - V1)\left(1 - \exp\frac{-(time - TD1)}{TAU1}\right)$
TD2 to ***TSTOP***	$V1 + (V2 - V1)\left(1 - \exp\frac{-(time - TD1)}{TAU1}\right) + (V1 - V2)\left(1 - \exp\frac{-(time - TD2)}{TAU2}\right)$

Figure 5-2. Exponential Function

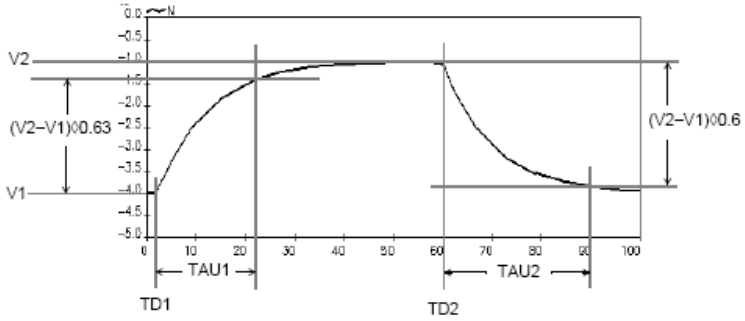

Figure 18: Components of double exponential function.

approximation can be seen in Figure 19. This figure shows a worst case example of the approximation being and underestimate and an overestimate at different times within the same pulse.

The next step in the simulation methodology evaluates the circuit under simulation at its desired static bias and extracts V_{DS} values for each transistor in the circuit. These V_{DS} values are logged in a file for future access by the characterization database created earlier. The V_{DS} values are extracted using a DC SPICE simulation with the Cadence IC5.1.41 Spectre simulator.

The SPICE netlist of the circuit under test is then modified by inserting double exponential current sources, which represent the single-event strike, into the circuit at drain to body junctions in the MOSFETs. The current sources are taken from the characterization database individually for each transistor in the circuit according to device type, V_{DS} value, LET, and strike location. All of the current sources are inserted simultaneously with time delays calculated such that the circuit has time to

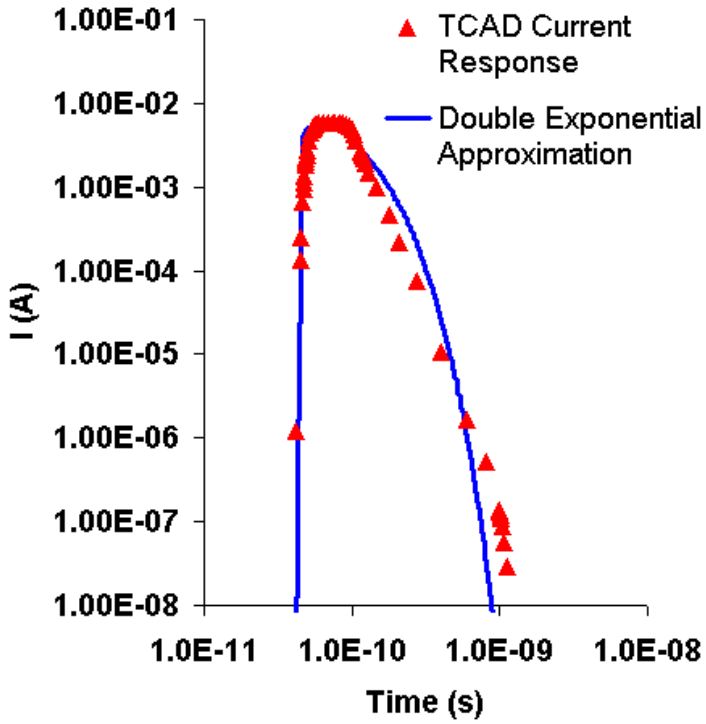

Figure 19: Double exponential approximation for drain currents generated by heavy ion strikes in TCAD simulations.

return to its original state between successive current sources being activated. This step in the methodology, which modifies the SPICE circuit netlist, and the following step, which runs the SPICE SEE simulation, will be looped for the total of 85 strike locations.

This method of inserting current sources is in agreement with traditional single-event modeling [13] and can be seen graphically in Figure 20. This figure includes parasitic resistances associated with the MOS transistor and the parasitic bipolar transistor that occurs in SOI technologies. It should be noted again that the LVDS SPICE circuits have layout parasitics back annotated into the SPICE netlist, and that the parasitic bipolar effect on the transistor has been accounted for in the heavy ion TCAD simulations.

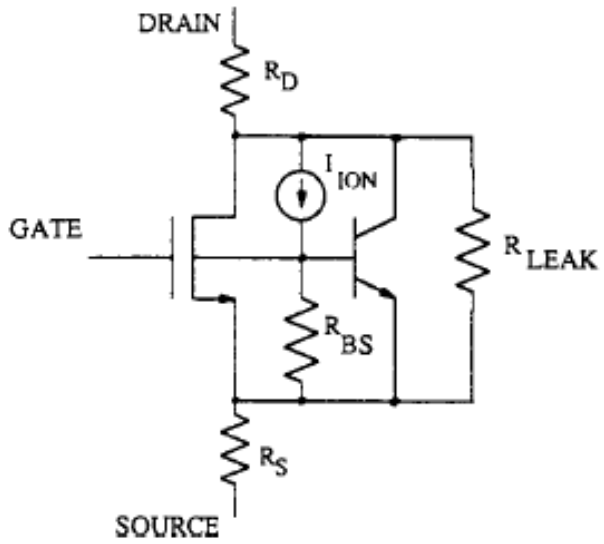

Figure 20: Insertion of current source in SPICE level circuit to model circuit-level radiation response to heavy ion strikes [19].

The next step in the simulation methodology uses the Cadence IC5.1.41 Spectre simulator to simulate the circuit response with the single-event currents inserted. The circuit is then simulated and the output is monitored to check for conditions that would constitute an error. These conditions, specified by the user in terms of voltage thresholds, would constitute an error if crossed. A Spectre output at this intermediate step is seen in Figure 22. This figure shows the output deviation as a result of striking every transistor in the LVDS receiver circuit in succession at a spatial location corresponding to the gate/drain edge in the middle of the transistor with an LET of 128 MeV·cm^2/mg. The output here is seen to drop from its nominal value of 3.3V to 0V a total of five times. These five times correspond to five transistors in the circuit in this simulation state that are 'sensitive' at this spatial location and will cause the output to deviate significantly from its nominal value when struck there. These output deviations due to single-event strikes are commonly referred to

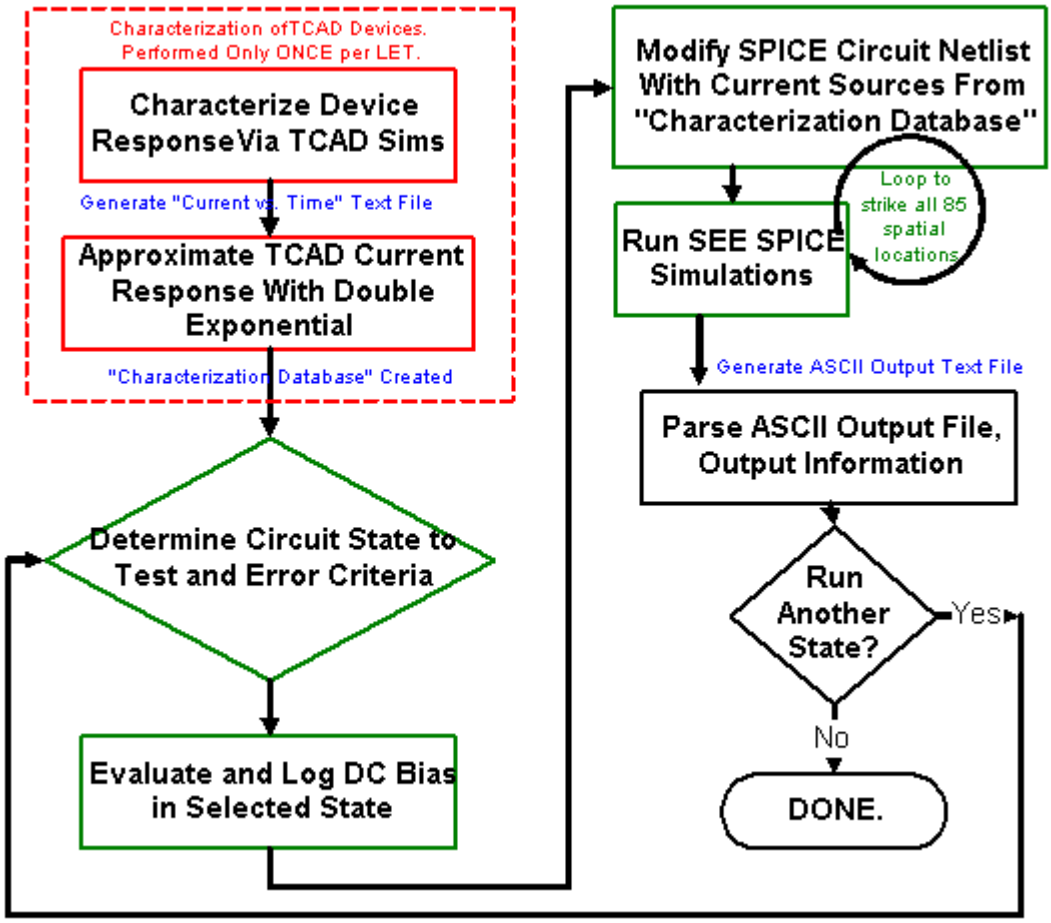

Figure 21: Flowchart of SEE simulation methodology used in this thesis.

as single-event transients (SETs). A SET is more formally defined as momentary voltage excursion (voltage spike) at a node in an integrated circuit [7] caused by a single-event interaction with the circuit.

The total number of spatial locations that produce an error is kept as a running total and used to generate the sensitive areas for each transistor in the circuit. The sum of all sensitive transistor areas in the circuit is then used to generate single-event sensitive cross-section area versus LET curves for each circuit according to simulation state. This entire simulation procedure is automated using the Python

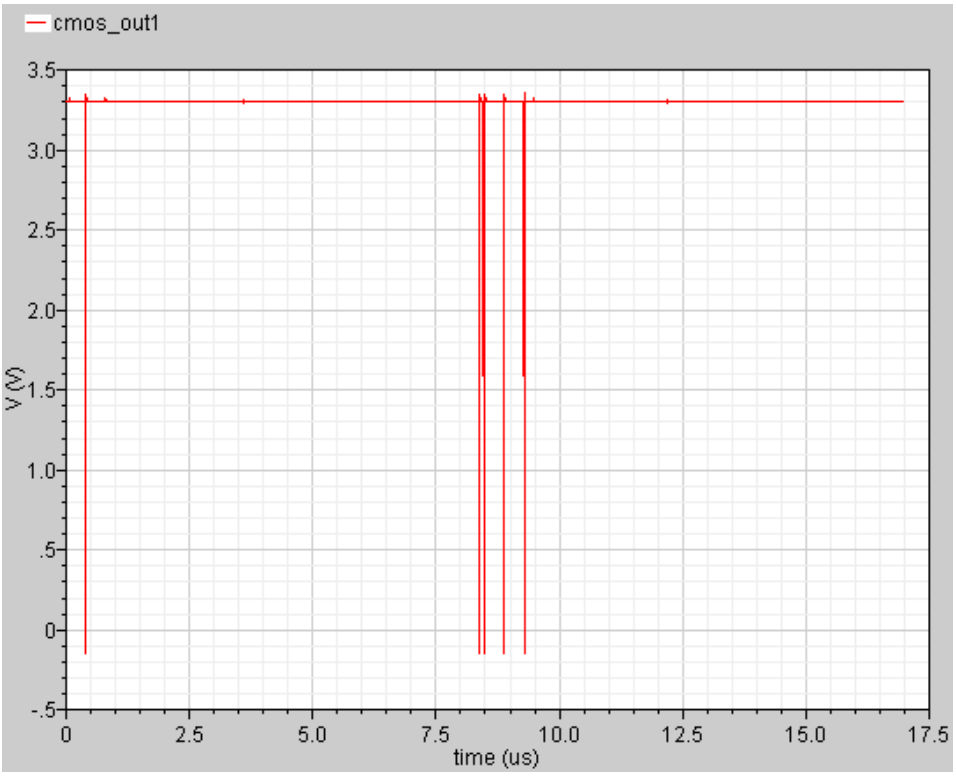

Figure 22: Sample circuit response of LVDS receiver showing circuit output response to heavy ion strikes at each transistor in circuit. Each output deviation can be traced back to the transistor being struck.

scripting language and can be applied to any arbitrary circuit implemented in the same proprietary process technology as the LVDS driver and receiver circuits [17].

This section presented an overview of single-event modeling methodology used in this work. The methodology building upon previously published and accepted methods for simulating a complex SPICE level circuit while adding additional simulation variables such as multiple strike locations, transistor bias considerations to improve simulation accuracy. The scalable nature of the technology used to fabricate these devices has been taken advantage of to allow for time-efficient simulations. The next Chapter will focus on the specific simulation parameters and results of the LVDS driver and receiver circuits.

CHAPTER V

HEAVY ION SIMULATION RESULTS

Heavy ion circuit simulation results are presented along with their corresponding simulation states, test conditions and failure criteria. The heavy ion simulation results are in the form of critical LET values, single-event sensitive circuit area cross sections versus LET, and the mapping of single-event sensitive area on individual transistors. The test conditions for the heavy ion testing are driven by the part specifications documents that were used in the design of these LVDS devices.

The first test condition in the heavy ion testing statically biased each LVDS circuit with its nominal supply voltages and nominal input voltages at an ambient temperature of 27 degrees Celsius. The circuit was struck for LETs values ranging from 4 to 128 MeV·cm^2/mg with zero angle of incidence. Errors in the LVDS receiver circuit were chosen to be defined as output deviations exceeding the specified V_{OH} and V_{OL} levels by any amount of voltage for any period of time. Errors in the LVDS driver circuit were chosen to be defined as output deviations exceeding the specified differential output voltage (V_{OD}) level by any voltage for any amount of time. These error definitions were chosen to match the error definitions defined in the radiation test plan that currently exists for upcoming physical test of these LVDS devices at a cyclotron facility.

The single-event sensitive cross section area versus LET curve from condition 1 is plotted in Figure 23. This figure shows errors occurring in the LVDS driver circuit but no errors occurring in the LVDS receiver circuit. The critical LET, which defines

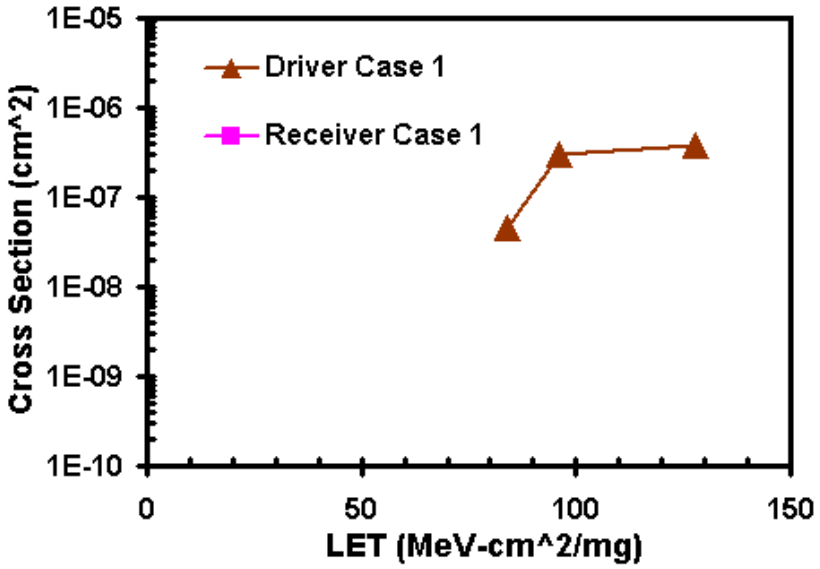

Figure 23: Heavy ion sensitive cross section curves for condition 1. Note that no errors were seen for the receiver circuit at this condition.

the lowest LET value shown to produce an error, is seen to be 84 MeV·cm^2/mg in the driver circuit. The critical LET of the receiver circuit is shown not to exist.

The driver simulations from condition 1 can be used to find the most sensitive areas on the NMOS transistor. At an LET of 128 MeV·cm^2/mg, the locations seen in Figure 24 contribute to errors in 5 different transistors, which is the largest number of sensitive transistors at this strike condition. Therefore, this figure shows the most sensitive area in the NMOS transistor corresponding to this condition. This figure shows that 22 of the strike locations resulted in errors for the LVDS driver at this LET and simulation condition.

The second test condition in the heavy ion testing statically biases each LVDS circuit with its nominal supply voltages at an ambient temperature of 27 degrees Celsius, but with worst case input voltages. This test condition was created because errors were not observed in the receiver circuit with test condition 1.

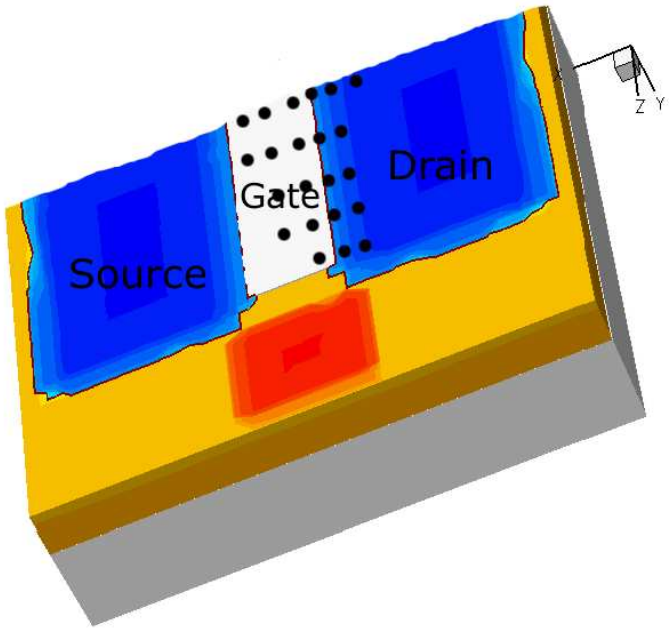

Figure 24: Strike points in most sensitive transistor in LVDS driver circuit at LET=128 MeV·cm^2/mg causing upsets for condition 1.

The single-event sensitive cross section area versus LET curve from condition 2 is plotted in Figure 25. This figure shows errors occurring in both the LVDS driver and receiver circuit. The critical LET at this condition is shown to be 84 MeV·cm^2/mg for both the driver and receiver circuits.

One possible explanation for heavy ion sensitivity to input conditions in the LVDS receiver circuit and the lack of this sensitivity to input conditions in the LVDS driver circuit can be seen with the aid of Figure 2 and Figure 4 from Chapter II. These figures show the generic LVDS driver and receiver architectures. The receiver has a Schmitt trigger immediately interfacing with the input signals in its LVDS circuitry. The driver however, is shown having its full scale CMOS "D" input immediately interfacing with the input signals in its LVDS circuitry. Since the driver is operating with full scale CMOS signals in its LVDS circuitry, it can easily apply pull-up or

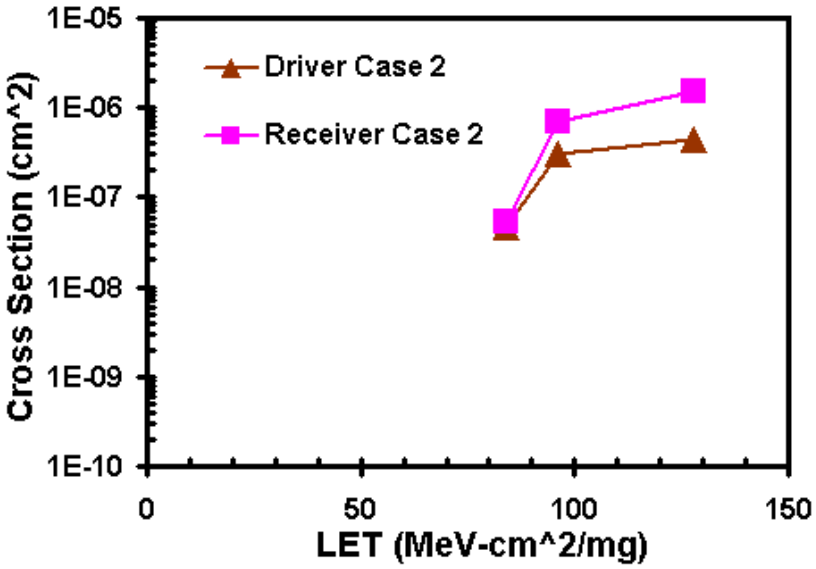

Figure 25: Heavy ion sensitive cross section curves for condition 2.

pull-down circuitry to guarantee a full scale CMOS signal enters its LVDS circuitry. The receiver must process the inputs as they appear, which can significantly change some of the node voltages in Figure 4. Altering these node voltages can alter the susceptibility to upset from a heavy ion strike, which may explain why upsets were only seen in the worst case input condition for the receiver in this work.

The results of the heavy ion simulations have been presented in this section. Two input conditions for both the LVDS Driver and Receiver were simulated. Under nominal input conditions, only the LVDS driver circuit experienced errors and was shown to have a critical LET value of 84 MeV·cm^2/mg. Under worst-case input conditions, both the LVDS driver and LVDS receiver circuit experienced errors with both circuits having a critical LET value of 84 MeV·cm^2/mg. A further discussion of these results is presented in the discussion section, located in Chapter VII. The next Chapter discusses the dose rate simulations and results.

CHAPTER VI

DOSE RATE SIMULATION SETUP AND RESULTS

The dose rate simulations of the LVDS driver and receiver were performed using models created by the Institute of Space and Defense Electronics (ISDE). These models were used in SPICE circuit simulations to determine what effect the dose rate had on various operating parameters of the driver and receiver circuits.

The models created by ISDE to model dose rate, which exist at the SPICE level for all MOSFETs and diodes in the circuit, introduce a photocurrent in the device corresponding to the desired dose rate level, duration of the dose rate event, and starting time of the dose rate event. The correlation of dose rate induced photocurrent in each device was obtained via experimental characterizations of test devices and device modeling with the proprietary SOI technology.

Dose rate circuit simulation results are presented along with their corresponding simulation states, test conditions and failure criteria. The simulation states, test conditions and failure criteria were designed to mimic experimental military dose rate testing as closely as possible. The dose rate test types include the reading of circuit photocurrents, glitch upset and associated recovery times, pushout, and propagation delay effects. The test conditions and types for the dose rate testing are driven by the part specifications documents that were used in the design of these LVDS devices. All of the simulations were performed at an ambient temperature.

The dose rate event was shown to have a large effect on propagation delay in the driver circuit and a large effect on the steady state output voltage in the receiver

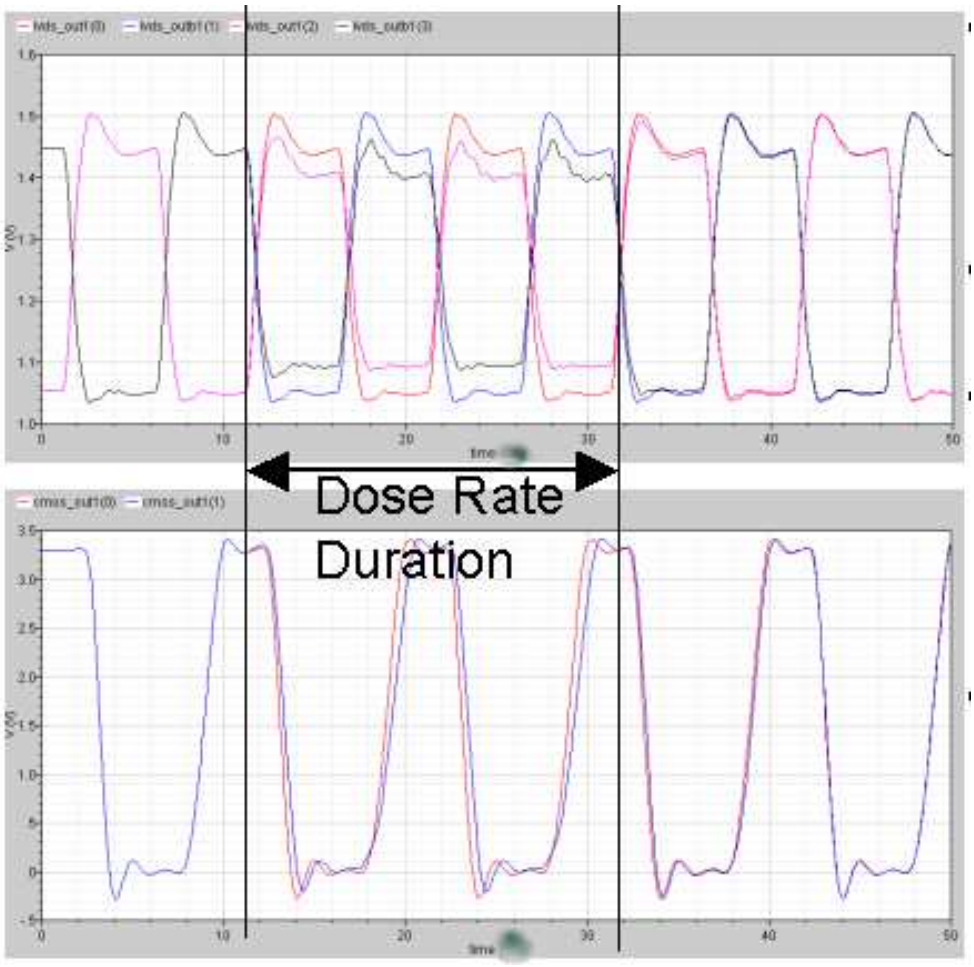

Figure 26: LVDS driver and receiver response to dose rate strike during transient operation. Driver is shown on top and receiver is shown on bottom of figure.

circuit. The response of the the driver and receiver to nominal transient inputs when the same dose rate parameters are applied to both circuits can be seen in Figure 26. This figure plots the dose rate outputs superimposed on the nominal outputs in both circuits. The deviations seen can be attributed solely to the dose rate event. The driver sees significantly more output voltage deviation than the receiver. The receiver however sees more of a change in propagation delay in comparison to the driver.

Dose rate induced photocurrents were measured in both the driver and receiver while biased with a nominal supply voltage. The photocurrents were read out of the

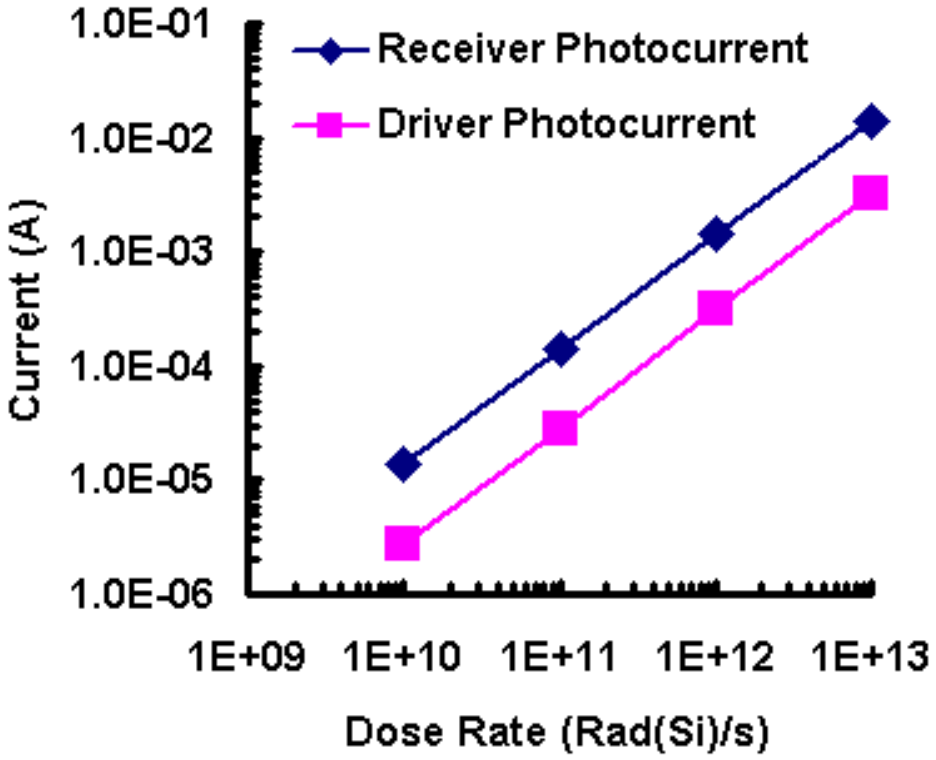

Figure 27: Photocurrents versus dose rate plotted for driver and receiver circuits.

Spectre simulator at the power supply node. These photocurrents are plotted for the driver and receiver in Figure 27. It can be seen in this figure that the receiver has a larger photocurrent value than the driver. It can also be seen that the photocurrent increases approximately linearly with increasing dose rate.

The glitch upset dose rate test type was also applied to the LVDS circuits. This test increased the dose rate level to determine when and if the circuits fail to meet their respective output voltage specifications. All biases in this test were nominal, with a nominal transient input applied to each circuit at the maximum specified frequency level. The dose rate levels were increased to the maximum levels that maintained accuracy of the models and physical sensibility, but no occurrences of glitch upsets were recorded. The absence of glitch upsets in this test rendered the

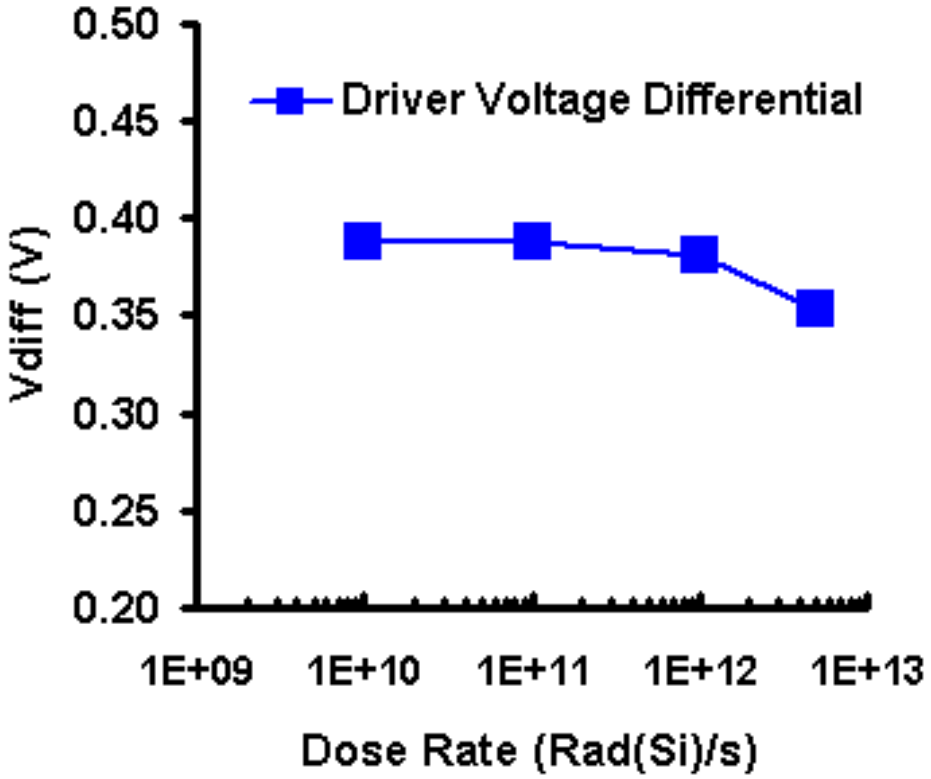

Figure 28: Driver output voltage differential plotted versus dose rate. Note that the receiver output deviations are not plotted due to lack of significant variance with dose rate.

recovery time metric moot. The recovery time was intended to measure the duration of the output glitch. The driver circuit, while not recording any glitch upsets, was shown to have the largest output variance with dose rate. A plot showing the driver's output differential voltage versus dose rate can be seen in Figure 28.

A test for the pushout phenomena was applied next. Pushout is defined in this thesis as the effect of dose rate pulse timing to the input signal signal switching edge on dose rate induced propagation delay. Both circuits were biased nominally in this test with nominal inputs operating at the maximum specified switching frequency. The dose rate pulse was applied at 5, 10, 15, 20, and 25 ns before the transition of the input signal. The results of this test can be seen in Figure 29. Here it is seen

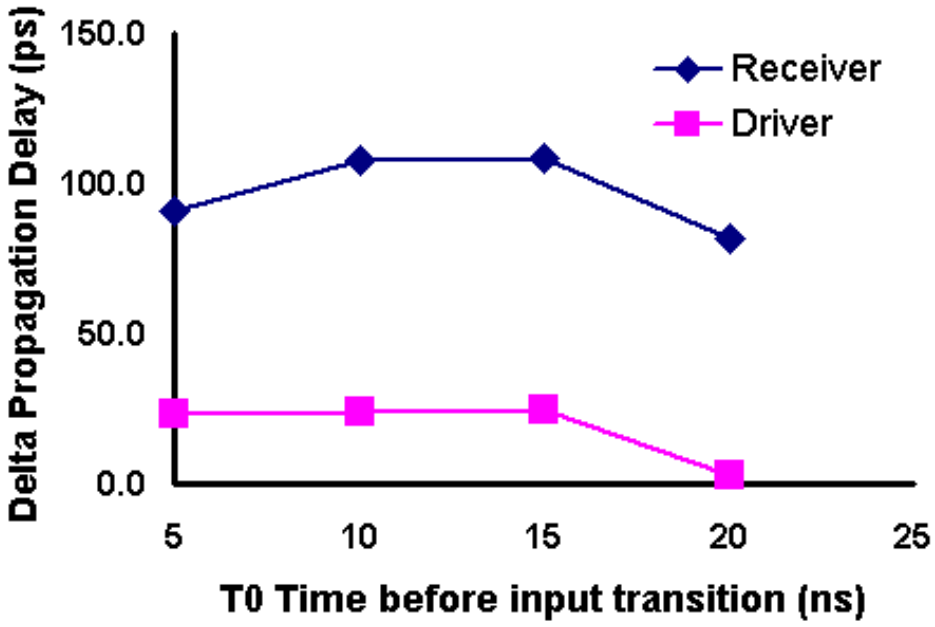

Figure 29: Change in propagation delay plotted versus location of strike in relation to input transition in driver and receiver circuits.

that strikes at roughly 15 ns before the input transition result in larger propagation delays than strikes at other times.

The effect of the dose rate level on propagation delay was also tested. The dose rate pulse was applied 15 ns before an input transition at the maximum specified frequency while the circuit was biased nominally. Figure 30 shows the results of this test which plots the increase in propagation delay versus applied dose rate. It can be seen that the receiver has the largest increase in propagation delay. It is also interesting to note that this propagation delay increases approximately linearly with applied dose rate.

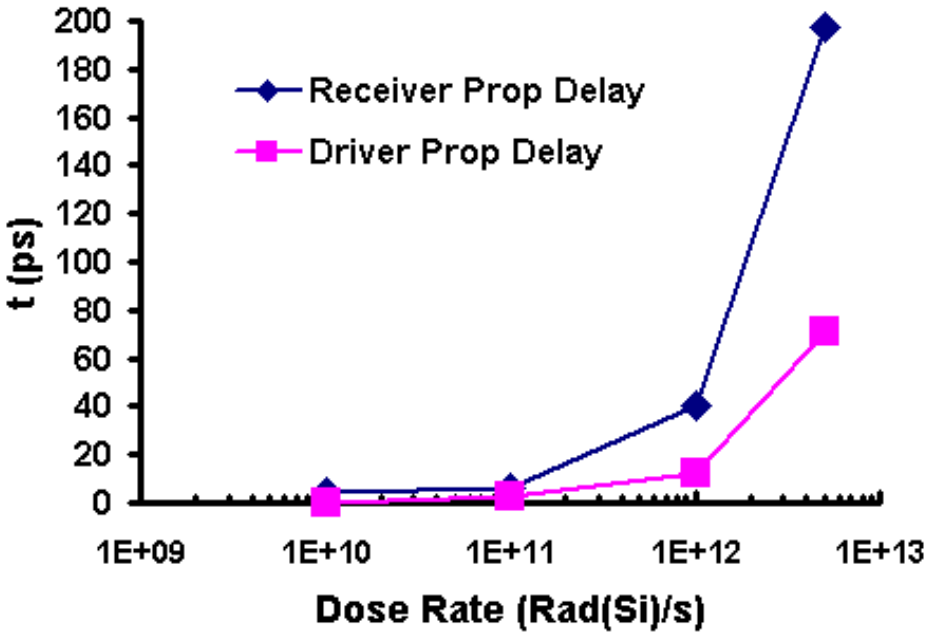

Figure 30: Change in maximum propagation delay plotted versus dose rate in driver and receiver circuits.

CHAPTER VII

DISCUSSION AND IMPLICATION OF RESULTS

The simulations presented in this work can help give insight into how these LVDS devices respond to interactions with heavy ions and dose rate radiation. Physical radiation testing of devices fabricated with the SPICE netlists used in these simulations is scheduled to occur in the future. The information obtained in this work can aid in the creation of radiation test plans as well as what conditions to incorporate into the testing. Possible examples of this include determining what ion species to select during heavy ion testing at a cyclotron based on the cross section curves presented in Figure 23. An ion capable of achieving an LET greater than the LET threshold of 84 MeV·cm^2/mg such as Au would be a good choice here. Another possible example includes determining where to place the edge of the dose rate pulse when testing at a linear accelerator facility when the worst-case radiation response is desired based on the pushout statistics plotted in Figure 29. Placing the beginning of the pulse 15 ns before the input transition edge would be a satisfactory answer to this example.

The heavy ion simulation results presented show errors occurring at LET values of 84 MeV·cm^2/mg and greater under worst case input conditions with nominal supply voltages. This LET value of 84 MeV·cm^2/mg indicates that the circuit should perform relatively well in the space radiation environment, where heavy ions are a primary concern. In the space radiation environment, the lower the LET of the cosmic ray, the higher probability it has of occurring. As can be seen from Figure 31 [18], particles with an LET of 1 MeV·cm^2/mg have a flux in space 16 orders of magnitude greater

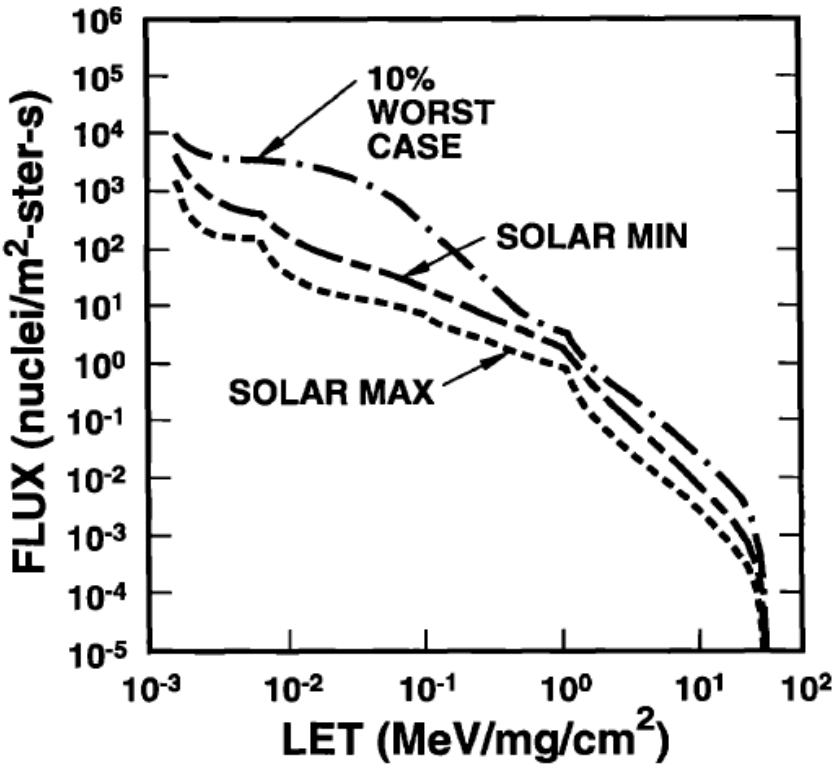

Figure 31: Ion flux as a function of LET [18].

than particles with an LET of 100 MeV·cm^2/mg. When designing electronics for use in space systems, there might exist a requirement to be radiation hard to particles with an LET of 35 MeV·cm^2/mg or less. At LETs above 35 the flux of heavy ions becomes very small.

The properties of the SOI process technology have a significant effect on the heavy ion and dose rate radiation response of these LVDS circuits. The small Si volume of which the pn junctions are implemented in the SOI technology is significantly smaller than that of a similar bulk technology. This small Si volume is responsible for limiting the amount of charge deposited, and thus collected, by a heavy ion strike on a SOI transistor. The smaller charge that is collected means that the circuit will see a smaller current created by the ion strike than it would in a bulk technology. The small

Si volume is also responsible for limiting the dose rate induced photocurrent. As can be seen in Equation 4, this Si volume is directly related to photocurrent generation.

There is also a parasitic bipolar structure that exists in this SOI technology. The parasitic bipolar can amplify the collected charge in the heavy ion environment and the photocurrents in the dose rate environments due to its electrical behavior. The parasitic bipolar transistor is typically turned on when the body of a bulk device develops a potential to bias its effective base emitter junction formed by the body and source junction of the SOI MOSFET. The effect of this parasitic bipolar is typically reduced by applying body ties or body contacts to the body region of the SOI transistor. These body contacts and ties allow the body potential to stay closer to the source potential, minimizing the parasitic bipolar's base emitter potential.

The heavy ion simulation methodology used in this work has several elements that are novel and new. It has advantages over simple SPICE SEE simulations because it incorporates the effect of transistor bias, ion LET, spatial location of the strike on the transistor, while efficiently striking every transistor on the circuit. This accounts for a significant amount of the variation in the charge collection profiles during an actual ion strike. It has advantages over conventional mixed mode (TCAD and SPICE) SEE simulations because it is able simulate larger circuits in shorter amounts of time. This methodology works because of the nature of the gate array ASIC technology with which these LVDS circuits are fabricated in. Each transistor has an identical channel region, and a scalable width region. Variable channel lengths would require more characterization to take place in order to implement this method.

This methodology lends itself easily to more simulations if changes are made to the circuit design or physical package of which it will be placed in. A change such

as this would simply require a new netlist to be run through pre-existing script files developed in this work. The characterization database with the charge collection statistics and automated error-checking tool would not need modification and could quickly output new results. Similarly, another CMOS circuit designed using the same technology could be quickly simulated in this methodology. The characterization database would remain unchanged, while the automated error checking tool would be modified to accommodate the new circuit.

It should be noted that specific SOI process information, architectural details and specifications of the LVDS circuits and specifications of the applied dose rate pulses were omitted from this publication. This information is considered either proprietary or ITAR and not deemed acceptable for unlimited distribution.

CHAPTER VIII

CONCLUSION

In this thesis a LVDS driver and receiver pair was evaluated in the heavy ion and dose rate radiation environments. Detailed quantitative computer simulations were performed to develop an understanding of the response of the LVDS driver and receiver circuits of dose rate radiation and heavy ion exposure. Existing simulation methodologies used for heavy ion simulations were evaluated and improved upon to obtain the most accurate results possible. A database simulation scheme was created to take advantage of the scalable nature of the devices. The simulation results are currently being used to aid in physical radiation test planning for the recently fabricated LVDS devices based on these designs.

Heavy ion simulations show and explain single-event sensitive area cross section versus LET curves for multiple test conditions on both the LVDS driver and receiver circuits. Under nominal supply, temperature and input conditions, a critical LET of 84 MeV·cm^2/mg was found in the driver circuit, while no upsets were found up to an LET of 128 MeV·cm^2/mg in the receiver circuit. Under nominal supply and temperature but worst case input conditions a critical LET of 84 MeV·cm^2/mg was shown to exist in both the driver and receiver circuit. For each test condition, the most sensitive areas in each transistor were obtained.

Dose rate simulations show and explain the response of the LVDS driver and receiver circuits to a multitude of different types of tests. Dose rate induced photocurrents were obtained for both circuits and display a linear trend versus applied

dose rate. The effect of dose rate on output deviations or glitch upset is presented, though not shown to occur in either the driver or receiver circuits. Propagation delay increase due to dose rate was shown to increase as much as 200 ps in the driver and 75 ps in the receiver at high dose rate. The effect of dose rate pulse timing on propagation delay was also explored. Dose rate pulse timing was shown to have its largest effect when occurring 15 ns before an input transition.

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