Fabrication and Characterization of Diamond Thin Films as Nanocarbon Transistor Substrates

By

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Introduction

The last few decades have witnessed tremendous advances in electronics, primarily due to the miniaturization or 'scaling' of electronic devices. In particular, the scaling of silicon based transistors has been important. Clearly feature scaling cannot continue indefinitely, as this approach will soon encounter both scientific and technical limitations. The current feature size of silicon transistors is already pressing the minimum size current techniques can produce. Soon the feature size will reach a fundamental limit. Here quantum tunneling effects will make isolation of transistors impossible and render them unusable. New approaches to materials and structures need to be explored to continue improving device performance. Nano-electric devices based on carbon nanostructures, such as carbon nanotubes (CNTs) and graphene, provide a promising alternative to silicon based electronics. This is due to their small size and extraordinary properties. [1] These materials have very large carrier mobilities, which have been shown to reach in excess of 200,000 $cm^2V^{-1}s^{-1}$. [2] Because of this, transistors fabricated from these carbon nanostructures have the possibility of being extremely fast and having low power consumption. Due to these factors, much work has gone into studying the transport properties of various forms of carbon. Typically, these devices are fabricated either suspended, or on top of silicon dioxide. For practical application of devices, fabrication on a substrate is necessary. It is the introduction of the substrate where problems enter. For nanostructures fabricated on SiO_2, the mobility drops significantly.

The defects in the substrate dominate the transport. [28, 29, 2] This problem becomes particularly pronounced when studying the effects of radiation on the mobilities of these carbon structures. In this case, the defects created in the substrate dominate the electrical response, obscuring information on the carbon nanostructures.

In order to circumvent these problems, an alternate substrate material is required. Diamond is a wide band gap semiconductor that it is generally considered an insulator. Additionally, it is one of the most radiation hard materials, making it a promising candidate for radiation studies. Diamond also has the property of being a non-polar material. Due to similarities between the diamond lattice and the honeycomb structure of graphene and carbon nanotubes, it may provide a much more natural, less strained interface. All of these properties make diamond a very promising candidate as a substrate for carbon electronics. To that end, we have grown a number of diamond films. These films have had their physical, material, and electrical characteristics investigated. The growth process has not yielded films that would be ideal for use as substrates. These fabricated films still have a number of properties that make them suitable and interesting substrates on which to study carbon electronics.

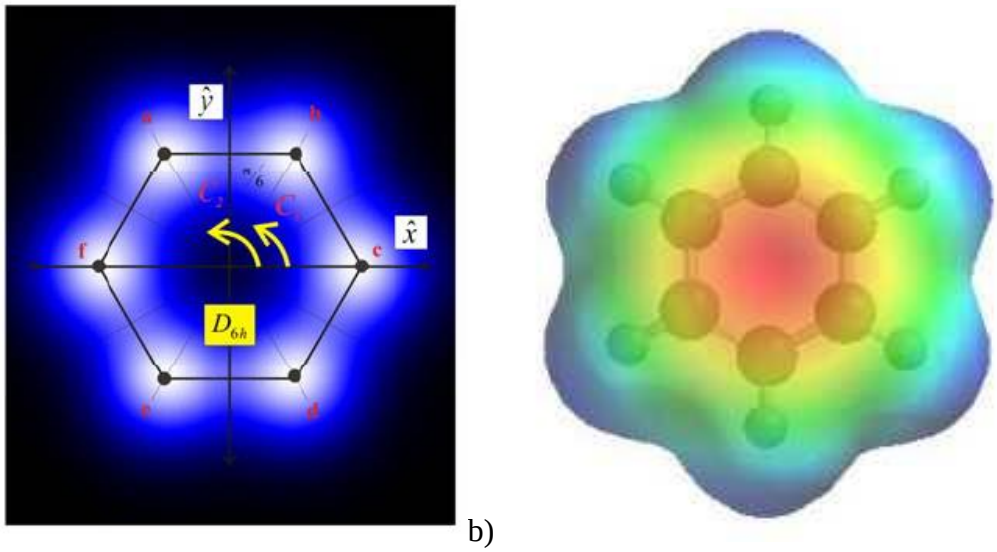
Chapter II

Background Information

II.1) Structure of Carbon

II.1.1) Aromatic Carbon Forms

According to Huckel's rule, planar rings consisting of 4n+2 π electrons (where n is an integer) can be considered to be aromatic. Aromaticity is believed to further stabilize σ bonded planar molecules by the contribution of each atomic constituent to a delocalized wave function. [3] The prototypical aromatic ring is benzene, a six member ring consisted of sp^2 bonded carbons which are hydrogen terminated. (Fig 2.1) This



a) b)

Figure 2.1: (a) Physical structure of benzene, approximated by linear combinations of p atomic orbitals located at each of the six carbon atoms. [3] (b) Electrostatic potential of benzene ring. Both demonstrate the delocalized nature of the p orbitals.

hexagonal carbon ring forms the basis for describing larger structures, such as graphene and carbon nanotubes (CNTs), which consist of many hexagonal aromatic rings attached together. Benzene's lowest energy state consists of six π electrons all in phase. This energy state is responsible for the additional stability associated with aromatic rings.

II.1.2) Graphene: a Polycylic Aromomatic

Graphene is the name given to a flat, monolayer of carbon atoms arranged into a tightly packed 2D honeycomb lattice. This honeycomb lattice consists of a large number of polycyclic benzene rings, making graphene a very large aromatic substance. As with benzene, its electronic structure can be described by the delocalization of π electrons; however, unlike benzene, the eigenvalues associated with graphene are not discrete. [3] They take on continuous values of k_x and k_y, which are wave vectors associated with the reciprocal lattice. The positive root corresponds to the antibonding band of the crystal

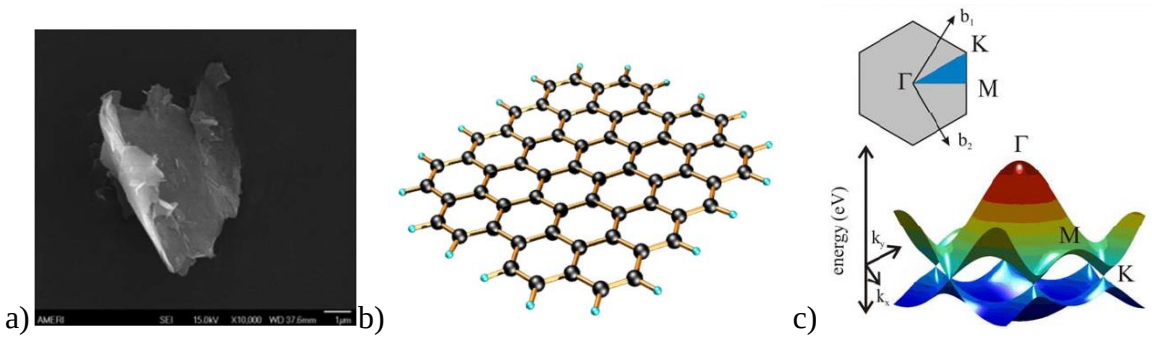


Figure 2.2: (a) SEM image of a single atomic layer of graphene. (b) Conceptual representation of a graphene sheet. (c) The 2D dispersion of the electron and hole bands in graphene.

orbital π*, and the negative root corresponds to the bonding band π, equivalently the electron and hole bands respectively. The energy levels of these bands in k-space are shown in Figure 2.2. Near the K-point, the bands approach each other linearly as a cone

and touch at the K-point, making graphene a semi-metal, or a zero-gap semiconductor. [4]

Graphene has a number of unique physical, electrical, and thermal properties. [5,6] Graphene exhibits a high conductivity, resulting from its extensive conjugated sp^2 network, reported to be as high as ~64 $mScm^{-1}$ [6] and which remains stable over a large temperature range. [3] Graphene has been shown to have achieved very large mobilities, which remain high even as the concentrations of electrons and holes increases. For example, mobility in excess of 200,000 $cm^2V^{-1}s^{-1}$ have been achieved at electron densities ~$2x10^{-11}$ cm^{-2} for a suspended graphene sheet. [2] By comparison the mobility of electrons in silicon is ~1000 $cm^2V^{-1}s^{-1}$. Not only have these fast charge carrier properties been shown to be continuous, it has been shown that these charge carriers can travel thousands of inter atomic distances without scattering. [5] This suggests that if graphene were to be used as a channel in a transistor, it could provide an extremely fast, low power consumption transistor.

II.1.3) Carbon Nanotubes: Graphene with a Twist

Single walled carbon nanotubes (SWNTs) are tubules of graphene that vary in diameter depending on how they are cut from the graphene sheet. They have a number of properties that make them potentially useful for many applications. Nanotubes exhibit extraordinary strength due to their sp^2 lattice, have unusual electrical properties that can be tuned for a number of applications, and are efficient thermal conductors.

For all practical purposes, nanotubes are treated as a one dimensional structure. The unit cell is defined by two vectors on the graphene plane; the translational vector that

maps out the length of the unit cell, T, and the chiral vector that maps out its circumference, C_h. [3] Both of these are defined in terms of the graphene lattice vectors $\mathbf{a_1}$ and $\mathbf{a_2}$.

$$\vec{T} = \frac{2m+n}{d_r}\overrightarrow{a_1} + \frac{2n+m}{d_r}\overrightarrow{a_2} \; and \; \overrightarrow{C_h} = n\vec{a}_1 + m\vec{a}_2 \qquad (2.1)$$

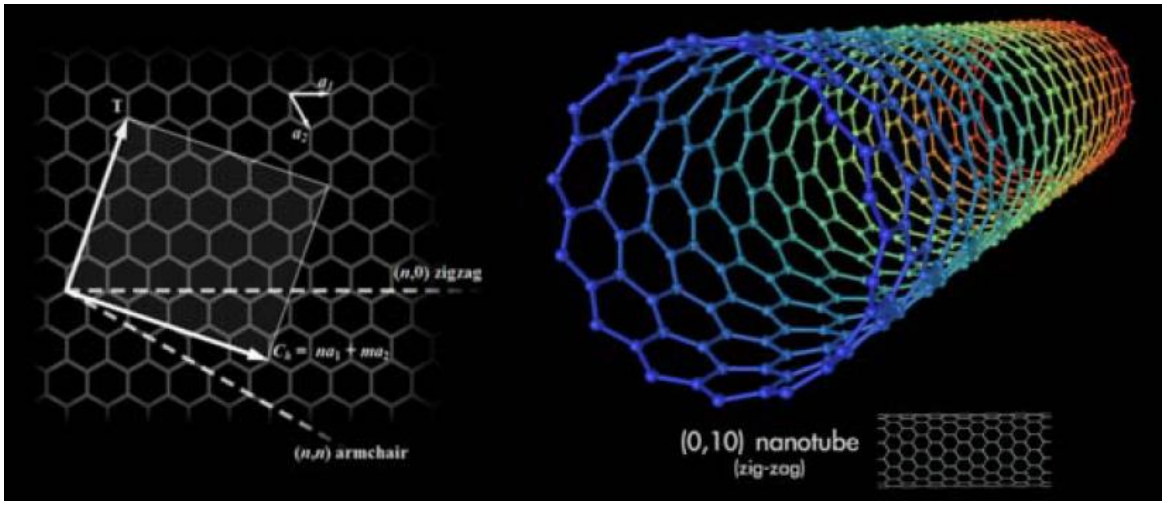


Figure 2.3: A graphene sheet showing the nanotube unit cell, and a representation of a rolled up zigzag nanotube.

SWNT can be classified into three types based on their wrapping indexes n and m. [40] Given a wrapping index (n, m), we calculate$n - m = 3q + p$, where p is either -1, 0, or 1. In the case where p = 0, the 1-D k_{ll} sub-band the aligns with the K1 point at the intersection of the conical electron and hole energy bands.

II.1.4) Diamond: sp^3 carbon

In addition to forming sp2 bonds and creating materials like graphene, carbon can form sp3 bonds and become diamond. While graphite is the more stable state at STP,

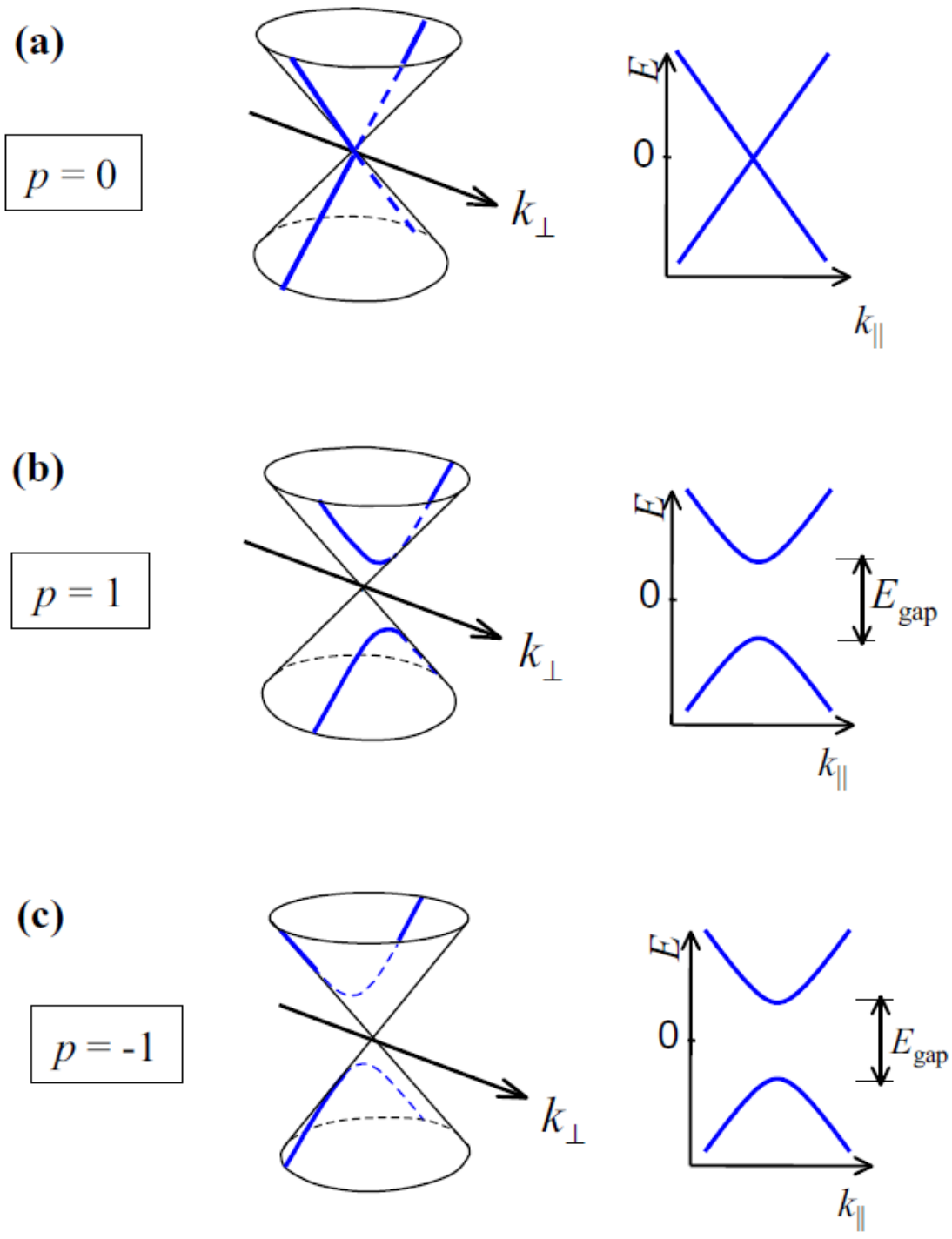
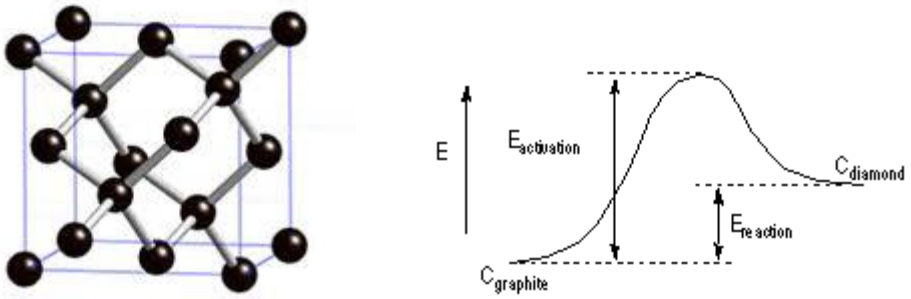


Figure 2.4: Difference in alignment between the dispersion cone at $\mathbf{K_1}$ and the allowed **k** for a carbon nanotube. When p=0 (a) the two align and no gap exists. However, when p=±1, (b, c) the misalignment between the $\mathbf{K_1}$and the nearest 1-D sub-band causes a gap to form leading to semiconducting nanotubes. [8]



a) b)

Figure 2.5: Representation of the diamond unit cell (a) and the energy barrier between the diamond and graphite phases. (b)

under conditions with a high temperature and pressure the diamond phase is the more energetically stable configuration for the carbon atoms to take. Under these conditions, diamond is able to form. Since there is an energy barrier in the transition between the two states, the diamond lattice constitutes a metastable state. Diamond has a unique blend of properties which make it an interesting material, including having high mechanical strength, being chemically inert and radiation hard, possessing a large breakdown voltage and relatively large dielectric constant, and having a large thermal conductivity while maintaining high electrical resistance due to its large band gap of 5.5 eV. These are the properties of an ideal crystal of diamond; however, only Type IIa diamonds grown with virtually no impurities are pure enough to exhibit the electrical properties of the ideal crystal. Other forms of diamond are imperfect crystals, and are more conductive due to the inclusion of defects, non-diamond phases, and scattering off of grain boundaries.

Much of the research that has been done has concentrated on diamond films which are poly-crystalline, CVD grown diamond, since it is cheaper and easier to

produce than single crystal diamond. Polycrystalline diamond is grown by first nucleating a surface and growing the diamond from these nucleated sites. This creates a film made of a many small diamond crystals, grains, which have grown together.

Nano-crystalline Diamond

A subset of polycrystalline diamond, nanocrystalline diamond, or "nanodiamond", is a material that occurs when the size of individual grains are on the order of nanometers instead of microns. Because of the small size of the nanodiamond crystals, the interfaces between the grains play a larger role in determining the material properties than in conventional bulk, or even microcrystalline, diamond. In addition to allowing for smaller dimensions, these surface effects give rise to a number of properties which differ from conventional CVD diamond: including smoother and more uniform surface morphology, increased (though still minute) sp^2 content, hardness and lowered internal stress, and wider latitude for integration with other materials. [37] Because of these properties, as well as the unique blend of properties which diamond normally has, nanodiamond has become a material of interest in a variety of fields. These fields include vacuum electron devices, NEMS, biosensors, electrochemistry, and other varied fields. [32-36]

II.2) Effects of Radiation

Total Ionizing Dose Effects

Ionizing radiation can cause degradation in CMOS circuits by creating electron hole pairs (EHPs) in the gate and isolation dielectrics. Recombination occurs between some of these pairs, and therefore does not affect the device. Due to the different mobilties of electrons and holes, the charges can separate and lead to the creation of

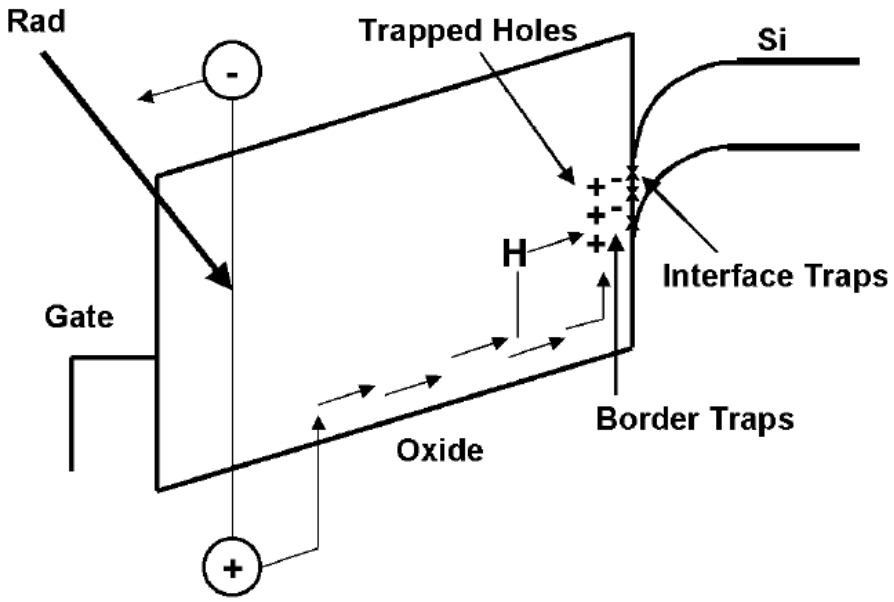


Figure 2.6: Energy Band diagram showing ionizing radiation creating electron-hole pairs in the SiO_2 layer of a MOS under positive bias. [10]

trapped charge states inside of the CMOS circuit. The percentage of EHPs that are able to escape initial recombination is governed by the strength of the dielectric electric field. A large field will lead to fewer recombination events. [10, 11] A significant portion of the remaining charges can become trapped at defects in the dielectric layer. The mechanism

of radiation induced charge generation and trapping in a SiO_2 gate dielectric is shown in Figure 2.6. This figure depicts the energy band diagram of a metal, p-type substrate MOS irradiated under positive bias. While electrons may be quickly carried away to the gate electrode, as is the case with SiO2, the holes remain relatively stationary. Over time these holes migrate to the oxide-semiconductor interface. At this interface some of these holes become trapped at deep level sites. [10] These holes will form a positively trapped charge density. While only the trapping of holes is depicted in this diagram, in most dielectrics a significant number of electrons also become trapped. The overall trapped charge in SiO_2 and most alternative dielectrics, tends to be a net positive charge. [12]

Oxide Traps

One of the common types of traps created by ionizing radiation is oxide traps. Oxide traps occur when a net charge (usually positive) is formed in the bulk region of a dielectric by trapping holes, in the case of a positive oxide trap, at defect sites within a dielectric. The density of oxide-charged traps is largest immediately following exposure to radiation. Over time annealing occurs, either by tunneling of electrons from the Si or thermal emission of holes from the trap sites. [13] Charge trapping in alternate gate dielectrics is a large concern, and IBM has shown that the probability of bias induced charge trapping in high-k dielectrics is extremely high. This is due to the large densities of intrinsic defects, as opposed to SiO_2, which generally has very few "as grown" defects, [14, 15]

Interface Traps

In addition to oxide traps, radiation can also change the interface trapping properties of a device. Interface traps occur directly at the interface, and have energies that lie in the Si band-gap. [16] Traps in the upper half of the Si band-gap are acceptor like, meaning they are neutral when filled and positively charged when empty. Traps in the lower half of the band gap are acceptor like, and are thus neutral when empty and negatively charged when filled. [14] Trap sites with energies of a few kT below the Fermi level are filled, and those with energies of a few kT above the Fermi level are empty. The number of occupied traps at the interface is therefore bias dependent, as the amount of band-bending determines the number of sites above or below the Fermi level. Thus when a device is biased at mid-gap, the interface traps are neutral. [17, 18] Unlike oxide traps, the interface trap states are stable and do not anneal. [42]

Single Event Effects

In addition to total dose effects, energetic particles, such as protons or alpha particles, can create single event effects (SEE). When a single energetic particle strikes a material, it generates a dense plasma of EHPs along the path of the particle which can trigger a variety of single event effects. [39] There are two classifications of SEE, hard and soft. A soft event causes no permanent damage to the device, and may be recoverable, while a hard event causes permanent damage to the device.

Radiation-induced Hard Breakdown

Catastrophic failure known as radiation-induced hard breakdown (RHB), also called single event gate rupture (SEGR), can occur under conditions of high electric field.

As a heavy particle passes through the dielectric, a conductive plasma path is formed, which allows the capacitor formed by this structure to discharge. If the energy stored in the dielectric is high enough, it can lead to a thermal runaway condition. [19] In extremely thin dielectrics, the electric field within the dielectric increases to conditions that pose a concern for potential SEGR to occur.

II.3) Dielectric Materials

Dielectric Constant

Dielectric materials function as the insulating material in many devices. The permittivity of a dielectric can be written

$$\varepsilon = \varepsilon_r \varepsilon_0 \qquad (2.1)$$

where ε_r is the relative permittivity and ε_0 is the permittivity of free space (8.85×10^{-12} $C^2/N \cdot m^2$). In practice, the relative permittivity is often referred to as the dielectric constant (ƙ). The dielectric constant indicates the amount of energy a dielectric can store compared to free space.

Charge Transport in Dielectrics

In dielectrics, the dominant charges are bound charges, namely charges that are bound by local atomic or molecular forces. Unlike in conductors, where the Fermi level lies above the conduction band and electrons are free to move through the material, charges in dielectrics are only able to shift slightly from their equilibrium position and

form dipoles. The process of forming these dipoles is referred to as polarization. Each dipole has a dipole moment:

$$\partial\rho = Ql \qquad (3.2)$$

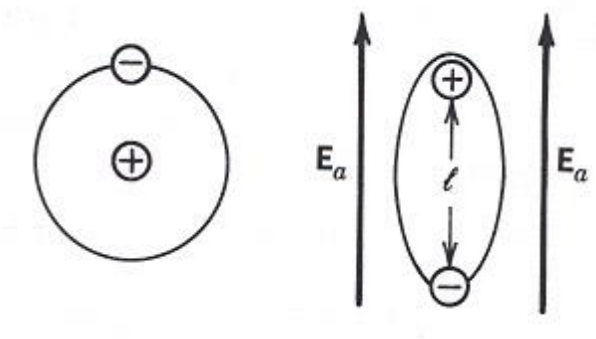


Figure 2.7: Schematic of an atom under equilibrium (left) conditions and under the influence of an external electric field (right)

Here Q is the magnitude of the charge and l is the separation between the charges. By summing the individual dipole moments, we can find the polarization of the material. This stretching of bonds is the basis for energy storage inside of a dielectric.

Polarization Mechanisms

There are three basic mechanisms of polarization: dipole polarization, ionic polarization, and electronic polarization. Dipole polarization occurs in materials with a permanent dipole moment. Even though these dipole moments are normally randomly oriented, they will align themselves when exposed to an electric field. Ionic polarization occurs in materials with ionic bonds. When exposed to an electric field, the ions will separate to the two poles of the field. Electronic polarization occurs when an electric field displaces the electron cloud relative to an atom's nucleus.

Types of Dielectric Materials

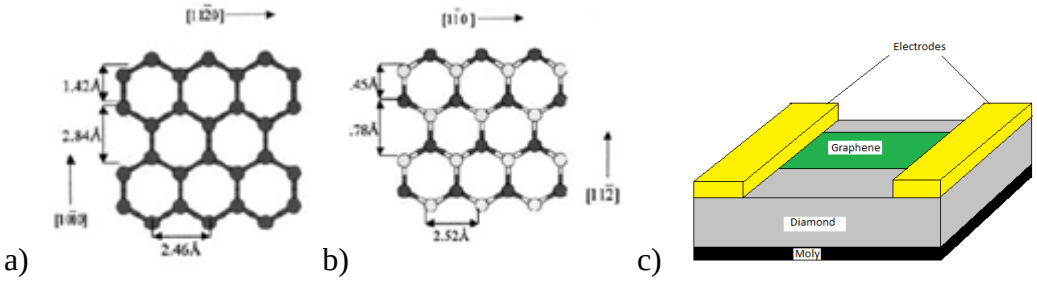
The total polarizability is a function of the three mechanisms mentioned above, however not all materials manifest all three forms of polarization. Non-polar materials are the simplest type of dielectric. In non-polar materials there is no net charge, no net dipole, and no net polarization in the absence of an external field. The charges are distributed in such a way that any negative and positive charges cancel each other out. In this case, only electronic polarization can occur. Diamond is an example of a non-polar material. The second type of dielectric is a polar dielectric. Polar dielectrics exhibit ionic polarization in addition to electronic polarization, but have no permanent dipole moments. Ionic crystals are an example of polar materials. Dipolar materials have a permanent dipole moment and are thus affected by all three forms of polarization. Water is an example of a dipolar material.

Chapter III

Fabrication of Diamond Films

Why Diamond makes an interesting Substrate for Carbon Devices

Graphene and CNTs have the highest room temperature intrinsic carrier mobility of any known material. However, the electron mean free path is less than 1 micron due to strong impurity scattering. [2] There is strong evidence that graphene is a nearly perfect two dimensional hexagonal lattice. It has been put forth that the scattering occurs from extrinsic sources, namely the interactions with the substrate. [2] In order to circumvent this problem, alternate dielectric substrates to SiO2 are needed. One very promising candidate for such a dielectric is diamond. Diamond possesses a number of electrical, material, and morphological properties that make it an ideal candidate for use



a) b) c)

Figure 3.1: Illustration of graphene (a) and a diamond (111) plane (b) viewed along the <111> projection. The lighter colored circles in the diamond structure represent raised atoms. (c) is a representation of our proposed graphene on diamond device.

with nanocarbon devices. Due to the geometric similarities between certain diamond orientations and graphitic sheets (shown in Fig 3.1 a and b), it has been shown that diamond can form chemically and mechanically hybrid interface structures. These

structures have low residual strain and no unsatisfied bonds. [20] Therefore, using diamond as a substrate for graphene or CNTs has the potential to minimize the interface defects that limit mobility.

Another area of interest is the effects of radiation on carbon nanostructures. Previous attempts to explore the subject have shown that the predominant damage is damage done to the substrate. [20] This obscures the information on the carbon structure itself. Diamond on the other hand, is known to be resistant to displacement damage and less likely to form trapped charges. [21] Therefore using it as a substrate for radiation testing purposes would allow for viewing the damage on the CNT or graphene instead of the underlying substrate.

Since the nature and properties of the substrate play such a large role in the transport of electrons, it is important to have a good understanding of the substrate itself. As we move towards thinner and more nano-crystalline diamond films to serve as dielectric materials in transistors, it is unclear what effect these increased non-idealities will have on the otherwise preferable properties of diamond.

Fabrication

Fabrication of Diamond Films

Diamond based metal-insulator-Silicon (MIS) devices (schematically represented in Figure 3.1c) were fabricated using two sequential layers of i-diamond on a supporting substrate of p-silicon. Silver contacts were then deposited on top of the films for use in electrical measurements. The diamond films were grown using microwave plasma-assisted CVD in a two-step (seeding and growth) process. The seeding step was performed on the prepared surface of the substrate in an evacuated chamber using a

mixture of 89% Hydrogen, 10% Methane, and 1% Nitrogen at 800°C, 11.5 Torr, and sustained by a 550 W plasma. These conditions were used for the seeding layer to encourage nucleation growth to form a uniform film over the whole of the substrate. The bulk layer was then grown using a 98.5% Hydrogen, 1% Methane, and 0.5%

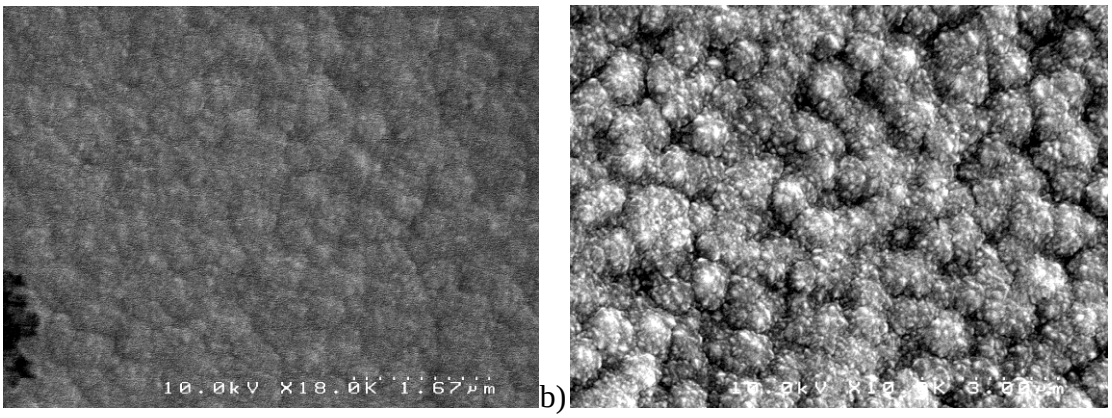


Figure 3.2: SEM image of the diamond surface after the first step (a) and second (b) step of the growth process.

Nitrogen mixture at 875°C, 11.5 Torr, and sustained by a 650 W plasma. Conditions were chosen to make the bulk layer as resistive as possible. By reducing the methane content, the growth is stunted, and the intense plasma conditions etch some of the graphitic content during growth. This should give a more pure sp3 bonded film, and thus a more resistive film. The samples were annealed at 500°C for 20 minutes. Figure 3.2 shows the surface structure of the 2 growth stages.

An important step in the CVD process is the original nucleation step. Defects on the substrate surface, e.g. scratches, grain boundaries, and dislocations, serve as sights for nucleation of diamond to occur [41]. Since these defect sites are the likely places for diamond growth to occur, it is important to have a high density of surface defects. Having a high density of nucleation sites ensures contiguous film growth, and allows for

thinner films to be grown. The latter statement is true because nanodiamond clusters grow in a roughly spherical form. A higher density of sites means less lateral spacing and consequently less vertical growth. Therefore the preparation of the surface, especially when using IC grade Si as a substrate with few natural defects, determines much about the growth of the resulting film. The introduction of defects, however, has a negative impact on the electrical performance of the insulator. It is important to balance defect creation with electrical performance. For the growth described above, nucleation was done by mechanical abrasion using nanodiamond powder. This technique was used because it gives the largest nucleation density and thus the thinnest films.

The two step process also allowed for the films to have two different possible surface morphologies. The second stage provided a rougher topology, which can be used to study the effects of strain on graphene. To make a smoother surface, several of the diamond films were brazed to molybdenum and had the silicon substrate etched away in KOH.

Metal contacts were formed using two different methods. 3mm contacts were deposited by either sputtering aluminum or using silver paint. Both aluminum and silver were chosen to make ohmic contacts. Sputtered contacts make good contact but may damage the diamond surface, introducing defects and making the film more conductive.

In addition to the standard method of film growth described in the previous section, a number of other methods were attempted. The brazing process changes the morphology of the diamond film, causing a wavy pattern to be observed on the diamond surface. This waviness corresponds to the way the underlying Ti:Co:Ag melts and then

cools. In order to test whether the brazing process alters the properties of the diamond film, a free standing diamond film was grown. A diamond film could be altered by either changing the surface morphology, introducing defects by straining the diamond film to conform to the Ti:Co:Ag, or defects caused by release of gas during the brazing process. The initial growth procedure was similar to the previously described process: abrasive nucleation on a Si substrate, followed by growth of nanodiamond in the CVD chamber. However, after initial film growth, the film was transferred to a high-power MPCVD chamber. A thick layer of Boron-doped microcrystalline diamond (~250 µm) was grown on top of the nanocrystalline layer. The Si layer was then etched in KOH, leaving an all diamond film.

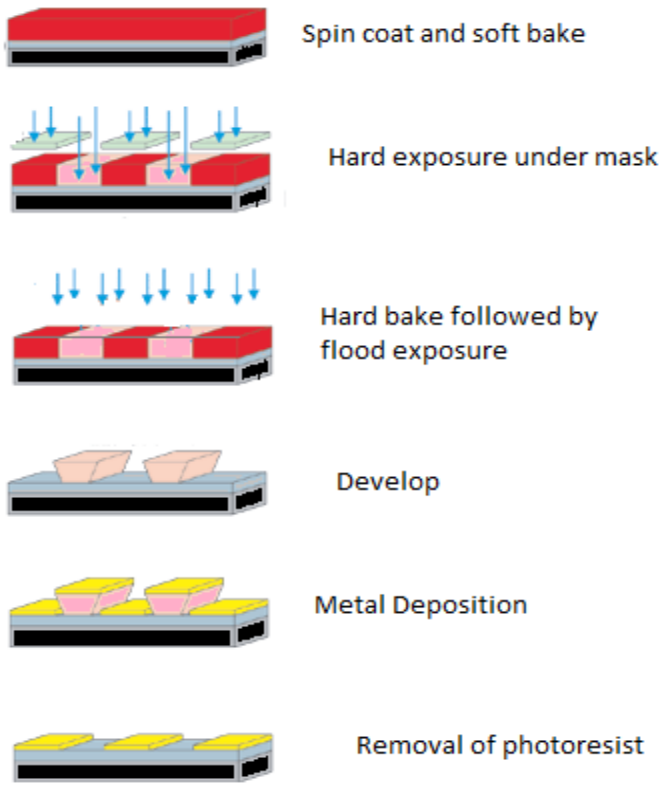
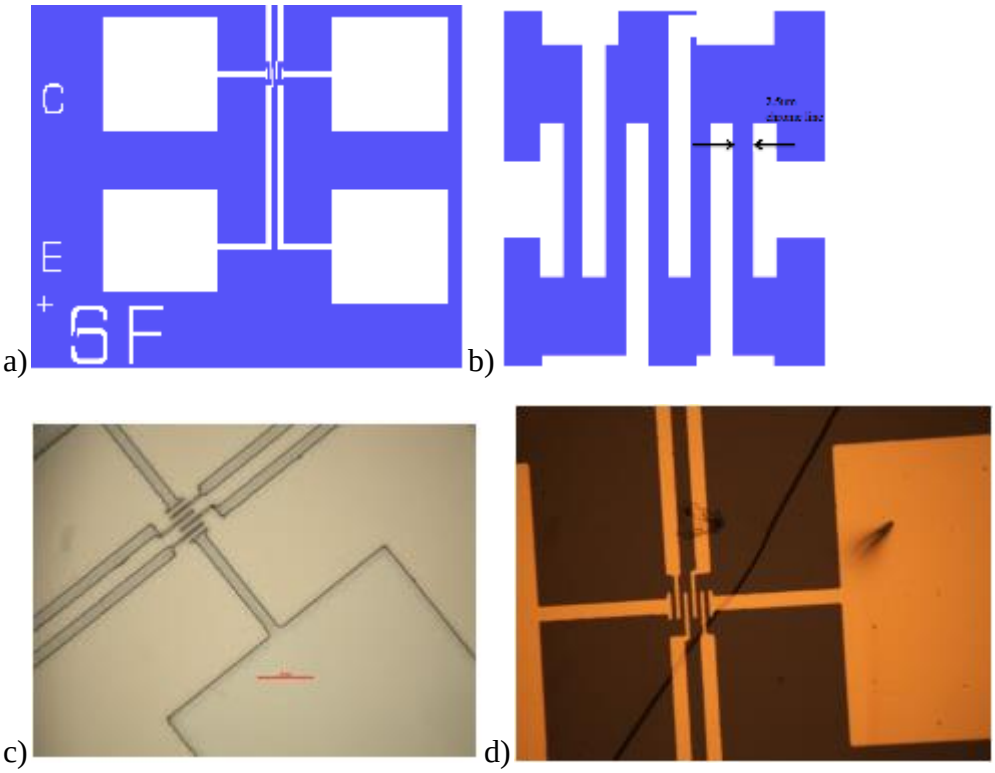


Figure 3.3: Representation of photolithography process step by step.

Fabrication of Carbon Transistor Devices from carbon nanotubes

Several of the "smooth" surface diamond films were used as transistor substrates. In these cases, contacts were patterned using a lift-off photolithographic process (described in Fig 3.3). Two microns of AZ-5214E photoresist were spun onto the substrates at 2000 RPM and



a) b) c) d)

Figure 3.4: (a, b) are schematics of the mask used for the photolithography process. (c) is inspection of development on a SiO2 substrate pre-metal deposition. (d) is post-metal deposition on a diamond substrate

subjected to a soft-bake at 95° C bake for 2 minutes. The sample was then placed in hard contact with our mask and exposed to light for 0.3-0.4 seconds depending on the source power, ~11.5-13.5 mW. The samples then underwent a hard bake at 115° C for 2 minutes before undergoing a flood exposure for 1 minute. The sample was then

developed and inspected using an optical microscope to confirm successful patterning. The sample was then placed in an Angstrom Resistive Evaporator and deposited with 40 nm of gold. The remaining photoresist was then removed using an acetone bath. The mask pattern is shown in Figure 3.4 along with optical images confirming successful patterning of substrates. In some cases the features were not sharp enough for the gold pattern on top of the photoresist to be discontinuous with the gold deposited onto the film. In these cases, sonication in acetone was performed to remove any excess photoresist.

Transistors were made by transferring CNTs onto diamond and SiO2 substrates. 90% pure semiconducting CNTs were procured from nanointegris, with a concentration of .01mg/ ml. The transfer process first proposed by Rinzler et al. [30] was used to transfer the CNTs onto a surface. The CNTs were in a surfactant solution and were sonicated at 9 watts for 20 minutes to disperse the nanotubes into solution. The solution was then filtered through a 0.45 micron pore size mixed-celluloid ester (MCE) filter in a vacuum filtration setup. The filtration was done for ~20 minutes, longer if needed to completely dry the filter. The filter, still under vacuum, underwent successive rinses with water to wash the surfactant away. The rinse was considered complete when bubbles quit appearing in the filtered portion. This process left a wet MCE filter with a carbon nanotube dispersion. This filter was then transferred onto the surface of the desired substrate and placed in compression while baking at 90° C for 45 minutes. . The

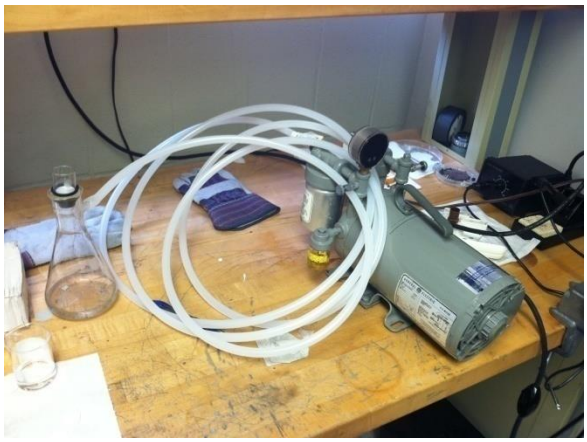


Figure 3.5: The experimental setup for the vacuum pump.

surface tension in the water brings the CNTs and the substrate into intimate contact and allows adhesion to form between the two. [30] The film and substrate are then transferred into successive acetone baths to completely remove the MCE filter. The end product is a substrate with a carbon nanotube film on its surface. Figure 3.6 shows the successful transfer of a several micron CNT film onto a diamond surface. Several variations on the

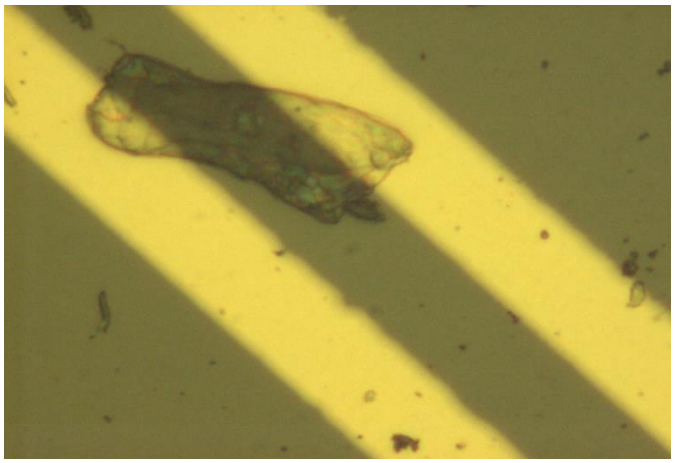


Figure 3.6: Transfer of a small carbon nanotube film onto a diamond substrate with metal contacts. The gap between the metal contacts is 7.5 microns.

above described procedure were performed in attempts to both maximize the amount of transferred CNTs, as well as ensure the cleanliness of those transferred films.

In addition to the simple back-gated devices shown previously, we wanted to create more complex devices. For these more complex devices, Si gates buried in a SiO2 layer were fabricated on a Si substrate with the intention of growing a thin diamond layer over the top layer of SiO2. These SiO2 gates (shown in Figure 3.7) were provided by Ji Ung et al. at Albany University.

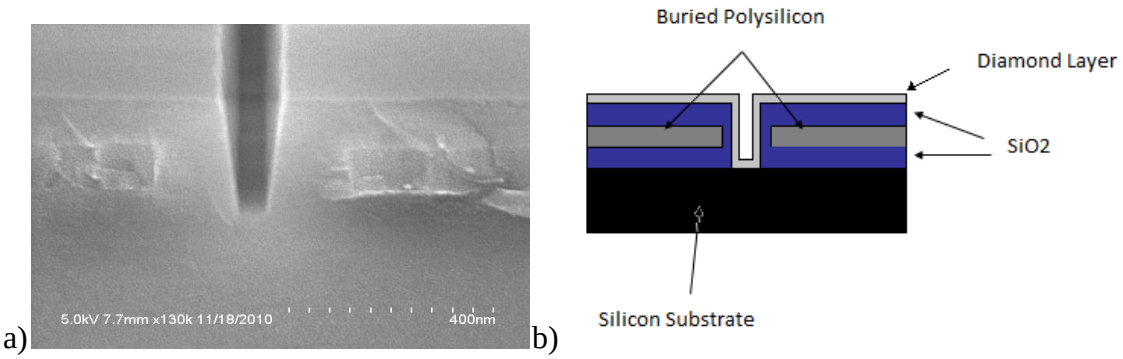


Figure 3.7: (a) SEM image of the cross section of one of the buried Si gates provided by Albany University. (b) schematic of the intended design after diamond deposition layer.

Figure 3.8 shows the three different nucleation techniques which were used in diamond growth attempts on Si/SiO_2wafers. These attempts were an effort to simulate the conditions that would be used in the diamond growth on the buried Si gate devices. The same growth conditions were used here as described earlier for growth on Si. The nucleation techniques used were: 1) electric field bias, 2) sonication in diamond nanopowder, and 3) light mechanical abrasion from diamond nanopowder.

As shown in Fig 3.8, none of the three shown nucleation techniques resulted in a cohesive film, free of pin holes. The sample grown under electrical bias had very little growth. The sample grown after sonication shows areas of "good" diamond growth, but also has large portions of the film which are sparsely nucleated. Even in the areas of "good" diamond growth, the film is neither cohesive nor free of pin holes. The sample grown after mechanical abrasion had fairly good growth, but contained pinholes. Still with further growth time, the clusters surrounding these pinholes may grow together

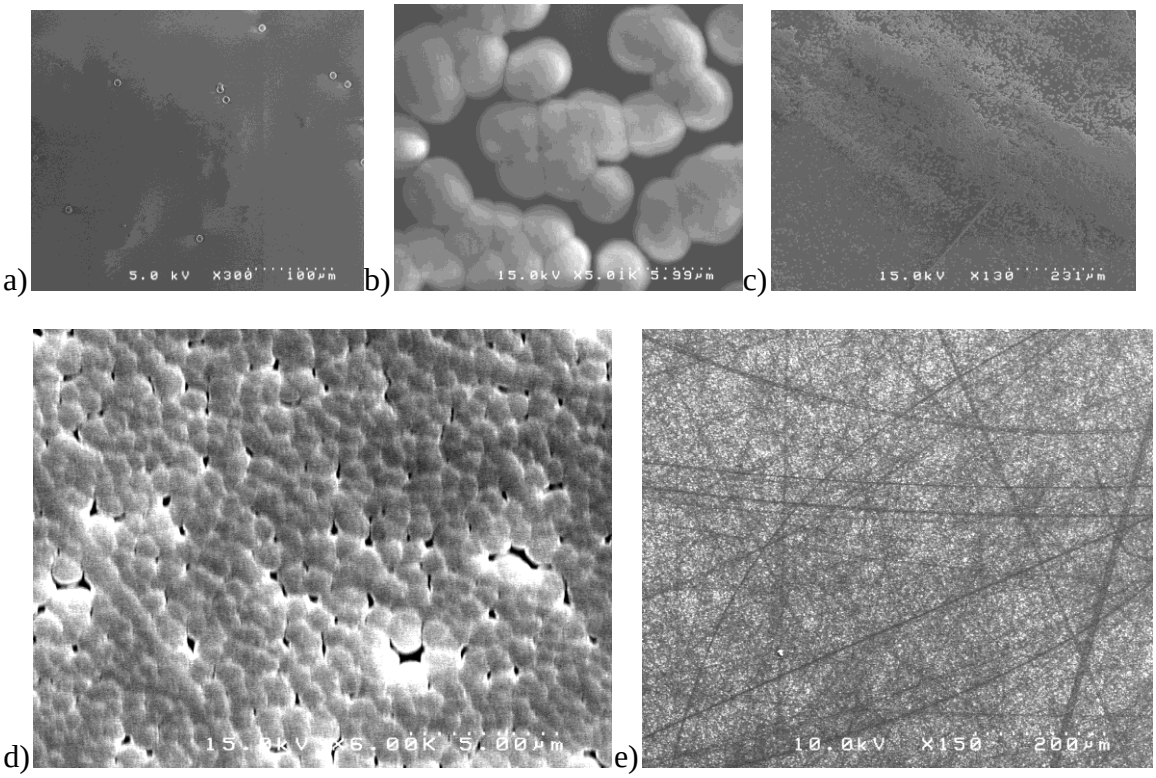


Figure 3.8: Results of diamond growth on SiO2 using various nucleation techniques. (a) Electric field bias (b and c) light sonication (d and e) light mechanical abrasion

eliminating them altogether. However the cluster size of the diamond grains in this sample is greater than 500 nm. This size would completely obscure the structure of the underlying gate, as it would bridge the crevice. This sample has the smallest of the

nanoclusters, so none of the above shown techniques would serve to fill the need of a thin, small clustered, contiguous film which was needed to coat these samples. A more aggressive mechanical abrasion should yield a denser nucleation density, which in turn would yield smaller clusters and a more contiguous film. However, doing so damages the interface and introduces traps. This limits its use as a dielectric for use in a transistor device.

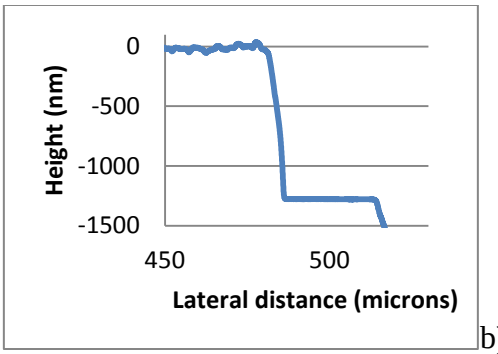
Chapter IV

Preliminary Analysis and Discussion of Diamond films

IV.1) Material Properties

Multiple films were grown at once under identical conditions. Some of the films were used to test the materials properties of the films while the others were used for testing their electrical properties. Since some of the materials characterization methods required damaging parts of the film, electrical and material characterization had to be carried out on separate films grown under identical conditions. After the films were grown, the thickness of one of the carbon films was measured using a profilometer. The diamond film and silicon wafer were broken into two pieces, and the height difference was measured across areas where the crack pattern had left areas of exposed silicon. The thickness was measured as 1370 ± 80 nm; the results are shown in Figure 4.1a. This indicated thickness is among the smallest reported for a continuous film, an order of magnitude smaller that the thinnest films possible even 5 years ago. [38]

Raman measurements were taken on both a nano-crystalline (NC) CVD diamond sample as well as a single crystal sample using a Thermo Scientific DXR Raman microscope with 785 nm diode laser. The results are presented in Figure 4.1b. The single crystal sample shows the expected single absorption peak around 1333 cm^{-1} which is indicative of sp^3 bonding in carbon. The nano-crystalline diamond sample also shows

a) 

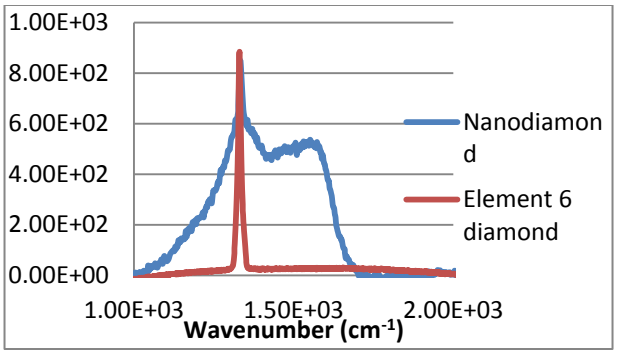
b) 

Figure 4.1: (a) Profilometry measurement showing a thickness o3 ~1400 nm for our carbon film. (b) Raman measurements showing our diamond film is largely diamond in content.

a sharp peak at 1333 cm^{-1}, indicating the presence of a large amount of diamond in our samples.

Figure 4.2 shows AFM images of the NC diamond surface. Figures 4.2a and 4.2b were made on the exposed side. Figure 4.2c was taken after etching the silicon substrate away. The surface of the substrate needs to be as smooth as possible to avoid adding strain to the graphene sheet or nanotube which would rest on top of it. Our AFM measurements showed that we could create films with only a few nm of variation in surface roughness, and with an RMS of less than a nm. This level of smoothness should be on par with the smoothness of SiO2 substrates that currently are used. These diamond sheets should be smooth enough for a graphene sheet on top to be minimally impacted.

Palasantsaz et al. [23] showed that surface roughness can have an effect on the capacitance of a thin film. Figure 4.2b shows that the average separation between the different clusters is around 50 nm. Due to this relatively large separation of clusters in our sample, each individual cluster acts relatively independently and we expect to see no increased capacitance as a result of our roughness.

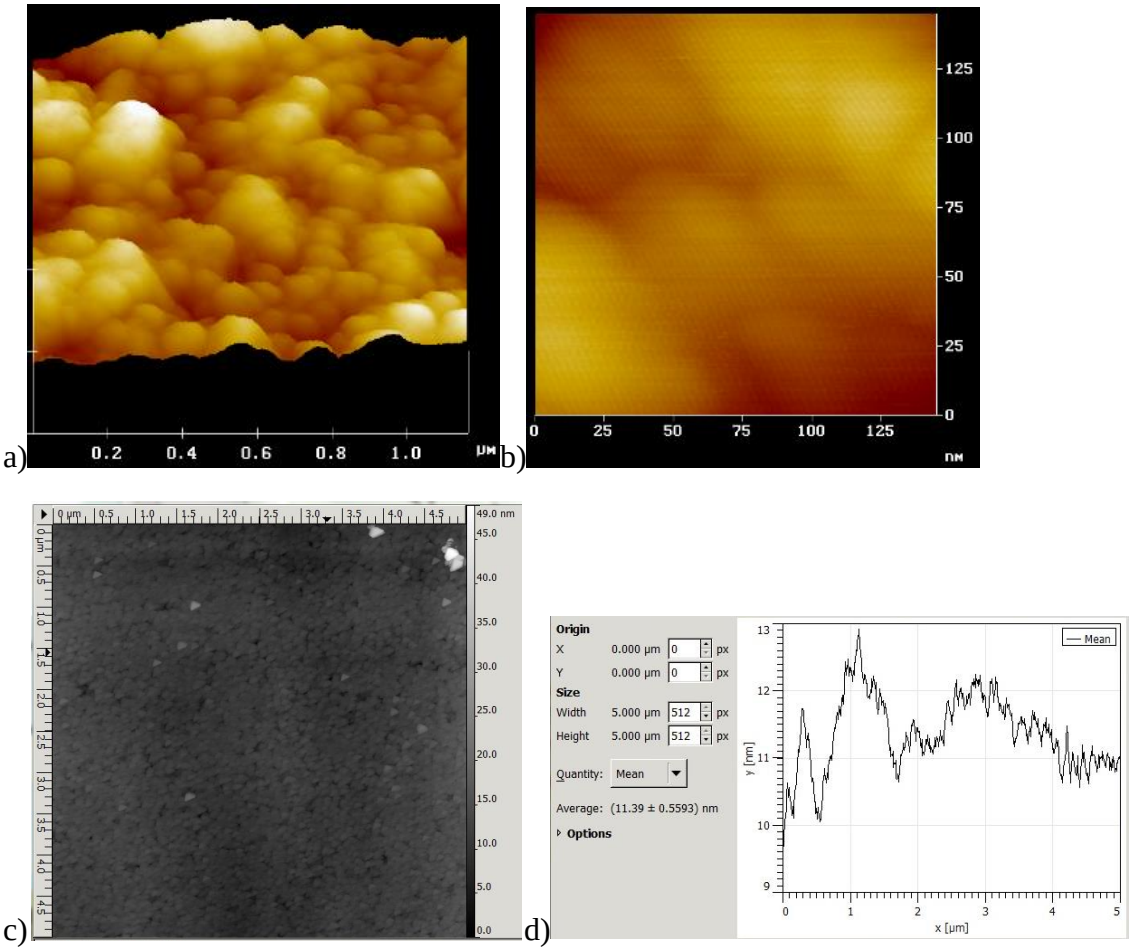


Figure 4.2: (a) and (b) are AFM of the exposed side, showing nano-crystalline clusters of approximately 50 nm in size. (c) is the AFM of the etched away side and (d) is a surface roughness analysis of figure c.

IV.2) Diamond as a Dielectric Material

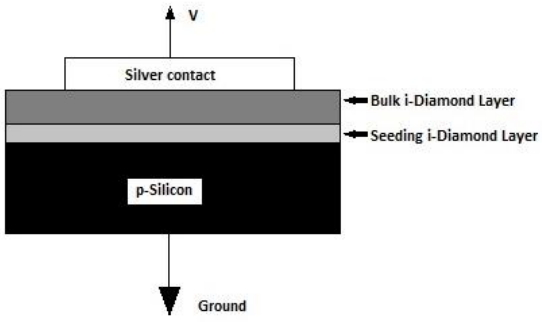


Figure 4.3: Schematic of the structure used in electrical testing.

The diamond films were characterized by their current-voltage (I-V) behavior using a Hewlett Packard 4156 Semiconductor Parameter Analyzer and the setup shown in Figure 4.3. The I-V characteristics are shown in Figure 4.4. The resistance can be drawn from the slope of the ohmic region of the I-V curve. This gives resistances of $5x10^{11}$ and $3x10^{11}$ ohms, for the sample with silver paint and sputtered contacts respectively. Using:

$$\rho = \frac{R*A}{d} \qquad (4.1)$$

We find resistivities of $2.58x10^{14}$ and $1.55x10^{13}$ Ωcm, for the silver paint and sputtered contacts respectively. The value of $2.58E^{14}$Ωcm is comparable to the resistivity of SiO2. With so little current flow through the diamond insulator, the structure should act as essentially an ideal oxide. Outside of about ±2 volts, the film begins to leak current and no longer exhibits ohmic behavior. This field strength (~$1.5 * 10^4$ Vcm^{-1}) is well below the breakdown strength of diamond (~10^7 Vcm^{-1}). This can be attributed to the presence of highly ordered pyrolytic graphene (HOPG) within the diamond film. HOPG is more conductive, and breaks down at a lower voltage than diamond. Therefore, the electrons

are able to find a less resistive path through the film. This could prove problematic as the diamond may begin to fail as a dielectric for some of the voltages we would need to use in our radiation testing.

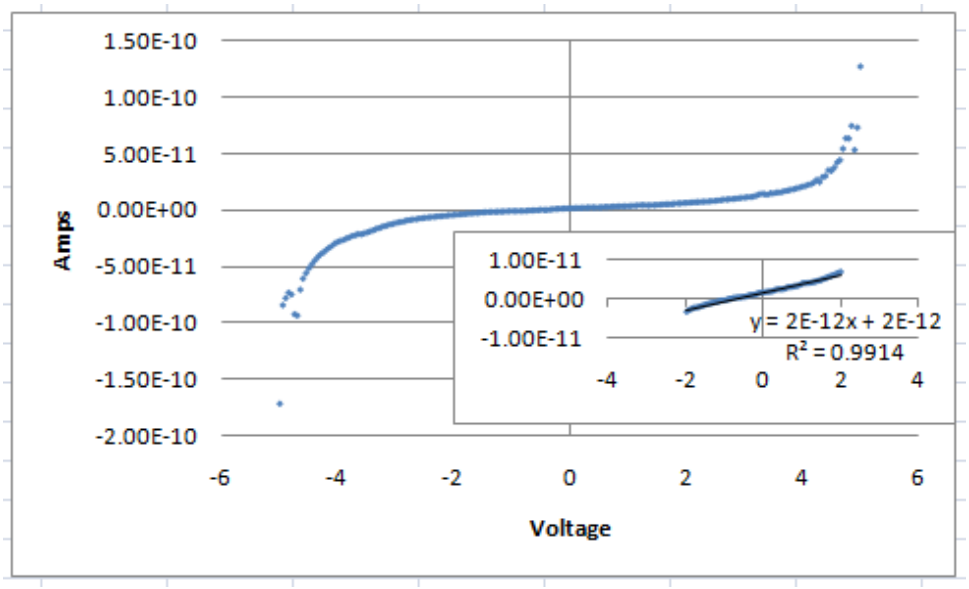


Figure 4.4: Typical I-V of one of the diamond substrates.

Capacitance-voltage measurements have not been taken on the diamond films reported on above; however C-V measurements were carried out on earlier films grown under similar conditions. The high frequency C-V behavior of these films was studied using a HP 4284 LCR meter. The C-V behavior of the silver paint film is shown in Figure 4.5. Since our device uses a simple parallel plate setup, the capacitance can be calculated:

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \qquad (4.2)$$

where ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the dielectric, A is the area of the electrodes, and d is the distance between the two electrodes. The plot

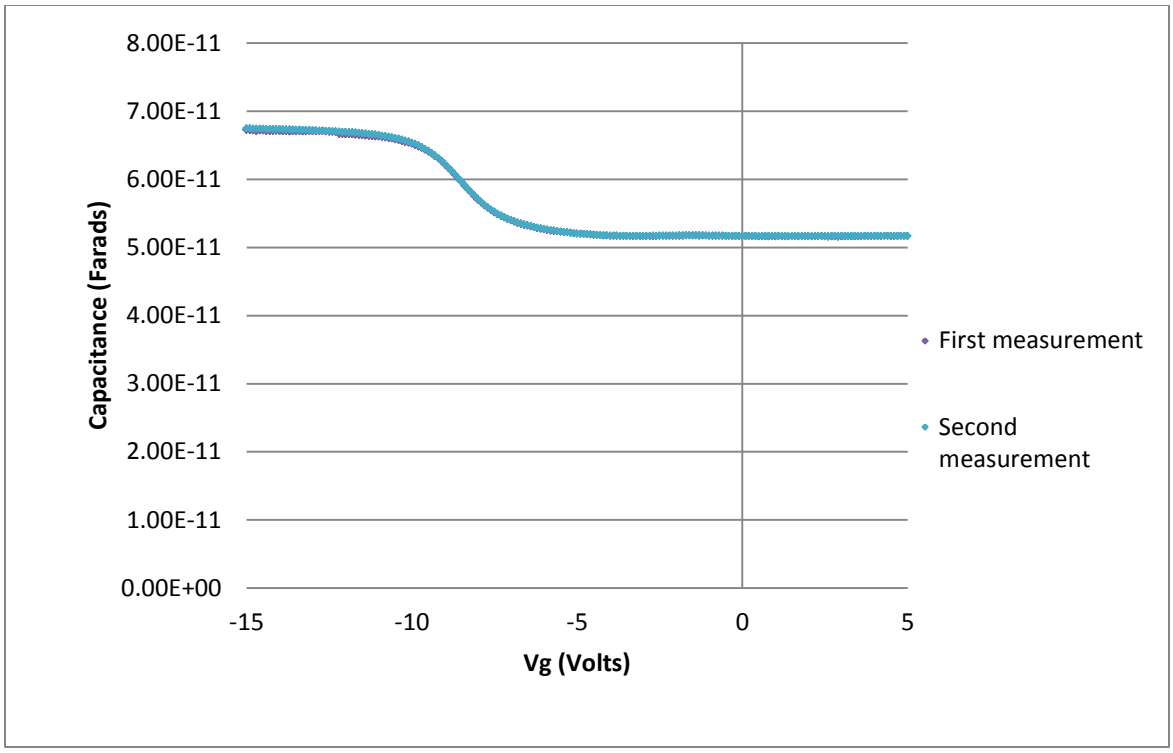


Figure 4.5: C-V plot of diamond MIS device.

shows an accumulation region where the capacitance is 6.75×10^{-11} farads. Using this as the diamond film's capacitance, we calculate a dielectric constant of 0.209, well below the expected value of 5.5. This is largely due to the large voltages at which this measurement had to be carried out. Our diamond films are no longer in the ohmic range around -2 volts, whereas it doesn't enter accumulation until -10 volts. At these voltages, excessive current is leaking through the device, and thus we expect a smaller capacitance. This observed large shift in the flat-band voltage indicates the existence of a substantial amount of oxide charges. The spread out nature of the depletion region indicates a fairly large number of interface traps. These defects would have a negative impact on the mobility of the carbon devices that would be supported by the diamond film, and effort needs to be made to minimize them if we desire to use polycrystalline diamond films as substrates. Despite the number of traps, the repeatability of the C-V measurement would

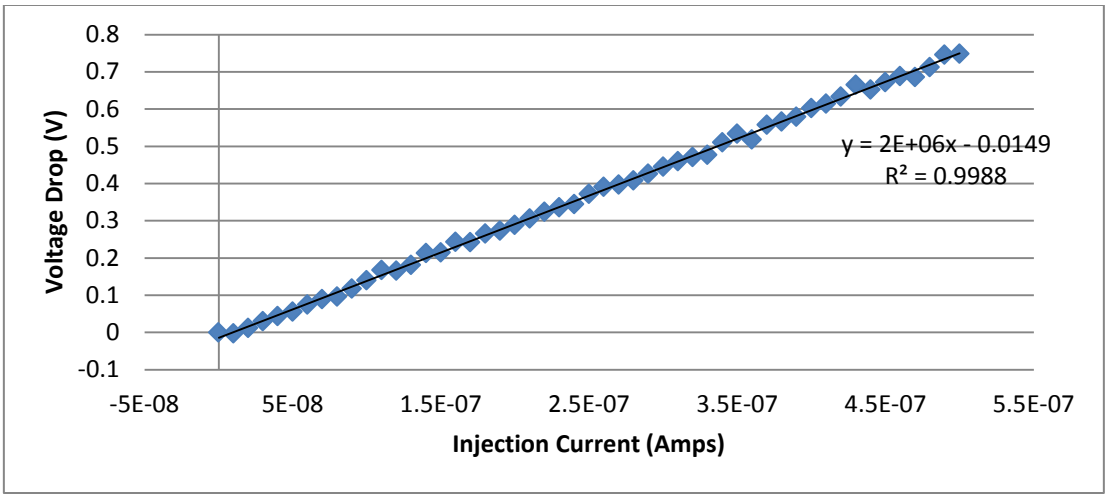
allow us to make meaningful, if not optimal, measurements of the supported channel device. Given the resistance of diamond to radiation, using these films as substrates could help provide useful insight into the mechanisms of radiation damage in graphene and carbon nanotubes.

In order to determine how well the diamond films would act as a dielectric substrate, the sheet resistivity was measured using the four point probe technique. Probes were contacted directly to the surface with a spacing of 2.3 mm between each of the probes. For a thin sheet with spacing between probes (s) much larger than the film thickness (t), the following formula gives the sheet resistance:

$$\rho = k*t\ (V/I) \qquad (4.3)$$

where t is thickness and k=4.53 for in a near ideal case with these geometric effects. Figure 4.6a shows the current vs. voltage measurement for a brazed diamond sample. From Figure 4.6, we can see that (V/I) is $2x10^6$, with approximately thickness of .0001 cm. Our sheet resistance is therefore ~$1x10^3$ Ωm. This value is not consistent with the high resistivity of 10^13 Ωcm and higher reported earlier measured through the film. This indicates that there is another current path, most likely along the grain boundaries on the surface of the diamond film. The measured sheet resistivities are rather low and could prove problematic when attempting to be used as dielectrics in a MOSFET. A significant amount of leakage through the diamond film would occur. The all diamond film's sheet resistivity was also measured using a four point probe technique to check if the brazing process had introduced any additional defects into the post-braze film. The all diamond film had a slightly higher sheet resistivity, by a factor of 2, but much of that.

a)



b)

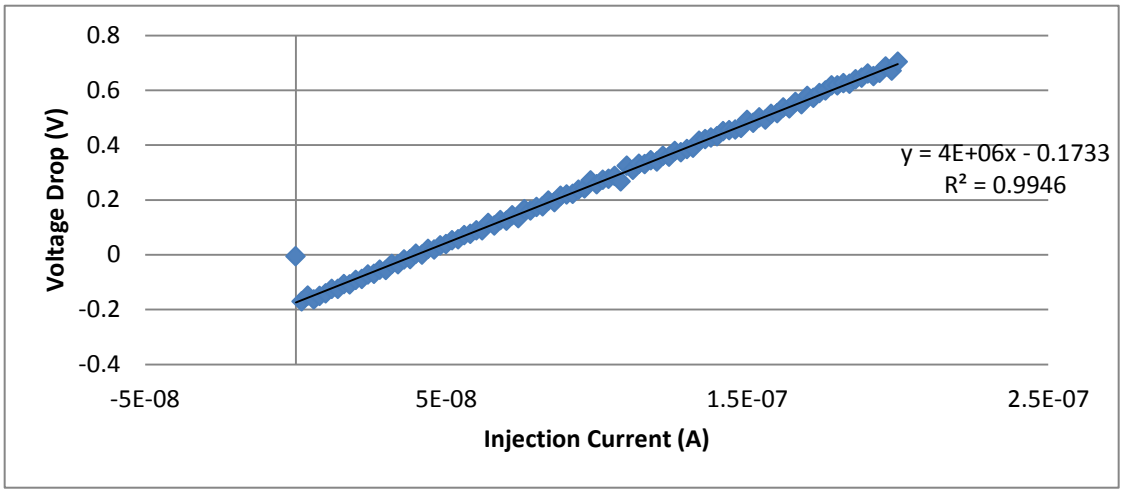


Figure 4.6: Four point probe measurements taken on a brazed diamond surface (a) and the all diamond surface (b)

could be accounted by either differences in the films' thickness or geometric considerations (different deviations from ideality). It does not appear that the brazing process is adding a large enough amount of defects to affect these samples significantly.

IV.3) Transfer of Carbon Nanotubes

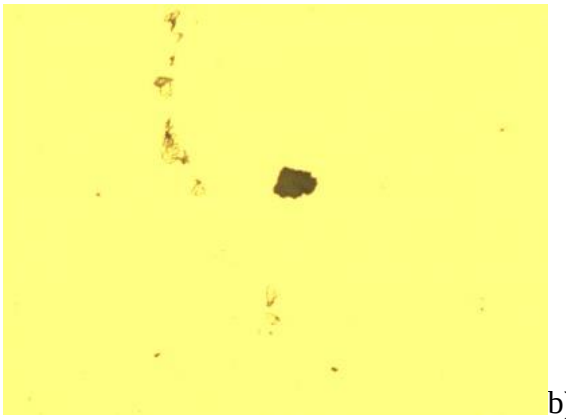
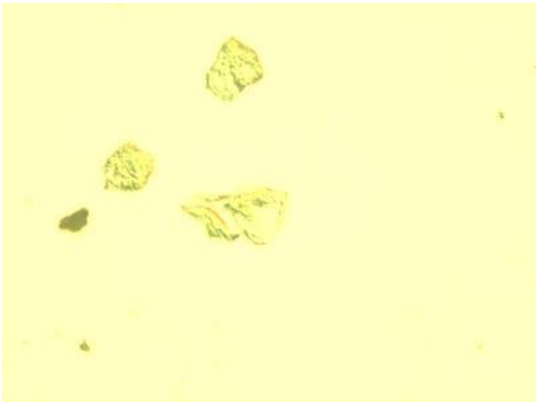
a)  b) 

Figure 4.7: Two attempts to transfer CNTs onto a Si surface.

A number of attempts have been made to transfer CNTs onto both the diamond and SiO_2 surfaces using the vacuum filtration process described in Chapter 5. The process described creates a distribution of CNTs on the surface, and we cannot choose where to place those CNTs. It is necessary to transfer a large amount of CNTs to ensure that the CNTs form a bridge across the electrode gaps. As Figure 4.7 shows, by using the vacuum filtration process we are unable to get a transfer of significant amounts of CNTs onto a surface. The image shown in Figure 3.6 was a lucky and unrepeated occurrence. Several attempts were made to increase the amount of material transferred during the filtration process, however it soon became apparent that the majority of the CNTs were passing through the MCE filters. In the waste of the filtration process, clumps of CNTs started to form. There are two possible explanations for this; either the vacuum generated is too strong, or the 0.45 micron pore size is too large. To test which of these two were correct, the filtration was performed without a vacuum. The resulting CNT distribution

looked similar to those in figure 4.7, meaning a smaller pore size MCE filter is needed for the successful transfer of CNTs.

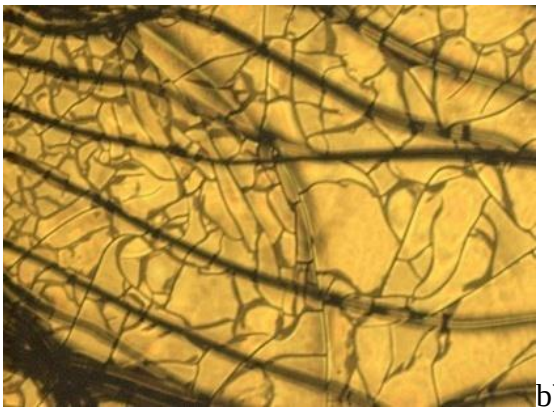
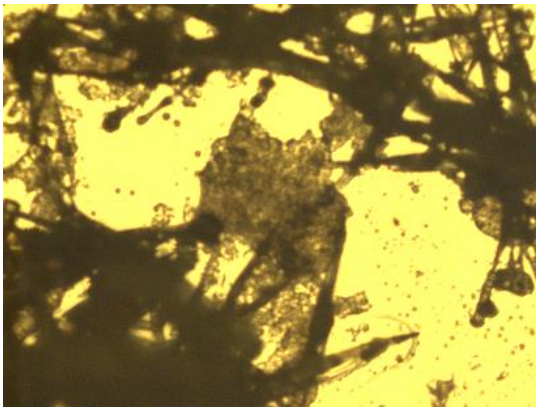
a)  b) 

Figure 4.8: (a) transfer of CNT solution directly from bottle. (b) Transfer of clumps of CNTs found in "waste" from vacuum filtration process

Attempts were also made to bypass the filtration process all together and directly transfer CNTs from solution onto the surface of SiO_2 films. Figure 4.8 shows a few of these attempts. In Figure 4.8a only the surfactant on the surface can be seen. In figure 4.8b, a much larger amount of CNTs appear to have been transferred to the surface, however the surfactant has not been removed and is obscuring possible electrical access to the transferred CNTs. Even after rinsing in water, as was done in the vacuum filtration process, the surfactant remains on the surface. The presence of the surfactant on the surface makes any testing of the CNTs impossible.

Chapter V

Summary of Work and Conclusions

Summary

The objective of this work was to fabricate diamond films for use as substrates in carbon electronic devices and determine the behavior of nanocarbon electronic elements on the substrate, including their response to radiation exposure. The diamond films have been characterized both electronically and physically. They have been shown to have a number of favorable traits for use as an insulative substrate. The three most important properties these films need to exhibit to be viable candidates as insulative substrates for reception of nanocarbon material and subsequent radiation testing are: very little surface roughness, a stable C-V plot, and a high surface resistance. Their roughness and resistance have been shown to be on par with that of silicon dioxide, and they have exhibited stable C-V characteristics. These features strongly support the use of diamond films for characterizing the radiation response of carbon nanostructures. While very promising as substrates for radiation testing, these particular films would make for very poor insulators due to the large number of dielectric and interface traps. These traps would limit the mobility of the graphene or CNT channel. The low sheet resistance would allow for electron transport along pathways other than through the nano-carbon channel. This would be a concern when trying to characterize a carbon channel on its surface. The existence of such pathways obscures information about transport in the channel material, limiting its usefulness as a dielectric substrate. Efforts could be made to minimize these defects in the growth and annealing processes. Future films may prove to be better candidates for an insulative substrate. Attempts to transfer nano-carbon

elements, specifically CNTs, onto surfaces proved difficult and unsuccessful. Only small amounts of CNTs were transferred; not enough to reliably make usable devices. Adjustments to the process need to be refined so that a larger volume of CNTs are transferred to the diamond surface.

Future Work

Graphene on diamond transistors will be made by two different methods. Graphene will be wither grown using CVD methods, or exfoliated and transferred to the surface. The CNT transfer process will also be modified to increase the amount of transferred CNTs onto the diamond surface. This will be done by several means, including weakening the vacuum, decreasing filter size, and other related actions. Once the transistor devices have been fabricated, the nature of the carbon-diamond interface will be measured using a variety of techniques. The conductance and mobility will be determined using four point probe and Hall Effect measurements. Raman spectroscopy should provide insight into the presence of strain that the graphene or CNTs may have. C-V measurements can provide information about traps that may exist at the interface between the two carbon structures. The results derived from graphene on diamond will be compared to graphene transistors formed in the same way, but using oxide (SiO_2) as the substrate. Likewise, a similar set of fabrication and test experiments will be performed on CNT transistors on diamond substrates.

After the graphene on diamond devices have been characterized, they will be exposed to radiation in the form of x-rays, electrons, and protons. Diamond films without graphene will also be tested post dosage in order to determine if there is damage

to the underlying substrate. We may engage additional types of radiation (e.g., alpha particles, heavy ions) if we can gain access to the necessary sources.

By their very nature, polycrystalline diamond films contain a number of imperfections, specifically at the interfaces of the individual crystals, i.e., grain boundaries. Single crystal diamond, on the other hand, has a lower defect density. A single crystal may provide a more ideal surface and interface for these other forms of carbon to rest. In order to provide a best case scenario, procuring single crystal substrates is an option. After performing AFM on these samples to make sure they are smooth enough to serve as a substrate, graphene transistors may be created and tested as described above.

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