A GENERALIZED SINGLE-EVENT ANALYSIS AND HARDENING OPTIONS FOR MIXED-SIGNAL PHASE-LOCKED LOOP CIRCUITS

By

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Dissertation

Submitted to the Faculty of the

Graduate School of Vanderbilt University

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

December, 2009

Nashville, Tennessee

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DEDICATION

This dissertation is dedicated to my late grandmothers Beverly Loveless, who always knew I would grow up to be an engineer, and Katherine Landry, who always wanted a doctor in the family.

ACKNOWLEDGMENT

First and foremost, I would like to thank my wife Mary who has been more supportive than I could ever have hoped. Mary provides me with so much valuable input and I can't thank her enough. I would also like to thank the rest of my family for being there no matter what, for the sacrifices they have made to ensure I went to excellent schools, and for the guidance they have provided me over the years. Next, I would like to thank Dr. Lloyd Massengill for his continual support, confidence, and guidance throughout this project. Dr. Massengill has been a tremendous source of assistance and encouragement. More importantly, he has helped me identify and develop my talents, allowing for creativity in my research.

I would also like to thank Dr. Bharat Bhuva, whose words have been a source of patience and guidance. Additionally, I would like to thank Drs. Tim Holman, Robert Reed, and Mark Ellingham for serving on my committee. This process has been enjoyable because of them.

Special thanks are also deserved for Drs. Art Witulski, Younes Boulghassoul, Wole Amusan, Ron Schrimpf, and Dan Fleetwood, (soon to be Drs.) Megan Casey, Sarah Armstrong, Brian Olson, Matt Gadlage, and Jon Ahlbin. They have directly or indirectly provided valuable input to this work. I would also like to thank Dale McMorrow, Joe Melinger, Phil Jenkins, and Jeff Warner from the Navy Research Lab for the testing support, and Craig Hafer from Aeroflex Colorado Springs for the excellent collaboration. Recognition is also deserved for my friends in the Radiation Effects group.

Finally I would like to show appreciation to the Defense Threat Reduction Agency Rad-Hard Microelectronics Program for the financial support of this research.

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CHAPTER I

INTRODUCTION

A reliability concern of growing interest in the microelectronics community is the deleterious effect of ionizing radiation. The so-called "single events" – single particles which can penetrate semiconductor material leaving ionized charge in their wake – can cause information corruption and transient system failure. Single events are ubiquitous – this radiation exists in the environment external to a circuit, and emanates from processing and packaging material integral to a circuit. Once only the concern of space-bound systems where increased susceptibilities to SEEs have been reported as device feature sizes decrease and operating frequencies increase [Bu01, Do96], integrated circuit (IC) density and power scaling have propelled this issue to the forefront of reliability concerns at current technology nodes in ground-based and space-deployed electronic systems.

The increased susceptibility to single-event effects (SEE) in advanced Complementary Metal-Oxide Semiconductors (CMOS) can be attributed primarily to factors associated with device scaling trends [Jo98]. Early scaling theories through the 1970's and 1980's followed two basic approaches: constant-voltage scaling and constant-field scaling [Ba84, De74]. In recent years, however, the higher currents necessary for greater operating frequencies, in combination with the need for higher packing densities, require the semiconductor devices to have shorter channel lengths and widths with higher oxide breakdown fields [Hu93]. These scaling pressures are principally constrained by

the acceptable leakage currents when the transistors are "off," and many works have focused on more complicated scaling algorithms to counteract these scaling tradeoffs. Ultimately, the fast-paced scaling trends in CMOS technologies, consequently decreasing nodal capacitances [Ba84], results in increased single-event (SE) vulnerabilities by reducing the minimum amount of charge (i.e., critical charge) required to alter the state of a circuit node [Pe82].

Furthermore, as device feature sizes decrease, the nodal separation between devices in an IC also decreases. The decrease in nodal separation results in a phenomenon not previously encountered in pre-nanometer technologies; that is, higher package densities result in increased probabilities of multiple devices collecting charge from a single ion strike (i.e., charge sharing). This phenomenon has recently been characterized in 130 nm technologies [Am06, Am07] and will no doubt be a primary concern for future CMOS electronics as the drive for faster speeds and higher packing densities continues.

An SE occurs when a high-energy ionizing particle, such as a heavy ion, strikes the circuit. As the particle penetrates the semiconductor material it loses energy through Coulombic interactions with the lattice structure and leaves a dense track of electron-hole pairs in the material. These excess carriers can be collected as charge on circuit nodes, resulting in undesirable circuit responses which can vary depending on the circuit topology and the amount of charge collected [Do03, Ma93]. In mixed-signal (analog and digital) systems, the effect of an SE particle strike is the generation of a transient signal (single-event transient or SET) that competes with the legitimate signals propagating through a circuit or perturbs the functionality of the circuit. In digital circuits, an SET can result in a single-event upset (SEU), that is, an alteration of the state of memory

circuits (e.g., a memory cell can be changed from a logic “0” state to a logic “1” state). The SEU can lead to a circuit error if the corrupted data propagates throughout the circuit and is observable at the output. These upsets are often termed “soft errors” as they do not result in permanent failures within the circuit. However, there exists no standard metric for soft errors in analog and mixed-signal circuits, as the effect of an SE is dependent on the circuit topology, type of circuit, and the operating mode.

Since first reported through heavy-ion induced experiments [Ko93], SET effects in analog microelectronics have been examined through a variety of experimental procedures [Bu87, Ec94, Mc03, Pe02, Po99, Sa02, Sa03] and computer simulation techniques [Ad00, Bo04a, Jo00b, Pe01, St02b]. Furthermore, the combination of experimental testing and simulation efforts has enabled an understanding of analog SEE that experimental testing alone did not provide [Bo04b].

In recent years, there is a particular interest in the effect of SETs on the phase-locked loop (PLL) because of the propensity to cause a loss of frequency integrity, and the resultant wide-spread impact on high-performance systems [Bo05, Bo06, Ch06b, Ch06a, Ha05a, Ha05b, Jo96a, Lo06, Lo07a, Lo08, Lo09, Lo07b, Lo07c]. In fact, voltage-controlled oscillators (VCO) - integral components of PLL circuits - have been reported to have increased susceptibilities to SEE in advanced technology nodes [Bo05]. Additionally, as PLLs (sometimes termed bit synchronization circuits, or clock-recovery circuits) are widely used in commercial and space-deployed electronics systems to reduce the phase delay associated with the distribution of clock signals, to generate high-speed clock signals, and to synchronize data transfer [Ba08, Be98], there is a growing interest on the impacts SETs in the PLL can have on circuit designs that utilize PLLs for clock

signals [SEE04]. Furthermore, recent works have not only identified the most sensitive PLL sub-circuit to SEs [Bo06], but have designed and verified radiation-hardened-by-design (RHBD) alternatives that reduce the effects of SEs in the PLL by orders of magnitude over conventional designs [Lo06, Lo07a, Lo07b, Mc07]. These results indicate that RHBD is effective for high-speed mixed-signal circuits using unconventional analog design techniques and targeted SE circuit simulations.

This dissertation applies circuit-level simulations and experimental testing to characterize the effects of SEs on a general PLL topology. The simulations and experimental procedures target the PLL sub-circuits so that individual contributions to the overall PLL SE vulnerability are distinguished and analyzed. RHBD alternatives to each sub-circuit are offered if necessary. Additionally, novel analyses are presented that can effectively predict the relative contributions of SET generation within the PLL. Furthermore, the analyses are utilized to develop a generalized model for single transient propagation through the PLL.

Although this work primarily discusses PLLs in the context of on-chip clock generation and skew reduction in the presence of single ionizing particles, it is the goal of this work to present a generalized model for single transient propagation through PLL topologies for a variety of applications and environments. The transient model is formulated from a conventional linear PLL model commonly used in a variety of noise analyses [Ha04, He04, Kr82, Me02]. However, the model is unique in that the resulting fundamental design equations are derived in closed-form under the assumption that transients are a result of single transient impulses applied to the various sub-circuits rather than continuous nondeterministic sources. This approach vastly simplifies the

analysis and provides insight into the closed-loop parameters that directly influence the generation and propagation of transients through the PLL. As a result, a list of design guidelines is developed that can be applied to all PLL topologies. The set of principles may be applied for 'analytical transient mitigation' to reduce the sensitivity of PLLs to single transients resulting from extrinsic noise sources such as single-event radiation and crosstalk noise.

Organization of Dissertation

The research effort presented in this dissertation is organized as follows:

1) Chapter I introduces the motivation for this work.
2) Chapter II provides a detailed background on phase-locked loop circuits, including a control-systems analysis and derivations of important electrical parameters and characteristics. Also discussed are the detailed topologies of each PLL sub-circuit and any critical design equations.
3) Chapter III provides a background on SEEs, especially those of particular pertinence to this work. An introduction to the space radiation environment is included along with a discussion of the various radiation effects including total-ionizing dose, displacement damage, and SEEs. However, the section primarily focuses on SEEs. Finally, charge generation and collection mechanisms for SEEs are discussed.
4) Chapter IV focuses on two common methods employed in this work for modeling SETs in circuit simulators. Also, some examples of various SETs observed in analog and digital circuits are presented.

5) Chapter V details SETs generated within unity gain PLL circuits specifically. Simulation and laser two-photon absorption experimental results will be presented for the phase-frequency detector, voltage-controlled oscillator, and charge pump sub-circuits.
6) Chapters VI and VII discuss SETs in the voltage-controlled oscillator sub-circuit exclusively. Various models, simulations, and novel analysis techniques are presented for the SET characterization of mixed-signal topologies. Additionally, numerous hardening options for the VCO are presented.
7) Chapter VIII provides an analysis of SETs in frequency divider topologies. Further, the various impacts of the divider configuration on SETs generated internal and external to programmable PLL topologies is discussed.
8) Chapter IX presents a systems-oriented analysis of SET generation and propagation in PLLs. Specifically, the closed-loop parameters that have a direct impact on SET generation are identified. Additionally, a novel design/analysis parameter, the 'PLL critical time constant', is presented to facilitate the design of PLL circuits in extrinsically noisy environments. A general list of design guidelines for the analytical mitigation of single transients in PLL circuits is provided.
9) Chapter X will provide some concluding remarks regarding the presented research.

CHAPTER II

PHASE-LOCKED LOOPS

Introduction

For a basic understanding of phase-locked loops (PLL), this chapter provides a background on PLL topologies and develops a set of linear models for PLL feedback systems, including the fundamental design equations for PLL development. A derivation of the closed-loop transient response and fundamental tracking properties is also provided as necessary for the subsequent chapters. Although PLL systems are highly non-linear in practice it is useful to approximate PLLs as linear negative feedback networks for a fundamental understanding of their functionality. The chapter will conclude by presenting the various PLL building blocks examined throughout this work, including the phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator, and frequency divider.

Basic PLL Topology

The general idea behind a PLL is to create a stable output signal that is synchronized to an input reference signal. The input reference signal, for example, may be a digital clock signal or data received from a transmission network. Therefore, in steady-state, the output phase of the PLL should be "in lock" with the phase of the input signal; that is, the difference between the input and output phases (Φ_{outVCO} - Φ_{ref}) should not be changing

over time. The basic architecture of a PLL is shown in Fig. II-1 and consists of a phase detector (PD), low-pass filter (LPF), and voltage-controlled oscillator (VCO).

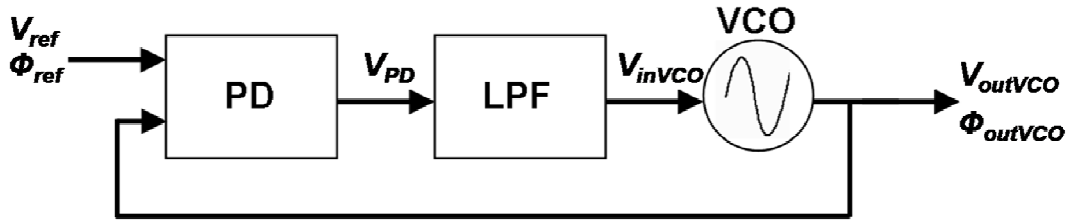


Fig. II-1. Diagram of a basic PLL consisting of a phase detector (PD), low-pass filter (LPF), and voltage-controlled oscillator (VCO).

The PD compares the phase of the output signal (V_{outVCO}) to the phase of the reference signal (V_{ref}), generating an error signal (V_{PD}) describing the phase difference (Φ_{outVCO} - Φ_{ref}) between V_{outVCO} and V_{ref}. Ideally the error signal consists only of a DC component for the control of the VCO; however undesirable high-frequency noise is typically coupled onto the node and must be filtered through a LPF. The resulting control voltage (V_{inVCO}) is then fed to the VCO to set the oscillating frequency.

As the PLL compares the phases of the input/output signals it requires no knowledge of the voltages or currents on the input/output nodes. Therefore, for sufficient phase gain (Φ_{outVCO} / Φ_{ref}), the phase difference between the two signals is expected to be small in steady state, denoting phase alignment (phase lock). Thus, in steady state Φ_{outVCO} - Φ_{ref} should be constant and close to zero. From this property, the loop is said to be in lock if Φ_{outVCO} - Φ_{ref} does not change with time, thus following Eqn. (II-1). As frequency is the derivative of phase with respect to time, Eqn. (II-2) also holds true for

PLLs in the lock state. Thus, for the PLL shown in Fig. II-1, the output frequency is equivalent to the input frequency while in phase lock (unity gain) [Ra01].

$$\frac{\partial \phi_{outVCO}}{\partial t} - \frac{\partial \phi_{ref}}{\partial t} = 0 \tag{II-1}$$

$$\omega_{outVCO} = \omega_{ref} \tag{II-2}$$

While a unity gain PLL that produces an output signal that is in phase with an input signal of equivalent frequency is not terribly practical, the basic topology may be developed for a variety of applications. For example, large ICs require a clock distribution network such that single or multiple clocks are required to drive thousands of transistors in multiple locations throughout the IC. Driving an entire IC with a single clock may result in clock skew and decrease the performance. Therefore a PLL may be designed to include high current drive buffers internal to the loop such that the high current drive output signal of the PLL is in phase lock with the reference clock, as seen in Fig. II-2. This technique may also be used to regenerate a full swing clock signal with large drive strength from an attenuated reference signal.

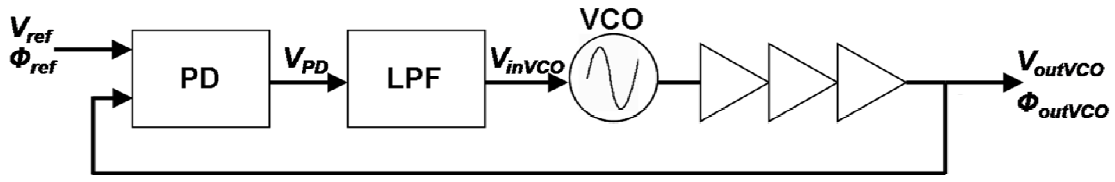


Fig. II-2. Diagram of a PLL for reducing the clock skew associated with clock distribution. Buffers are included internal to the closed-loop.

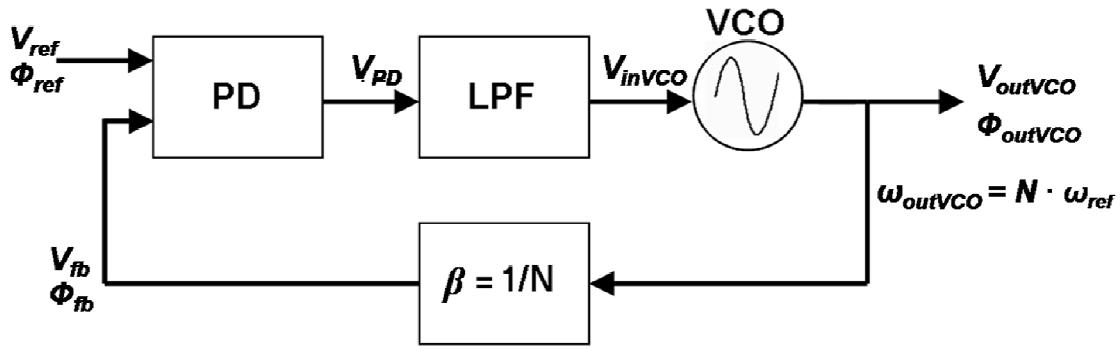


Fig. II-3. Diagram of a PLL for high-frequency clock generation.

Many applications, such as frequency synthesis and high-frequency clock generation, require the signal generated by the PLL to have a different frequency than the reference signal. High-frequency clock generation, for example, may be achieved by designing a high-frequency VCO and including a frequency divider in the loop feedback network. In this case, the output phase of the frequency divider (Φ_{fb}) is compared to phase of a low-frequency reference signal (Φ_{ref}), as shown in Fig. II-3. Thus, the output frequency of the PLL is a multiple of the input frequency and is related to the input frequency by Eqn. (II-3). Rather than creating a high-frequency clock off-chip and supplying the signal to the IC, this technique allows for high frequency clock generation on-chip, thus reducing the clock skew associated with the input capacitance. Frequency divider circuits may also be placed in additional locations internal and external to the closed-loop for a variety of frequency synthesis applications in order to generate signals at multiple frequency levels [Ba08, Be98, Le04a, Ra01].

$$\omega_{out} = N\omega_{ref} = \frac{\omega_{ref}}{\beta} \tag{II-3}$$

Although many applications for PLL circuits exist, this section shows three basic configurations commonly referred to throughout this dissertation. The following section discusses the linearized models used for the design of the PLLs discussed throughout this work.

A Linear PLL Model

The basic linear model of the PLL is shown in Fig. II-4, where K_{PD} is the gain of the phase detector (PD), $F(s)$ is the LPF transfer function (integrator), K_{VCO} is the gain of the VCO, and β is the feedback factor (adapted from [Be98]). K_{PD} has units of volts/radian or amps/radian (dependent on the type of PD) and K_{VCO} has units of radians/(second·volt). Since the PLL compares the phases of the output and reference signals rather than the frequencies, the integral of the VCO stage must be used in order to obtain the phase. As the Laplace transform of a constant C is C/s, the gain of the VCO stage is K_{VCO}/s, and thus adds a pole to the loop.

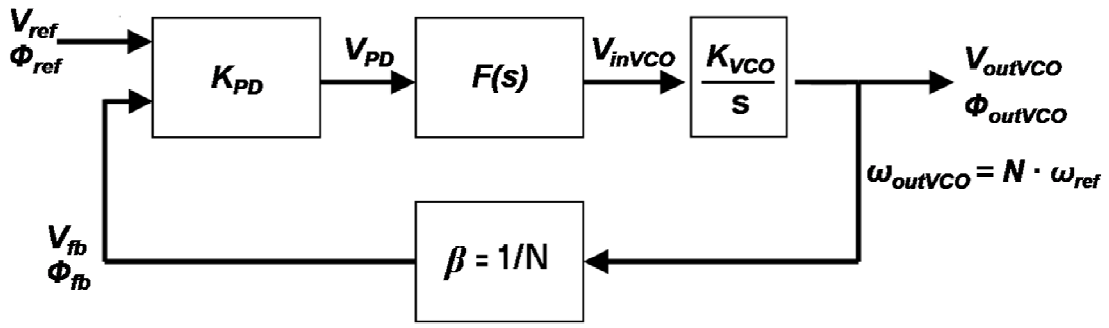


Fig. II-4. Linear model for a PLL (adapted from [Be98]).

Open and Closed Loop Analyses

The linear model displayed in Fig. II-4 is the fundamental building block for a wide variety of PLL analyses; consequently, the open-loop transfer function is given by Eqn. (II-4).

$$G(s) = \frac{\phi_{out}}{\phi_{ref}}(s)\bigg|_{open} = K_{PD}F(s)\frac{K_{VCO}}{s} \tag{II-4}$$

The closed-loop transfer function (*H(s)*) may be readily obtained from Eqn. (II-4) through a standard control-systems analysis and is shown by Eqn. (II-5).

$$H(s) = \frac{G(s)}{1+\beta G(s)} = \frac{K_{PD}F(s)\dfrac{K_{VCO}}{s}}{1+\beta \cdot K_{PD}F(s)\dfrac{K_{VCO}}{s}} = \frac{K_{PD}F(s)K_{VCO}}{s+\beta \cdot K_{PD}F(s)K_{VCO}} \tag{II-5}$$

$$F(s) = \left(R_P + {}^{1}\!\!\diagup\!\!{}_{C_1 s}\right) = \frac{1+sR_PC_1}{sC_1} \tag{II-6}$$

Assuming the loop filter consists of at least one pole and is of the form shown by Eqn. (II-6), the PLL is minimally a second order closed-loop system and therefore has a natural frequency (ω_n) and damping ratio (ζ). Accordingly, the closed-loop transfer function can be expressed as Eqn. (II-7), such that the denominator is in the format $s^2 + 2s\zeta\omega_n + \omega_n^2$.

$$H(s) = \frac{K_{PD}K_{VCO}\left(1 + sR_pC_1\right)}{s^2 + s\left(K_{PD}K_{VCO}\beta\right) + \frac{K_{PD}K_{VCO}\beta}{C_1}} \tag{II-7}$$

The 2nd order transfer equation indicates that the PLL system can be overdamped ($\zeta > 1$), underdamped ($\zeta < 1$), or critically damped ($\zeta = 1$), where ζ is the damping ratio. Some works commonly refer to the Q factor rather than the damping ratio, where $Q = 1/(2\zeta)$. Accordingly, the natural frequency (ω_n) and the damping ratio (ζ) may be determined by Eqns. (II-8) and (II-9), respectively. The natural frequency is a measure of the response time of the loop, whereas the damping ratio measures the loop ringing and overshoot. Conventional guidelines suggest that the natural frequency should be designed to be as large as possible in order to minimize the loop response time [Ba08]. Furthermore, to obtain a maximally flat magnitude in the pass band, ζ should be designed to equal $1/\sqrt{2}$. In order to avoid excessive ringing ζ is typically designed to be approximately equal to 1.

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}\beta}{C_1}} \tag{II-8}$$

$$\zeta = \frac{\omega_n}{2} R_P C_1 \tag{II-9}$$

The closed-loop PLL system as described by Eqn. (II-7) has two poles given by Eqn. (II-10). Thus, if $\zeta > 1$, both poles are real and the system is overdamped. On the other hand, both poles are complex and the system is underdamped for $\zeta < 1$. Furthermore, if $\zeta = 1$, both poles are equal to $-\omega_n$ and the system is critically damped.

$$s_{1,2} = -\zeta\omega_n \pm \sqrt{(\zeta^2 - 1)\omega_n^2} = \omega_n\left(-\zeta \pm \sqrt{\zeta^2 - 1}\right) \quad \text{(II-10)}$$

The loop equations predict that if the input frequency changes slowly ($s \rightarrow 0$) the output will track the input, as expected. Also, if the input frequency changes abruptly and given enough time to settle ($s \rightarrow 0$), then the change in the output frequency is equal to that of the input frequency divided by the feedback factor. However, as the PLL system consists of multiple poles, the damping ratio suggests that given a unit step change in the input frequency, the output will take some time to track the input and settle. The initial tracking time (t_{acq}) and settling time (t_s) is of particular importance for most PLL applications. Overdamped systems ($\zeta > 1$), for example, will take longer to track the input frequency shift over a critically damped system ($\zeta = 1$). For underdamped systems ($\zeta < 1$), the output frequency can be expected to overshoot the input frequency and take some time, t_s, to settle.

Let f_0 be the initial frequency at the output of the VCO and let $f_{lock} = N{\cdot}f_{ref}$ be the desired lock frequency such that $\Delta f = \Delta\omega/2\pi$ is the frequency shift required at the output to obtain lock. As previously mentioned, the damping ratio of the closed-loop indicates that there are three possible cases that determine the acquisition properties of the PLL ($\zeta < 1$, $\zeta = 1$, or $\zeta > 1$), however only two of the three cases will be considered.

1. $\zeta < 1$ - the system is underdamped: The output frequency of the PLL will overshoot f_{lock} by a frequency $f_{overshoot}$ [Ba06]. Fig. II-5 illustrates an underdamped response of a PLL to a unit step frequency change on the input. The output frequency overshoots the input frequency and rings at the natural frequency, ω_n. Following, the output frequency will decay exponentially

towards f_{lock} with a time constant of $\zeta\omega_n$ [Ba06, Ra01]. For this case, the required frequency shift at the output is $\Delta f^* = \Delta f + f_{overshoot}$ during the tracking time, t_{acq}. Then, the system will require some time, t_s, to settle about f_{lock}. The total time to phase-lock is given as $t_{lock} = t_{acq} + t_s$. The settling time is derived in [Ba06].

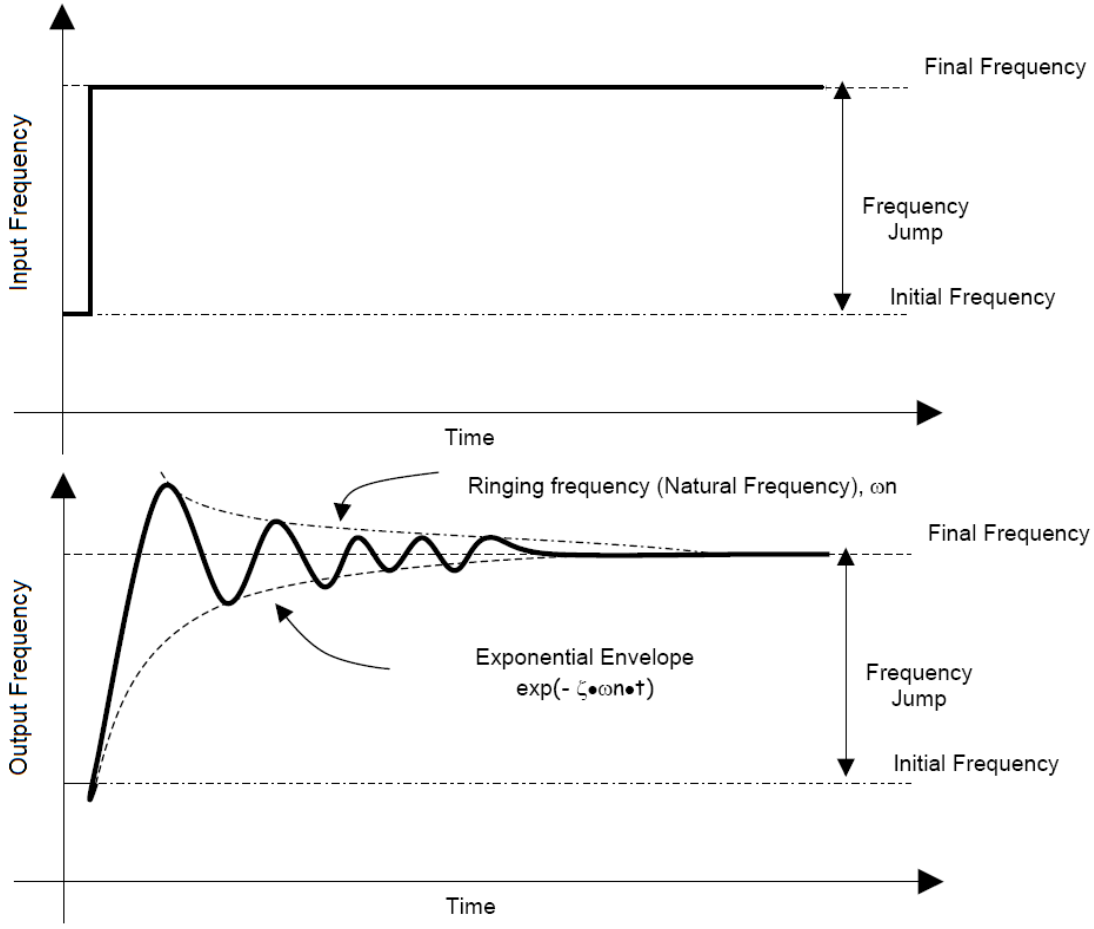


Fig. II-5. Underdamped response of a PLL to a unit frequency step at the input (adapted from [Ra01] and [Ba06]).

2. $\zeta = 1$ or $\zeta > 1$ - the system is critically damped or overdamped, respectively: Theoretically, the output frequency of the PLL will track the input frequency without any frequency overshoot. Thus the total time to lock is given as $t_{lock} = t_{acq}$ for a frequency shift of $\Delta f^* = \Delta f$. For increasing $\zeta > 1$, however, the time to pull-in phase lock grows rapidly and it may become increasingly difficult to obtain and maintain lock. As it is many times impractical to design for $\zeta >> 1$, it is therefore assumed for the remainder of this work that ζ is close to 1.

Moreover, it can be shown that for minimum settling time, $\zeta\omega_n$ must be maximized. For this type of PLL, Eqns. (II-8) and (II-9) yield a critical trade-off between settling speed and ripple on the VCO control line, given by Eqn. (II-11) where ω_{LPF} is the -3 dB frequency of the loop filter [Ra01]. That is, the lower ω_{LPF}, the greater the PD high-frequency noise suppression but the longer the settling time. This point is especially important when considering the SE performance, as discussed in later chapters.

$$\zeta\omega_n = \frac{1}{2}\omega_{LPF} \tag{II-11}$$

Linear VCO Model

In order to develop a suitable first-order model of the PLL transient response, the approximation of the VCO functionality is critical. The gain, K_{VCO}, is a linear estimate of the VCO transfer function. However, in practice the VCO is a highly non-linear sub-circuit. Fig. II-6 illustrates the transfer function of a VCO designed using the IBM 90 nm CMOS9SF (9SF) process-design-kit (PDK) and indicates the linear range of operation.

The gain, K_{VCO}, is determined by finding the slope during the linear range. Also displayed in Fig. II-6 is the linear approximation of the VCO transfer characteristics, as determined by Eqn. (II-12). Eqn. (II-2) may be used in the time domain to monitor loop changes for $f_{outVCO}(V_{inVCO})$ in the range of **F**, where **F** $\in$ [f_{min} f_{max}]. In order for this approximation to hold true the output frequency at V_{inVCO} of 0 V (f_0) must be estimated as the y-intercept in Fig. II-6.

$$f_{outVCO}(V_{inVCO}) = \frac{K_{VCO}V_{inVCO}}{2\pi} + f_0 \qquad \text{(II-12)}$$

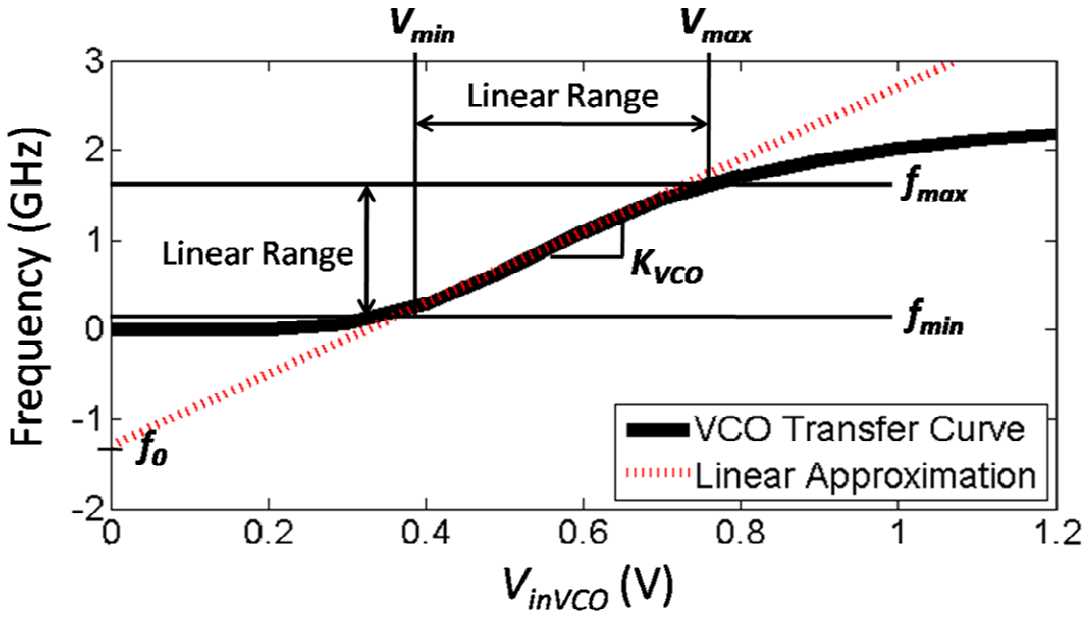


Fig. II-6. Illustration of the linear approximation for the VCO transfer curve.

PLL Locking Characteristics

The analysis in the previous section shows that an input frequency step response will cause the PLL to begin tracking the output signal. Furthermore, it will take some amount

of time for the frequencies to be equivalent, and an additional amount of time to settle such that the phase of the output signal is in lock with the phase of the input signal. As the output frequency of the PLL is equal to the input frequency divided by the feedback factor (a constant) when in phase lock, it is useful to think of the phase transfer function in terms of output frequency rather than phase. Also, since a change in output frequency must be accompanied by a change in the VCO control voltage, the relationship shown in Eqn. (II-13) may be derived. Thus, the response of the closed-loop system can be obtained by monitoring the variations in the VCO control voltage, V_{inVCO} [Ra01].

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) \propto \frac{\omega_{out}}{\omega_{in}}(s) = \frac{V_{inVCO} K_{VCO}}{\omega_{in}}(s) \qquad \text{(II-13)}$$

Fig. II-7 illustrates a simulation of the VCO control voltage versus time from PLL start-up to steady-state, and is called the acquisition and lock curve. The basic topology of the PLL simulated is shown in Fig. II-2. The PLL was designed using the IBM 130 nm CMRF8RF (8RF) PDK for a center frequency of operation of 400 MHz, a minimum frequency of 150 MHz, a maximum frequency of approximately 1 GHz, and a power supply of 1.2 V [Lo06, Lo07a]. First, the acquisition curve illustrates the tracking (frequency acquisition) period where the output frequency of the PLL is less than the input frequency and is increasing versus time, as shown by zoom area 1 and Fig. II-8 [Lo07a]. Phase lock is represented by the period when V_{inVCO} is constant versus time, denoting a phase error close to zero and $\omega_{out} = \omega_{in}$, as shown by zoom area 2 and Fig. II-9 [Lo07a].

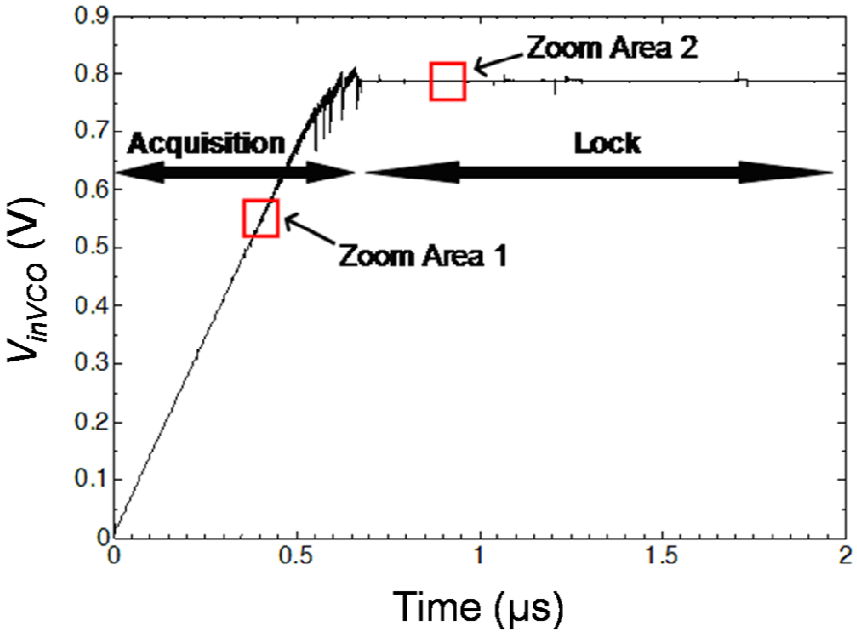


Fig. II-7. Acquisition and lock curve: V_{inVCO} versus time at 700 MHz operation. The reference and output signals represented by the highlighted boxes (*Zoom Area 1* and *Zoom Area 2*) are displayed in Fig. II-8 and Fig. II-9 [Lo07a].

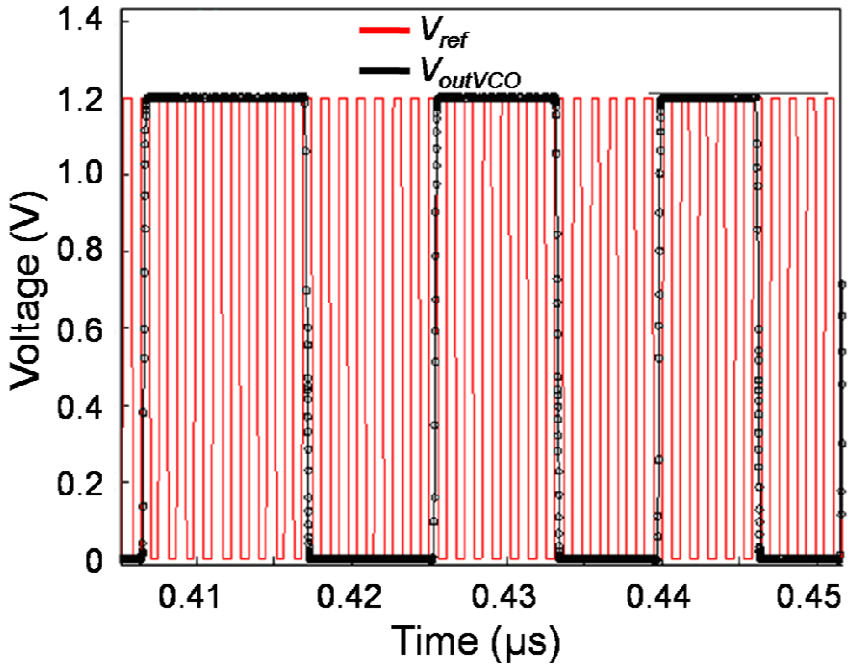


Fig. II-8. V_{ref} and V_{outVCO} during the acquisition period, as indicated by *Zoom Area 1* in Fig. II-7 [Lo07a].

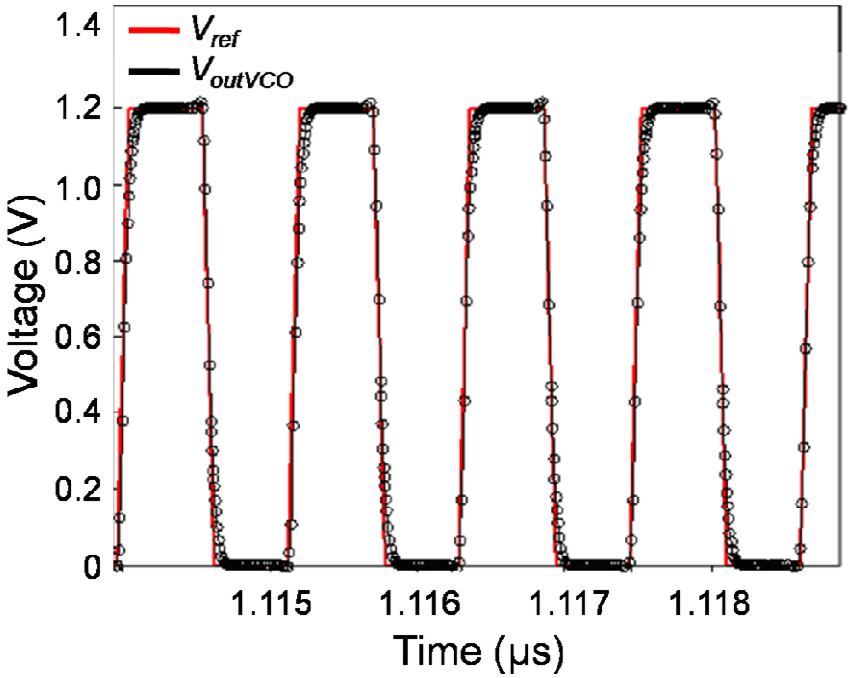


Fig. II-9. V_{ref} and V_{outVCO} during the lock period, as indicated by *Zoom Area 2* in Fig. II-7 [Lo07a].

PLL Lock Time Estimator

The importance of an accurate first-order model for the PLL acquisition is crucial for the error propagation model presented in Chapter IX. This sub-section is devoted to deriving an estimate of t_{acq} based on the fundamental linear PLL model.

Many works have examined the tracking and settling characteristics of PLLs and a wide range of estimators for a PLL lock time (acquisition and/or settling) have been provided for various PLL types [Ba06, Ba08, Ga79, Ga05]. This work defines a PLL lock time as the time required by a PLL to track the reference frequency from start-up and settle into a stable phase-locked state. An estimator for the PLL lock time is provided in subsequent sections under the following conditions:

- the reference frequency undergoes a unit step frequency shift of $\Delta\omega_{in}$ requiring an output frequency shift of $\Delta\omega = N\Delta\omega_{in}$
- $\Delta\omega$ is assumed to be much greater than ω_n, $\Delta\omega >> \omega_n$
- the final output frequency in phase lock, ω_{lock}, is within the VCO linear operating range ($\omega_{lock} \in 2\pi \cdot \mathbf{F}$)

The natural frequency of the PLL is a useful performance metric because it provides a measure for the response time of the loop (i.e., the time it takes for a signal to propagate through the loop, or the time it takes the PLL to respond to a change at the input). The loop response time is given as Eqn. (II-14).

$$t_{loop} = \frac{2\pi}{\omega_n} \tag{II-14}$$

Assuming that when activated, the PD sub-circuit sources/sinks a constant current (I_{CP}) to the loop filter's capacitance (C_1), Eqn. (II-15) describes the amount of voltage shift (V_{loop}) at the VCO input during time t_{loop}. Note that the mechanism for the current source/sink by the PD is discussed in subsequent sections. Derivations may be followed by assuming $K_{PD} = I_{CP}/2\pi$.

$$V_{loop} = \frac{I_{CP} t_{loop}}{C_1} = \frac{2\pi I_{CP}}{C_1 \omega_n} = \frac{4\pi^2 \omega_n}{\beta K_{VCO}} \tag{II-15}$$

It follows that the slope of the acquisition curve (V_{inVCO} versus time), as illustrated in Fig. II-10, is given by Eqn. (II-16). This result is consistent with that shown in [Ra01].

$$m = \frac{V_{loop}}{t_{loop}} = \frac{2\pi\omega_n^{\,2}}{\beta K_{VCO}} = \frac{I_{CP}}{C_1} \tag{II-16}$$

This result indicates that for high-gain PLL circuits where $\Delta\omega >> \omega_n$, the acquisition time will be determined by the PD current, loop filter capacitance, and the required output frequency shift.

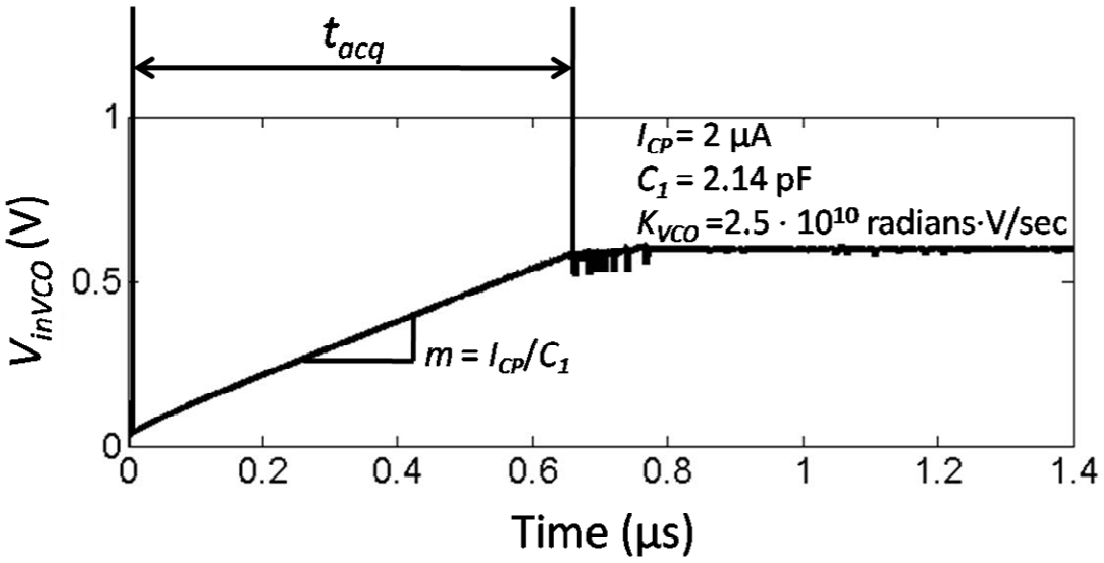


Fig. II-10. Simulated acquisition curve (V_{inVCO} versus time) for PLL designed using the IBM 9SF PDK at a center frequency of 1.1 GHz. Calculated acquisition time is 607 ns, whereas the simulated acquisition time is approximately 650 ns (ignoring the final settling time).

Utilizing Eqn. (II-12) describing the VCO transfer characteristics, the voltage shift required at the VCO input (ΔV_{inVCO}) is given as Eqn. (II-17), where V_{lock} is the voltage at ω_{lock}, V_0 is the voltage at ω_0, and $\Delta\omega^*$ is the required frequency shift as previously discussed. The acquisition time (t_{acq}) is thus given as Eqn. (II-18).

$$\Delta V_{inVCO} = V_{lock} - V_0 = \frac{\omega_{lock} - \omega_0}{K_{VCO}} = \frac{\Delta\omega^*}{K_{VCO}} \tag{II-17}$$

$$t_{acq} = m^{-1} \cdot \Delta V_{inVCO} = \frac{C_1}{I_{CP}} \frac{\Delta\omega^*}{K_{VCO}} = \frac{\Delta\omega^* \beta}{2\pi\omega_n{}^2} \tag{II-18}$$

Therefore to the first-order, the acquisition time increases linearly with increasing frequency steps and decreases as a quadratic with increasing natural frequency. Furthermore, the result shows that the acquisition time is independent of β as changes in β result in proportional changes in $\omega_n{}^2$ (Eqn. (II-8)). Also note that the initial acquisition time is independent of the damping ratio, which primarily affects the final settling characteristics. Phase acquisition will be a non-linear process for small $\Delta\omega$ as determined by the closed-loop damping response discussed in the previous section.

Fig. II-10 illustrates the simulated acquisition curve for a PLL designed using the IBM 9SF PDK for a center frequency (frequency at which V_{inVCO} is $V_{dd}/2$) of 1.1 GHz (VCO transfer curve shown in Fig. II-6). The design parameters I_{CP}, C_1, and K_{VCO} are provided in the figure. The simulation is for an output frequency of 1.1 GHz and V_{inVCO} initialized to 0 V. The acquisition time as calculated by Eqn. (II-18) is 607 ns, which is within approximately 7% of the simulated acquisition time of 650 ns (ignoring settling time). Note that the frequency step, $\Delta\omega^*$, used for the calculation requires the initial frequency (f_0) as given by the linear VCO approximation in Eqn. (II-12) and not the actual VCO transfer curve.

Additional approaches have been developed for estimating the lock time that may result in a wide range of predictions under various assumptions. Banerjee has provided a

first order approximation that is useful in estimating the lock time, t_{lock}, time to peak frequency, t_{peak}, and the amount of frequency overshoot, $f_{overshoot}$. The approximations depend only on the damping ratio, natural frequency, and the amount of the input frequency step [Ba06]. A variable, *tol*, in units of Hz is also included to represent the settling tolerance of the output frequency. As $tol \rightarrow 0$, the estimated lock time will approach infinity, thus an appropriate frequency tolerance based on the nominal phase error and control voltage variation during the lock state must be chosen. Eqns. (II-19), (II-20), and (II-21) represent the approximations for t_{lock}, t_{peak}, and $f_{overshoot}$, respectively [Ba06]. As expected, t_{lock} and t_{peak} may be minimized by designing the natural frequency to be as high as possible. Also consistent with the results in previous sections, $f_{overshoot}$ depends strongly on the damping ratio.

$$t_{lock} = \frac{-ln\left(\frac{tol}{f_{final} - f_{initial}} \cdot \sqrt{1-\zeta^2}\right)}{\zeta \cdot \omega_n} \tag{II-19}$$

$$t_{peak} = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}} \tag{II-20}$$

$$f_{overshoot} = \frac{f_{final} - f_{initial}}{\sqrt{1-\zeta^2}} \cdot e^{\frac{-\zeta \cdot \pi}{\sqrt{1-\zeta^2}}} \tag{II-21}$$

Although Eqns. (II-19), (II-20), and (II-21) provide a quick estimate they are not valid for $\zeta \geq 1$, that is, for critically damped or overdamped PLL systems. Also, many factors

can degrade the locking performance of the PLL such as nonlinearity in the VCO, discrete sampling effects in the PD, input/output capacitances, and current mismatches [Ba06]. These factors may cause the simulated and tested parameters to deviate from the estimated parameters significantly; therefore extreme caution should be used when utilizing locking performance estimators. The estimations may be useful, however, in determining trends in the performance variation over various design parameters.

Generally, the PLL lock time is defined as the time it takes to for the PLL to move from one frequency to another specified frequency within a given frequency tolerance [Fo02]. However, Baker refers to this definition as the pull-in time, and the lock time is defined as the amount of time it takes the PLL to obtain phase lock within one single beat note [Ba06]. Baker also provides an approximation of the classical definition of lock time, similar to that described by Banerjee [Ba06] for various phase detector implementations. Baker's definitions are referred to as the pull-in time rather than lock time. In order to avoid confusion, this paper uses the classical definition of lock time provided in [Fo02].

Charge Pump PLLs

Although many PLL topologies have been developed utilizing various phase detectors for a variety of applications, perhaps the most common topology is the charge pump (CP) PLL shown in Fig. II-11. The CP PLL considered in this work is a negative feedback closed-loop system consisting of five primary components: the phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), and a divide-by-N frequency divider (β). The PD sub-circuit shown in the previous sections

can be segmented into two components: the PFD and the CP. Additionally, "*e*-graded" buffers are included subsequent to the VCO module to account for loading effects and to reduce the clock skew. On start-up the PFD compares the phase and frequency of the input reference signal (V_{ref}) and the feedback signal (V_{FB}). When V_{FB} is lagging (leading) V_{ref} in phase and frequency, an output pulse will be generated on the UP (DOWN) output of the PFD. This leads the CP module to source (sink) charge to (from) the LPF, thus changing the VCO control voltage (V_{inVCO}) and adjusting the output frequency of the VCO. The following sections will discuss the design of each individual component.

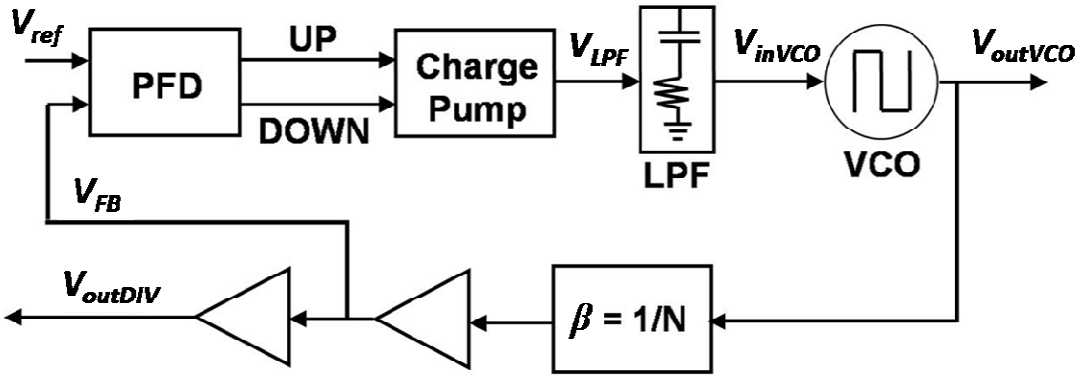


Fig. II-11. Block diagram of the charge pump PLL including the phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), and frequency divider (β). Additionally, "e-graded" buffers are included in order to account for loading effects.

The Phase-Frequency Detector

A simplified implementation of the phase-frequency detector (PFD) used in this work is shown in Fig. II-12 in order to facilitate the discussion of the circuit operation [Ba08]. Rather than depending only on the phase difference between the inputs, the PFD measures differences between the phase and frequency of the two inputs, V_{ref} and $V_{FB.}$

The actual PFD used in this work is an all CMOS variant of the PFD and is displayed in Fig. II-13. The circuits displayed in Figs. II-12 and II-13 are functionally equivalent.

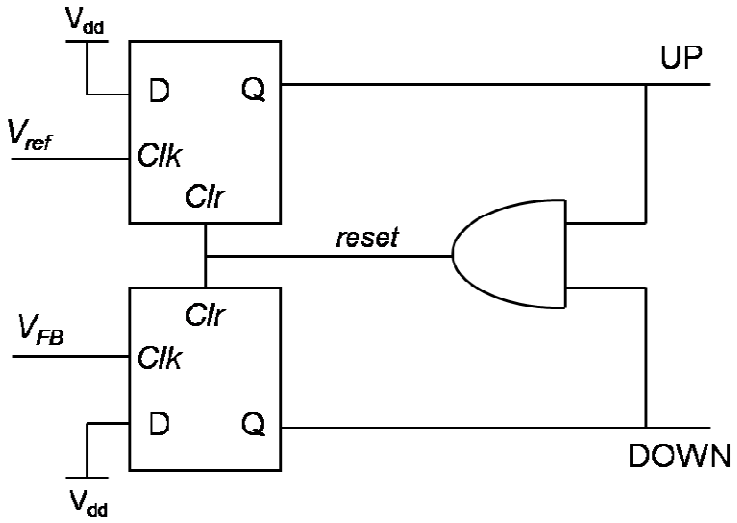


Fig. II-12. Simplified block diagram of the phase-frequency detector [Ba08].

In contrast to a phase detector, the PFD cannot lock onto a harmonic frequency (that is, a multiple of the input frequency), as it compares the phase and frequency of V_{ref} and V_{FB}. It achieves this by requiring the rising edge of both V_{ref} and V_{FB} to be present for a phase comparison. Three states can be considered for the PFD and are graphically illustrated in Fig. II-14, respectively.

1) The rising edge of V_{FB} is lagging the rising edge of V_{ref} (Fig. II-14 (a)):

The rising edge of V_{ref} causes the UP signal to transition to a logic high value. Upon the arrival of the rising edge of V_{FB}, the DOWN signal will momentarily go high, causing the *reset* line to go high, thus resetting the latches and causing both the UP and DOWN signals to return to a logic low state. The UP signal therefore represents the phase difference between the rising edges of V_{ref} and

V_{FB}, and indicates that the VCO output frequency should be increased in order to decrease the phase difference. Care should be taken to minimize the momentary spike on the DOWN line, so as both the UP and DOWN lines are not simultaneously in the logic high state for a significant amount of time.

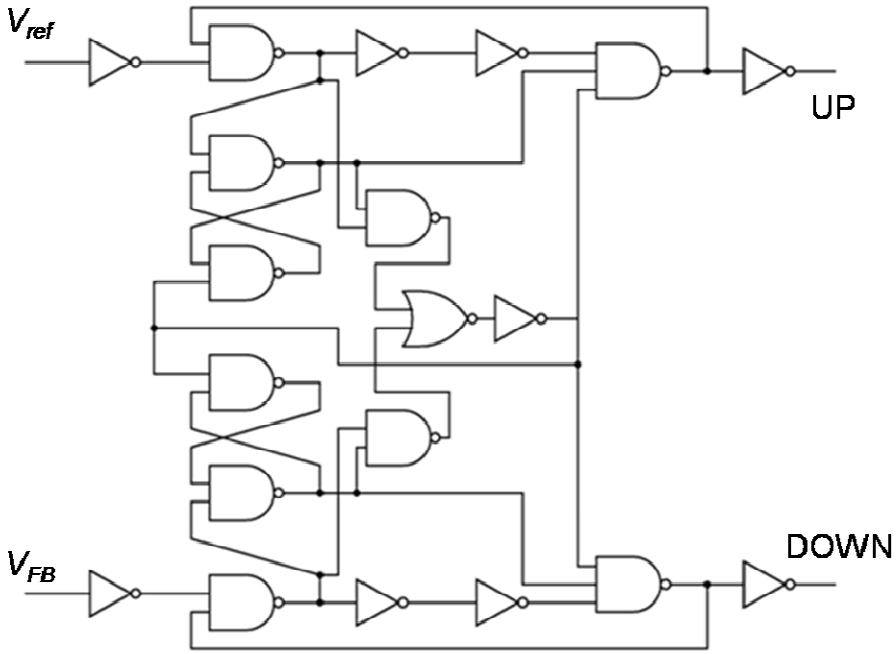


Fig. II-13. CMOS implementation of the phase-frequency detector used in this work [Ba08].

2) The rising edge of V_{FB} (V_{outVCO}) is leading the rising edge of V_{ref} (Fig. II-14 (b)):

Similar to the first state, the rising edge of V_{FB} causes the DOWN signal to transition to a logic high value. Upon the arrival of the rising edge of V_{ref}, the UP signal will momentarily go high, causing the *reset* line to go high, thus resetting the latches and causing both the UP and DOWN signals to return to a logic low state. The DOWN signal therefore represents the phase difference

between the rising edges of V_{ref} and V_{FB}, and indicates that the VCO output frequency should be decreased in order to decrease the phase difference. Care should be taken to minimize the momentary spike on the UP line, so as both the UP and DOWN lines are not simultaneously in the logic high state for a significant amount of time.

3) The rising edge of V_{FB} (V_{outVCO}) is in phase with the rising edge of V_{ref} (Fig. II-14 (c)):

   Momentary spikes will appear on the UP and DOWN signal lines if both rising edges arrive at the same time, causing the *reset* line to clear the latches, returning both the UP and DOWN signal lines to a logic low value. Thus, in phase lock, the UP and DOWN lines in the PFD ideally remain at logic low. In contrast, phase lock is represented in typical PDs with active UP and DOWN signal lines, where signals are inverses of one another with 50% duty cycles. As the PFD does not generate any output signals during phase lock, the amount of control voltage ripple is therefore reduced, subsequently reducing the phase jitter due to the phase detector characteristics.

Based on the functionality of the PFD, numerous characteristics can be described. First, a rising edge from V_{ref} and V_{FB} must be present when making a phase comparison. Second, the widths of V_{ref} and V_{FB} are irrelevant. Consequently, the PFD will not lock on a harmonic of the data. Next, the outputs of the PFD are both logic low when the loop is in lock, eliminating voltage ripple on the output of the loop filter. Although the PFD has numerous advantages over standard PDs, the PFD has poor input noise rejection; that is, a false edge on either input will affect the outputs of the PFD [Ba08].

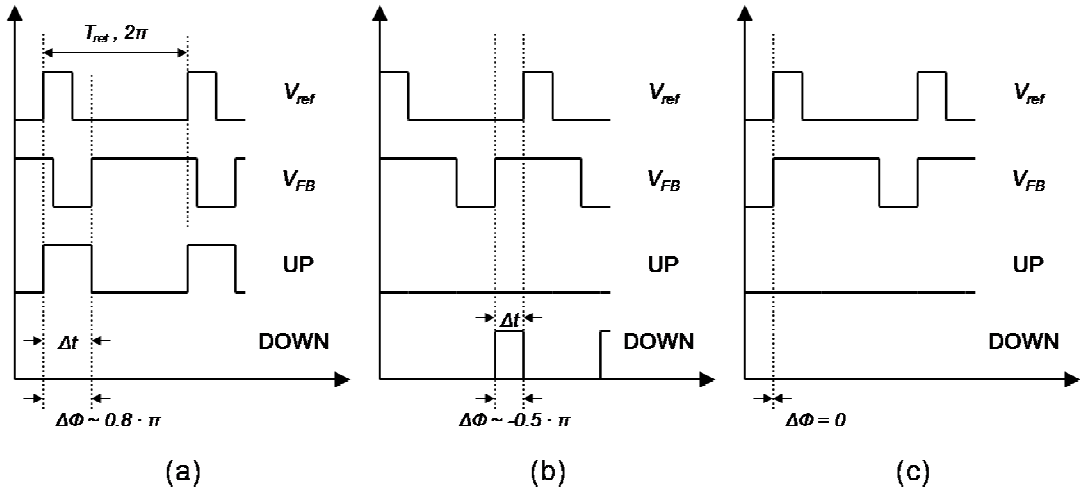


Fig. II-14. PFD inputs and outputs for (a) V_{FB} lagging V_{ref}, (b) V_{FB} leading V_{ref}, and (c) V_{FB} in phase lock with V_{ref} (adapted from [Ba08]).

The Charge Pump and Loop Filter

The charge pump is a circuit capable of converting the PFD output signals, representing the phase difference between V_{FB} and V_{ref}, into an electrical current or voltage. Fig. II-15 illustrates two basic topologies of charge pump circuits. For the case of the current-based charge pump (Fig. II-15(a)), the UP/DOWN outputs of the PFD drive pMOS/nMOS switches to source/sink current (I_{CP}) to/from the LPF. Similarly, a voltage-based charge pump (tri-state) may be used where the UP/DOWN outputs of the PFD connect the charge pump output to either V_{dd} or GND (or a voltage reference). Typically, current-based charge pumps are used because they show higher immunity to power supply variations over voltage-based charge pumps (power supply rail is closely coupled to the VCO control voltage). Finally, the PFD gain (K_{PD}) is directly controlled by the chosen value of I_{CP} (for the current-based charge pump) or the power supply voltage (for the voltage-based charge pump). Furthermore, it can be shown that

Eqns. (II-22) and (II-23) represent the PFD gain for the current-based charge pump (K_{PDI}) and the voltage-based charge pump (K_{PDV}), respectively.

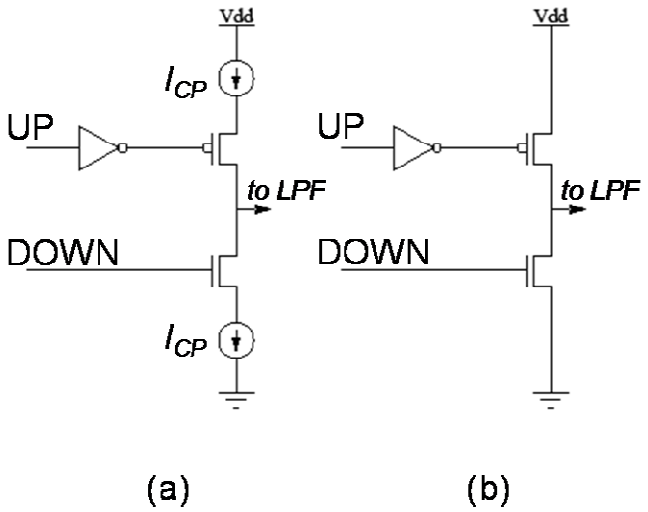


Fig. II-15. Basic schematic of (a) current-based charge pump and (b) voltage-based charge pump (tri-state).

$$K_{PDI} = \frac{I_{CP}}{2\pi}(amps/radian) \tag{II-22}$$

$$K_{PDV} = \frac{V_{dd}}{4\pi}(volts/radian) \tag{II-23}$$

Following the charge pump, the loop filter integrates the charge supplied by the switching of the charge pump. Basic loop filters required for the current-based and voltage-based charge pumps are shown in Figs. II-16 (a) and (b), respectively. As shown in previous sections the design of the loop filter is crucial in determining the overall performance of PLL system. The impacts of the loop filter on the PLL performance are

derived by determining the transfer equation for the chosen loop filter, inserting it into the PLL loop transfer equations, and calculating the PLL performance parameters such as the natural frequency and damping ratio.

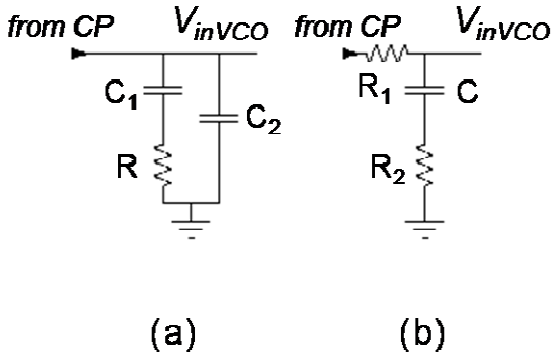


Fig. II-16. Basic loop filters for the (a) current-based and (b) voltage-based charge pumps.

First, for the loop filter shown in Fig. II-16 (a), the loop filter transfer function is given by Eqn. (II-6) as previously discussed. The capacitance C_2 is ignored as it is typically much smaller than C_1. Typically, C_2 is chosen to be approximately 10 times smaller than C_1 (or less) in order to improve the stability of the loop while in lock. Thus, the closed-loop transfer function for the PLL shown in Fig. II-4 is given by Eqn. (II-7). Subsequently, the loop natural frequency and damping factor are given by Eqns. (II-8) and (II-9), respectively.

Thus, for the current-based charge pump the natural frequency is influenced by the source/sink current (I_{CP}) and the capacitance of C_1 in the loop filter. As C_1 is increased the natural frequency is decreased. Also, the time constant RC_1 directly influences the

damping ratio. A larger time constant that suppresses high-frequency noise also increases the damping ratio and may lower the natural frequency of the loop.

Next, Eqn. (II-24) represents the loop filter transfer function shown in Fig. II-16 (b). When the filter is driven by the voltage-based charge pump, no current flows through either resistor when the output of the charge pump is in the high impedance state. Thus, the filter can be thought of as an ideal integrator with a transfer function given by Eqn. (II-25). Furthermore the closed-loop transfer function, natural frequency, and damping ratio for the PLL shown in Fig. II-11 are given by Eqns. (II-26), (II-27), and (II-28), respectively.

$$K_F = \frac{1 + sR_2C}{1 + s(R_1 + R_2)C} \tag{II-24}$$

$$K_F{}' = \frac{1 + sR_2C}{s(R_1 + R_2)C} \tag{II-25}$$

$$H(s) = \frac{\phi_{VoutVCO}}{\phi_{REF}} \frac{K_{PDV}K_{VCO}\dfrac{1 + sR_2C}{(R_1 + R_2)C}}{s^2 + s\dfrac{K_{PDV}K_{VCO}R_2C\beta}{(R_1 + R_2)C} + \dfrac{K_{PDV}K_{VCO}\beta}{(R_1 + R_2)C}} \tag{II-26}$$

$$\omega_n = \sqrt{\frac{K_{PDV}K_{VCO}\beta}{(R_1 + R_2)C}} \tag{II-27}$$

$$\zeta = \frac{\omega_n}{2} R_2 C \tag{II-28}$$

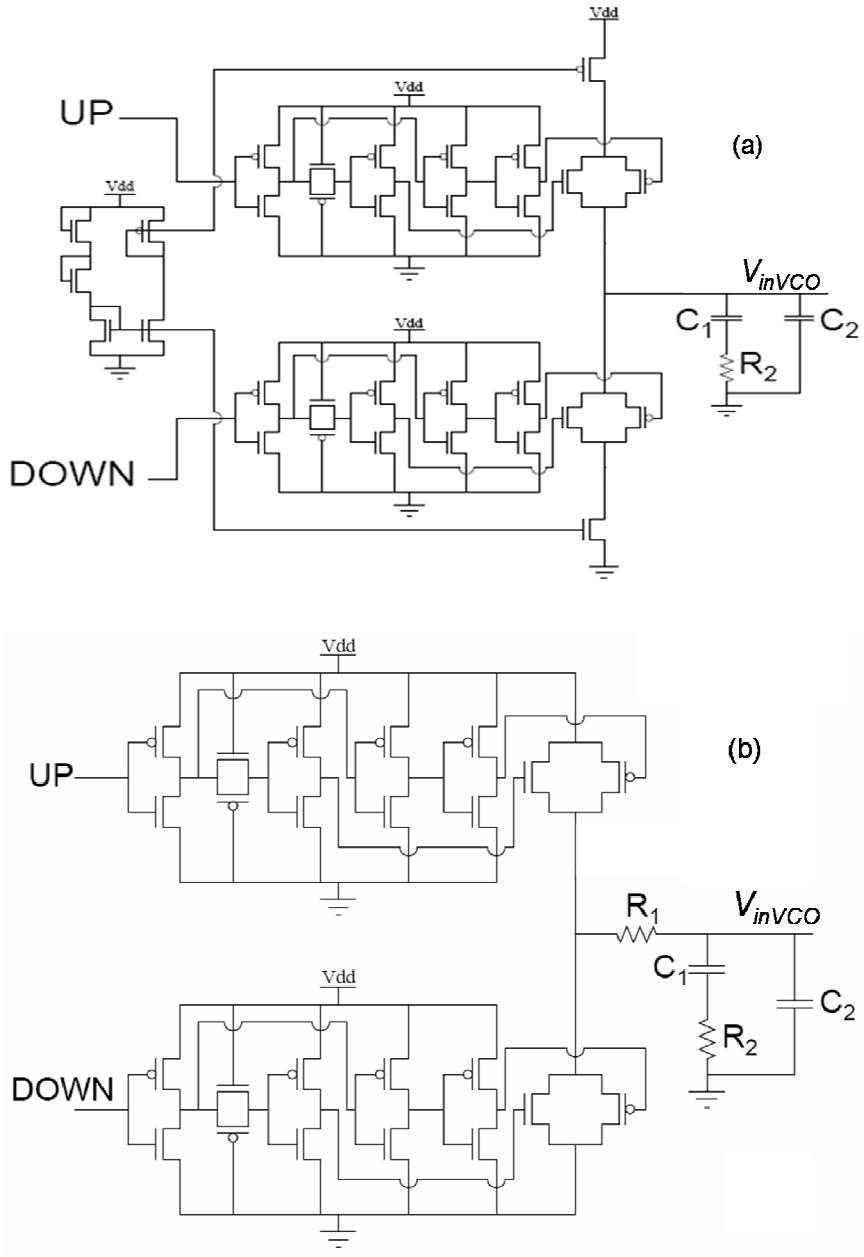


Fig. II-17. Practical implementations of the (a) current- and (b) voltage-based charge pumps and respective loop filters.

Thus, for the voltage-based charge pump the natural frequency is influenced by the power supply voltage and the loop filter time constant $(R_1+R_2)C$. As the time constant is increased the natural frequency is decreased. Also, the time constant R_2C directly influences the damping ratio. A larger R_2C time constant increases the damping ratio and may lower the natural frequency of the loop.

Finally, Figs. II-17 (a) and (b) illustrate practical implementations of the current- and voltage-based charge pumps along with their respective loop filters used for this work [Bo06, Lo06, Lo07a, Lo07b]. In both cases the UP and DOWN switches utilize transmission gates. To ensure that the nMOS and pMOS devices in the transmission gates turn on and off simultaneously, circuitry consisting of four inverters and a transmission gate delay cell are used. Additionally, for the current-based charge pump, the current sources should be sized such that the sink and source currents are equivalent when biased through displayed bias circuit.

The Voltage-Controlled Oscillator

The charge pump is a circuit capable of converting the measured phase difference between the inputs of the PFD into an analog control voltage applied to the input of the voltage-controlled oscillator (VCO). The VCO, therefore, is required to generate an oscillating output signal at a frequency determined by the input voltage, V_{inVCO}. This work concentrates primarily on current-starved VCO topologies as they typically have wide operating frequency ranges; however, current-starved VCOs may not be suitable for low jitter applications, in which case an LC tank VCO with low jitter and a small frequency range may be used [Ba08].

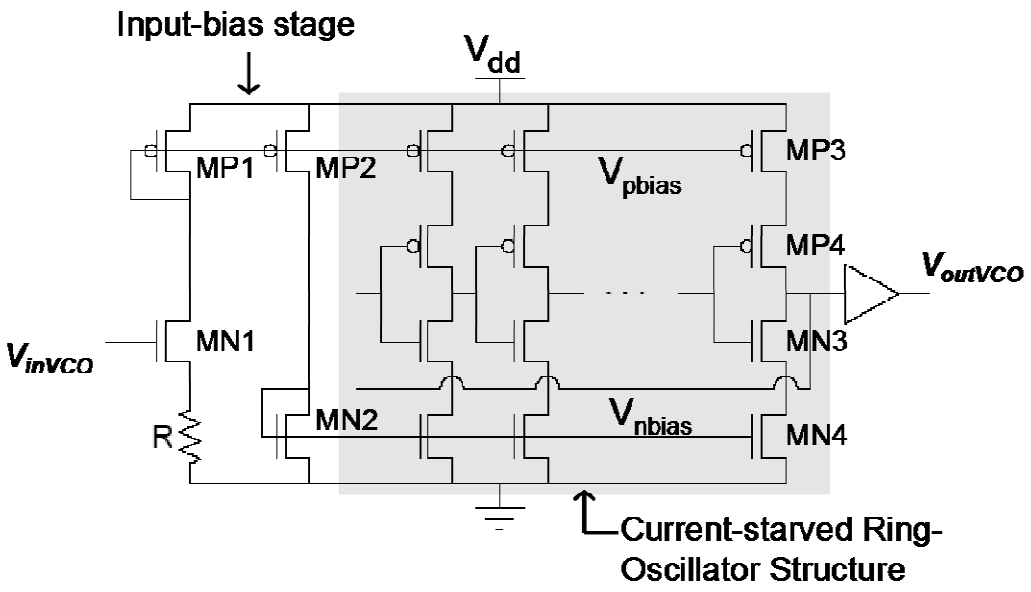


Fig. II-18. Schematic of the current-starved VCO.

Fig. II-18 illustrates the schematic of the current-starved VCO used throughout this work and indicates the input-bias stage and the current-starved ring-oscillator stage. MOSFETs MP4 and MN3 operate as an inverter, while MOSFETs MP3 and MN4 limit the current available to the inverter, thus setting the delay of the current-starved inverter stage. The input-bias stage is used to force the current in the MOSFETs to be linearly related to V_{inVCO}. The width of MOSFET MN1 is made wide (a W/L of ~100/1) so that V_{GS} is always approximately V_{TN} (close to independent of V_{inVCO}). The current in MOSFET MP1 is then mirrored to MOSFETs MP2 and MN2 to control the current used in the current-starved ring-oscillator stage. Alternative biasing schemes may be utilized [Ba08].

The design equations for the VCO may be developed by considering the simplified schematic of one current-starved inverter stage, as in Fig. II-19. The total capacitance on

the drains of the inverter (MP4 and MN3), C_{tot}, can be described as the sum of the output and input capacitances of the inverter, and can be shown to be approximately equal to Eqn. II-29. If we assume that $I_{P3} = I_{N4} = I_D$, and the time for C_{tot} to discharge from V_{dd} to 0 V is equivalent to the time for C_{tot} to charge from 0 V to V_{dd}, then the charge (t_1) and discharge (t_2) time (or the total delay time of the cell (t_D)) is represented by Eqn. (II-30).

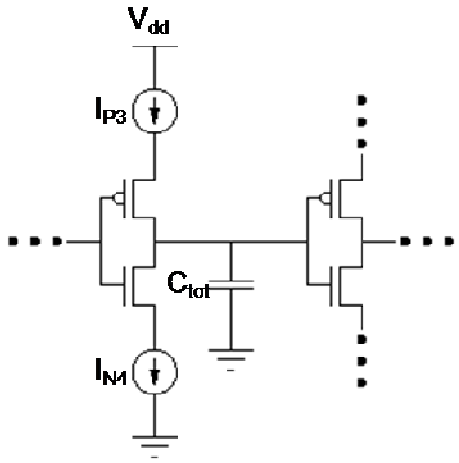


Fig. II-19. Simplified schematic of a single current-starved stage in the VCO.

$$C_{tot} = \frac{5}{2} C_{ox}^{'} \left(W_P L_P + W_N L_N \right) \tag{II-29}$$

$$t_D = t_1 + t_2 = \frac{C_{tot} \cdot V_{DD}}{I_D} \tag{II-30}$$

Thus, the oscillating frequency of the VCO for N (an odd number ≥ 5) number of stages is represented by Eqn. (II-31) [Ba08].

$$f_{osc} = \frac{1}{N(t_D)} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \tag{II-31}$$

Examples of the frequency characteristics for the current-starved VCO are shown in Fig. II-20, where output frequency is plotted versus V_{inVCO} for a 'good' design and a 'bad' design [Bo05]. The designed center frequency (the frequency at which V_{inVCO} is $V_{dd}/2$) should be within ± 10% of $(f_{max} - f_{min})/2$ in order to ensure a symmetric range of linear operation around the center frequency (f_c) [Ba08, Bo05]. The frequency transfer curve for the 'bad' design is a result of deliberately mismatched W/L ratios for MOSFETs MP2, MP3, MN2, and MN4.

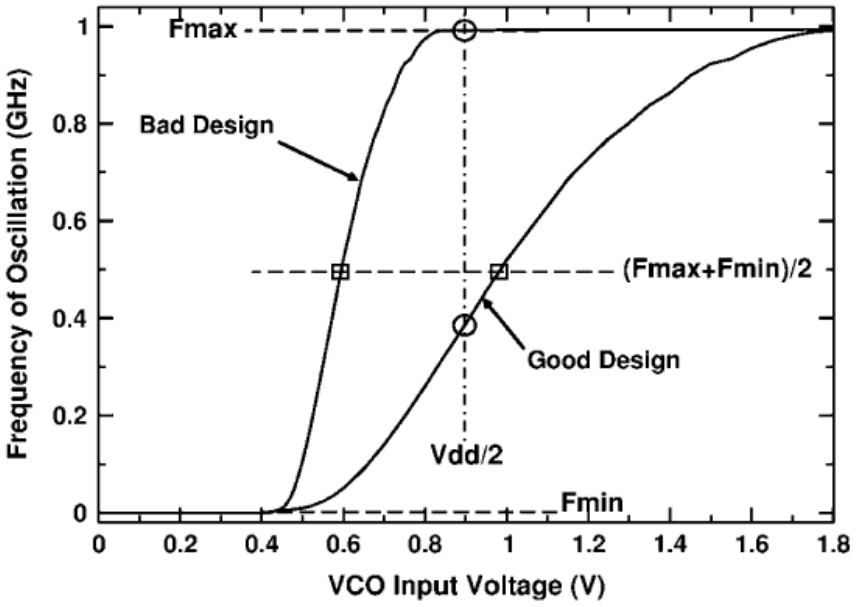


Fig. II-20. Current-starved VCO gain characteristics illustrating an example of a poor VCO design where the frequencies f_c and $(f_{max} + f_{min})/2$ are far apart, to be contrasted with a desirable design example where the frequencies are within 10% of each other [Bo05].

The gain of the VCO, K_{VCO}, is in units of radians per seconds per volts. K_{VCO} is typically approximated by finding the slope of the linear portion of the transfer curve shown in Fig. II-20. Eqn. (II-32) shows the gain of the VCO, where f_{max} and f_{min} are the maximum and minimum frequencies of the VCO operating range, respectively. Similarly, V_{max} and V_{min} are the input voltages that result in f_{max} and f_{min}, respectively.

$$K_{VCO} = 2\pi \cdot \left(\frac{f_{\max} - f_{\min}}{V_{\max} - V_{\min}} \right) \quad (radians/sec)/V \tag{II-32}$$

$$\Delta t_{jitter} = \frac{1}{f_c - \Delta f_{VCO}} \quad (sec) \tag{II-33}$$

An additional design variable often useful for VCO designs is the estimated phase jitter. Phase jitter describes the amount of time or phase fluctuation present in the output signal of the VCO during steady state. A simple method of estimating the phase jitter is to first monitor or estimate the amount of voltage variation on V_{inVCO}. Next, from the VCO transfer characteristics, the corresponding frequency fluctuation, Δf_{VCO}, may be obtained. Then, Eqn. (II-33) may be used to estimate the jitter, Δt_{jitter}, in the output [Ba08].

The Frequency Divider

Frequency dividers are commonly used in PLLs for frequency synthesis applications or high frequency clock generation applications. The frequency dividers are typically implemented as an asynchronous cascade of divide-by-*2* circuits, where each stage is

clocked by the previous one [Le04b, Ra95]. The general block diagram of a single divide-by-*2* frequency divider is shown in Fig. II-21 (adapted from [Le04b]). The D-Flip-Flops are connected in a master-slave fashion with the output of the slave stage fed back to the input of the master stage. The frequency divider displayed may be cascaded in order to form a divide-by-*N* frequency divider, where *N* is a multiple of 2. Additionally, a multiplexer may be used to select the desired outputs of the frequency dividers. Many other digital and analog implementations have been developed for improved jitter performance and low power, however all designs may be thought to have similar functionality for the use in PLL applications.

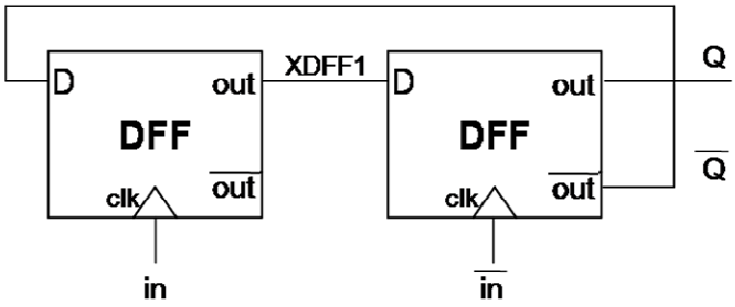


Fig. II-21. Diagram of a single divide-by-*2* frequency divider (after [Le04b]).

Conclusion

This chapter presents a detailed background on phase-locked loop circuits, beginning with a control-systems analysis of the general functionality. Derivations of important electrical parameters such as the natural frequency, damping ratio, and lock time, along with the electrical characteristics are also provided. Finally, the detailed circuit topologies and any critical design equations of each sub-circuit within the charge pump PLL are provided. The next chapter presents a background on single-event phenomena

and the radiation environments that are of particular concern to mixed-signal circuit topologies, such as the PLL, designed for operation in space.

CHAPTER III

RADIATION EVIRONMENTS AND SINGLE-EVENT PHENOMENA

Introduction

Microelectronic circuits in space-deployed systems are subject to a variety of radiation environments and their characteristic particles. In order to ensure the reliability and durability of the components it is crucial to consider all of the potential effects irradiation can have on circuit operation. Irradiation can result in a wide variety of device and circuit level effects such as Displacement Damage (DD), Total-Ionizing Dose (TID), Prompt Dose (Dose Rate), and Single-Event Effects (SEE). With the continual advancement of microelectronic technology, SEEs are likely to become an increasingly important upset mechanism for ICs deployed in space and terrestrial applications [Ma93], therefore will be the primary focus of this discussion. In fact, as shown in Fig. III-1, Koons *et al.* showed that SEEs account for over 28% of spacecraft anomaly records, including electrostatic discharge (ESD) damage, other radiation damage, plasma and micrometeoroid impacts, and uncategorized solar energetic particle effects [Ko99, Ma02]. Additionally, SEUs account for over 84% of all radiation effects observed, as seen in Fig. III-2 [Ko99, Ma02]. Although not discussed in this work, DD [Sr03], Prompt Dose [Al03], and TID [Ol03] references are included for the interested reader.

The remainder of this chapter will discuss the various radiation environments of particular concern for SEEs. Next, a discussion on the fundamental charge generation and collection mechanisms for SEEs will be provided. The chapter will conclude with

details of the different types of SEEs that can occur in ICs with a particular emphasis on Single-Event Upsets (SEU) and Single-Event Transients (SET).

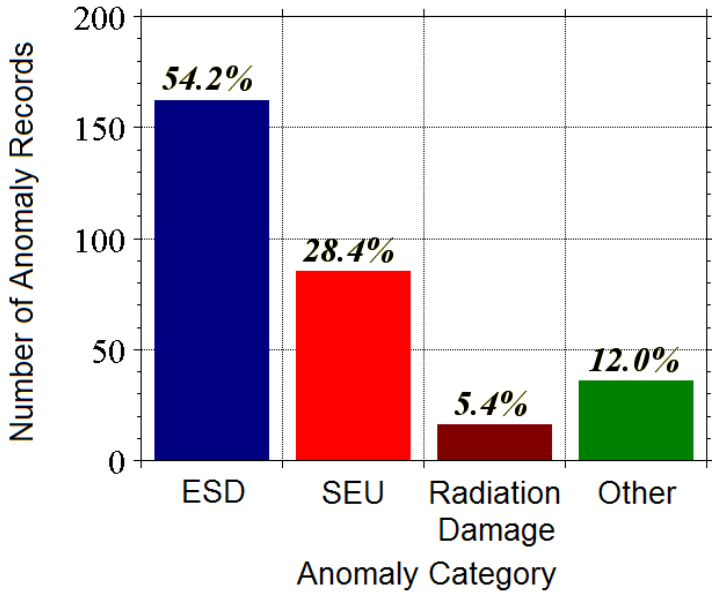


Fig. III-1. Distribution of spacecraft anomaly records versus anomaly type (ESD: electrostatic discharge; SEU: single event upset) [Ma02] (data from [Ko99]).

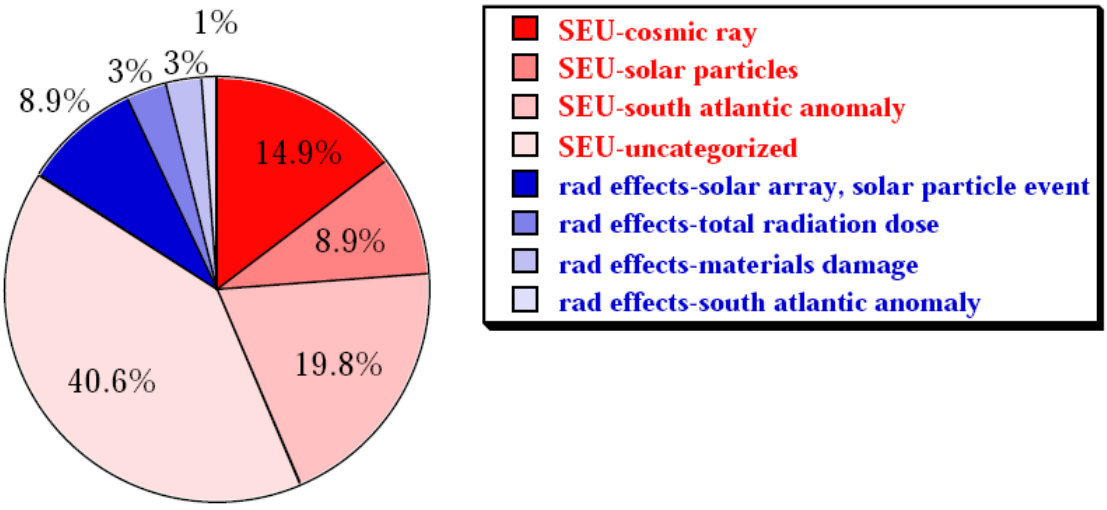


Fig. III-2. Breakdown of SEU and radiation damage anomaly records [Ma02] (data from [Ko99]).

Radiation Environments and Single-Event-Inducing Particles

Ionizing radiation interacts with various materials used in an IC to produce results depending on the nature of the radiation source. The primary contributors to the space radiation environment are galactic cosmic rays (GCR), solar flares, and particles trapped within the Earth's magnetosphere.

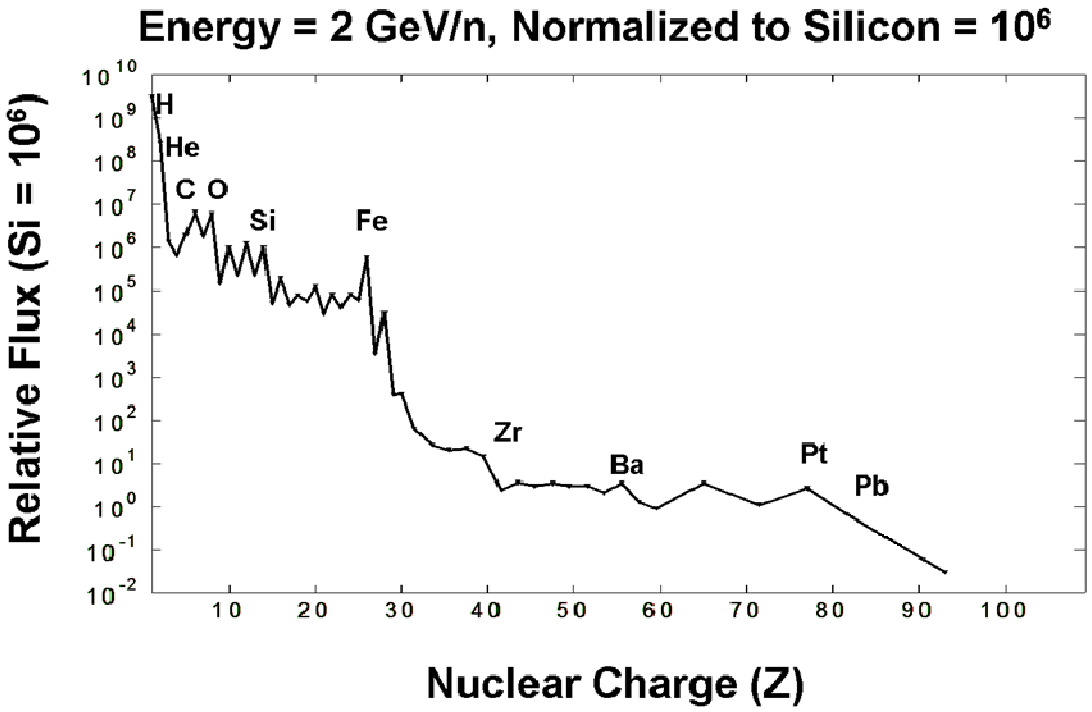


Fig. III-3. Galactic cosmic ray particle spectrum as a function of atomic number (adapted from [Me74] and [Ba98]).

Galactic Cosmic Rays

While the actual source of GCRs is unknown, one likely explanation is the several supernovae (exploding stars) that occur within the galaxy each century. The ionizing particles that are carried by the GCRs include most elements present in the periodic table with energies varying from 10^9 eV up to the highest ever reported of 10^{20} eV [Bi95]. The

relative abundance of elements present in GCRs is shown in Fig. III-3 (adapted from [Me74] and [Ba98]), where hydrogen is the most abundant element.

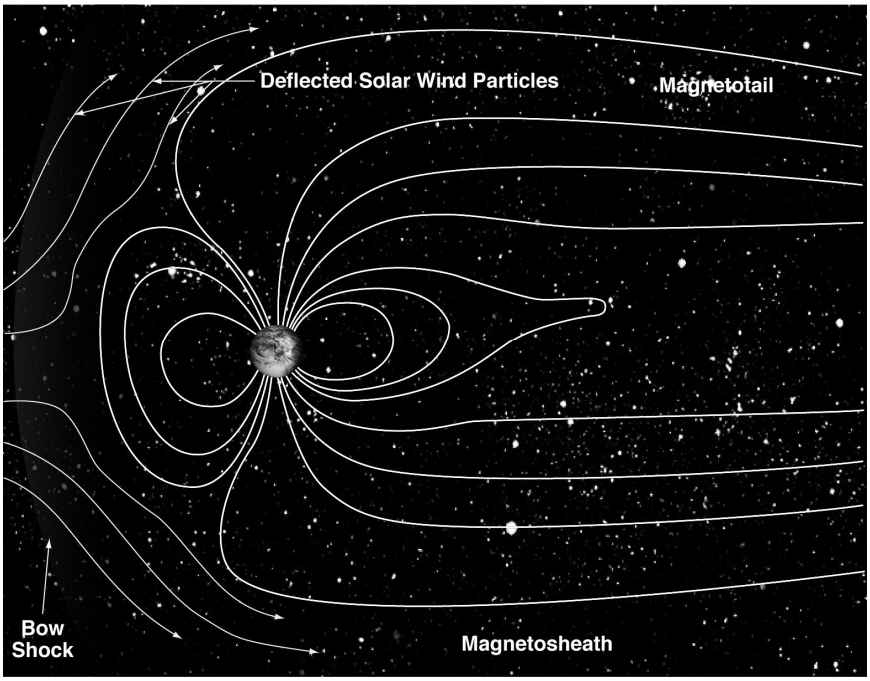


Fig. III-4. The Earth's magnetosphere [Xa06].

An additional source of space irradiation is the sun. The cyclical activity of the sun, which averages as an 11 year cycle, not only contributes to trapped electron fluxes, which are typically a TID concern, but also trapped proton fluxes in the Low Earth Orbit (LEO) [Xa06]. Trapped protons, which reach their maximum during solar minimum, can cause TID effects, DD effects, and SEE, where most proton-induced SEE occur as a result of secondary recoil products that result from interactions with the incident proton [Xa06]. Furthermore, the continual solar wind (plasma or ionized gas emitted by the sun) interacts with the Earth's magnetosphere. As depicted by Fig. III-4, the Earth's magnetosphere is shown to consist of both an external and an internal magnetic field. The external field is

the result of the solar wind, whereas the internal (geomagnetic field) originates primarily from within the Earth and is approximately a dipole field. During solar maximums the solar wind diverts GCRs from the magnetosphere (the magnetosphere can be compressed to approximately 6 Earth radii), whereas higher GCR fluxes are typical of solar minimums (the magnetosphere can be expanded to approximately 10 Earth radii) [Xa06].

Solar Flares and Coronal Mass Ejections

Solar flares and coronal mass ejections are sudden, rapid, and intense bursts of gases and plasma emitted from the sun's atmosphere and corona. Typically, the most energetic and frequent solar flares occur within the 7 years of high activity within the 11 year solar cycle. Two types of solar flares can occur: gradual eruptions and rapid, intense bursts. Gradual eruptions (lasting days) are rich in protons with energies spanning from 30 MeV to 100 MeV, whereas the most intense eruptions (lasting hours) may contain energies as high as 100 GeV. Also, the radiation that is emitted during a solar flare spans virtually the entire electromagnetic spectrum, from radio waves to x-rays and gamma rays, and will increase the fluxes of cosmic rays that penetrate the Earth's magnetosphere [Ho07]. The largest ever recorded solar flare, captured by the Solar and Heliospheric Observatory (SOHO) satellite, occurred on April 2, 2001 as a coronal mass ejection. The eruption projected particles into space at roughly 7.2 million kilometers per hour and produced a radio blackout on the sunlit side of the Earth. Fig. III-5 illustrates the event through a series of photos captured by charge coupled devices (CCD) [Ma99, SOHO]. As protons from the event reach the instrument's CCDs, they "pepper" the image with transients.

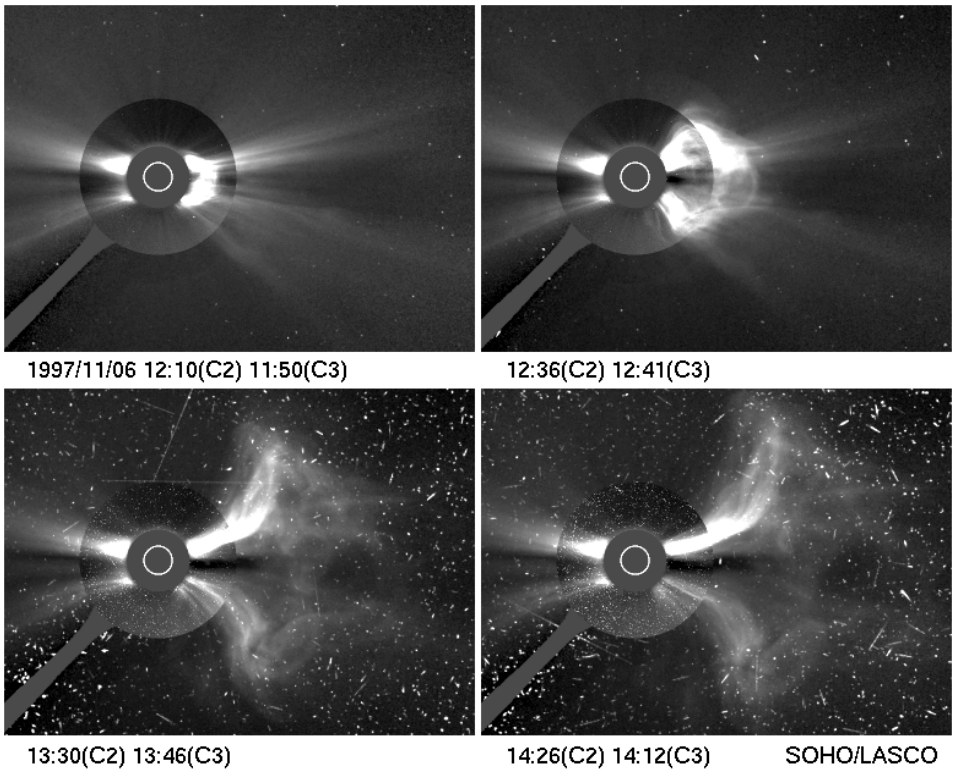


Fig. III-5. The most energetic solar flare ever recorded, Monday, April 2, 2001. Coronagraphs from the SOHO satellite follow the evolution of a coronal mass ejection. Protons from the event reach the instrument's charge coupled devices (CCD) and "pepper" the image with transients in the lower two panels [Ma99, SOHO].

The Trapped Radiation Environment

An additional source of radiation is trapped charged particles within the Earth's magnetic field. Charged particles in the near-Earth atmosphere can become trapped by the constraining geo-magnetic field lines. The charged particles in this field move in a spiral fashion around the magnetic field lines, tightening as they approach the magnetic poles where the field strength increases. Eventually the field strength is sufficient to compel the particle to reverse direction. Fig. III-6 illustrates the motion of trapped charged particles in the Earth's magnetic field [St88b, Xa06].

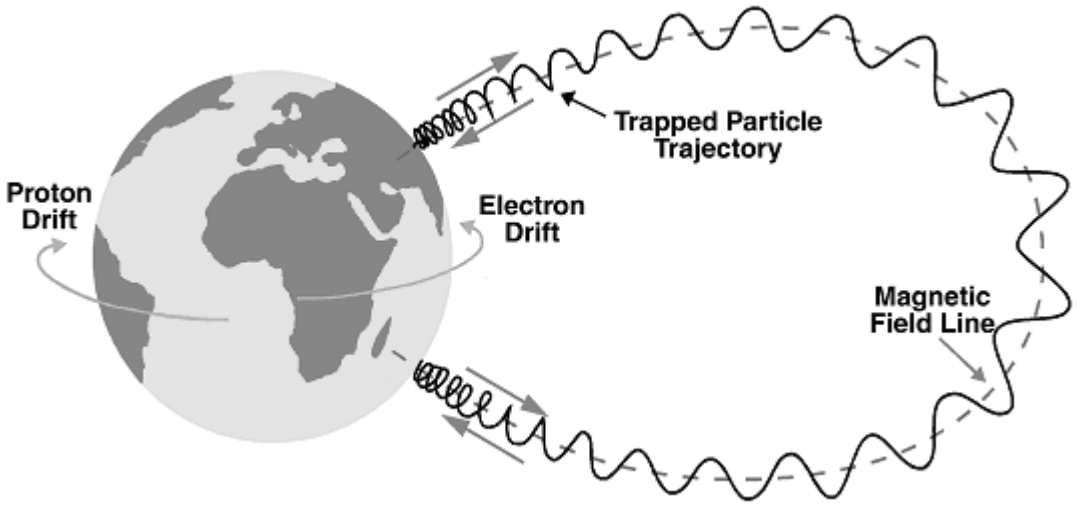


Fig. III-6. Motion of trapped charged particles in the Earth's magnetic field [St88b, Xa06].

The trapping of charged particles results in an accumulation of charged particles along the magnetic field lines, termed the Van Allen radiation belts [Va59]. There are two permanent belts, as shown by the drawing in Fig. III-7: an outer zone centered at approximately 6 Earth radii and an inner zone centered at approximately 2.5 Earth radii. The outer zone comprises of primarily electrons and some protons trapped from solar flare events, whereas the inner zone consists of primarily protons and some trapped electrons [Ba03, St88b]. Electrons contribute to most radiation events in the outer zone, whereas protons contribute to the majority of events in the inner belt [Ma02]. The proton and electron domains within the two primary belts are indicated in Fig. III-8 [St88b]. During intense solar activity, additional belts may appear, however are temporary and therefore will not be discussed in detail.

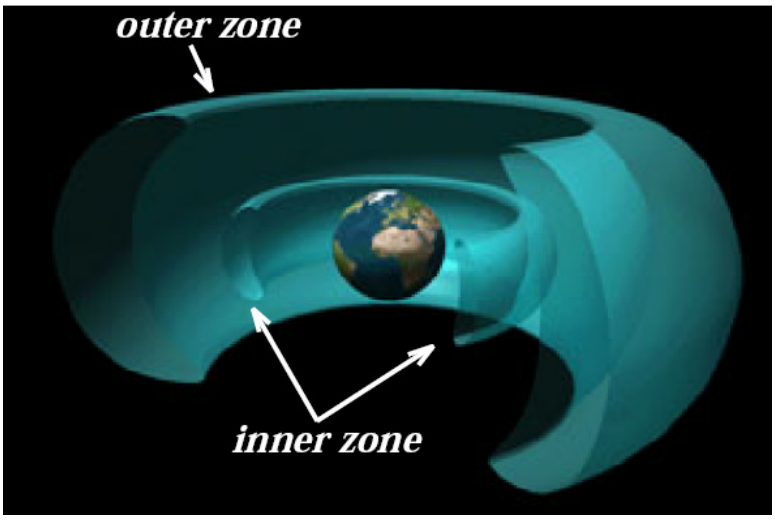


Fig. III-7. Diagram of the Earth's Van Allen radiation belts [Ma02].

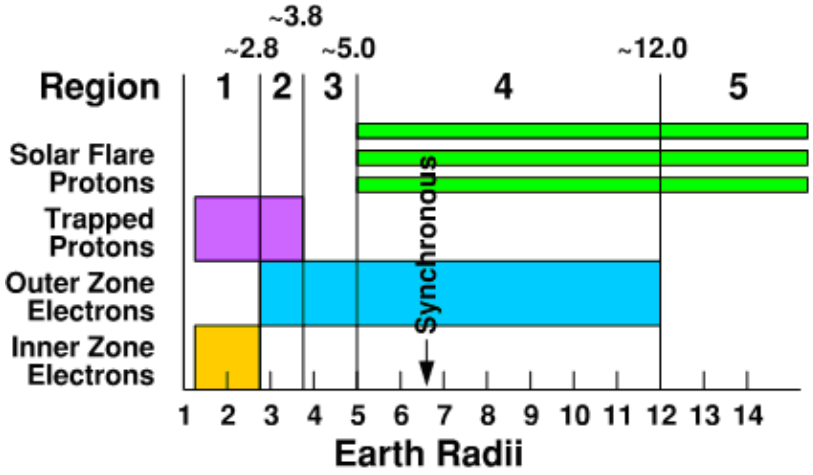


Fig. III-8. The proton and electron domains within the two primary Van Allen belts [St88b].

Protons are the most predominant source of SEEs for spacecrafts in near-Earth (1.5 to 3.5 Earth radii) and polar orbits, with energies ranging from tens of keV to hundreds of MeV. Fluxes for these energies range from over 10^6 protons/(cm^2-day) (for 10^2 MeV protons) to 10^9 protons/(cm^2-day) (for 10^{-2} MeV protons). In fact, proton spectra in Low-

Earth Orbit (LEO) tends to remain fairly stable across energy with the proton flux decreasing by only 4 orders of magnitude between 50 MeV and 500 MeV [St88b].

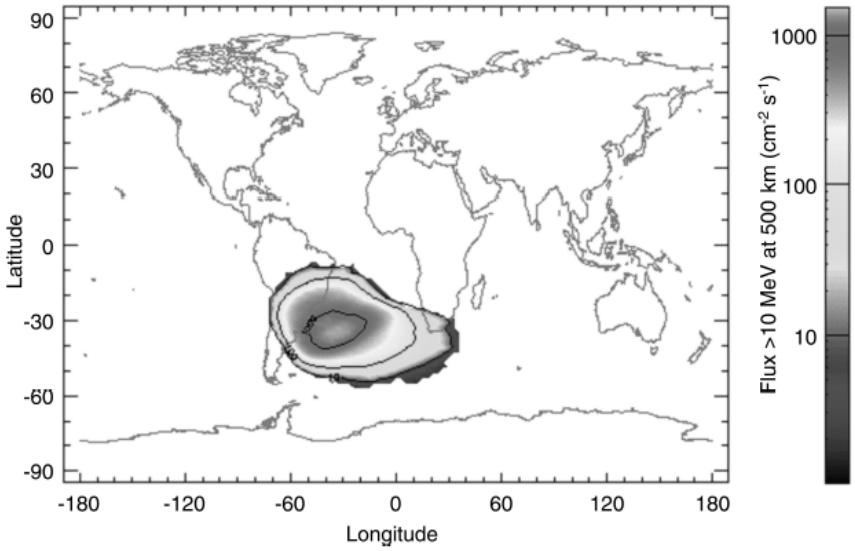


Fig. III-9. Contour plot of proton fluxes > 10 MeV in the SAA at a 500 km altitude during solar maximum [Xa06].

The proton belt also contains an anomaly of particular concern for near-Earth orbiting vehicles. The anomaly, named the South Atlantic Anomaly (SAA), is located off the coast of South America and displays a great increase in proton flux at altitudes less than 1000 km. The "dip" in the proton belt is a result of the tilt and shift of the Earth's geomagnetic and rotational axes relative to each other, causing a displacement of the magnetic field from the center. Fig. III-9 shows a contour plot of proton fluxes > 10 MeV in the SAA at a 500 km altitude during solar maximum. The lower magnetic field region of high proton fluxes is localized to an area off the coast of Argentina.

Single-Event Mechanisms

Heavy ions, alpha particles, and trapped protons from the radiation environments previously discussed can result in significant damage to microelectronic circuits. When an energetic particle penetrates semiconductor material it loses energy through Coulomb collisions with the target electrons and nuclei of the lattice structure, leaving a dense track of electron-hole pairs in the material [Re08]. These excess carriers can be collected as charge on circuit nodes, resulting in undesirable circuit responses which can vary depending on the circuit topology and the amount of charge collected. The resulting effect from this interaction is termed a Single-Event Effect (SEE) as it results from the penetration of a single energetic particle into the material. In fact, as previously stated, a compilation of spacecraft anomalies [Ko99] shows that SEEs account for over 84% of the radiation damage that occurs to critical on-board electronics, and over 28% of the total records, including ESD events, plasma, micrometeoroid impacts, and uncategorized solar energetic particle effects.

Charge Generation

Energetic particles that pass through microelectronic circuits can generate charge in a semiconductor device through two fundamental mechanisms: indirect ionization and direct ionization. Indirect ionization occurs through the nuclear reactions of an incoming particle with elements of the molecular lattice. The nuclear reactions can be inelastic collisions producing Si recoils, Alpha/Gamma particle emission and the recoil of a daughter nucleus, and spallation reactions, each of which can independently recoil

[Do99]. The nuclear reactions can thus result in the emission of heavier ions that can interact with the semiconductor devices through direct ionization.

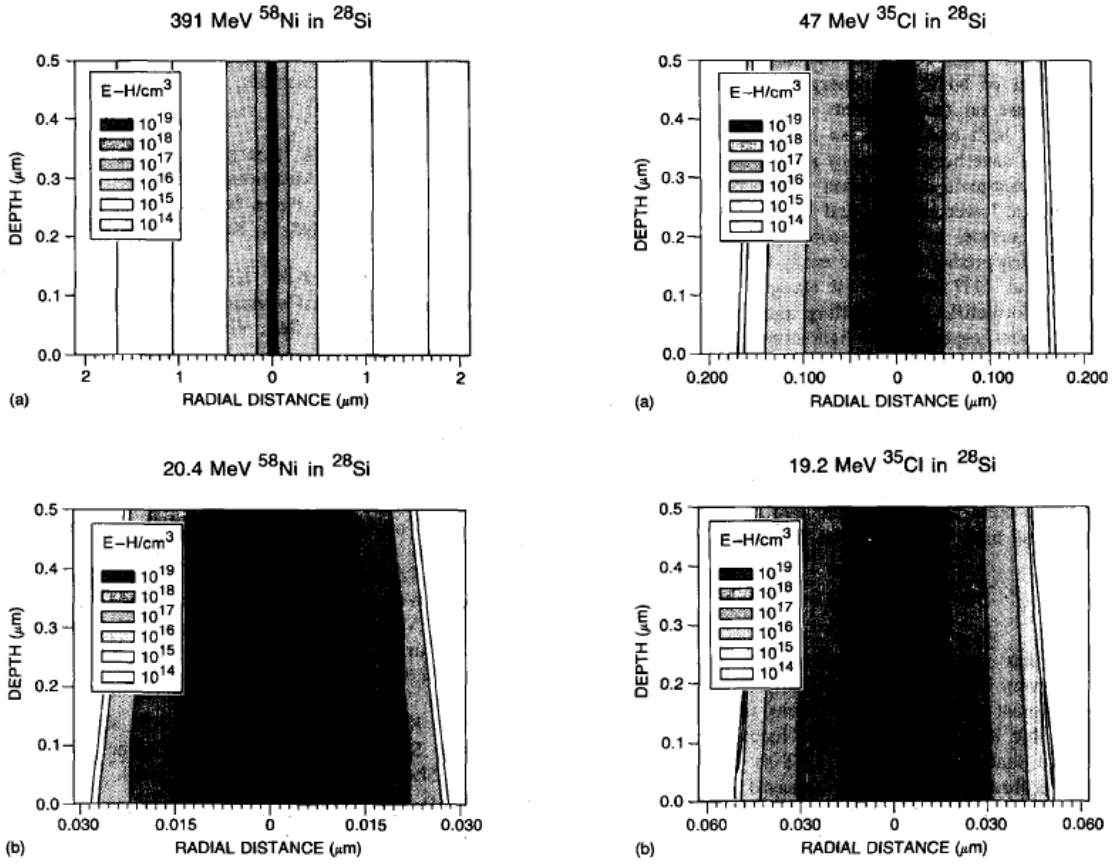


Fig. III-10. Radial distributions of the electron-hole pair densities surrounding the ion path (after [St88a]).

Direct ionization typically requires heavy-ion ($Z > 1$) or low-energy proton [Si09] strikes and occurs when the ion itself penetrates the semiconductor material, losing energy through Coulomb interactions with the target electrons and nuclei of the lattice structure [Re08]. As the ion transfers energy to the lattice, electrons are excited from the valence band into the conduction band, thus leaving behind valence band holes. The

excitation of the electrons can further emit photons and phonons, which can create new electron-hole pairs. This scattering, which follows the Compton scattering effect, leaves a dense plasma track of excess carriers that follows the range (path length) of the incident ion. Fig. III-10 shows calculations of electron-hole distributions through the silicon's depth versus the radial distance of the plasma track created by Ni and Cl ions of various energies. In both cases the higher energy particle produces a less dense track due to the decreased interaction efficiency of the energetic ion with the bound electrons within the lattice. Subsequent paragraphs explain the phenomenon further.

Linear Energy Transfer (LET) is typically used to describe this energy loss of the ionizing particle through the material. LET is the energy loss per unit length normalized by the density of the target material, and is typically given in units of MeV-cm^2/mg. Thus, LET is a function of the incident particle, ion energy, and penetration depth.

Fig. III-11 shows LET versus penetration depth for 210 MeV chlorine ions in silicon, where the integral of the curve represents the total energy deposition. As the particle penetrates deeper into the structure it slows allowing for a more effective interaction with the bound electrons and the LET gradually increases. Finally, maximum energy loss occurs close to the particles resting point when the remaining energy is released into the structure. This point (peak of curve) is referred to as the Bragg peak (Fig. III-11 [Do99]), and following the Bragg peak the LET dramatically decreases. Such information is useful for SEE analysis because it provides information as to the depth that the majority of the charge is generated within the devices. This knowledge can be used to assist in device and circuit modeling for the simulation of SEEs.

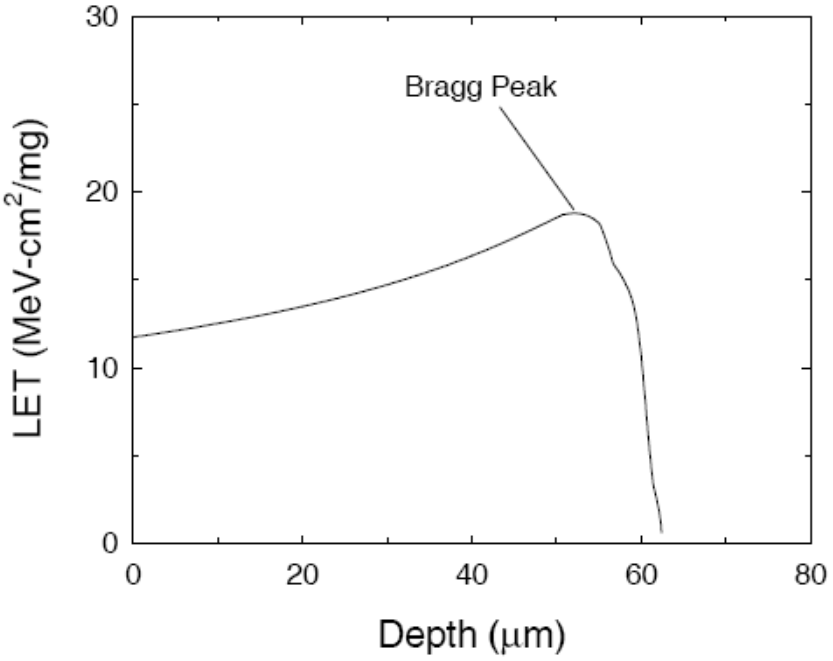


Fig. III-11. Linear energy transfer (LET) vs. depth curve for 210 MeV chlorine ions in silicon [Do99].

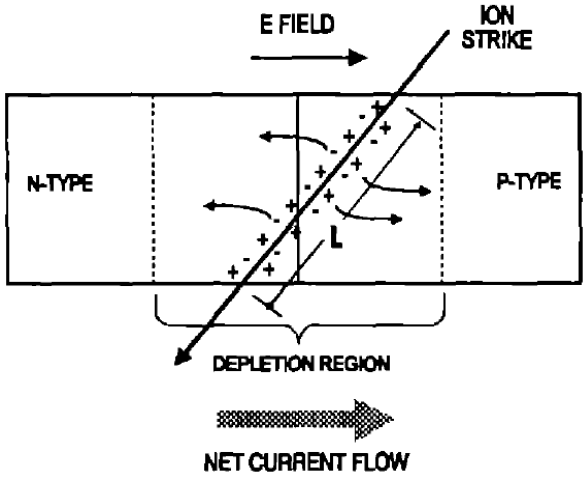


Fig. III-12. Depletion region drift collection from an ion strike [Ma93].

Charge Collection

The excess carriers generated from an SE strike present a problem for ICs when the charge is collected on circuit nodes, resulting in undesirable circuit responses. If the charge is collected near a p-n junction, the built-in electric field at the junction causes holes to be swept into the p-region and electrons into the n-region (drift current), as displayed by Fig. III-12. Drift current is limited by the saturation velocity of the carriers; therefore, the resulting current transient is typically on the order of picoseconds in length [Ma93].

Early investigations on the effects of ionizing particle strikes on p-n junctions showed that the plasma track of free carriers generated from the strike distorts the potential gradients along the track length, creating a field funnel [Hs81]. The plasma track of free carriers between the n- and p-regions effectively creates a wire between the regions along the track, allowing electrons to move toward, and holes to move away from the positively biased n-region. The spreading resistance along the wire results in a voltage drop along the length of the track and effectively collapses the junction electric field. Thus, the potential which initially appeared across the depletion region is distributed down the plasma track, and exposes carriers outside the original depletion region to the electric field [Ma93]. The overall result is an increase in charge collected drift current. Fig. III-13 illustrates the creation of the plasma wire leading to the field-assisted funneling. In modern devices at the sub-nanometer scale this process may be more complicated as the radial dimension of the plasma wire may be on the order of the transistor size or greater; however the fundamental concept is still useful for understanding the basic charge collection mechanisms. For the interested reader, references have been provided for

recent works that have analyzed charge collection mechanisms in sub-100 nm devices not previously encountered in 130 nm and older technology nodes [Da07a, Da07b].

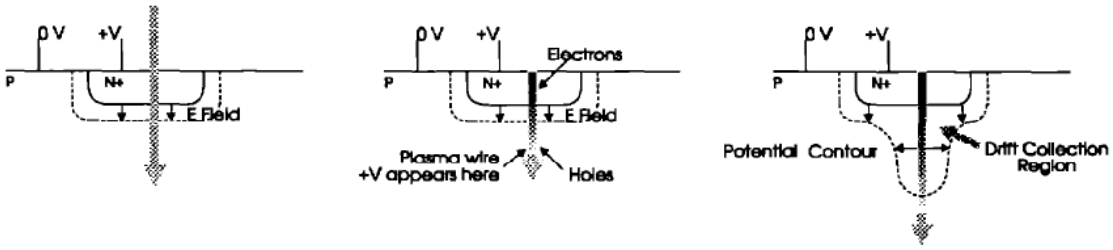


Fig. III-13. Qualitative view of the funnel effect: a) creation of the ion-induced plasma track, b) movement of electrons toward the positive bias, and c) potential drop along the track and redistribution of equipotential lines down the track [Ma93].

Additionally, charge generated from an ion strike may be collected by a diffusion process rather than a drift process. Diffusion collection arises when charge is generated within a diffusion length of a junction. The charge may be collected by the hit node or neighboring nodes, possibly affecting multiple nodes at once. In contrast to drift collection with a time domain on the order of picoseconds, diffusion collection can result in current transients on the order of hundreds of picoseconds to nanoseconds. Though the collection may last longer, diffusing charges through the semiconductor bulk are more susceptible to recombination mechanisms [Mu03], decreasing the amount of electrons and holes that reach a junction. Fig. III-14 illustrates the charge collected through drift and diffusion processes in a reverse-biased n+/p junction [Ba05]. The initial charge collection is due to field-assisted drift, followed by the collection of charge diffused through the substrate.

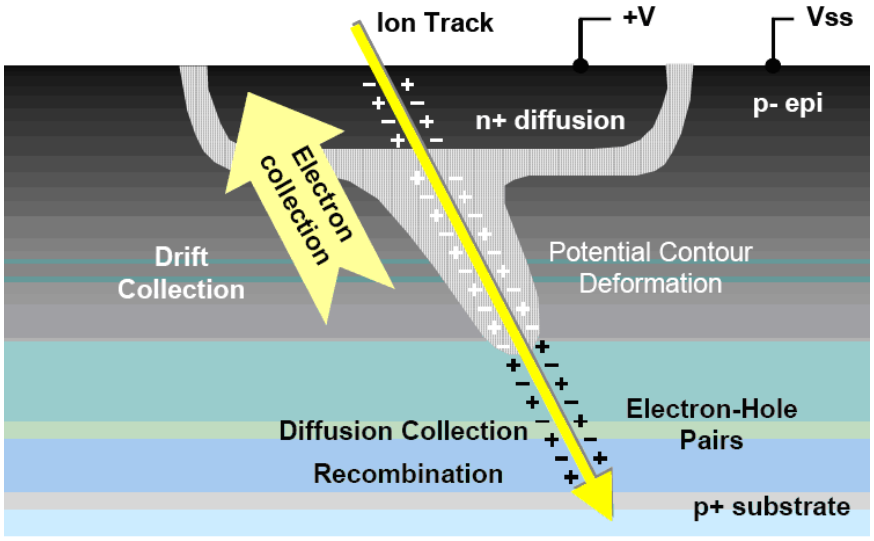


Fig. III-14. Illustration of an ion strike on a reverse-biased n+/p junction [Ba05].

Additional collection mechanisms such as the ion shunt effect [Ha85] and parasitic bipolar amplification [Am06, Do96, Fu85, Ke89, Ol05, Ol07, Wo93] are increasingly important in modern ICs. Briefly, the ion shunt effect occurs when an energetic ion passes through two proximal junctions. The plasma track of free carriers penetrates the two junctions and can conduct current if the two regions are of the same type, thus resulting in increased charge collection at a node. Parasitic bipolar amplification has also been shown to enhance charge collection from an SE strike, especially in pMOS devices in an n-well with p-substrate. Following an ion strike, the collection of electrons in the n-well reduces the n-well potential. This potential collapse, along with the additional carriers present in the substrate due to the ion strike, turns on the parasitic PNP bipolar transistor between the drain (collector), body (base), and source (emitter), resulting in increased charge collection. Drift and diffusion are the dominant charge collection mechanisms for nMOS devices.

A consequence of charge generation and collection within a semiconductor device is radiation-induced photocurrents at the device terminals. The shape of the current pulse is related to the collected charge by Eqn. (III-1), where I is the current, Q is the charge, and t is the time. As seen in Fig. III-15, an initial spike of current occurs due to drift collection, followed by a slow decrease in current due to diffusion collection [Ma93].

$$I = \frac{dQ}{dt} \left[Amps \right] \tag{III-1}$$

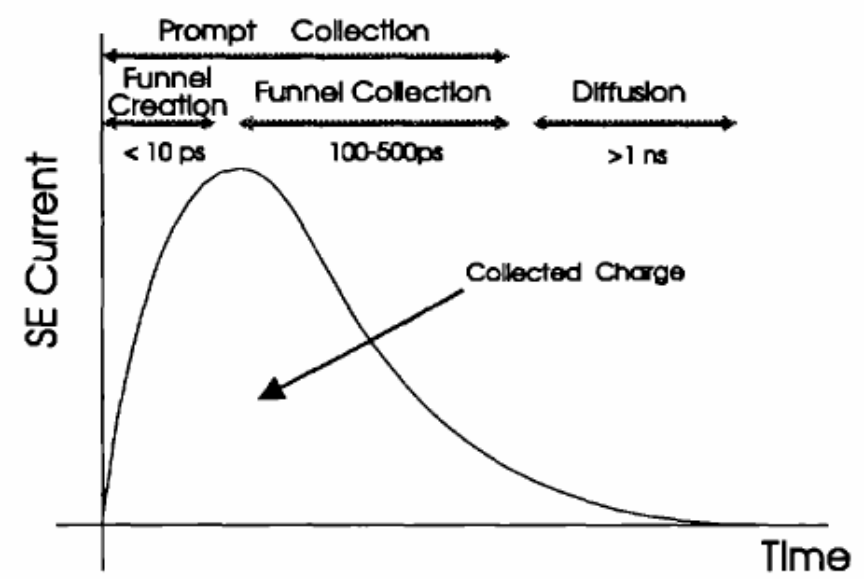


Fig. III-15. Typical shape of the SE current at a junction. The total collected charge corresponds to the area under the curve [Ma93].

An additional phenomenon, although not discussed in detail within this paper but is increasingly more important as modern electronics scale to sub-100 nm dimensions, is multiple-node charge collection. Due to the decreased feature sizes and increased packing densities, the plasma track of free carriers (electron-hole cloud) generated from

an ion strike may span multiple device junctions, allowing for charge collection by drift and diffusion processes at multiple device terminals. Fig. III-16, for example, illustrates the relative range of the electron-hole cloud created by a single-ion strike in a 1 µm CMOS technology and a 90 nm CMOS technology [Da07a]. The width of the electron-hole cloud is technology independent; however the electron-hole cloud spans multiple charge collection terminals in the advanced technology, resulting in the potential modulation of many junctions and current transients at multiple locations.

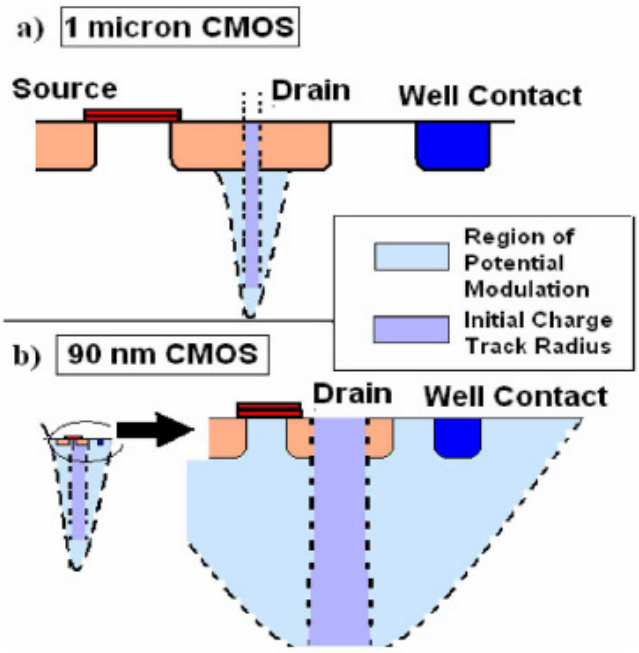


Fig. III-16. Relative range of the electron-hole cloud in a 1 µm and a 90 nm technology. Top figure (a) shows the electron-hole cloud creating a potential perturbation only on a small portion of the drain. Bottom figure shows a strike with the same radius covering the source, drain and well contact [Da07a].

An additional mechanism that can result in multiple node charge collection is illustrated in Fig. III-17 where a proton collides with a single sensitive volume of bulk silicon, producing secondary particles including a 14 MeV oxygen ion, a proton, gamma

rays, and alpha particles. In this case the heavy oxygen ion continues to transverse six additional sensitive volumes of silicon, depositing between 30 fC and 40 fC of charge within each volume [Ti06]. This type of multiple-bit-upset, along with those resulting from charge collection by diffusion of charge to nodes within proximity of the strike, are expected to increase with scaling and are progressively more important for full SE characterization.

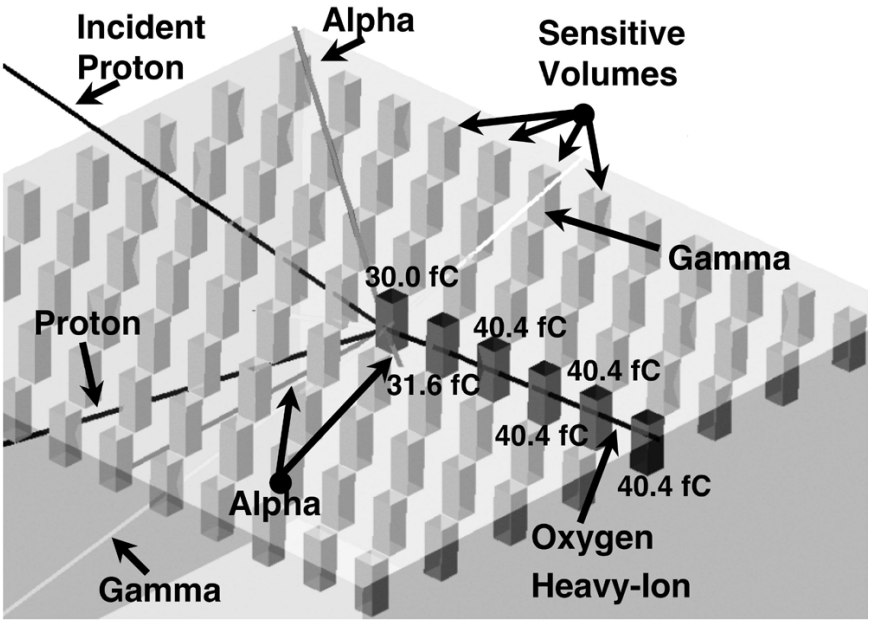


Fig. III-17. Simulated nuclear event with a 63 MeV incident proton. Proton interacts with a silicon nucleus producing secondary particles including a 14 MeV oxygen ion, a proton, gamma rays, and alpha particles. The heavy oxygen ion transverses six sensitive volumes, which collect between 30 fC and 40 fC each [Ti06].

Single-Event Effects

Excess carriers collected as charge on circuit nodes through the previously described mechanisms can result in multiple types of SEEs. Some SEEs are destructive and can lead to catastrophic system failures. These permanent SEEs (i.e., hard errors), such as

single-event burnout (SEB), single-event gate rupture (SEGR), and single-event latchup (SEL), will not be discussed in detail in this work; however, various references are provided for the interested reader [Do99, Ga96, Jo96b, Wa86].

Single-ion perturbations in CMOS electronics commonly manifest as temporary (i.e., soft error) errors. One type of effect resulting from SEs in an IC is a single-event transient (SET). SETs are undesirable asynchronous electrical pulses that can propagate through signal paths and result in a variety of erroneous circuit responses. In digital circuits, an SET can result in a single-event upset (SEU), that is, an alteration of the state of memory circuits (*e.g.* a memory cell can be changed from a logic "0" state to a logic "1" state). Similarly, a multiple-bit upset (MBU) may occur if the ion perturbs multiple nodes within the circuit. The SEU/MBU can lead to a circuit error if the corrupted data propagates throughout the circuit and is observable at the output. In analog and mixed-signal circuits, however, there exists no standard metric for soft errors, as the effect of a single-event is dependent on the circuit topology, type of circuit, and the operating mode.

Conclusion

This chapter presents a brief introduction into the primary space radiation environments that are of particular concern for SEEs in microelectronic circuits. Additionally a background of the basic charge generation and collection mechanisms following the interaction of ionizing particles with semiconductor material is presented. Finally, various SEEs are discussed with an emphasis on SETs. The remainder of this work will be focused on SETs, specifically in mixed-signal phase-locked loop circuits.

The following chapter will describe SETs in digital and analog electronics, as well as various methods for modeling SETs in circuits.

CHAPTER IV

SINGLE-EVENT TRANSIENTS

Introduction

The previous chapter describes the radiation environments and the processes that lead to charge generation and collection following the impact of an ionizing particle with a semiconductor device. Following a particle strike near or at a junction, charge can be collected and manifest as a single-event transient (SET) – an undesirable asynchronous electrical pulse at an IC node that competes with the legitimate signals propagating through a circuit or perturbs the functionality of the circuit. If the SET characteristics (amplitude and width) exceed the circuit tolerances, the SET can propagate through signal paths and result in a variety of erroneous circuit responses. SETs can occur in digital and analog circuit topologies and are termed digital single-event transients (DSET) and analog single-event transients (ASET), respectively. This chapter is devoted to discussing details on modeling SETs in circuit and device simulators. Additionally, ASETs and DSETs that are of particular concern to the mixed-signal phase-locked loops presented in later chapters will be discussed.

Modeling Single-Event Transients

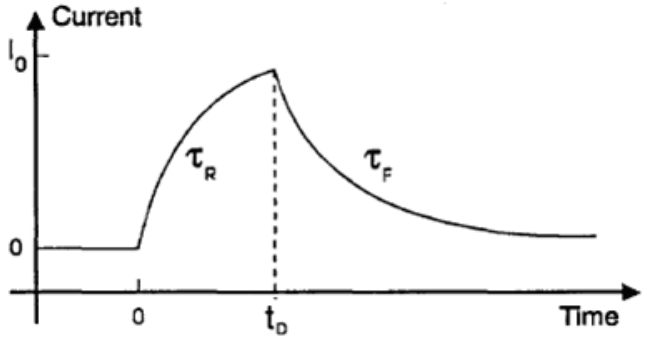
Since spacecraft malfunctions (NASA's TOPEX/Poseidon satellite in 1992 [Bu05, Ko93]) were first attributed to SETs, the SET phenomenon has been widely researched through both experimental and simulation efforts. The increased interest in SETs can be

attributed to three main factors. First, the LET threshold (minimum LET for which SETs can be observed) for SET generation is low; heavy-ions with an LET as low as 1 MeV-cm^2/mg can generate SETs in certain analog circuit configurations, thus allowing for a large number of heavy-ions being capable of creating SETs [Ko93]. Second, SETs have been observed with amplitudes spanning the power supply rails (or greater) and durations as long as milliseconds [Bo04b]. Finally the energy threshold (minimum particle energy required for SET generation) is low; protons and even alpha-particles have been shown capable of generating SETs in advanced CMOS electronics [Bu05, Ga08].

In recent years, heavy-ion broadbeams [Sa03], ion microbeams [Pe02], and several types of lasers [Bo04b, Bu87, Lo07b, Mc03, Po99] have been used to characterize SETs in ICs. Additionally, with increasing computing capabilities, recent works have shown the feasibility of computer models and device-, circuit-, and system-level simulations for predicting SETs in advanced IC designs, as well as the ability to identify many aspects that experimental testing alone does not provide [Bo04b, Bo06, Lo06, Lo07a, Lo07b]. As SETs in complex ICs may be simulated and analyzed quickly before experimental testing, it is crucial that we have descriptive and accurate models for the analyses. Modeling and simulation tools for predicting and analyzing SETs in ICs include: circuit simulators for modeling the circuit response to SEs, device simulators for modeling the interaction of the generated charge with the semiconductor device, mixed-mode simulators (a hybrid of circuit- and device-level simulators), and error rate predicting codes. The following sections discuss circuit-level and mixed-mode simulators for their pertinence to this work.

Circuit-Level Simulations

Though many circuit simulators exist, this work utilizes the Cadence Virtuoso Spectre simulator exclusively. All work was performed using the IBM 130 nm 8RF and 90nm 9SF PDKs for simulating complex designs at the transistor level. All transistor and device models were calibrated to experimental device parameters as will be discussed in later chapters.



$$I(t) = \begin{cases} I_o\left(1 - e^{-t/\tau_R}\right) & ; \ t < t_D \\ I_o\left(1 - e^{-t_D/\tau_R}\right) e^{-(t-t_D)/\tau_F} & ; \ t > t_D \end{cases}$$

$$Q = I_o\left[t_D + \tau_F - \tau_R - (\tau_F - \tau_R) e^{-t_D/\tau_R}\right]$$

Fig. IV-1. The double-exponential current pulse model used for circuit-level simulations of radiation-induced photocurrents. Also shown are the piece-wise equations directly compatible with SPICE-level circuit simulators. The total charge (Q) delivered by the current pulse is obtained by integrating $I(t)$ over time, t [Ma93].

The most common approach for representing the radiation-induced photocurrents in a circuit-level simulation is a double-exponential current source, and was developed by

Messenger in 1982 [Me82]. Fig. IV-1 shows the double-exponential current profile, along with the SPICE-compatible equations of a piece-wise exponential function [Ma93]. The current profile can be compared to the typical photocurrent shape shown in Fig. III-15.

In order to implement the current profile(s) in a circuit-level simulator, current sources may be placed across the junction terminals, as in Fig. IV-2 [We02]. The use of a current source simplifies the charge collection process (a given ion penetrates the device to a certain depth, depositing a certain amount of charge that can be collected at a junction), while still maintaining the total charge collected over time.

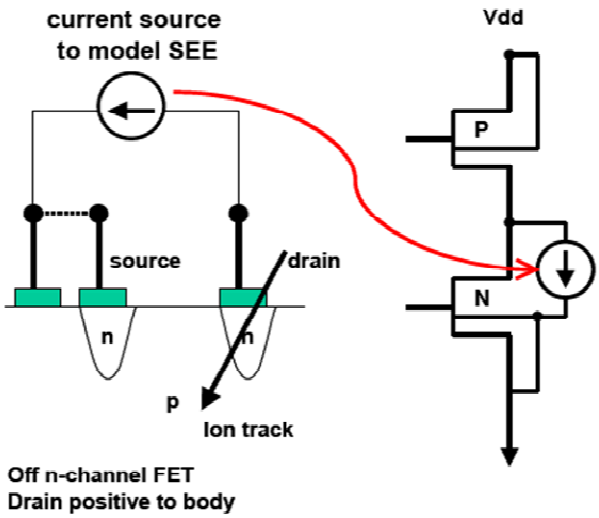


Fig. IV-2. Placement of current sources to model the radiation-induced photocurrents (after [We02]).

Mixed-Mode Simulations

DasGupta, *et. al.* recently suggested that while the double-exponential profile adequately models the radiation-induced photocurrents in older technologies, the model

may not accurately predict the SE current pulse generated from particle interactions (large LET values) in advance sub-100 nm technology nodes [Da07a, Da07b]. In order to obtain tolerable current models in deep sub-micron technologies, two types of mixed-mode simulations may be performed: decoupled and coupled.

The current profiles in decoupled mixed-mode simulations may be extracted from device-level simulations and imported into the circuit-level simulator as a current source. The most common decoupled technique involves the 3D TCAD simulation of a single transistor loaded either by an *RC* time constant or a minimum sized inverter. The single device is connected to compact models calibrated to the PDK for a given technology, as in Fig. IV-3. Following the simulated ion strike, the current profile at the irradiated node is extracted from the 3D TCAD simulation and imported as a current source in a circuit-level simulation. The imported current source is connected to the circuit as described in the previous section discussing the implementation of the double-exponential current source model.

While the decoupled mixed-mode technique preserves the physics within the single device, any larger scale effects that may impact multiple devices, such as the potential collapse within the substrate, are not captured by the technique. Also, the decoupled technique assumes that the loading for the struck device remains constant. Furthermore, for ICs where transistors of varying device dimensions are used, the SE current profiles for each device may be necessary. Using a single current profile for multiple device dimensions and loading may be adequate depending on the circuit's level of complexity; however, in many analog and mixed-signal designs the device dimensions vary widely. In order to fully characterize each node, decoupled mixed-mode simulations should be

performed for every device and loading combination in the circuit. However, simulating all devices and loading combinations typically requires large amounts of computing time and therefore may not be feasible. Each current profile used in this work is therefore an approximation based on the minimum device dimensions and standard loading.

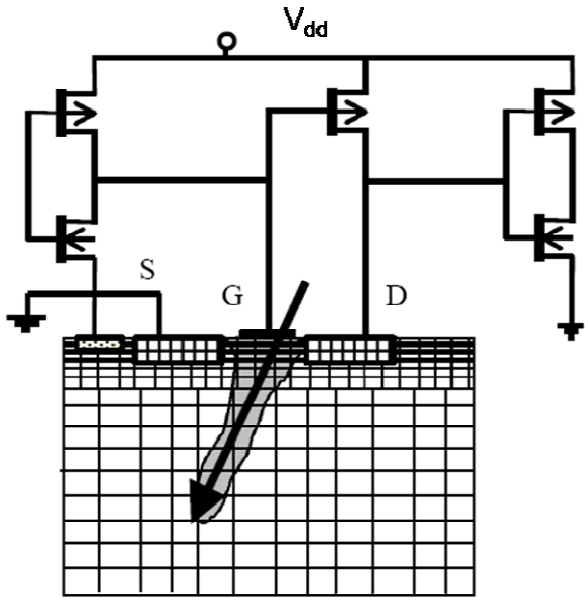


Fig. IV-3. Mixed mode device/circuit simulation (after [Bu01]).

Coupled mixed-mode simulations allow for device-level interactions while maintaining the integrity of the circuit operation. In coupled mixed-mode simulations, the 3D TCAD device is electrically connected to the calibrated compact models for the entire circuit, rather than importing the current profile into a circuit-level simulator as in the decoupled mixed-mode approach. For small digital circuits this approach is ideal as the simulation can characterize effects such as a substrate potential collapse across multiple devices. However, for large-scale analog electronics with varying device

dimensions this approach is currently computationally infeasible. The following sections discuss analog and digital single-event transients that are of particular concern to the phase-locked loop circuit presented in later chapters.

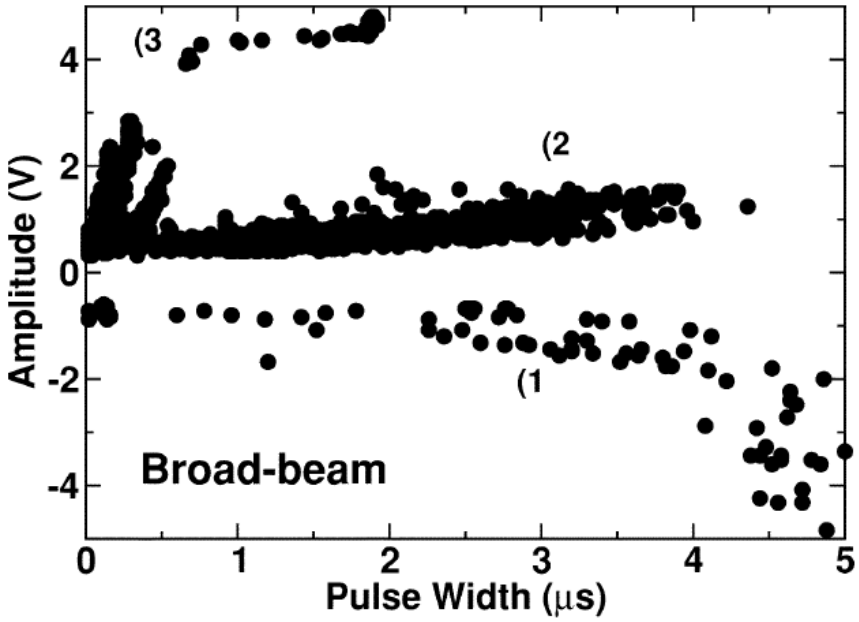


Fig. IV-4. Amplitude versus time-width (at full-width at half-maximum of amplitude) of an SET observed at the LM124 output. The ions used during the broad-beam experiment are 100 MeV Br, 150 MeV Mg, and 210 MeV Cl. The corresponding LET values of the ions used are 38.6, 6.25, and 11.5 MeV-cm^2/mg, respectively [Bo02].

Analog Single-Event Transients

Since the radiation effects community has recognized analog single-event transients (ASET) as a significant source of various anomalies in space missions, there has been an increased interest in SETs in analog topologies such as voltage comparators, operational amplifiers, voltage references, DC/DC converters, voltage-controlled oscillators, and phase-locked loops [Ad00, Bo04a, Bo05, Bo06, Bo04b, Ch03, Ch06b, Ch07, Ch06a, Ec94, Jo96, Jo00a, Jo02, Jo00b, Ko00, La02, La06, Lo06, Lo07a, Lo07b, Lo07c, Lo08,

Lo09, Pe01, Pe02, Sa02, Sa03, St02b]. Part of the challenge in characterizing and hardening against ASETs is the widely varying amplitudes and widths that can occur in the various topologies, as the ASET characteristics typically depend not only on the ion and LET value, but the circuit node and state as well. Fig. IV-4, for example, shows a scatter plot of ASET amplitudes versus time-width (at full-width at half-maximum of amplitude) for heavy-ion experiments on an LM124 operational amplifier [Bo02]. The figure shows the wide range of amplitudes and pulse widths observed, identifying three specific trends: 1) slowly increasing transients with negative amplitude, 2) slowly increasing with positive amplitude, and 3) quickly increasing with positive amplitude and a saturation effect.

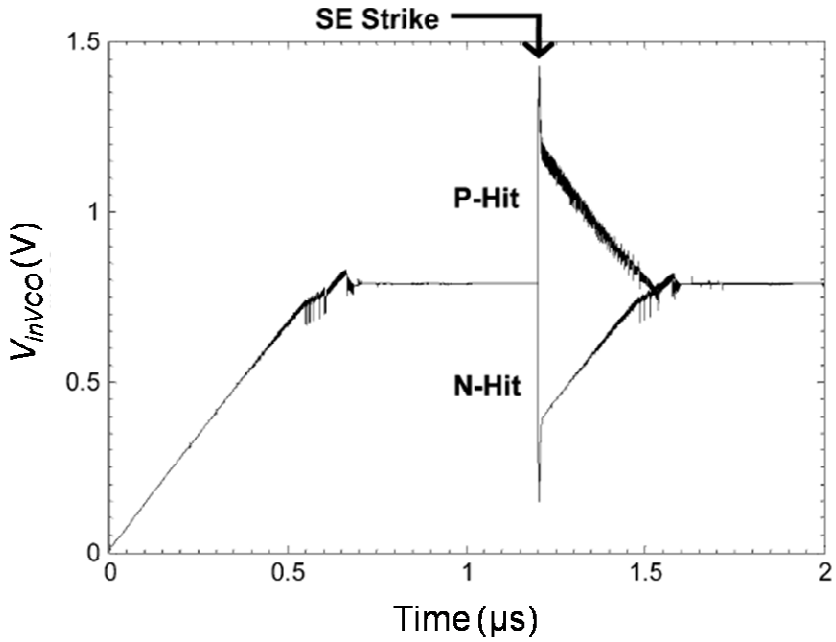


Fig. IV-5. Input of VCO (V_{inVCO}) vs. time for PLL at 700 MHz operation. Simulated SE strikes occur at 1.2 µs and span over approximately 280 clock cycles, lasting over 500 ns. The P-Hit curve represents the response of a strike on a pMOS device, whereas the N-Hit curve represents the response of a strike on an nMOS device [Lo06].

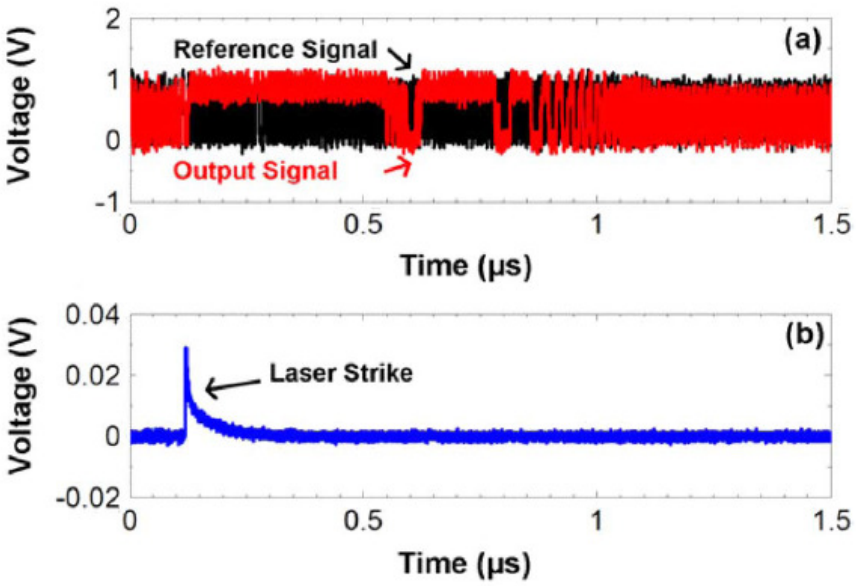


Fig. IV-6. (a) The reference and output signals versus time following a laser strike of incident energy 30 nJ in the charge pump component of the PLL at 200 MHz. (b) Voltage representation (output of diode detector) of the laser strike [Lo07b].

Additional analog topologies, however, may have different ASET characteristics. Fig. IV-5 illustrates a simulation showing two types of transients that can occur on the voltage-controlled oscillator's (VCO) input within the phase-locked loop (PLL) circuit [Lo06]. The simulated transients are generated following an ion strike depositing 200 fC of charge on the output node of the charge pump sub-circuit. The transients reach 640 mV in amplitude and last approximately 400 μs, spanning over 280 clock cycles [Lo06]. These large voltage transients ultimately manifest as frequency modulations at the PLL output and can affect the integrity of the systems for which the PLL is a part. Fig. IV-6 illustrates an experimentally captured transient within the output signal of a PLL designed in the IBM 130 nm 8RF technology [Lo07b]. The frequency transient is a manifestation of a similar voltage transient to that shown in Fig. IV-5. The experimental transient was captured through the use of a two-photon absorption laser [Bo86, Mc02,

Mc03, Mc07, St85] technique by striking an nMOS device within the charge pump sub-circuit [Lo07b].

Figs. IV-4, IV-5, and IV-6 show some examples of various ASETs that can be generated within a single analog topology. As each topology can impact the characteristics of the ASETs generated, and each application typically has individual upset thresholds, it is important to fully characterize the transient response for each circuit and its application. Additionally, mixed-signal topologies, such as the PLL, may also include some digital components that may impact the overall SET vulnerability of the IC. The next section is devoted to examining digital single-event transients (DSET) and their relationship to soft error generation within digital and mixed-signal topologies.

Digital Single-Event Transients

Single-event transients (SET) in digital microelectronics have generally received less attention at the device level over ASETs, although in recent years DSETs have been of particular interest. In 0.25 μm technologies and older the error rates for digital electronics have been dominated by single-event upsets (SEU). With the decreasing feature sizes and increasing operating frequencies, however, SETs are expected to dominate the soft error rates for space-deployed electronics systems [Ma02, Mc07]. Moreover, the overall error cross-sections in advanced deep submicron CMOS technologies have been shown to increase for increasing operating frequencies due to DSETs in latches [Be04].

Similar to the transients in analog topologies, DSETs are spurious electrical signals that can propagate through signal paths and result in a variety of erroneous circuit

responses. In digital circuits, an SET can result in a single-event upset (SEU), that is, an alteration of the state of memory circuits (*e.g.* a memory cell can be changed from a logic "0" state to a logic "1" state). The SEU can lead to a circuit error if the corrupted data propagates throughout the circuit and is observable at the output. These upsets are often termed "soft errors" as they do not result in permanent failures within the circuit. With increasing operating frequencies, SETs are more likely to result in SEUs because the SET time-widths span a larger portion of the operating period, thus increasing the window of vulnerability for upset. This effect is illustrated by the increase in SEU cross-section for various frequencies, as in Fig. IV-7 where the heavy-ion SEU cross-sections for dual interlocked cells (DICE) designed in a 180 nm technology are shown for frequencies varying from 10 MHz to 300 MHz [Ga04]. The cross-section, thus the error rate, increases with increasing frequency.

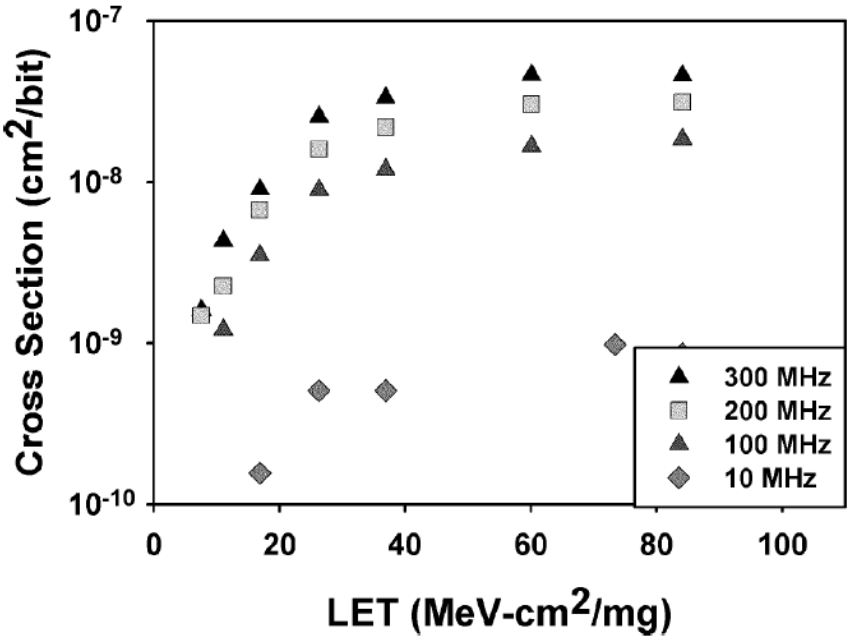


Fig. IV-7. Data from a 0.18 μm DICE latch showing the frequency dependence on the cross section [Ga04].

The increasing sensitivity of ICs to SETs with increasing frequency and decreasing feature sizes presents numerous challenges for future technology nodes. Also, in mixed-signal technologies where DSETs and ASETs can result in a wide variety of circuit responses, the characterization of complex microelectronics in advanced technologies requires novel analyses, simulation, and testing techniques in order to ensure the reliability and integrity of the designs for radiation environments. The next chapter discusses various novel analysis techniques and designs for un-hardened and radiation-hardened PLL circuits, as well as simulation and experimental verification of each design.

Conclusion

As SEUs have been shown to account for over 84% of all radiation effects observed in space-deployed systems [Ko99, Ma02], and SETs are suspected to become the dominant contributor to SEUs in advanced microelectronics [Ma02, Mc07], it is crucial that reliable models for SET generation and propagation exist for digital and analog topologies. This chapter is devoted to describing early and recent developments for SET modeling in circuit and device simulators. Also discussed are the various impacts SETs can have on various testing approaches and the overall error-rates of the systems in-flight. The following chapter utilizes the simulation techniques presented throughout this chapter in order to analyze the various SETs that are of concern to mixed-signal PLL topologies. Additionally, hardening approaches for each sub-circuit (if necessary) in the PLL will be presented along with any experimental results corroborating the developed models and simulations.

CHAPTER V

SINGLE-EVENT EFFECTS IN UNITY GAIN PHASE-LOCKED LOOPS

Introduction

In this chapter, the SET performance of a general unity gain PLL circuit is analyzed through the use of simulations and targeted two-photon absorption (TPA) laser experimentation [Bo86, Lo07b, Mc02, Mc03, St85]. PLLs were designed using the IBM 130 nm 8RF CMOS PDK and fabricated through the MOSIS foundry system. Table V-1 shows the simulated and tested frequency specifications for each PLL discussed throughout this chapter.

TABLE V-1
PLL GENERAL DESIGN SPECIFICATIONS

PLL Type/Name	Technology	Design Specifications: Parameter	Simulated	Measured
Current-based CP PLL / CPLL	130 nm	Center Frequency (fc)	400 MHz	200 MHz
		Frequency Range	50-850 MHz	40-550 MHz
Voltage-based CP PLL / VPLL	130 nm	Center Frequency (fc)	400 MHz	200 MHz
		Frequency Range	50-850 MHz	40-600 MHz

Experimental testing was performed using a two-photon absorption (TPA) laser technique [Bo86, Mc02, Mc03, St85] on the PLL circuits for single-event upset (SEU) mapping and SET error signature characterization. SEU mapping is used to quantify the vulnerable areas of each PLL sub-circuit, indicating an approximate 99% reduction in the sensitive area of the radiation-hardened-by-design (RHBD) charge pump over the

conventional design. Second, analysis of the measured PLL output error signatures is used to quantify the relative hardness of PLL circuits implementing a voltage-based charge pump (V-CP) over a design implementing a current-based charge pump (C-CP), demonstrating 2.3 orders of magnitude improvement in SE tolerance. Further, demonstration of the SE sensitivity of the integrated voltage-controlled oscillator (VCO) and phase-frequency detector (PFD) is investigated [Lo07b].

PLL Circuit Description

Two PLL topologies were designed for this work using the IBM 130 nm 8RF CMOS technology available through the MOSIS foundry. Similar to the PLLs presented in chapter II, both PLLs consist of four primary components: the phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), and voltage-controlled oscillator (VCO), as shown in Fig. II-11. Buffers were included subsequent to the VCO module to account for loading effects. The first PLL was implemented with a conventional C-CP while the second PLL was implemented with an RHBD V-CP. Finally, both PLLs employed a feedback factor of 1 such that the PLL was in a unity gain configuration.

Charge Pump Designs

The C-CP, schematically represented in Fig. II-17(a), was designed to source/sink 2 μA of current upon receiving a signal on the UP/DOWN signal lines. Due to the fixed current sourcing/sinking capability of such a charge pump, the removal time of collected charge due to an SE hit is directly proportional to the total charge deposited. This results in long recovery times, and higher vulnerability of this type of design for heavy ion

exposure. This type of charge pump is typically used because of the high linearity and power supply noise rejection. However, previous works have shown that the C-CP is the most sensitive PLL sub-circuit to SEs [Bo06, Lo06, Lo07a].

Recent work with circuit-level simulations has suggested a voltage-based charge pump (V-CP) for improved SE tolerance [Lo06, Lo07a]. The V-CP and LPF, schematically represented in Fig. II-17(b), was designed such that the input to the LPF is switched between V_{dd} and GND. In contrast with the C-CP, current to/from the LPF depends directly on the control voltage of the VCO (V_{inVCO}) and the RC time constant of the LPF. As described in [Ga80, Lo06, Lo07a], although the V-CP is more sensitive to power supply variations than the C-CP module, numerous advantages are gained. First, the RHBD V-CP reduces the number of vulnerable nodes present in the charge pump. Second, as the rate of charge sourcing and sinking is increased, a faster acquisition/recovery time can be achieved. Additionally, the operational performance can be improved (i.e. an increased natural frequency, improved damping, increased loop bandwidth) while reducing the vulnerability of the charge pump to SEs. Finally, the RHBD V-CP provides a mechanism (the addition of the resistor R_1 in the LPF) to isolate the vulnerable output node of the charge pump from the control voltage of the VCO [Lo06, Lo07a].

Simulation Study of Single-Event Transients in the PLL

As discussed, previous works have shown that the SET response of the PLL is dominated by the SET response of the charge pump module [Bo06, Lo06, Lo07a]. Fig. IV-4 (see Chapter IV) displays two simulated transients occurring on the input

voltage of the VCO as a result of strikes on pMOS (P-Hit) and nMOS (N-Hit) devices depositing 200 fC of charge in the C-CP module. The simulations were performed using the CADENCE EDA tool suite, the SPECTRE environment, and calibrated IBM 130 nm 8RF device models. Charge collection from heavy-ion strikes were simulated using a double exponential current source injected into the circuit with time constants calibrated to the drift and diffusion processes affecting the free-carriers in the technology nodes of study [Bo06, Lo06, Lo07a]. The transients last approximately 500 ns and result in approximately 120 erroneous clock pulses [Lo06, Lo07a]. Similar hits in hardened PLL designs result in only a few erroneous clock pulses.

An additional metric that can be useful in examining the response of the PLL to SEs is the amount of phase displacement present in V_{outVCO}. The phase displacement is the amount of phase shift that occurs in the output of the PLL. For the SE strike to cause an erroneous pulse a phase displacement of at least 2π radians (360 degrees) must occur. Fig. V-1 shows that the accumulated output phase displacement (the phase shift present in the output signal with respect to the ideal reference signal) resulting from strikes within the PLL can be reduced by approximately two orders of magnitude by implementing the RHBD V-CP module [Lo06, Lo07a]. Also shown in Fig. V-1 is the output phase displacement versus frequency for simulated ion strikes in the VCO. These simulation results are verified experimentally using laser exposures and are presented in the following sections.

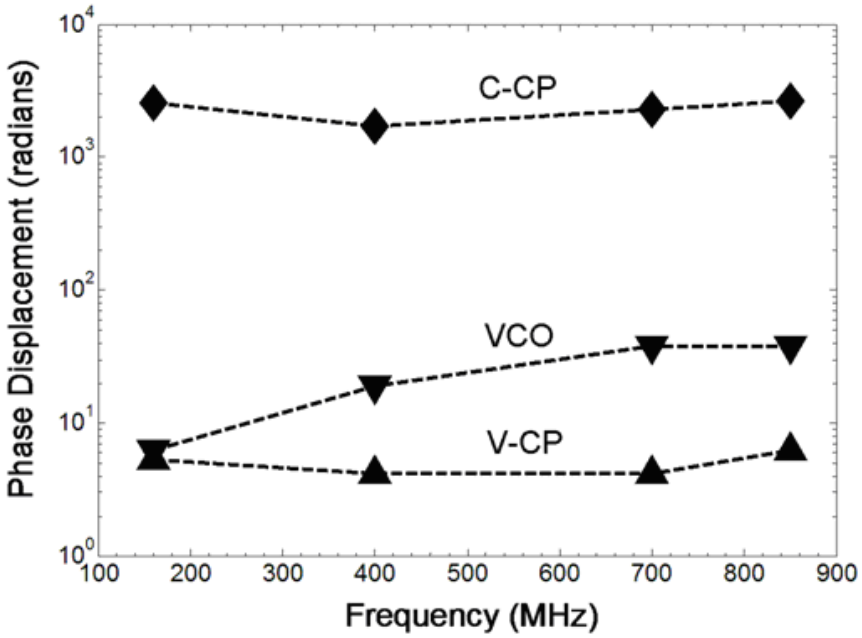


Fig. V-1. Simulation results showing the maximum phase displacement vs. frequency for SE strikes depositing 500 fC of charge in the C-CP, VCO, and V-CP. At least 2 orders of magnitude improvement is achieved by the V-CP over the C-CP [Lo06, Lo07a].

Laser Two-Photon Absorption Experimental Details

Recently, a method of laser-induced carrier generation for single-event effects (SEE) applications based on two-photon absorption (TPA) using high peak power femtosecond pulses at sub-bandgap optical wavelengths has been demonstrated [Mc02, Mc03]. A primary motivation for the development of the TPA SEE technique is its ability to interrogate SEE phenomena through the wafer using backside irradiation. This eliminates interference from the metallization layer stacks that are prevalent in modern devices, and circumvents many of the testing issues associated with flip-chip-mounted parts. In this paper, the through-wafer TPA SEE technique is used to perform SEU mapping of the PLL circuits, and to investigate and characterize the SET response of PLL circuits.

The TPA SEE experimental setup is described in [Mc02, Mc03]. The device under test (DUT) was mounted on a motorized xyz translation platform with 0.1 μm resolution. Optical pulses are focused through the wafer onto the front surface of the DUT with a 100x microscope objective, resulting in a near-Gaussian beam profile with a typical diameter of approximately 1.6 μm at focus [Mc02]. Because the carrier deposition varies as the square of the irradiance (I^2), where I represents the laser pulse intensity [Bo86, Mc02, St85], this corresponds to a Gaussian carrier density distribution with an approximate diameter of 1.1 μm (full-width-at-half-maximum). All experiments were performed at room temperature.

Description of the DUT

The DUT, schematically represented in Fig. V-2, includes two PLL circuits (CPLL and VPLL) and two additional VCO circuits to serve as the reference signals. The CPLL was designed with the C-CP, whereas the VPLL implemented the RHBD V-CP. For both PLLs the reference signals (V_{REF1} and V_{REF2}) and the outputs ($V_{outCPLL}$ and $V_{outVPLL}$) are bonded to output pads. Fig. V-3 illustrates the circuit schematics of the VCO, C-CP, and V-CP and indicates the most sensitive node(s) of each design. The most sensitive nodes (as defined in [Bo05, Bo06, Lo06, Lo07a, Lo07b, Lo07c]) are represented in the schematics by laser targets consisting of 1 μm x 1 μm diffusion areas tied to the circuit nodes in the layout. The diameters of the additional diffusion areas for the laser targets were chosen to be approximately the diameter of the laser spot size (~1 μm) and were used to facilitate the SET characterization experiments. Furthermore, Fig. V-4 displays an image of the VCO circuit for the CPLL captured by the Indigo Alpha near-infrared

(NIR) focal plane array, and indicates a laser target connected to the output of a current-starved inverter stage within the VCO. Additionally, the reference clock circuit for the CPLL and some of the output buffers are also displayed in Fig. V-4.

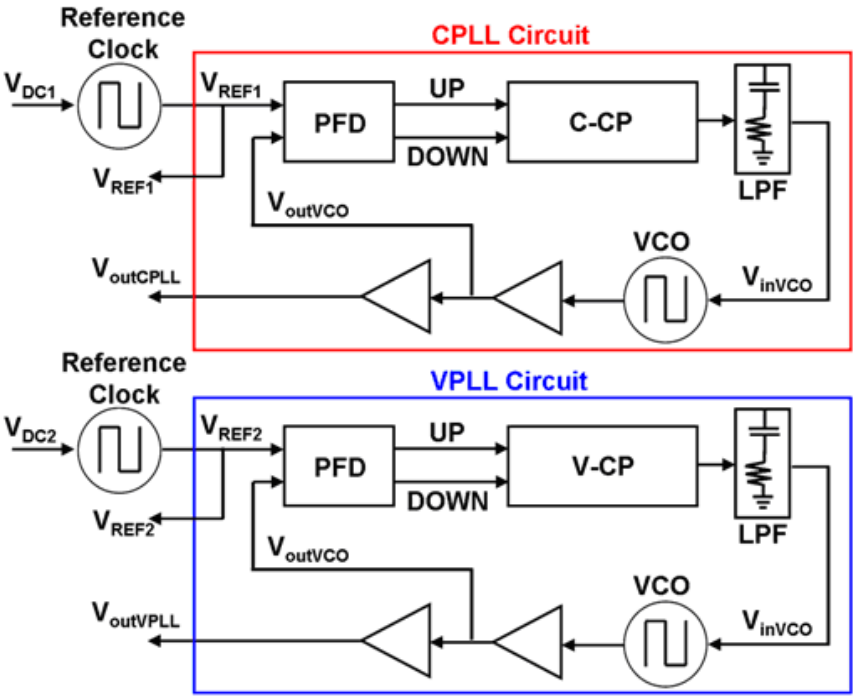


Fig. V-2. General block diagram of the DUT, including the two PLL circuits (CPLL and VPLL) and two on-chip reference clock generating circuits.

The VCO circuits for the experiments were designed to achieve a center frequency (frequency at which $V_{inVCO}=V_{dd}/2$) of approximately 200 MHz. The maximum frequency for the VCO in the PLL implementing the C-CP (*VCO a* in Fig. V-5) was measured to be approximately 530 MHz, whereas the maximum frequency measured for the PLL implementing the RHBD V-CP (*VCO b* in Fig. V-5) was measured to be approximately 600 MHz. For both PLL circuits, the locking range was between approximately 40 MHz and 350 MHz.

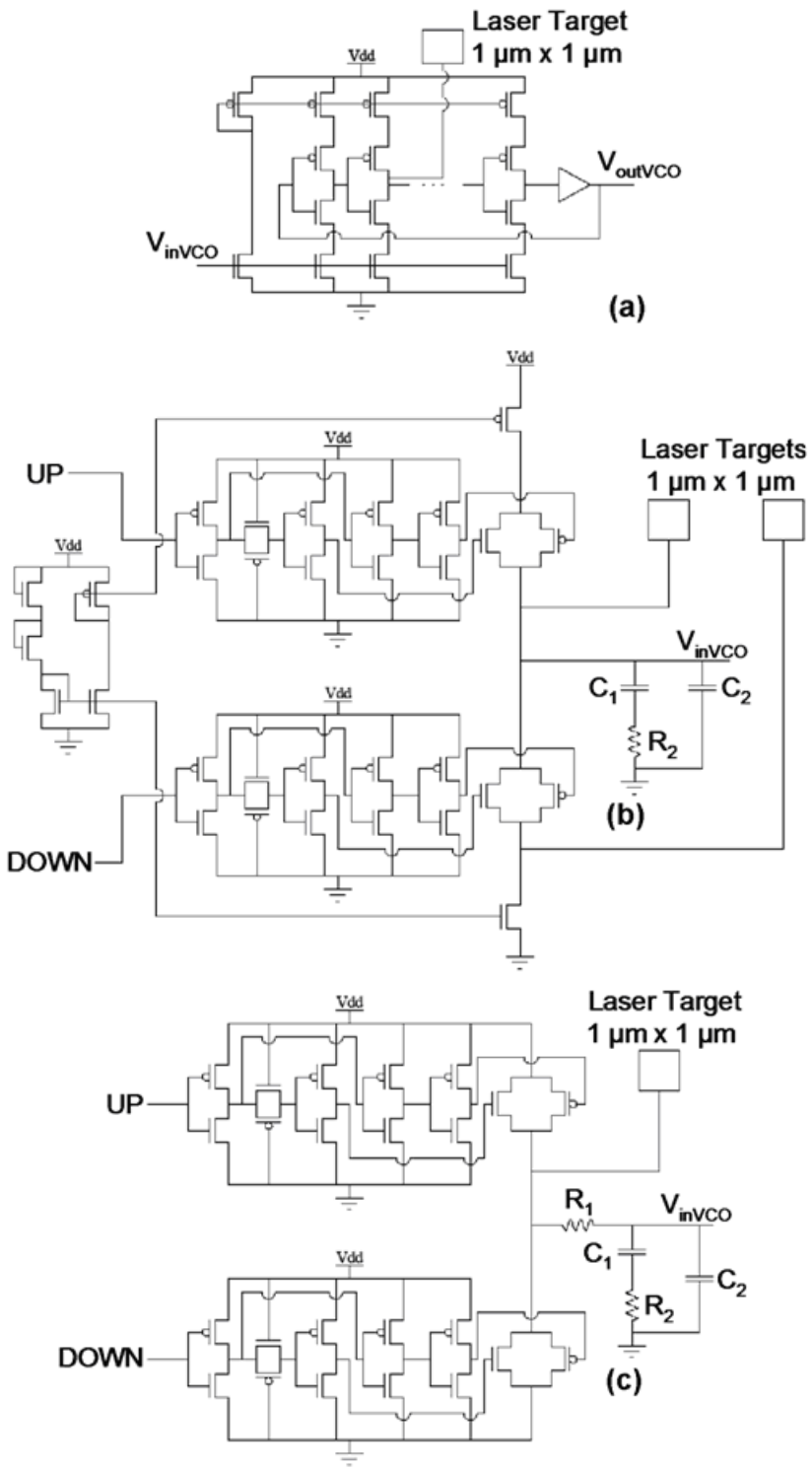


Fig. V-3. Schematics of the (a) VCO, (b) C-CP, and (c) V-CP circuits indicating the locations of the 1 µm x 1 µm diffusion areas used for the laser targets.

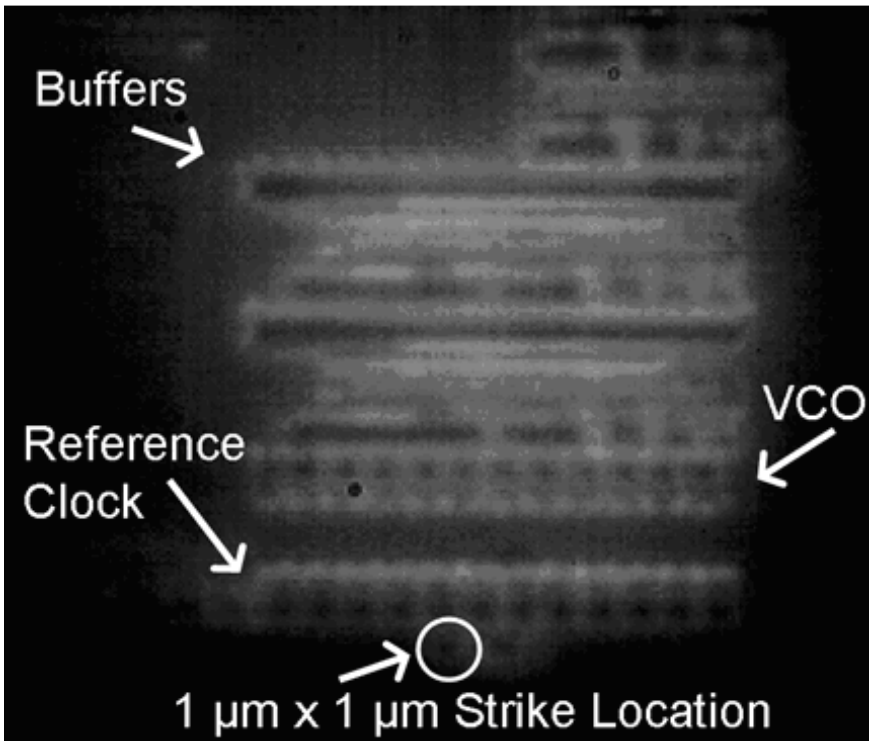


Fig. V-4. Near-infrared photo of one strike location tied to a node in the VCO circuit located in the CPLL. Also indicated is the reference clock generation circuit and output buffers.

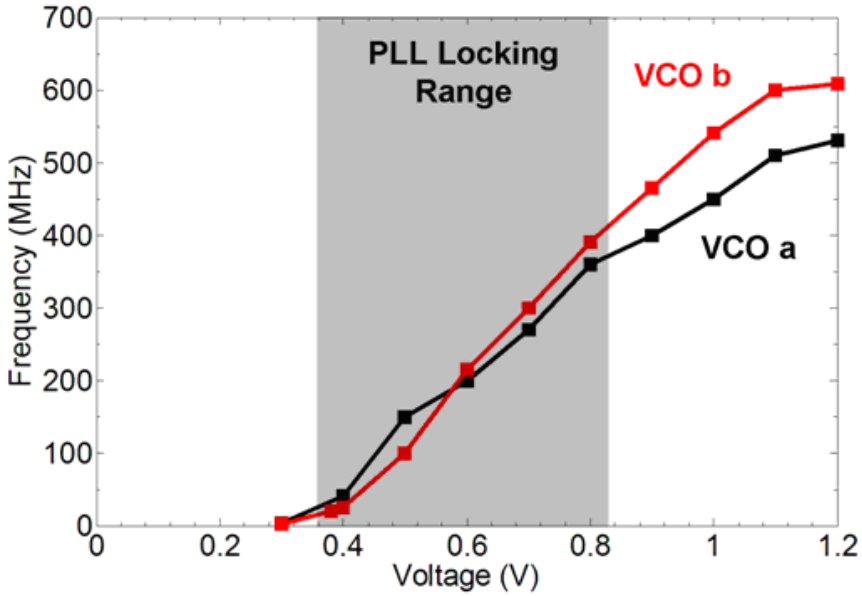


Fig. V-5. Measured transfer characteristics of the VCO circuits.

Fig. V-5 illustrates the measured transfer characteristics (output frequency versus V_{inVCO}) of the VCO circuits and indicates the PLL locking range. Although the maximum frequencies of the VCO circuits differ slightly, the operating ranges of the PLLs are closely matched and can be varied independently, thus a direct comparison between the circuits can be made.

TPA-induced SEU Mapping

Using the through-wafer TPA technique, SEU maps of the sensitive regions in the PLL sub-circuits were generated. The SEU maps display the 2-dimensional spatial dependence of the PLL error signatures that cannot be determined through the use of broadbeam heavy-ion measurements. The experiments were performed as a function of x-y location, the incident laser pulse energy, and PLL sub-circuit. For each scan the PLLs were operated at 200 MHz.

In order to quantify an SEU, the definition of a PLL upset must be established. We have defined an SEU as a single-event that resulted in a PLL loss-of-lock. However, loss-of-lock is customarily dependent on the manufacturer and the type of lock detector implemented. Table V-2 shows five sets of criteria for loss-of-lock provided by various PLL manufacturers [An06, Fr04, Ha05a, Id04] together with our criteria for loss-of-lock used to quantify an SEU. For this work, loss-of-lock was determined to occur if the phase error was greater than 2.5 ns for at least 6 cycles in a window of 160 clock pulses. In order to determine if this criteria for loss-of-lock occurred, a Tektronix-TDS6124C oscilloscope sampling at 20 GS/s was used. The trigger was setup to acquire a signal that

met the criteria for a loss-of-lock. Upon the occurrence of a triggered signal, the x-y location of the SEU was recorded.

TABLE V-2
CRITERIA FOR LOSS-OF-LOCK

Manufacturer	Frequency Range or Operating Frequency	Phase Error	Number of consecutive cycles	Window (pulses)
A	(6 MHz, 200 MHz)	30 ns	>=5	-
B	(25 MHz, 225 MHz)	540 ps	>=4	256
C	-	2.5 %	>=2	112
D[1]	(6 MHz, 100 MHz)	2 ns	>=1	-
D[2]	(100 MHz, 200 MHz)	800 ps	>=1	-
This Work	200 MHz	2.5 ns	>=6	160

Part D may function in [1]low-frequency or [2]high-frequency operating modes.

The SEU maps were generated by scanning the laser over a defined region of interest at 0.2 μm/step. The laser was operated at a 1 kHz repetition rate, and was focused on each grid point for 10 ms, thus allowing for ten laser strikes per grid point in the scan area. The 10 ms focus time for each grid point was an adjustable parameter and was chosen to ensure that the data captured by the oscilloscope and the software corresponded to the proper grid point. However, SEUs resulting from noise could also be present in the data sets. The erroneous upset signatures that could unambiguously be identified as

being in error were removed from the data. Additionally, multiple runs were performed in order to help eliminate erroneous data points resulting from noise.

For each x-y location in the grid, an upset was recorded once the criteria for a loss-of-lock were satisfied. Fig. V-6 illustrates an example of a captured SEU resulting from a strike in the C-CP sub-circuit. The PLL was operating at 200 MHz, and lost phase lock at approximately 70 ns with respect to the time origin of the image. Although the phase and frequency recovery of the reference signal cannot be visualized in Fig. V-6, phase lock was regained 420 ns following the laser strike.

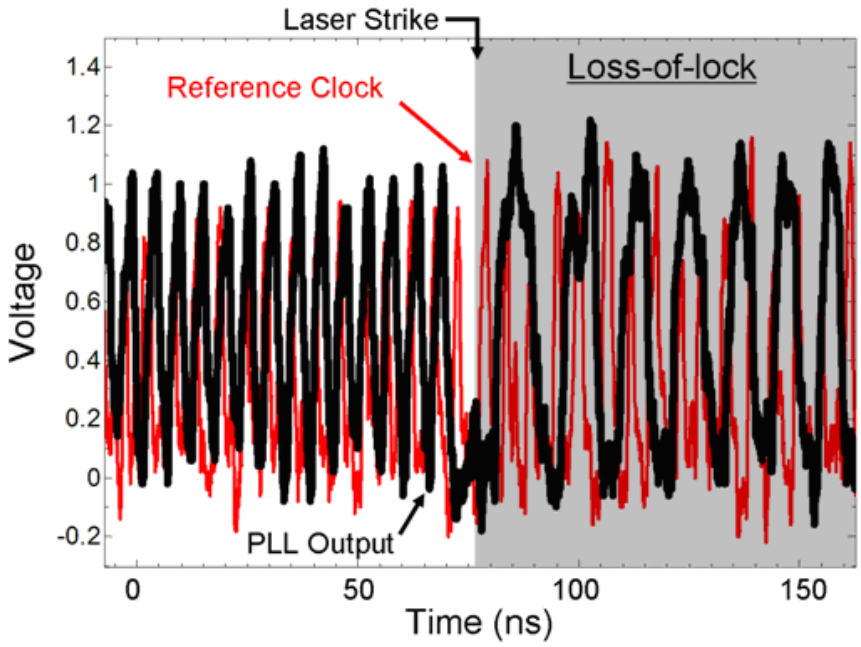


Fig. V-6. Capture of an SEU (PLL loss-of-lock) following a 70 nJ laser strike in the conventional current-based charge pump sub-circuit. The PLL was operating at 200 MHz and lost phase lock for approximately 420 ns.

SET Characterization

Additionally, the TPA technique was used to investigate and characterize the error signatures of the PLL sub-circuits. This experiment utilized the critical nodes [Lo06, Lo07a] with at least 1 μm x 1 μm diffusion areas within each sub-circuit. In contrast with the SEU mapping experiments for which the incident pulse energy was variable, all SET error signature experiments were performed for incident pulse energy of 30 nJ.

During steady-state operation, the output of the PLL is locked to the phase and frequency of the reference signal. A SE occurring within the PLL is expected to cause a temporal perturbation in the output signal [Bo06, Lo06, Lo07a]. By monitoring and comparing the reference signal to the PLL output signal, the number of erroneous (missing or additional) pulses present in the output of the PLL following a strike can be extracted.

Data were collected for a total of ten laser strikes per strike location for varying input bias conditions (V_{REF1} and V_{REF2}) representing various frequencies of PLL operation. For all strikes the reference signal and the PLL output signal were recorded following the strike until the PLL returned to its locked state. Fig. V-7 illustrates an example of the reference and output signals following a laser strike of energy 30 nJ in the C-CP component of the CPLL. The PLL loses phase/frequency lock as the output frequency is reduced following the strike. Subsequently the frequency gradually increases until the PLL returns to the locked state after 2.6 μs.

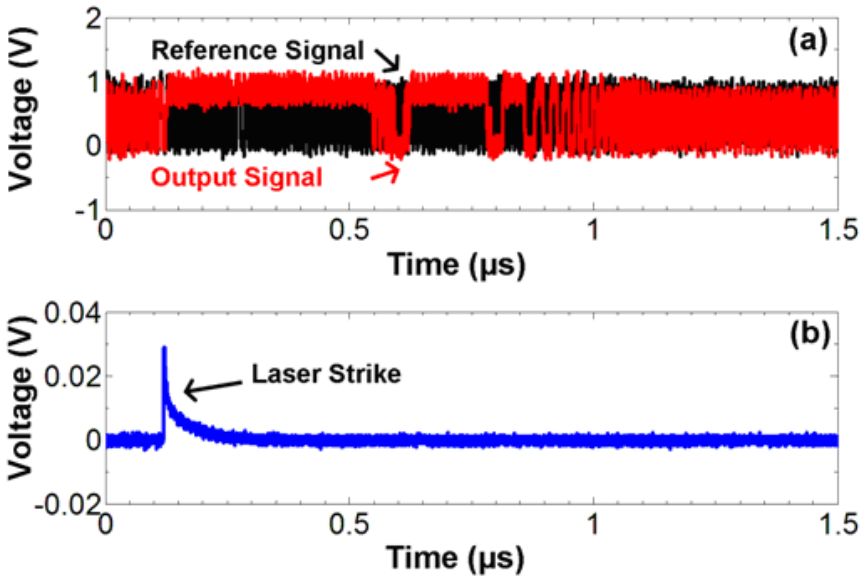


Fig. V-7. (a) The reference and output signals versus time following a laser strike of incident energy 30 nJ in the C-CP component of the CPLL at 200 MHz. (b) Voltage representation (output of diode detector) of the laser strike.

Experimental Results

TPA-induced SEU Mapping

Fig. V-8 illustrates the layout view of the VCO and indicates the input and output stages. Also displayed are the TPA-induced SEU maps of the VCO circuits for incident laser pulse energies of 1.9 nJ, 2.8 nJ, and 7.0 nJ. Laser strikes in the input bias stage, three internal nodes, and the output stage resulted in SEUs for the lowest energies tested (1.9 nJ and 2.8 nJ). Strikes in the input bias stage will alter the bias voltages applied to each current-starved inverter in the structure and thus modulate the frequency of oscillation [Lo06, Lo07a]. Therefore, almost every strike occurring within the input bias stage will result in an SEU.

Conversely, strikes occurring within the current-starved inverter structures will result in an oscillation failure depending on the drive current of the current-starved inverter and

the temporal location of the strike with respect to the oscillation cycle [Lo06, Lo07a]. In addition, a strike occurring closer to the output buffer will be more likely to result in an SEU as the transient is more likely to propagate to the output. Hence, SEUs were recorded for lower incident energy strikes in some of the internal VCO nodes and the output nodes. Furthermore, as the incident laser pulse energy was increased, the number of SEUs increased, resulting in a larger vulnerable area.

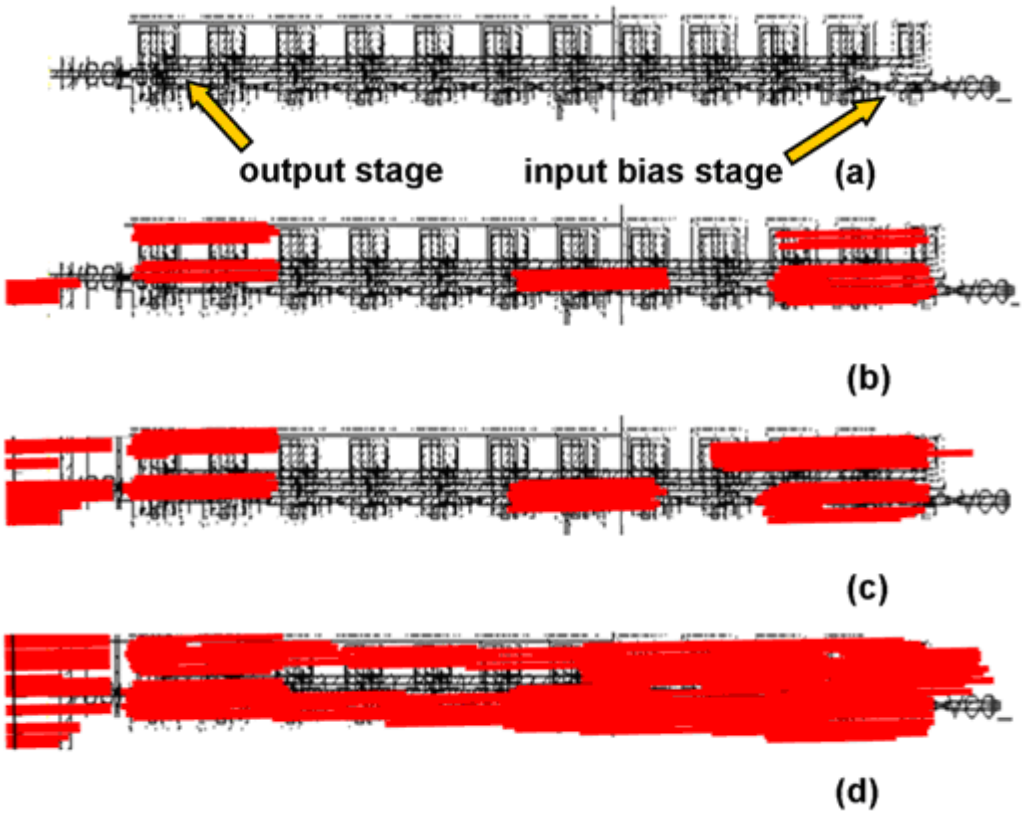


Fig. V-8. (a) The layout view of the VCO circuit indicating the input and output stages. Also shown are the TPA-induced SEU maps of the VCO circuit for incident laser pulse energies of (b) 1.9 nJ, (c) 2.8 nJ, and (d) 7.0 nJ.

Fig. V-9 illustrates the layout view of the PFD and RHBD V-CP sub-circuits. Also displayed is the TPA-induced SEU map of the PFD and V-CP circuits for incident laser

pulse energy of 7.0 nJ. No SEUs were recorded at energies below 7.0 nJ. Moreover, only strikes in the output stages of both the PFD and V-CP resulted in SEUs at the highest incident energy tested (7.0 nJ).

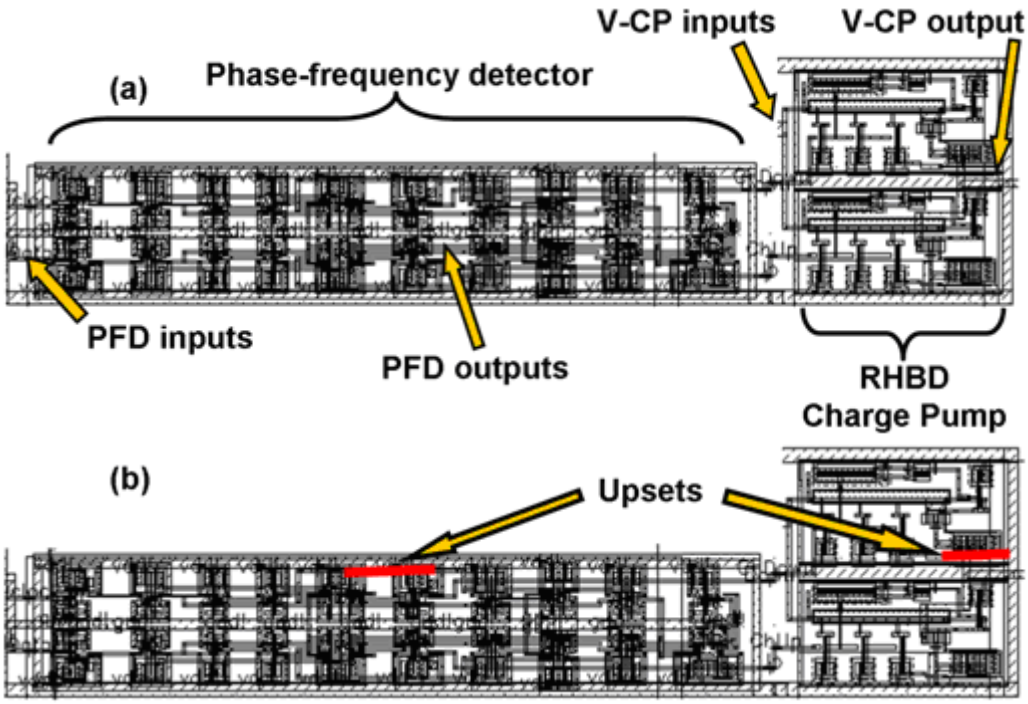


Fig. V-9. (a) The layout view of the PFD and V-CP sub-circuits. Also displayed is the TPA-induced SEU map of the PFD and V-CP sub-circuits for incident laser pulse energy of (b) 7.0 nJ.

Finally, Fig. V-10 displays the layout view of the C-CP sub-circuit. Also displayed are the TPA-induced SEU maps of the C-CP circuit for incident laser energies of 2.5 nJ, 3.7 nJ, and 7.0 nJ. Strikes at incident laser energy of 2.5 nJ in one of the output transmission gates resulted in SEUs, indicating that the output node of the C-CP is the most sensitive node. As charge is deposited directly onto the output node, the control voltage of the VCO (V_{inVCO}) is perturbed, thus altering the output frequency of the PLL

[Bo06, Lo06, Lo07a]. Additionally, as the laser energy was increased to 3.7 nJ, strikes in some of the delay inverters and delay transmission gates–located in the "dead-zone" circuitry as defined in [Bo06, Lo06, Lo07a]–also resulted in SEUs. Strikes in the delay inverters and gates alter the state of the output transmission gates, resulting in a false activation of the charge pump. Furthermore, at the highest energy tested of 7.0 nJ almost every device in the charge pump resulted in an SEU.

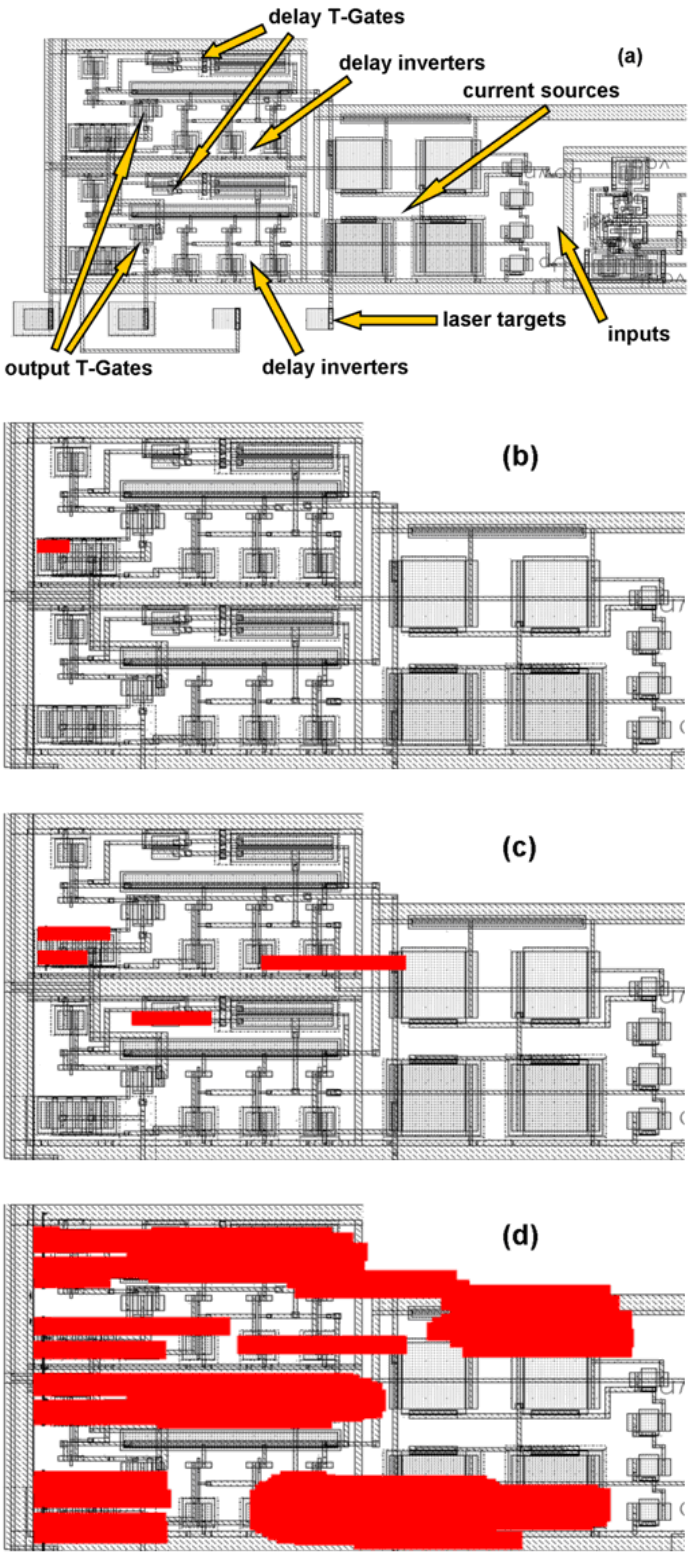


Fig. V-10. (a) The layout view of the C-CP sub-circuit. Also displayed are the TPA-induced SEU maps of the C-CP sub-circuit for incident laser energies of (b) 2.5 nJ, (c) 3.7 nJ, and (d) 7.0 nJ.

In order to quantify the results of the TPA-induced SEU maps, laser sensitive areas were calculated for each sub-circuit. The sensitive areas were calculated by multiplying the area of each grid point in the 2D scan (0.2 μm x 0.2 μm) by the number of SEUs per scan. However, as the laser spot size was on the order of 1 μm in diameter and was greater than the dimension of the scan resolution, the laser sensitive area will be an under-estimation of the true sensitive area. Therefore, we calculated error bars based on the amount of area the laser spot extended past each sensitive area. Eqn. (V-1) represents the error in the cross-section calculation for a single upset, where LS is the diameter of the laser spot in μm and SR is the scan resolution in μm.

$$e_{\text{single}} = \frac{\pi \cdot LS^2}{4} - SR^2 \tag{V-1}$$

However, when multiple SEUs are grouped together, Eqn. (V-1) cannot be used as the cross-sections for each individual SEU will overlap. Therefore, to avoid a gross over-estimation of the error in cross-section, a script was developed to account for the larger area of the laser spot size (~1 μm^2) with respect to the scan resolution (0.2 μm x 0.2 μm). Using the script to calculate the error in laser sensitive areas, Fig. V-11 displays the calculated cross-sections of each PLL sub-circuit versus the square of the laser energy, because carrier generation in the two-photon process is proportional to the square of the laser pulse irradiance (I^2) [Bo06, Mc02, St85]. Only upper error bars are included as the calculated laser cross-section is lower bounded by the 2D scan resolution.

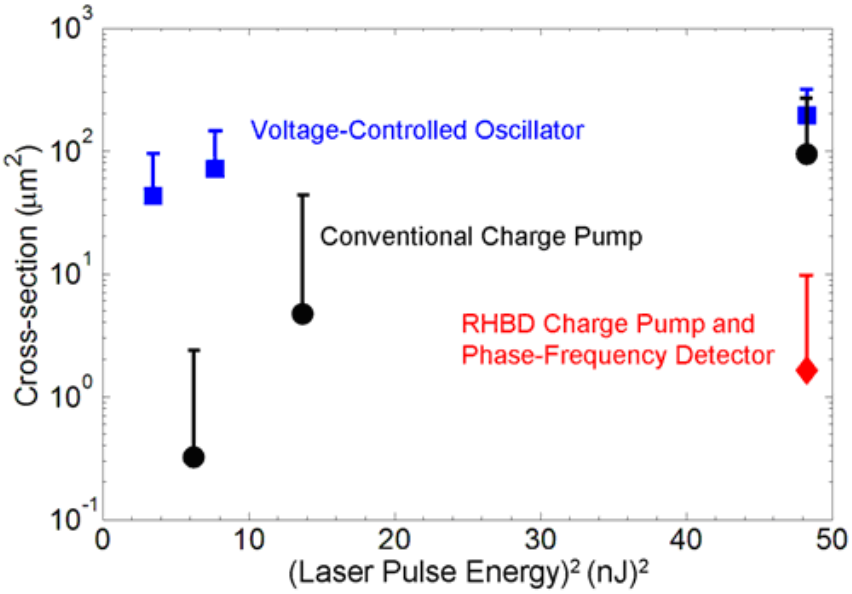


Fig. V-11. Laser sensitive area versus the square of the incident laser energy. Upper error bars were calculated from a script that accounted for the amount of additional area that the laser spot size covered over the scan resolution.

The VCO has the greatest sensitive area versus laser energy, followed by the conventional charge pump (C-CP) sub-circuit and the RHBD charge pump (V-CP) and PFD modules. When comparing the charge pump sub-circuits directly, the RHBD V-CP reduces the vulnerable area, by approximately 99%, almost 2 orders of magnitude, at 7.0 nJ. These data indicate that the VCO and C-CP modules dominate the number of SEUs that will occur in the PLL. Moreover, implementing the RHBD V-CP can significantly reduce the overall sensitive area of the PLL, reducing the total sensitive area of the PLL by approximately 32%.

PLL Error Signature Characterization

The second set of experiments examined the SET characteristics and error signatures of the PLL sub-circuits. Data were collected for 10 strikes per location per input bias

condition, and the number of erroneous clock pulses (missing or additional pulses in the output of the PLL) was calculated as a result of strikes in the various PLL components. The maximum number of erroneous pulses in the output of the CPLL and VPLL following strikes in the C-CP, VCO, and RHBD V-CP modules are displayed in Fig. V-12 as a function of the frequency of operation on a semi-log scale.

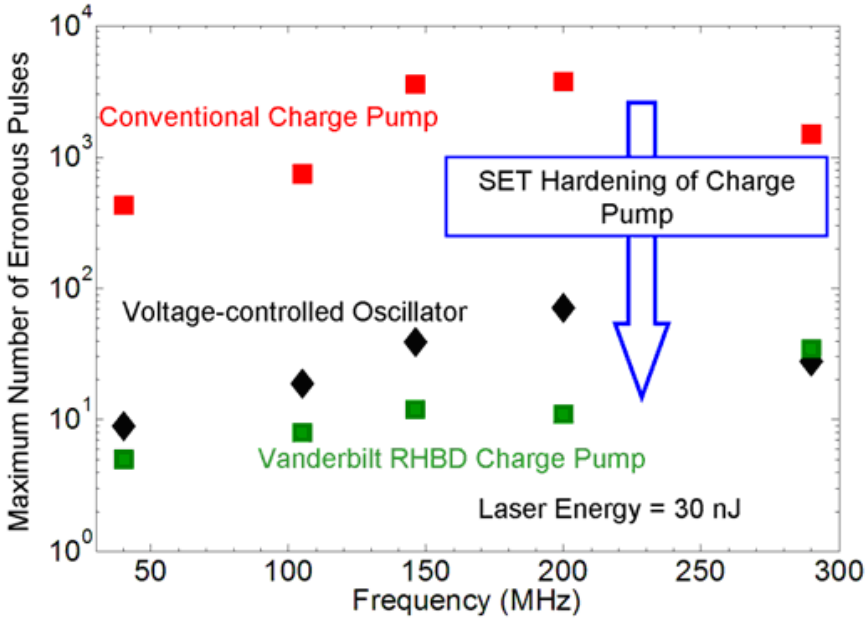


Fig. V-12. Maximum number of erroneous clock pulses versus frequency for laser strikes in various PLL sub-circuits. A maximum of 2.3 orders of magnitude improvement was achieved by the RHBD charge pump over the conventional design. The incident laser energy was 30 nJ.

Laser strikes in the C-CP result in a maximum of 2.3 orders of magnitude more erroneous pulses than strikes in the V-CP, and between 1 and 2 orders of magnitude more erroneous pulses than strikes in the VCO. This result illustrates the reduced vulnerability of the PLL implementing the V-CP over the C-CP. For the C-CP, the maximum number of erroneous pulses due to a single hit (3745 missing pulses) occurs at 140 MHz and

results from strikes on the output node. The maximum number of erroneous pulses due to a single strike in the VCO and V-CP circuits occurs at 200 MHz with 54 erroneous pulses and 290 MHz with 35 missing pulses, respectively. The average number of erroneous pulses is plotted in Fig. V-13 (note the difference in y-axis scale). In agreement with the results of Fig. V-12, the mean number of erroneous pulses is approximately 2 orders of magnitude lower for strikes occurring in the V-CP over the C-CP. Error bars represent 1 standard deviation from the mean.

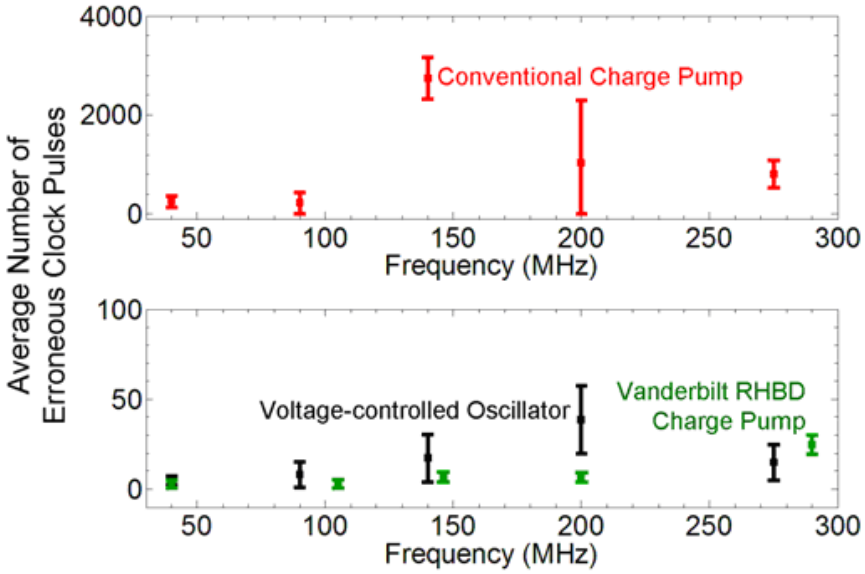


Fig. V-13. Average number of erroneous clock pulses versus frequency for laser strikes in various PLL sub-circuits (note the difference in y-axis scale). The mean number of erroneous pulses is approximately 2 orders of magnitude lower for strikes occurring in the V-CP over the C-CP at incident laser energy of 30 nJ. Error bars represent one standard deviation from the mean.

Fig. V-14 illustrates the average number of erroneous pulses for the VCO and V-CP in the VPLL circuit when operating at two different supply voltages. For the VCO, the reduction in the power supply voltage from 1.2 V to 1.0 V results in an increased

vulnerability to SEs and a decrease in the frequency of operation. Although the frequency of oscillation decreases due to the lower drive current in the VCO, the restoring drive of the VCO responsible for the SET recovery also decreases. The frequency decrease will improve the SE response because the SET width will span a smaller percentage of the PLL output pulse width, resulting in a smaller perturbation on the output. However, the overall increase in the number of erroneous PLL output pulses indicates that the reduction in drive current dominates the reduction in the frequency, and highlights the importance of drive current in determining the SET response of VCO sub-circuit.

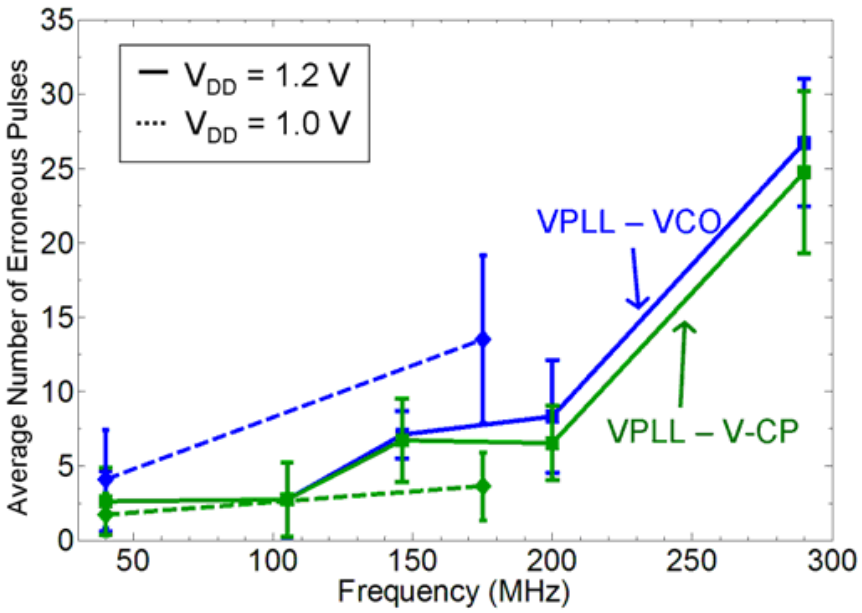


Fig. V-14. Average number of erroneous pulses versus frequency for various power supply voltages in the VCO and V-CP of the VPLL circuit.

Conversely, the response to strikes in the V-CP for a reduced power supply of 1.0 V versus 1.2 V is a slight decrease in the overall susceptibility to SEs, indicating that the

reduction in the power supply has a minimal effect on the SE response to strikes in the V-CP module. This effect results from the fundamental mechanisms controlling the RHBD V-CP. As there are no fixed current sources setting the drive current as in the VCO and the C-CP, the reduction in drive current is minimal because the current depends strongly on the RC time constant in the LPF. Therefore, the reduction in frequency is the dominant contributor to the decrease in erroneous PLL output pulses as the power supply voltage is reduced.

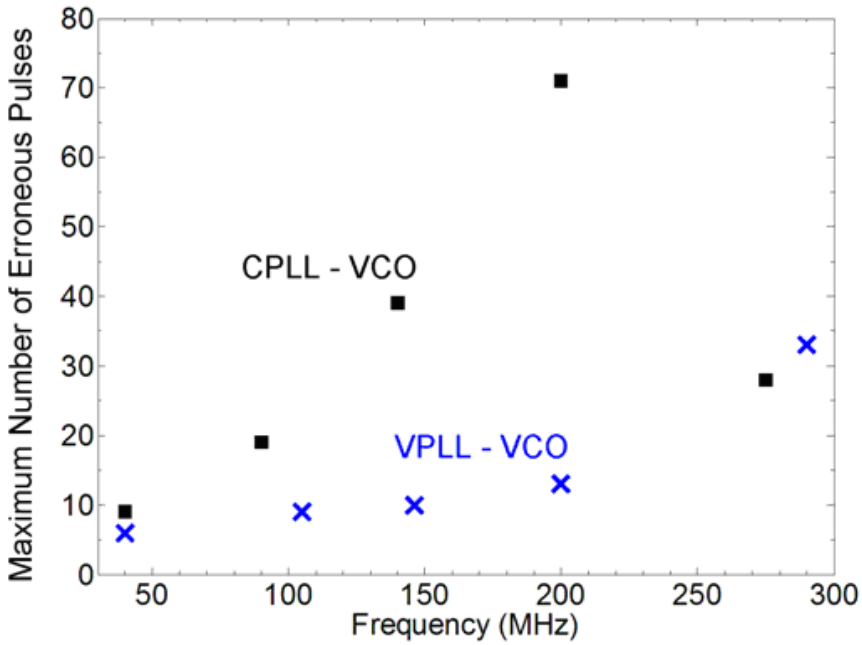


Fig. V-15. Maximum number of erroneous pulses versus frequency in the outputs of the CPLL and VPLL for strikes in the VCOs.

An additional effect observed is illustrated in Fig. V-15 in which the number of erroneous pulses in the hardened (VPLL) and non-hardened (CPLL) PLL outputs is compared for strikes in the VCOs. Typically, the maximum number of erroneous clock pulses resulting from strikes in the VCO will increase with increasing frequency of

operation. However, once the increasing drive currents within the VCO begin to dominate the SE response of the VCO, the number of erroneous clock pulses will begin to decrease with increasing frequency of operation [Bo05, Lo06, Lo07a, Lo07c]. This effect corresponds to the decrease in the maximum number of erroneous clock pulses for the VCO in the CPLL as the frequency is increased from 200 MHz to 290 MHz. Moreover, although the VCOs are identical, the slope of the number of erroneous pulses versus frequency is greater for the CPLL than the VPLL. This result indicates that a faster response time of a closed-loop PLL improves the overall SE response and impacts the shape of the maximum number of erroneous pulses versus frequency for strikes in the VCO module. As a strike in the VCO will result in a frequency perturbation, the response time of the loop will determine the length of time the PLL will take to recover from the SE. Therefore, since the VPLL's loop response time is decreased due to the implementation of the RHBD V-CP, the susceptibility of the VPLL to SETs is also reduced. The decreased slope of the VPLL is due to the increased natural frequency and decreased damping when implementing the V-CP over the C-CP [Lo06, Lo07a].

Conclusion

Two phase-locked loop circuits were designed, fabricated, and tested in the IBM 130 nm CMRF8RF process available through the MOSIS foundry for SET sensitivity and the effectiveness of RHBD mitigation. The first PLL implements a conventional current-based charge pump technique, the second utilizes a RHBD voltage-based charge pump for improved SE performance. Results from a through-wafer two-photon absorption

technique show 2.3 orders of magnitude improvement in the number of erroneous pulses present in the output of the PLL following a SE strike in the hardened design. TPA-induced SEU maps indicate that implementing the RHBD voltage-based charge pump over the conventional current-based module reduces the vulnerable area of the charge pump module by approximately 99%. The proposed hardening technique effectively reduces the sensitivity of the charge pump sub-circuit below the upset level of the voltage-controlled oscillator. Additional improvements are possible by addressing upsets in the VCO. These results show that RHBD is effective for high-speed, mixed-signal circuits using unconventional analog design techniques and targeted single-event circuit simulations.

CHAPTER VI

MODELING AND MITIGATING SINGLE-EVENT TRANSIENTS IN VOLTAGE-CONTROLLED OSCILLATORS

Introduction

The previous chapter presented a simulation and experimental characterization of single-event upsets (SEU) and single-event transients (SET) for two types of unity gain PLL circuits. The first, a conventional current-based charge pump PLL, was shown to possess an inherent vulnerability to SETs in the charge pump module. Therefore, a voltage-based charge pump was proposed to significantly reduce not only the length and magnitude of SETs generated within the charge pump, but also the cross-sectional area sensitive to SEUs [Lo06, Lo07a, Lo07b]. Also, it is shown that if the charge pump functional block is hardened to a sufficient level, the VCO becomes the dominant SE upset source at 130 nm. These results illustrate that VCOs can contribute to the overall single-event (SE) susceptibility of mixed-signal systems [Lo06, Lo07a, Lo07b]. Furthermore, previous work has shown an increased sensitivity to SEs in VCO topologies as technologies scale [Bo05]. These observed sensitivities and trends warrant a closer look into the fundamental mechanisms governing the generation and propagation of SETs in the VCO.

This chapter presents an analytical model to predict the response of the stand-alone VCO to SEs, and radiation-hardened-by-design (RHDB) techniques to improve the SE tolerance of VCO designs. All RHBD techniques presented in the following sections were implemented on VCO designs developed in the IBM 9SF 90 nm process. The effectiveness of the RHBD techniques is illustrated through the use of circuit-level

simulations, and further compared to analytical calculations. By using the RHBD techniques presented here, the amount of phase displacement in the output of the VCO can be reduced by up to 66%. As a result, the novel RHBD techniques of this chapter, which can be applied to all current-starved inverter structures, can reduce the susceptibility of the VCO to SEs and significantly harden the mixed-signal circuits of which it is a part. Furthermore, the analytical model may serve as a tool for designers in developing VCOs to not only meet design specifications, but to minimize the effects of SEs.

The Current-Starved Voltage-Controlled Oscillator

Description of VCO Circuit Topology

The VCOs discussed in this chapter follow the topology presented in Chapter II, Fig. II-18. The VCO circuits in this study were designed with the IBM 9SF 90 nm PDK using low-voltage threshold (LVT) devices for a power supply voltage of 1.0 V. All of the circuits presented share the same overall topology with appropriate changes in bias and ring-oscillator (RO) stages for the RHBD techniques. Fig. VI-1 illustrates the transfer characteristics of the VCO designed with 7 RO stages and a center frequency (f_c) of approximately 1.3 GHz. The VCO was designed such that for $V_{inVCO} = V_{dd}/2$ (f_c), the oscillating frequency was within 10% of $(f_{max}+f_{min})/2$ to ensure the proper balance between gain, jitter, and stability [Bo05].

Furthermore, the linear region of operation was maximized by introducing an additional pMOS device, a wide nMOS device, and a resistor in the input-bias circuit, as described in [Be98]. The primary advantages of the linearization is an increase in the

input operating voltage range and the predictability ($\Delta f/\Delta V$ is constant) across the operating range. A decrease in the maximum operating frequency will arise with this linearization scheme; however, this decrease in maximum operating frequency will also result in decreased jitter. Although the design does result in an increase in power (~3% for 11 RO stages) and vulnerable area to SEs (~100% for 11 RO stages), it is ideal for operation in a PLL as the linearized VCO results in a large linear operating range and decreased jitter in the output.

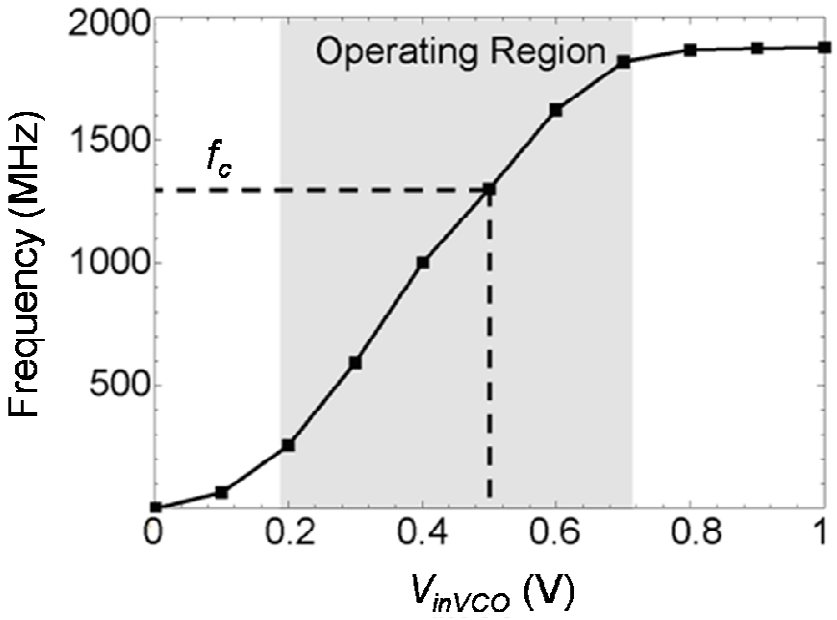


Fig. VI-1. Transfer characteristics, output frequency versus input voltage, of the VCO designed for a center frequency of 1.3 GHz and implemented with 7 RO stages.

Single-Event Response of the VCO

In order to separate the effects of the negative feedback within the PLL on the SE response of the VCO, the remainder of this chapter discusses the response of the VCO to SEs as a stand-alone oscillator. To analyze the SE response of the VCO, two

mechanisms representing SE strikes in either the input-bias stage or in a current-starved inverter must be studied. SE strikes in the input-bias stage will alter the biasing voltages, V_{pbias} and V_{nbias} (see Fig. II-18), resulting in altered current through the current mirrors and current-starved inverters. This ultimately results in a frequency modulation of the output signal. For example, Fig. VI-2 shows a typical response following a strike in the bias circuit. The output frequency of the VCO prior to the simulated ion strike is fixed to approximately 1.6 GHz. The frequency is determined by the current dissipation through each RO stage, which directly depends on the bias voltages V_{pbias} and V_{nbias}. Immediately following the ion strike, voltage V_{pbias} is reduced below its normal operating value, consequently increasing voltage V_{nbias} above its normal operating value. The changes in bias voltages result in stronger current drives through each RO stage and temporarily increase the output frequency of the VCO to approximately 3 GHz (positive frequency modulation). Cases where negative frequency modulation (the output frequency is temporarily reduced) may also occur.

On the other hand, SE strikes in a current-starved inverter stage will either deposit or deplete the charge stored on the output node of the inverter stage. The voltage on the affected node will remain perturbed until this charge is dissipated, ultimately resulting in a temporary oscillation failure until the perturbation is removed, as shown in Fig. VI-3.

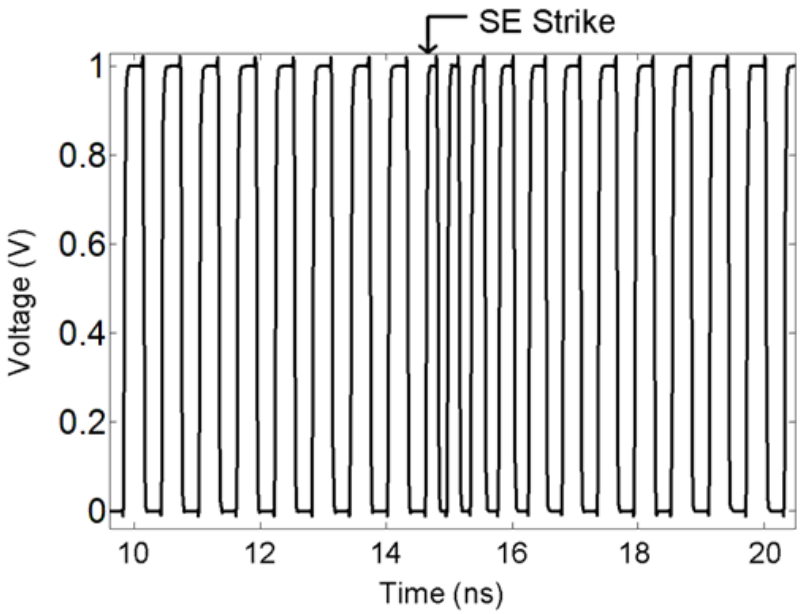


Fig. VI-2. The output voltage of the VCO during an SE in the input bias stage. The strike occurs at approximately 15 ns and has an LET of 80 MeV-cm^2/mg. A frequency modulation occurs until the current can be restored to its initial value.

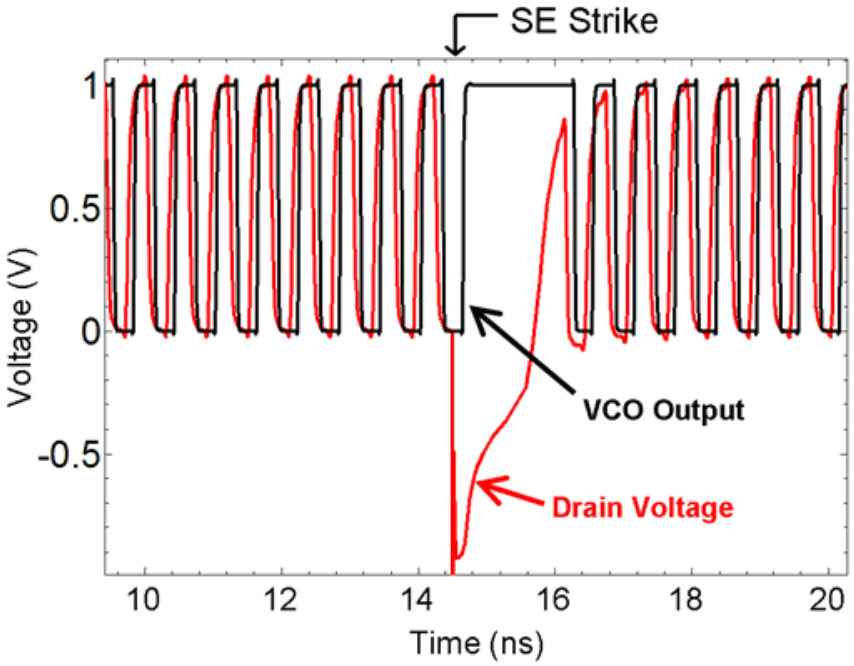


Fig. VI-3. The output voltage of the VCO and drain voltage of the hit device during a single-event in a current-starved inverter stage. The strike occurs at approximately 15 ns and has an LET of 80 MeV-cm^2/mg. The output of the VCO is locked to V_{dd} until the drain voltage recovers.

Modeling SETs in the VCO

As the basic mechanism affecting the current-starved inverter response to an SE strike is its ability to dissipate deposited charge, one possible RHBD technique for SET mitigation is to decrease the localized delay of each current-starved inverter stage and compensate for the decrease in overall system delay by increasing the number of total stages. Although increasing the number of stages also has the adverse effect of increasing the total active area, it is initially assumed that the individual stage vulnerabilities will be reduced. A simple model depicting the response of the VCO to SE hits can be represented by two current sources (I_D) representing the restoring device current in a current-starved inverter, an output nodal capacitance (C), and a current source representative of the current induced by the SE (I_{hit}), as shown in Fig. VI-4.

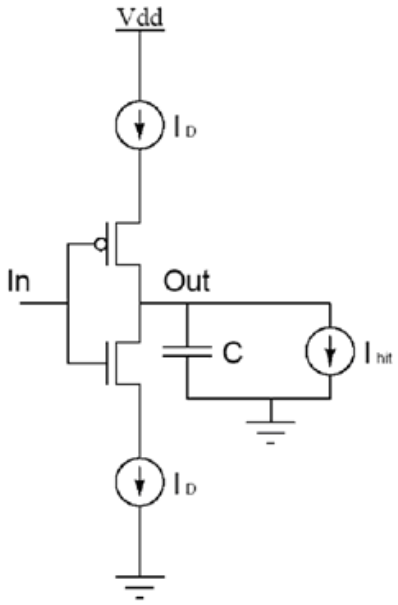


Fig. VI-4. A simple model for an SE hit in a current-starved inverter can be represented by two current sources (I_D) representing the restoring device current in an inverter, an output nodal capacitance (C), and a current source representative of the current induced by the SE (I_{hit}).

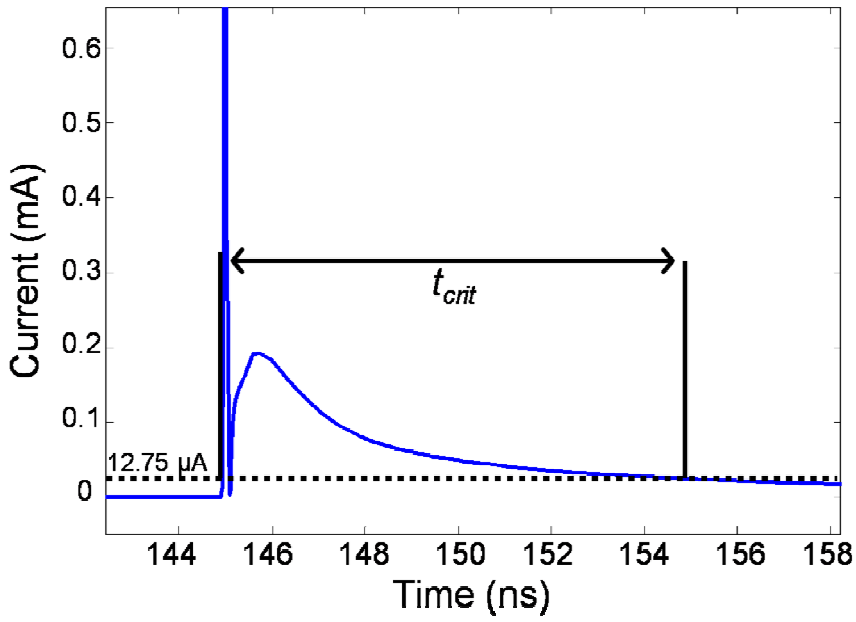


Fig. VI-5. Current pulse generated by a simulated heavy-ion with an LET of 80 MeV-cm^2/mg. The critical time of the VCO with a current drive of 12.75 µA is illustrated.

As long as I_{hit} exceeds I_D, the capacitor voltage will be controlled by I_{hit}, resulting in a perturbed voltage at the inverter output node. When I_{hit} is less than I_D, the output node will begin to recover. This recovery can be used to define the critical time for a VCO as the time for which $I_{hit} > I_D$ or the time during which the output node voltage stays "upset". The critical time was determined through current profiles for heavy ion hits that were obtained through 3D TCAD simulations of device models calibrated to the IBM 90 nm 9SF process [Da07a, Da07b].

Specifically, the current profiles were extracted by performing SE simulations on a 5-inverter (minimum device dimensions) cascade, with either the pMOS or nMOS device within the middle inverter implemented in TCAD. The remaining devices were employed using compact models calibrated to the PDK [Da07a, Da07b]. Although the

devices in each simulation were constructed with minimum device dimensions and identical loading (the actual circuit consists of various device dimensions), the current profiles have been shown to provide adequate modeling of the ion-induced transient effects [Lo08, Lo09]. In fact, identical techniques discussed in Chapters VII, VIII, and IX are used to produce experimentally supported results for various circuit topologies including current-starved ring oscillators.

The current profiles for an incident ion with varying LET at the drain of the struck device were extracted and compared with device currents, I_D. Fig. VI-5 illustrates an example of a current profile extracted from 3D TCAD mixed-mode simulations with the critical time labeled as the amount of time that the SE-induced current exceeded the current-starved inverter's drive current of 12.75 μA. Moreover, the phase error (Φ_e), defined as the number of degrees for which the output is perturbed, can be represented by Eqn (VI-1).

$$\phi_e = t_{crit} \times f_{osc} \times 360° \tag{VI-1}$$

Phase error (specifically termed phase displacement when directly resulting from single-events) can be used to determine the severity of a hit and is used in the rest of this chapter. Thus, to reduce the impact of SE hits, or reduce the critical time for a VCO, the designers can increase I_D for each stage. However, the frequency of oscillation, f_{osc}, is determined by Eqn. (II-31) (see Chapter II) where I_D is the current through each inverter stage, N is the number of RO stages, and C_{tot} is the equivalent capacitance at the output of each RO inverter stage [Be98].

For a fixed frequency (f_{osc}), I_D is directly proportional to N; therefore, any increases in the current drive for each inverter stage must be accompanied by either increasing N or C_{tot}. The rest of the chapter deals with increasing N to mitigate SE hits, but increasing C_{tot} proportionally with increasing I_D will also yield similar results (see Eqn. (II-31) in Chapter II). As these designs with different combinations of I_D and N will yield slightly varying f_{osc} due to parasitics, care should be taken to ensure proper operation.

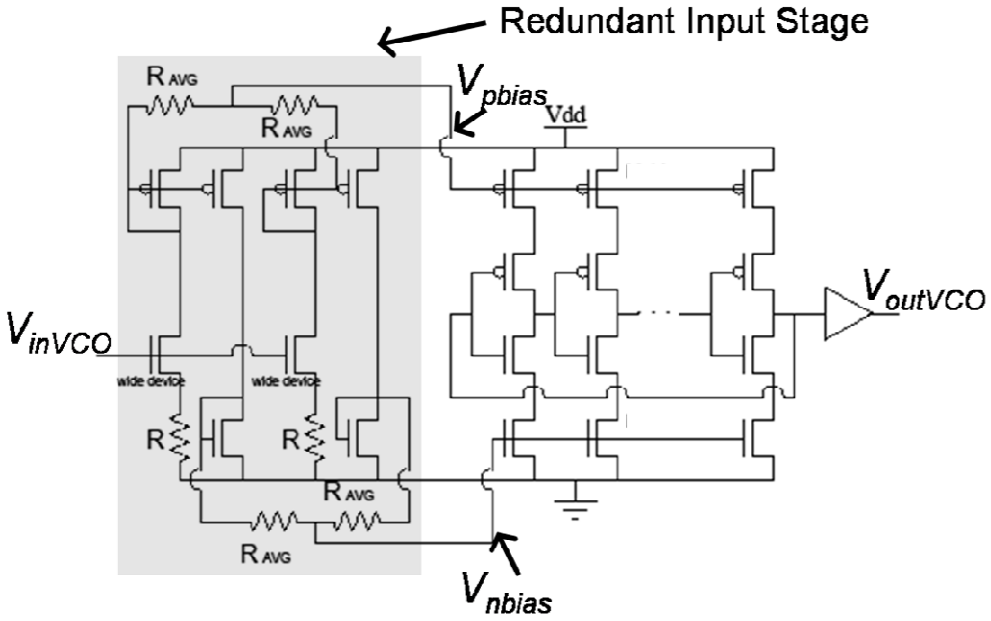


Fig. VI-6. Schematic representation of the VCO implementing analog redundancy in the input-bias stage in order to reduce the voltage perturbation on V_{pbias} and V_{nbias} resulting from an ion strike in the bias stage. The input stage is implemented with 2 identical copies and averaged with identical resistors, R_{AVG}.

An SE that occurs in the input-bias stage of the VCO will result in transients on the bias voltage nodes, V_{pbias} and V_{nbias}, and ultimately result in a frequency modulation of the output signal. This type of transient can be effectively mitigated through the use of analog redundancy, as shown in Fig. VI-6. The input-bias stage is replicated M times and

averaged using identical resistors, thus reducing any perturbation (ΔV) due to an SE strike on any one copy to $\Delta V/M$. Simulations show that for 2 copies of the input stage, the phase displacement in the output of the VCO can be reduced by 35%. To achieve a desired level of error mitigation, an appropriate value of M (number of copies) can be used. Proper layout techniques must be used to avoid charge-sharing between these stages. It is also important to note that the total active area, thus the total area subject to SEEs, will also be increased.

A second type of transient that can occur within the VCO will result from a strike in a RO stage, which will temporarily impede the oscillations. This type of transient can be mitigated by increasing the number of RO stages, N, and equivalently increasing the drive current, I_D, through each RO stage.

To verify these models and RHBD techniques, 5 VCO circuits were designed with 7, 11, 15, 19, and 23 RO stages with V_{inVCO} ranging from 300 mV to 800 mV. The transfer characteristics for these VCO circuits designed for identical center frequencies are displayed in Fig. VI-7. The VCOs differed in the number of current-starved inverter stages, N, and the current drive of each inverter stage, I_D, to control the delay through each stage. Among the 5 designs, the center frequencies varied by only 1.5%. In addition the gains of the VCOs decreased by 20% from 7 stages to 23 stages and the maximum frequencies reduced by 11%. In general, a PLL will not be designed to operate at the maximum frequency of the VCO, thus the reduction in maximum frequency is generally not significant unless it also decreases the linear operating region. Moreover, the slight gain reduction results in a diminished overall jitter with no considerable impacts on the VCO operation.

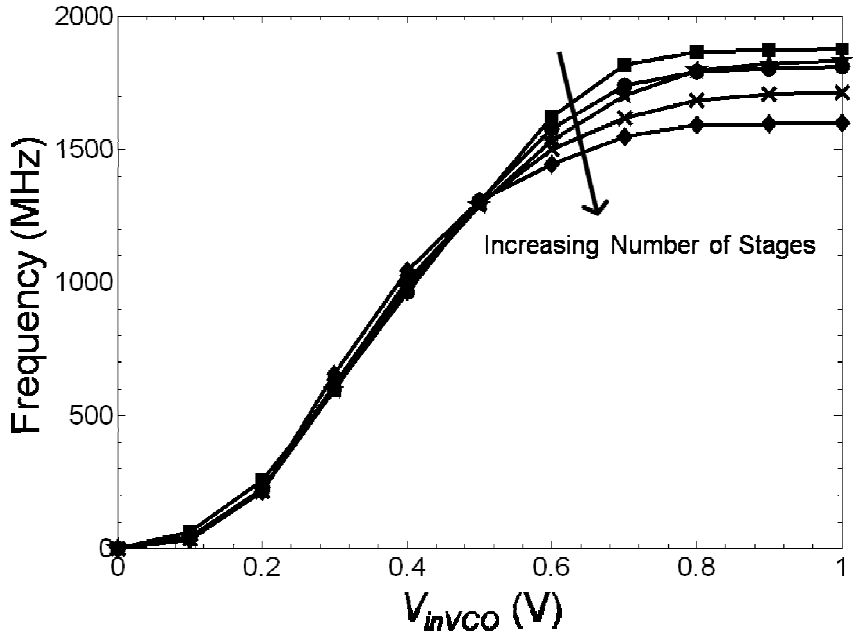


Fig. VI-7. Transfer characteristics, output frequency versus input voltage, for VCOs designed with 7, 11, 15, 19, and 23 current-starved inverter stages.

SET Simulations and Modeling

Single-event transient simulations were performed on the VCO circuits using the CADENCE EDA tool suite, the SPECTRE environment, and IBM 90 nm 9SF process parameters. All simulations were performed using the Advanced Computing Center for Research & Education (ACCRE) computing cluster at Vanderbilt University [ACCRE]. The ion strike current profile, obtained from 3D TCAD simulations, was injected into every node in each VCO circuit. The primary metric that was considered when analyzing the effects of the SETs on the VCO was the phase displacement in the output signal of the VCO. Fig. VI-8 illustrates the phase displacement versus the input voltage and the number of stages as obtained from the analytical model. As expected, for a fixed frequency at higher I_D values (larger number of current-starved inverter stages, N), the

VCO shows lower phase displacement for SE hits. Figs. VI-9 and VI-10 compare the results of the analytical model to the SET simulations at 80 MeV-cm^2/mg.

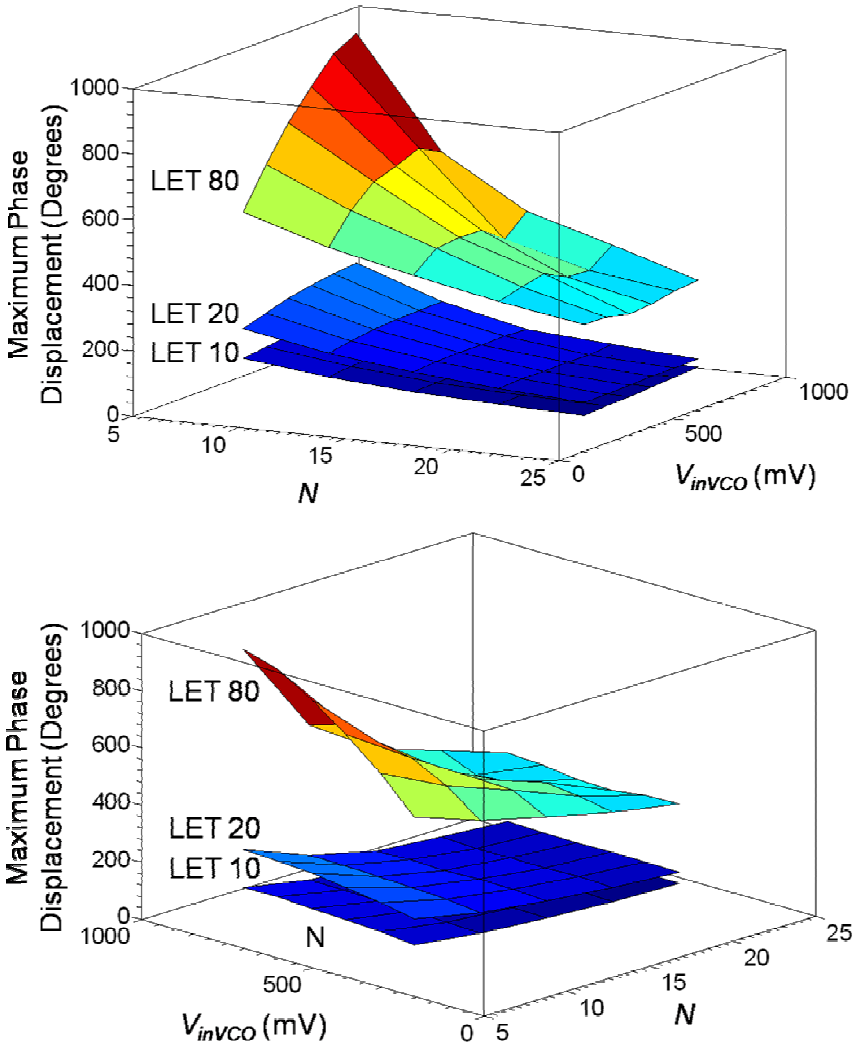


Fig. VI-8. (a) Maximum phase displacement versus input voltage (V_{inVCO}) and number of RO stages (N) for varying LET values (MeV-cm^2/mg) as generated by the analytical model. (b) Alternative view.

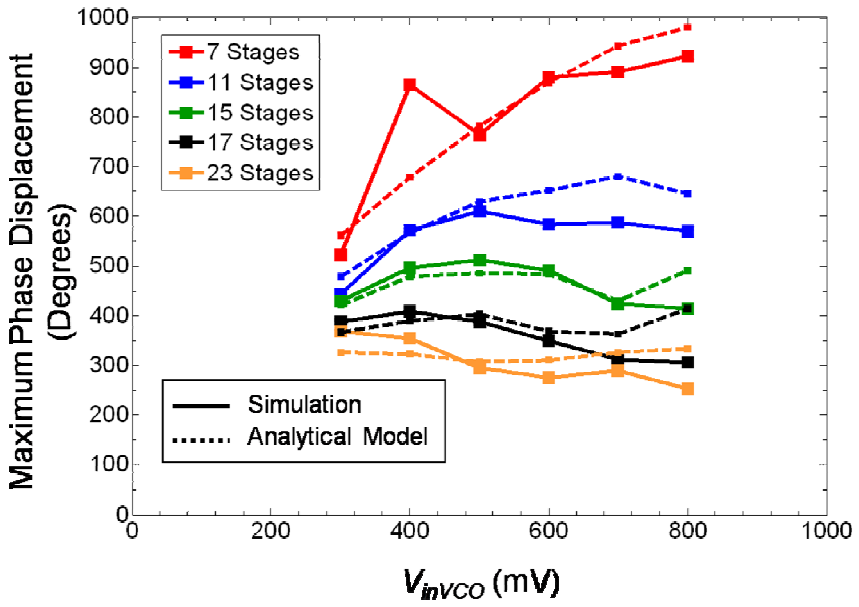


Fig. VI-9. Maximum phase displacement versus input voltage for the VCO circuits at 80 MeV-cm^2/mg. Results obtained from the analytical model are compared to simulations for various *N*.

Three main observations can be made from these results. First, as the number of stages increases the maximum phase displacement decreases as expected. Up to 66% reduction in maximum phase displacement was achieved when implementing 23 stages over 7 stages. Second, the trends of the phase displacement versus input voltage change for varying number of stages (Fig. VI-9). For a low number of stages the maximum phase displacement increases for increasing bias voltage. The increase in phase displacement results from the increase in frequency of operation. As the frequency increases there are a greater number of oscillations during the time the voltage is perturbed within the VCO, thus there will be a greater phase displacement in the output. Conversely, for a higher number of stages the maximum phase displacement begins to increase for increasing input bias and proceeds to decrease. The decrease in phase displacement versus input voltage occurs because the stronger drive currents begin to

overcome the effects of the increasing frequency. Finally, the jagged curves, as produced by the simulations, are a result of a low statistical resolution. That is, in order to smooth the curves out, a large number of simulations are required for various temporal strike locations with respect to the operating frequency. This point will be further described in the following chapter.

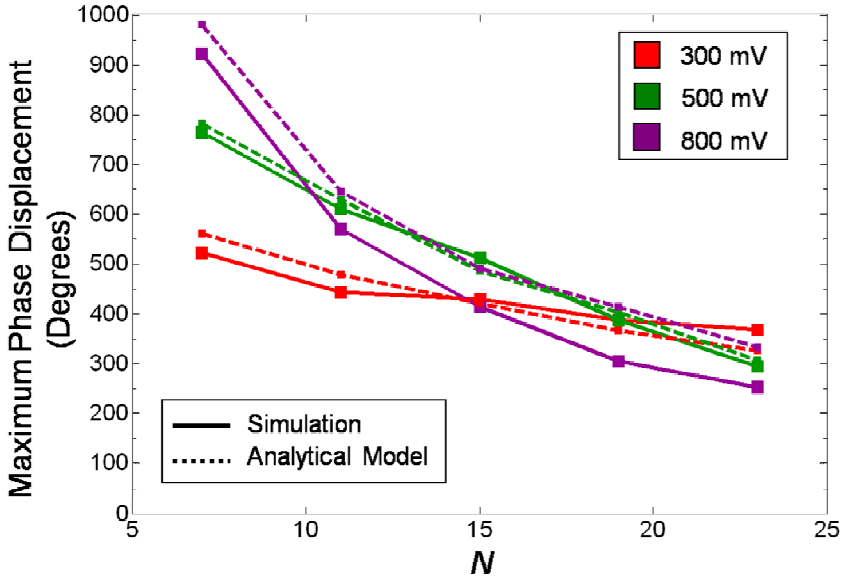


Fig. VI-10. Maximum phase displacement versus the number of inverter stages (N) for 3 bias conditions (300 mV, 500 mV, and 800 mV) at 80 MeV-cm^2/mg. Results obtained from the analytical model are compared to simulations.

Finally, a plot of phase displacement versus the number of stages (Fig. VI-10) shows an increasing slope with increasing input voltage. This result indicates that increasing the number of stages is more effective for bias conditions in the upper range of the linear region of operation. Furthermore, the linearity and accuracy of the VCO designs can be evaluated by examining this plot for a given input voltage. The phase displacement reduces linearly for increasing number of stages because the drive currents in the inverter

stages increase linearly. This linearity can be visualized when examining Φ_e/N for 300 mV and 500 mV. The slope is constant for all N, thus the center frequencies of the VCOs and frequencies for low bias voltages were closely matched. However, as the number of stages is increased the maximum frequency was decreased, thus the frequency at 800 mV for the VCO designed for 7 stages is different than the VCO designed for 23 stages, which results in a non-linear slope Φ_e/N.

Design Tradeoffs

Though implementing the hardening techniques as described throughout this chapter can result in a significant improvement in SET susceptibility, certain electrical performance and design tradeoffs such as area and power must be considered. Eqn. (VI-2) represents the total vulnerable area (TA) of the VCO where N and M represent the number of current-starved inverter stages and the number of redundant input bias stages, respectively.

$$TA(N,M) = c_1 N^2 + M\left(c_2 N + c_3\right) \tag{VI-2}$$

The coefficients c_1, c_2, and c_3, can be determined by Eqns. (VI-3), (VI-4), and (VI-5), respectively.

$$c_1 = \frac{A_I}{N_B} \tag{VI-2}$$

$$c_2 = \frac{A_{BN1}}{N_B} \tag{VI-3}$$

$$c_3 = A_{BN2} \tag{VI-4}$$

A_I represents the vulnerable area of 1 current starved-inverter stage (drain and source areas of the inverters and drain areas of the current sources), A_{BN1} represents the vulnerable area of the input-bias network (drain areas of pMOS and nMOS devices) excluding the wide nMOS device, and A_{BN2} represents the vulnerable area of the wide nMOS device (drain and source areas). The vulnerable areas were determined from the original VCO design with 7 RO stages. Because many of the device sources are not connected directly to the power rails (e.g. a current-starved inverter), the sources as well as the drains are included in the calculation of the vulnerable areas. Additionally, N_B, represents the number of stages in the original VCO design for which all other design parameters were extracted. Furthermore, the coefficients, c_1, c_2, and c_3, represent the area of 1 inverter stage, the area of 1 bias stage excluding the wide nMOS device, and the area of 1 wide nMOS device, respectively.

Fig. VI-11 represents the total vulnerable area of the VCO circuits for varying numbers of input-bias stages and current-starved inverter stages. The different curves represent the vulnerable areas obtained by varying the number of input-bias stages. Additionally, the area determined analytically is compared to the actual achieved areas for the cases of 1 and 2 input-bias stages.

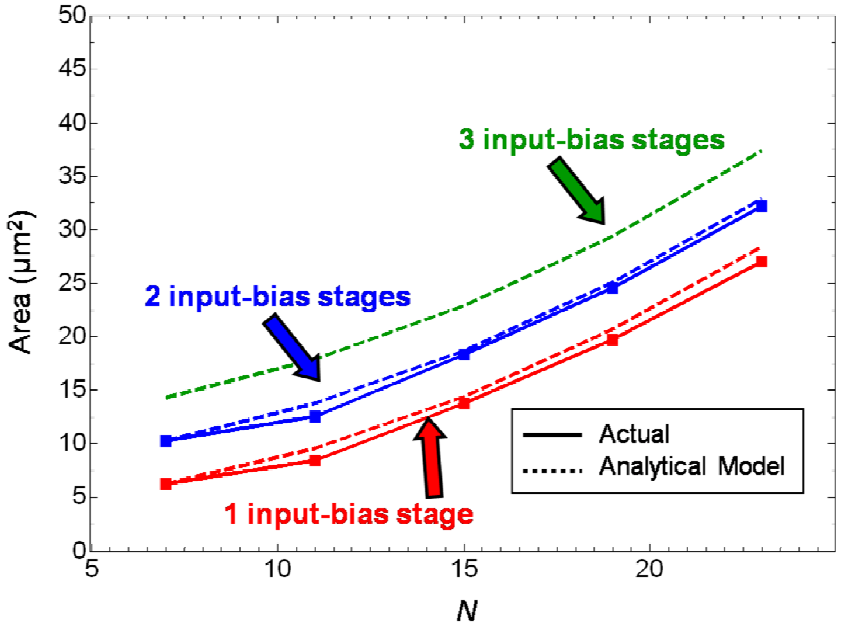


Fig. VI-11. Total vulnerable area versus N for different numbers of input bias stages. The dashed lines represent the area obtained analytically and the solid lines represent the actual achieved areas.

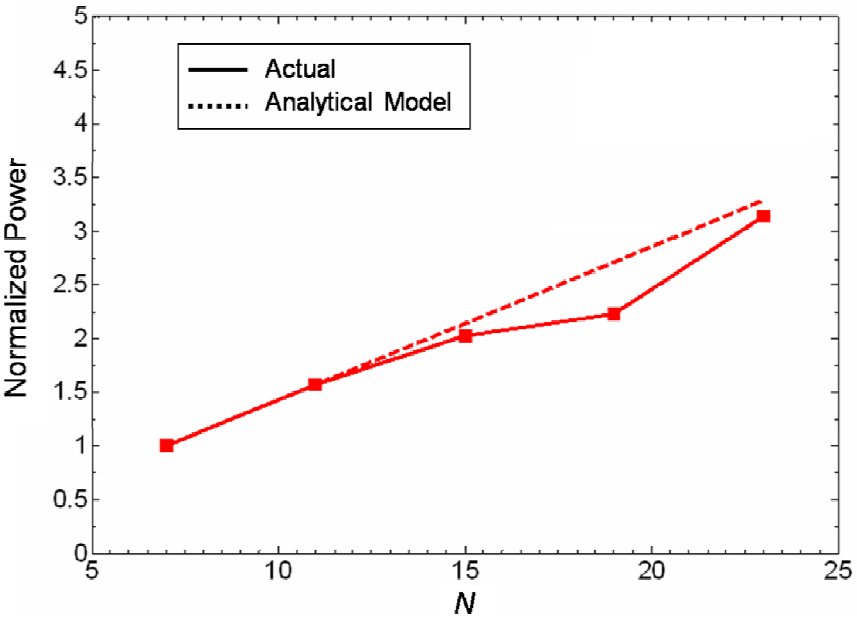


Fig. VI-12. Average power dissipation versus N normalized to the power dissipation for 7 RO stages. The dashed line represents the power obtained analytically and the solid line represents the actual power dissipation.

Finally, the average power consumption, normalized to the power achieved at 7 stages, is plotted versus the number of stages (Fig. VI-12). As the average power dissipation of a VCO is linearly related to the drive current, I_D, as described in [Be98], and the RHBD technique as described throughout this work requires I_D to increase by the same factor as N, the power dissipation therefore increases linearly with increasing number of RO stages (N).

Conclusion

Because of the high sensitivity of the voltage-controlled oscillator (VCO) to single-events (SEs) an analytical model was developed to determine the VCO design parameters and the associated SE vulnerability. The model has been validated with simulations performed using the IBM 90 nm 9SF process parameters with SE strikes represented by current profiles obtained from 3D TCAD mixed-mode simulations of varying LET values. Additionally, RHBD techniques for mitigating SEs in VCOs have been presented. The proposed mitigation techniques have been shown to reduce the output phase displacement following an SE by approximately 66%. As significant power and area penalties result from implementing the mitigation techniques, application specific tradeoffs must be considered based on the dominant design constraints. The availability of such a technique and the analytical model will improve the SE performance of PLL designs to ensure a specified tolerance to SEs. As this chapter discusses a specific model and SET characterization technique in terms of the worst-case operating conditions, the following chapter presents an additional analysis technique for a complete probabilistic SET characterization of mixed-signal topologies such as the VCO and PLL.

CHAPTER VII

A PROBABILISTIC ANALYSIS TECHNIQUE APPLIED TO A RADIATION-HARDENED-BY-DESIGN VOLTAGE-CONTROLLED OSCILLATOR FOR MIXED-SIGNAL PHASE-LOCKED LOOPS

Introduction

The previous chapter presented a model and simulation results for the SET characterization of conventional and hardened VCO topologies. The SET characterization and determination of the SET vulnerability presented is strictly based on the measured worst-case transients (in terms of maximum phase displacement values following ion strikes). In this chapter, the SET response of a stand-alone, five-stage current-starved VCO designed for a center frequency of 1.75 GHz using the IBM 90 nm 9SF PDK is analyzed from a probabilistic point-of-view. Next, an RHBD VCO for SET mitigation is presented that effectively reduces the output phase displacement following ion strikes in the VCO to below the normal operating noise floor. Also, a novel probabilistic analysis of the conventional and RHBD VCOs is presented to show that maximum reduction in output phase displacement is achieved by the RHBD VCO. This analysis technique can be readily applied to all analog topologies and provides not only detailed quantification of the transients, but a first step into quickly estimating the likelihood of transient generation and propagation within circuit topologies of interest. Next, the probabilistic analysis is experimentally verified on a standard VCO topology designed and fabricated in the IBM 130 nm 8RF process available through the MOSIS foundry, and illustrates the feasibility of the technique for the characterization of complex SET signatures. Finally, detailed design considerations for the RHBD VCO are

provided. Although the RHBD VCO increases the required area and power, the phase jitter due to supply noise and device variations/mismatch is reduced. Furthermore, the proposed RHBD technique can be readily implemented within any mixed-signal PLL and delay-locked-loop (DLL) application for improved radiation tolerance.

VCO Circuit Description

The Current-Starved VCO Circuit Topology

The conventional, unhardened VCO designed for this work is equivalent to the general topology presented in the previous chapter. The circuit, however, was designed using the IBM 90 nm 9SF PDK with a power supply voltage of 1.2 V, and includes five current-starved inverters, such that the center frequency of operation (the frequency at which $V_{inVCO} = V_{dd}/2$) is approximately 1.75 GHz.

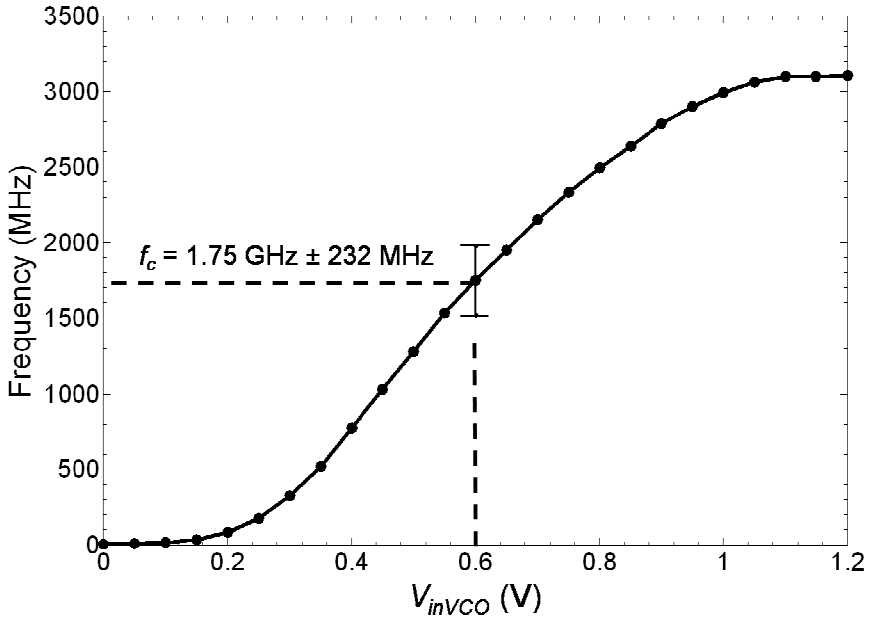


Fig. VII-1. Frequency transfer characteristics of the unhardened five-stage VCO.

VCO Electrical Specifications

The frequency transfer characteristics for the VCO are displayed in Fig. VII-1. Additionally, 100 Monte Carlo simulations of 3σ-process variations provided by the PDK were performed using the CADENCE EDA tool suite, the Spectre Environment, and the ACCRE computing cluster at Vanderbilt University [ACCRE]. The results show that the standard deviation from the center frequency, f_c, is approximately 232 MHz, an approximate 12% deviation from f_c. This value is within an acceptable range for use in PLL applications.

Definition of Phase Jitter

In order to facilitate the SET analyses of the VCO circuits, this section presents an approach for quantifying phase jitter so that SETs may be directly compared to a common and critical performance specification for VCO designs. Phase jitter represents the amount of phase or time fluctuation in the output signal during steady state operation. Many factors, such as power supply fluctuations and unmatched current sources, can result in phase jitter [Ba08]. This work quantifies phase jitter as the amount of time each consecutive period of the output signal, V_{outVCO}, deviates from the ideal period, T_{clk}. This definition is commonly referred to as cycle-to-cycle phase jitter. The cycle-to-cycle phase jitter is calculated by creating a vector, $\mathbf{jitter_{cc}}$, as shown in Eqn. (VII-1) and illustrated in Fig. VII-2, where t_i is the i^{th} clock period and T_{clk} is the ideal clock period. The ideal clock period, T_{clk}, may not be known, in which case the mean, or expected clock period, must be used.

RMS phase jitter is a typical metric used to quantify the cycle-to-cycle phase jitter and is calculated by finding the standard deviation of $\mathbf{jitter}_{cc}$, as defined by Eqn. (VII-2), where Var(X) is the variance of X [He99].

$$\mathbf{jitter}_{cc} = \begin{bmatrix} t_1 - T_{clk} \\ t_2 - T_{clk} \\ \vdots \\ t_i - T_{clk} \\ \vdots \\ t_N - T_{clk} \end{bmatrix} \tag{VII-1}$$

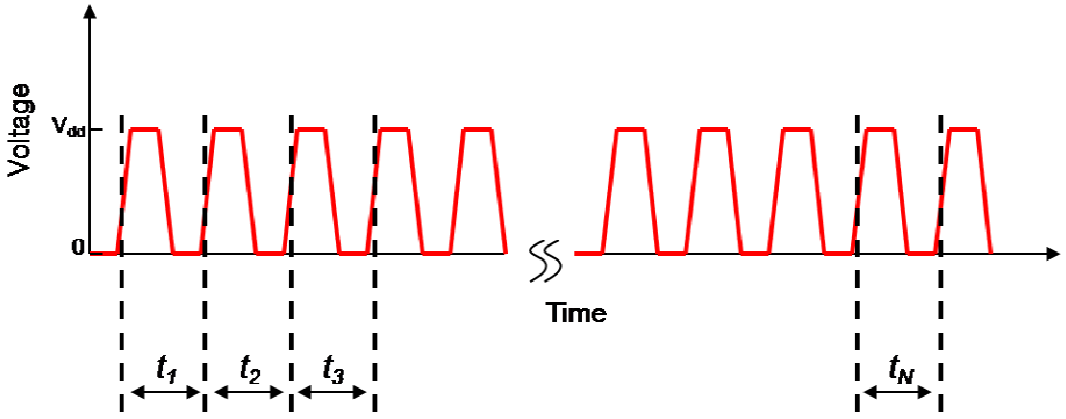


Fig. VII-2. Illustration of time-domain measurements of the local operating periods (t_i) used for the calculation of phase jitter, *rms* phase jitter, and the expected value of peak phase jitter, $\overline{\phi_e}$, as described by Eqns. (VII-1 to VII-3).

$$jitter_{rms} = \left[\mathrm{Var}(\mathbf{jitter}_{cc})\right]^{\frac{1}{2}} \tag{VII-2}$$

In order to simulate the phase jitter due to power supply variation, a noisy power supply was created by connecting an ideal DC power supply in series with a pseudo-random-noise source generating an error value within ±2% of V_{dd} (1.2 V). Additionally, a low frequency sinusoidal source with amplitude of 15% of V_{dd} was also connected in series with the noise source. The resulting noisy power supply was utilized during all simulations of the VCO.

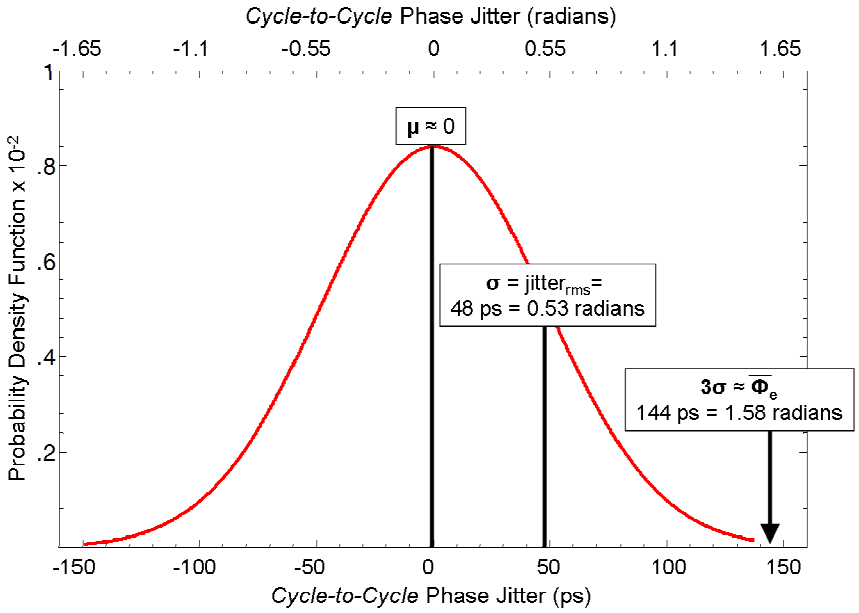


Fig. VII-3. Simulated cycle-to-cycle phase jitter fit to a probability density function for a Guassian distribution with a mean value of 0 ps and a standard deviation (*rms* phase jitter) of 48 ps.

As expected, the cycle-to-cycle phase jitter due to a noisy power supply was found to follow a Gaussian distribution with a mean of 0 ps. The *rms* phase jitter of the VCO at a center frequency of 1.75 GHz was calculated to be approximately 48 ps and is indicated in Fig. VII-3 where the simulated cycle-to-cycle phase jitter is fit to a probability density

function (pdf) for a Guassian distribution. Typically, phase jitter is quantified in units of ps; however, in order to relate the phase-displacement resulting from SEs in the VCO to the oscillator phase jitter, it is also useful to express the phase jitter in units of radians, by dividing the phase jitter by the period of oscillation and multiplying by 2π. Thus, the *rms* phase jitter (due to a noisy power supply) in units of radians is approximately 0.53 radians and the 3σ value is approximately 1.58 radians.

$$\overline{\phi_e} = 3\left[\mathrm{Var}(\mathbf{jitter}_{cc})\right]^{\frac{1}{2}} = 3\,jitter_{rms} \qquad \text{(VII-3)}$$

In order to distinguish the phase jitter due to noise from any phase error following an SE (described in further detail in subsequent sections), it is useful to quantify the upper bound of the noise floor. Throughout the rest of this paper we will approximate the upper bound of the noise floor as the 3σ value of the cycle-to-cycle phase jitter, as described by Eqn. (VII-3). The 3σ value of cycle-to-cycle phase jitter is thus an approximation of the expected peak value of phase jitter due to factors other than SEs. A large number of finite-length samples are required to estimate the expected peak value of phase-error for these factors accurately. It follows that for *M* transient samples of finite length, the peak jitter for each sample will generate a distribution of peak jitter values with a mean approximately equal to that of the 3σ value of cycle-to-cycle phase jitter. Furthermore, the expected peak value of phase-error has a standard deviation, σ′, resulting in 99.6% of the output pulses with phase jitter less than or equal to 1.58 ± σ′ radians as shown in Fig. VII-3. Consequently, if an SE occurring within the VCO results in a phase-displacement less than 1.58 ± σ′, it cannot be distinguished from the nominal phase noise.

This point will be described in further detail during the SET analysis presented in later sections, and will be used to distinguish SETs from phase jitter due to noise.

The Radiation-Hardened-by-Design Voltage-Controlled Oscillator

The basic premise behind the RHBD VCO structure is to create a single oscillator that does not degrade operating performance specifications, such as phase jitter. Multiple designs involving the alteration of device sizes and the number of inverters have been proposed that improve the radiation response with minimal performance degradation [Lo07c]. In this chapter, an approach based on triple-modular-redundancy (TMR) is used for achieving radiation tolerance levels higher than those for previously proposed approaches. The conventional TMR implementation – three self-running VCOs in parallel, each with its own feedback path – is difficult to synchronize and may result in increased phase jitter. This is because any minor variations in device or parasitic elements result in unsynchronized operation and increased jitter.

Therefore, rather than implementing three self-running VCOs in parallel, three voltage-controlled variable-delay lines (VCDL) are implemented with current-starved inverters in parallel. It is important to note that each VCDL utilizes its own bias circuitry. A single bias circuit may be used but will increase the SET vulnerability of the VCO significantly, as will be explained in further detail in later sections. The VCDLs may also be implemented with any other single-ended or fully-differential delay cell. The outputs of the three VCDLs are then fed into inverting buffers, a non-inverting majority voting circuit, and an inverting output buffer for increased current drive. The output of the final buffer device is then fed back to the inputs of the three VCDLs,

ensuring that the three VCDLs are synchronized, as shown in Fig. VII-4. This implementation may also be used to create an RHBD VCDL for use in a DLL by removing the feedback path.

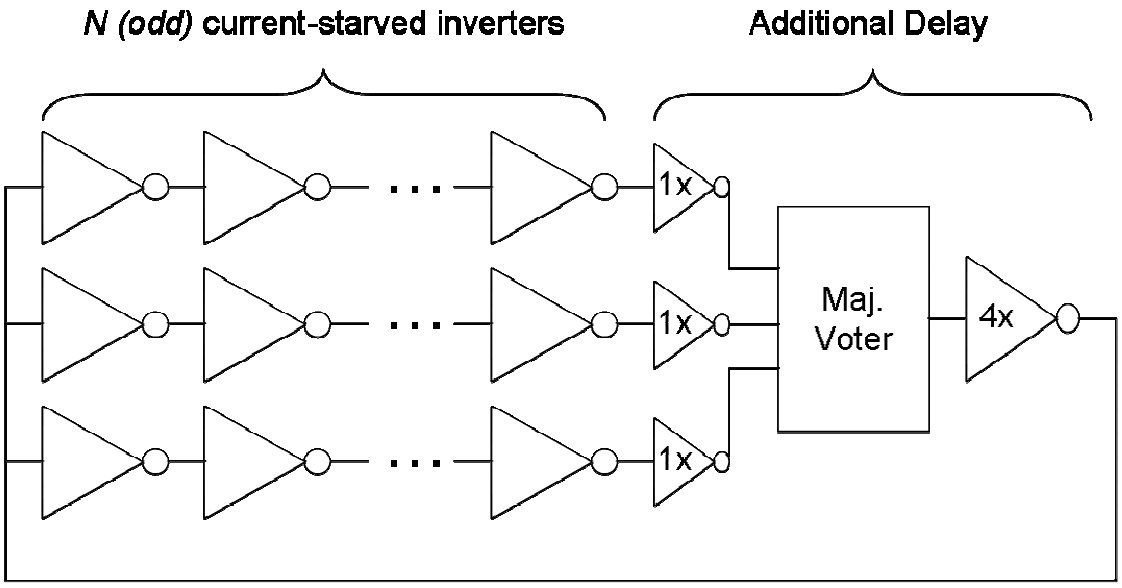


Fig. VII-4. Simplified diagram of the RHBD VCO excluding the input-bias stages and current-sources required to set the delay in each delay stage.

The RHBD VCO was designed with five delay stages in each VCDL, as in the original, unhardened VCO design. However, implementing the additional output buffers and majority voting circuit introduces a constant delay which slows the operating center frequency by some factor. In this case the center frequency was slowed down by approximately 20%. Therefore, the device aspect ratios of the current sources in each delay element were increased to approximately 2.5 times the original specifications so as to increase the current drive to match the respective center frequencies. Depending on the number of delay elements and the designed center frequency, the slow-down factor

and required compensation may vary, but will nevertheless be required. The final frequency transfer curve of the RHBD VCO is shown in Fig. VII-5 and is compared to the unhardened VCO. The center frequencies are within 2% of each other, and the gain (slope) of the RHBD VCO is reduced by approximately 25%. The gain reduction, while decreasing the maximum operating frequency, widens the input voltage range, consequently decreasing the *rms* phase jitter to 43 ps, a 10% reduction from the 48 ps *rms* phase jitter value achieved by the unhardened VCO.

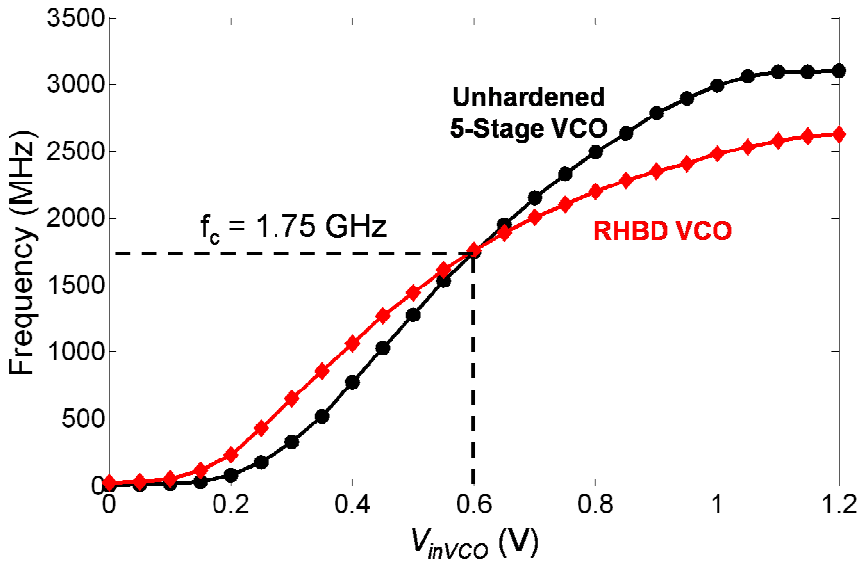


Fig. VII-5. Frequency transfer characteristics of the RHBD VCO compared to the unhardened five-stage VCO.

One hundred Monte Carlo simulations of the 3σ-process variations were again performed and show that the standard deviation of the operating center frequency is 181 MHz, an approximate 9% deviation from the mean value. Thus, by implementing the RHBD VCO, a 40% reduction in the center frequency variance due to device

variations was achieved. Similar design adjustments to decrease the *rms* phase jitter on the unhardened VCO may also be made by limiting the current and adjusting the device dimensions, however these adjustments will not significantly change the SET performance.

Single-Event Transient Simulation Parameters

Simulations of the unhardened and RHBD VCOs were performed using the CADENCE EDA tool suite, the Spectre Environment, and the ACCRE computing cluster at Vanderbilt University [ACCRE]. All simulations were performed over four design parameters: the circuit node of the strike, the simulated ion Linear-Energy-Transfer (LET) value, the temporal location of the strike within the clock period, and the input-bias condition. Ion-strike current profiles were obtained from 3D TCAD simulations on device models calibrated to the IBM 90 nm 9SF PDK [Da07b], and were injected into every node in each VCO circuit. The circuits were simulated over ten different input-bias conditions ranging from 0.3 V to 1.2 V, spanning the VCO operating frequency ranges, and three LET values (10 MeV-cm^2/mg, 20 MeV-cm^2/mg, and 80 MeV-cm^2/mg). Additionally, for each set of parameters (node, bias, LET), the temporal location of the strike was varied ten times within a cycle in order to span the operating period of the signal. Simulating over all combinations of the four simulation parameters (node, bias, LET, and temporal location) required over 13,000 simulations on the unhardened VCO and over 38,000 on the RHBD VCO. The large number of simulations were performed in order to ensure that all operating conditions are represented by the results and to achieve statistical significance. All simulations were

performed with a noisy power supply as described previously, and for each simulation the output phase displacement [Lo06, Lo07c] following the ion strike was measured.

Single-Event Transient Response

Quantification of Single-Event Transients

SEs occurring within the current-starved VCO can result in two effects and are described in detail in previous chapters. Briefly, strikes within the input-bias stage and current sources can result in a frequency modulation of the output signal, whereas strikes within the current-starved ring-oscillator structure can result in a temporary oscillation failure. Both upset mechanisms can be quantified by calculating the output phase displacement, Φ_{disp}, following an SE, where phase displacement in units of radians is the difference between the SET perturbation at the output node (T_e) and the operating period (T_{clk}), normalized by the nominal period of oscillation, T_{clk}, multiplied by 2π, as given in Eqn. (VII-4).

$$\phi_{disp} = \frac{2\pi\left|T_e - T_{clk}\right|}{T_{clk}} = \left|T_e - T_{clk}\right|\omega_{clk} \quad \textit{(radians)} \tag{VII-4}$$

The phase displacement is useful to quantify the effect of the SET as the number of erroneous clock pulses and perturbation time can be derived [Lo06, Lo07a]. Also, the phase displacement may be related to conventional oscillator parameters, such as phase jitter, by representing phase jitter in units of radians. Additionally, the phase displacement may be directly implemented in phase analyses of PLL and DLL applications. Fig. VII-6 shows an example of a temporary loss-of-oscillation resulting

from an SE in a current-starved inverter, as well as the time perturbation, T_e, used to calculate Φ_{disp}.

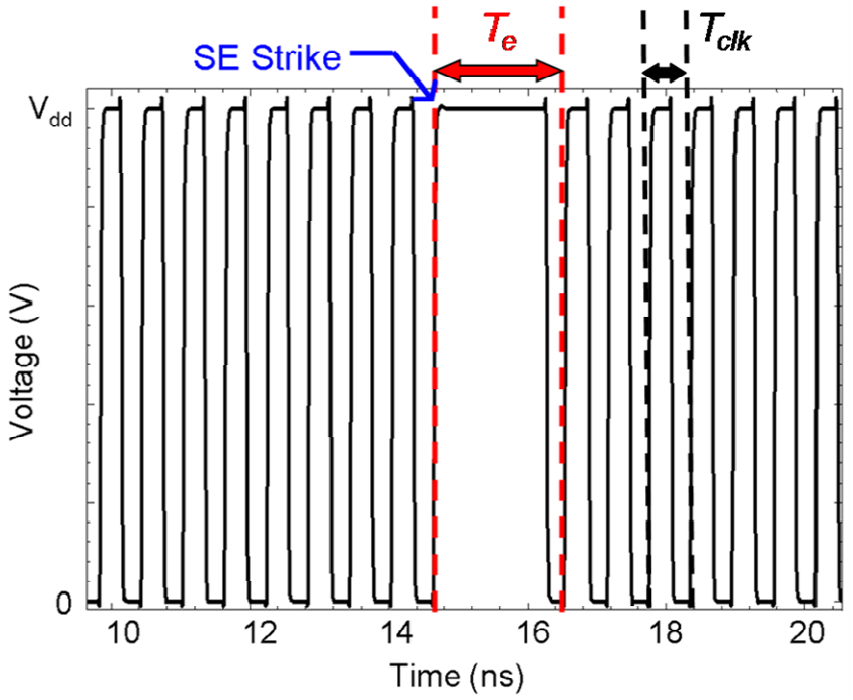


Fig. VII-6. Illustration of the time perturbation, T_e, used to calculate the phase displacement resulting from an SE.

Maximum Phase Displacement

Fig. VII-7 shows the maximum phase displacement and corresponding number of erroneous pulses versus input voltage, V_{inVCO}, following simulated ion strikes in the unhardened VCO and RHBD VCO. The number of erroneous pulses, n, can be related to phase displacement by Eqn. (VII-5) where k is a positive integer.

$$n = k \quad \text{for} \quad 2\pi \cdot k \le \phi_{disp} < 2\pi \cdot (k+1), \; k \ge 0 \tag{VII-5}$$

For example, one erroneous pulse requires at least 2π radians of phase displacement, whereas 2 erroneous pulses require at least 4π radians of phase displacement.

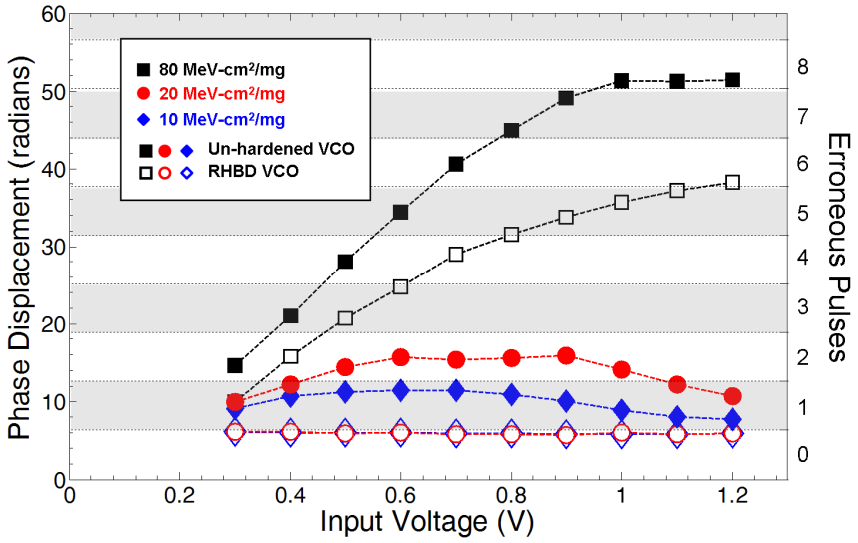


Fig. VII-7. Maximum phase displacement (radians) and corresponding number of erroneous pulses versus input voltage for the unhardened VCO and RHBD VCO. Square, circle, and diamond symbols represent LET values of 80, 20, and 10 MeV-cm^2/mg, respectively. Closed symbols represent the unhardened VCO whereas the open symbols represent the RHBD VCO.

For simulated LET values of 10 and 20 MeV-cm^2/mg, the maximum phase displacement at the output of the RHBD VCO was decreased by approximately 5-6% over that of the conventional VCO. The small decrease in the maximum phase displacement for the RHBD VCO will be further investigated in subsequent sections. The maximum phase displacement at the output of the RHBD VCO was decreased by approximately 30% at an LET of 80 MeV-cm^2/mg. Although the maximum phase displacement for strikes (over all LET values simulated) in the unhardened VCO shows a specific trend versus input-bias that is consistent with that of other work such as [Bo05,

Lo06, Lo07a, Lo07b, Lo07c], the RHBD VCO appears to follow trends typical of combinational logic circuits tested at high data rates [Ha06, Ma04 Su06].

In the case of the RHBD VCO, phase displacement can be directly related to a burst-error that may contain multiple erroneous data bits (e.g. 2π radians of phase displacement is equivalent to 1 erroneous data bit). The largest numbers of erroneous data bits (clock pulses) resulting from strikes in the RHBD VCO were generated from strikes within the majority voter and buffers as SETs generated within in the VCDLs were voted out. Thus, the number of erroneous pulses is expected to follow combinational logic trends versus frequency. At an LET of 80 MeV-cm^2/mg for the RHBD VCO, for example, the maximum phase displacement monotonically increases with increasing input voltage. As the output frequency increases, the number of clock periods that span the SET pulse width increases, subsequently increasing the output phase displacement and number of erroneous clock pulses.

However, at LETs of 10 and 20 MeV-cm^2/mg for the RHBD VCO, the maximum number of erroneous pulses is 1 versus all input voltages simulated. This characteristic has also been shown in SEU error signatures for SiGe logic at high speed data rates [Ha06, Su06]. For the frequency range of the oscillator, the SET pulse widths generated at 10 and 20 MeV-cm^2/mg are less than one clock period, and therefore result in a maximum of 1 erroneous data bit, or approximately 2π radians of phase displacement. A similar effect would occur at an LET of 80 MeV-cm^2/mg for sufficiently low frequencies. Also, at 10 and 20 MeV-cm^2/mg, the maximum phase displacement versus input voltage would monotonically increase for sufficiently high frequencies where the SET pulse width is greater than the period of the operating frequency.

The trends in phase displacement (erroneous data bits) versus frequency observed for strikes in the combinational logic portion of the RHBD VCO suggest that burst-error behavior, previously only observed for high data-rate SiGe logic [Ha06, Ma04, Su06], is also a concern for CMOS combinational logic devices operating at GHz speeds.

A Probabilistic Comparison of the Unhardened and RHBD VCOs

Although the maximum phase displacement is a useful tool in determining the worst-case response of the VCO, it does not provide any information on the likelihood of the large phase displacements following SEs or the distribution of phase displacement values that can be expected. Figs. VII-8 and VII-9, for example, shows histograms of the phase displacements for LET values of (a) 10, (b) 20, and (c) 80 MeV-cm^2/mg at an input voltage of 0.6 V (1.75 GHz) for strikes in each node and at each temporal location simulated. All of the histograms are normalized such that the sum of all bins is equal to one; as a result, the histograms represent a discrete probability density function (pdf) of phase displacement values for a particular operating condition. Fig. VII-8 represents the pdfs for the unhardened VCO, whereas Fig. VII-9 represents the pdfs for the RHBD VCO. It is important to note that if the phase displacement following the strike falls within the normal operating phase jitter, or less than or equal to the calculated noise floor, the maximum phase displacement of the simulation cannot be distinguished from that of the phase jitter due to noise. Thus, the pdf always contains a sub-distribution resembling that of a Gaussian distribution located at the edge of the noise floor. The mean of this distribution is approximately equal to the 3σ value of the phase jitter as calculated previously.

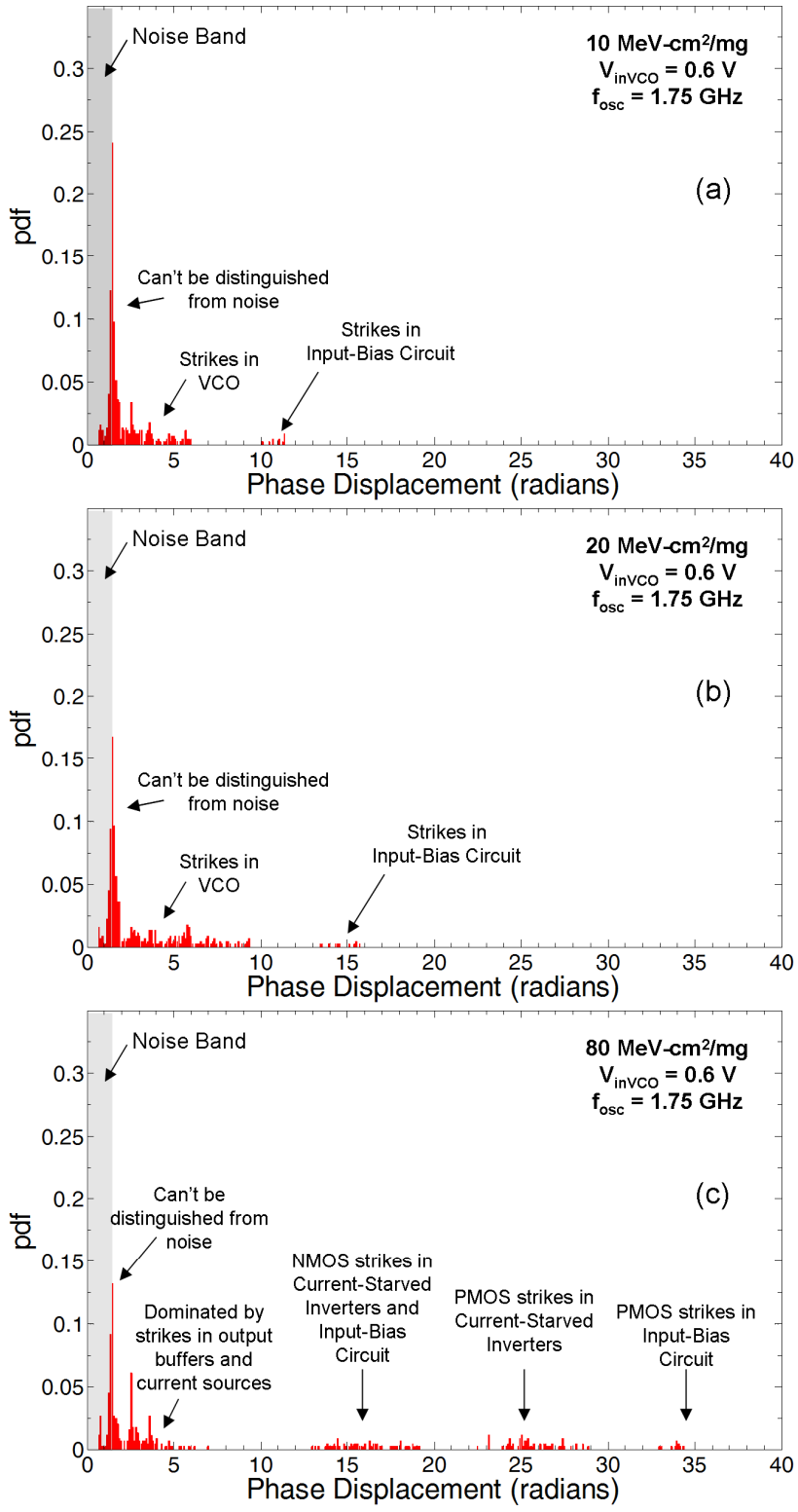


Fig. VII-8. Histograms of maximum phase displacement (radians) for the unhardened VCO at various LET (MeV-cm^2/mg) for an input voltage of 0.6 V, corresponding to a frequency of 1.75 GHz. All histograms are normalized so that the total area is 1, so as to represent the discrete pdf of phase displacement.

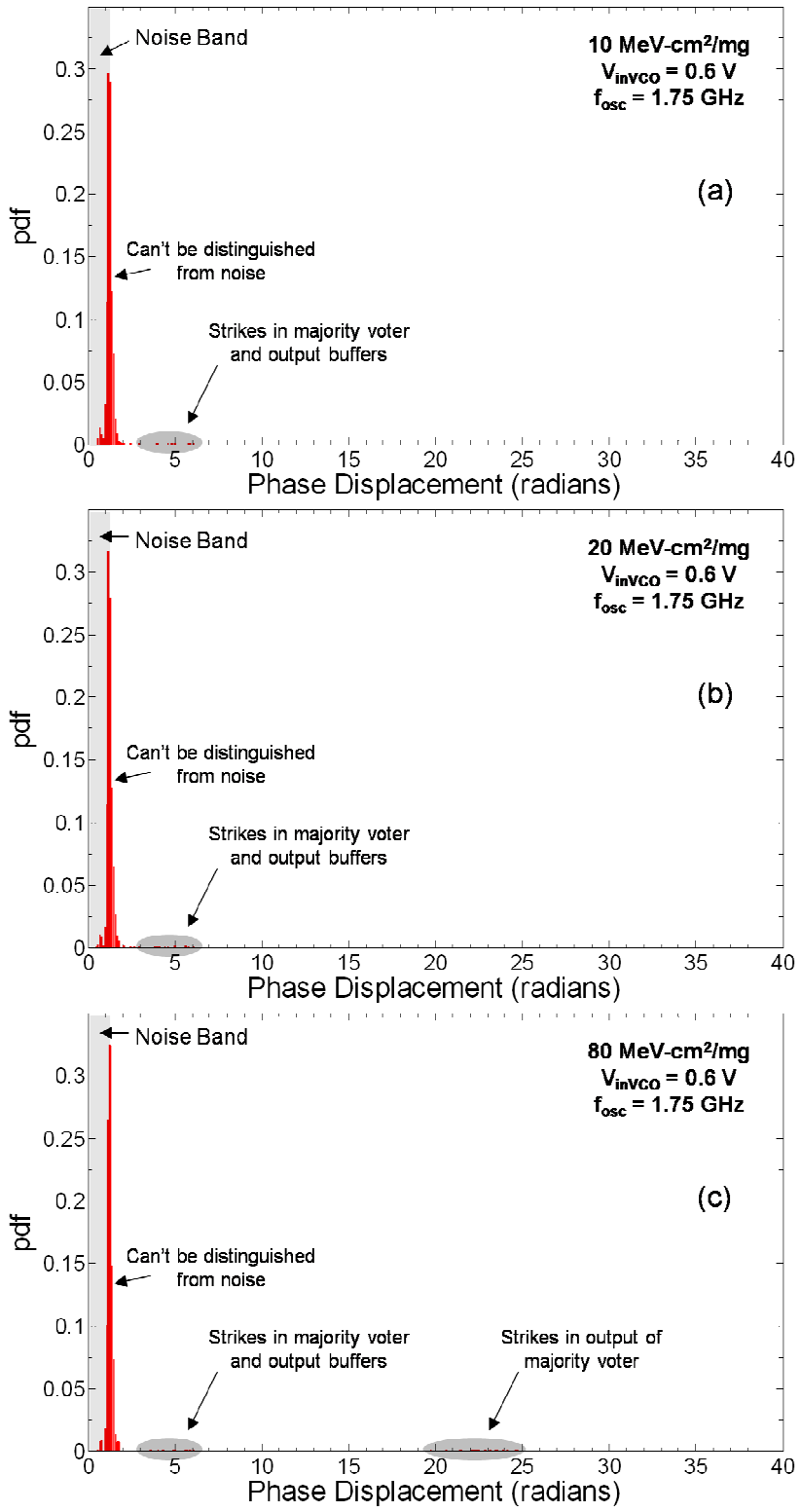


Fig. VII-9. Histograms of maximum phase displacement (radians) for the RHBD VCO at various LET (MeV-cm^2/mg) for an input voltage of 0.6 V, corresponding to a frequency of 1.75 GHz. All histograms are normalized so that the total area is 1, so as to represent the discrete pdf of phase displacement.

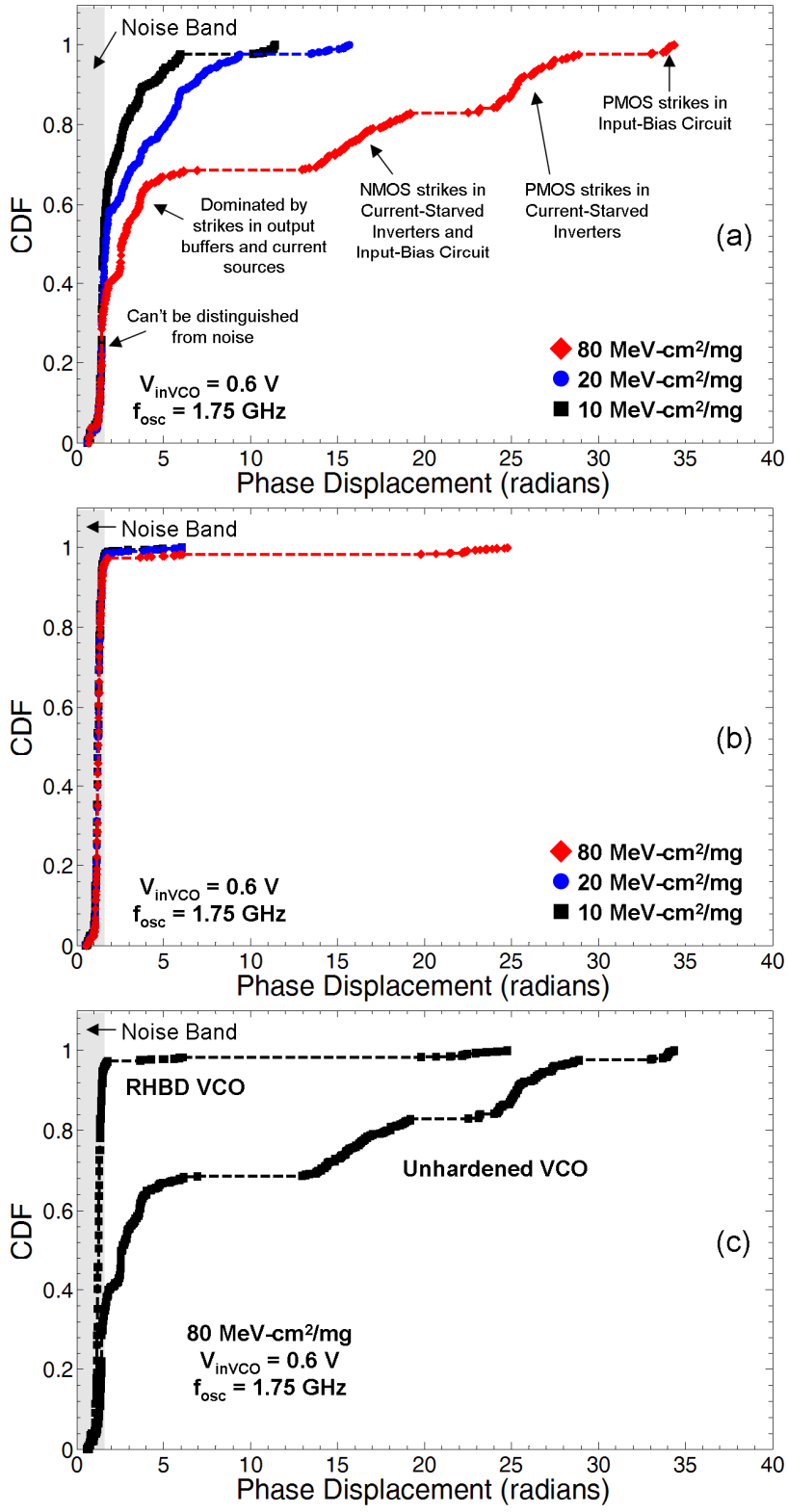


Fig. VII-10. Empirical Cumulative Distribution Functions (CDF) of phase displacement (radians) for the (a) unhardened VCO and (b) RHBD VCO for various LET at an input voltage of 0.6 V. (c) Also shown is a direct comparison of the two circuits at 80 MeV-cm^2/mg and an input voltage of 0.6 V.

Furthermore, for the unhardened VCO (shown in Fig. VII-8), there are numerous data points that lie outside the noise band. The outliers in Fig. VII-8 (a) and (b) visually group into two distinct clusters; the largest phase displacement values were a result of strikes in the input-bias circuit. At the maximum LET simulated, as seen in Fig. VII-8 (c), the outliers are visually segmented into well-defined clusters representing the phase displacement following strikes in the input-bias circuit, current sources, or current-starved inverters. Moreover, the results indicate that the largest transients at the center frequency are generated by strikes on the PMOS devices within the input-bias circuit. This further emphasizes the importance that each VCDL line should contain its own bias circuitry in order to eliminate the largest transients.

In contrast, the pdfs for the RHBD VCO, (Fig. VII-9), do not contain clustered outliers. First, the near-Gaussian distributions on the left-most portion of the histograms have approximately the same mean value equal to that of the 3σ value of the phase jitter, further indicating that the values comprising the distribution are a result of normal phase jitter due to noise. Additionally, the few outliers are all due to strikes in the majority voter circuit or the output buffers. The largest phase displacement values for an LET of 80 MeV-cm^2/mg are a result of PMOS strikes on the output node of the majority voting circuit. The phase displacement for strikes on the output node of the majority voter may be reduced by increasing the nodal capacitance; however, the oscillating frequency will subsequently decrease and must be compensated for by increasing the current drive within the delay chains. As described in detail in section V-B, the output phase displacement for LET values of 10 and 20 MeV-cm^2/mg never takes on values greater than 2π radians because the generated SET pulse widths are never greater than a single

clock period. For operating frequencies such that the clock period is on the order of the SET pulse width or less, the output phase displacement is expected to increase.

Although the histograms provide detailed information as to the relative density of phase displacements and the physical location of the strikes responsible for the various phase displacements, cumulative distribution functions[1] (CDFs) of phase displacement provide an estimate of the likelihood of a particular value occurring. CDFs were calculated empirically for the simulations of strikes in every node within each VCO and are displayed in Fig. VII-10. As expected, as the LET is increased from 10 MeV-cm^2/mg to 80 MeV-cm^2/mg for the unhardened VCO, the CDF curve translates to the right (Fig. VII-10 (a)), indicating an increased probability of encountering larger phase displacements as the LET is increased. Additionally, the clusters of phase displacement values resulting from strikes in the various components of the VCO can be visualized by the break-points in the CDF curve. The CDFs for the RHBD VCO (Fig. VII-10 (b)), however, do not translate, but remain relatively constant versus LET, indicating that the majority of the strikes do not result in a phase displacement greater than the noise floor. In fact, the probability that the output phase displacement is below the noise floor is approximately 0.95, indicating that no additional hardening of the VCO is necessary unless the phase noise of the circuit can be reduced significantly. Fig. VII-10 (c) directly compares the CDFs of phase displacement for the unhardened and RHBD VCOs at 0.6 V and 80 MeV-cm^2/mg.

It is important to note that these calculations assume that each node within the VCO is equally likely to be struck by a heavy-ion. Further refinement of the estimations can be

[1] The cumulative distribution function (CDF) is also termed probability distribution function (PDF) in some texts [St02a]. The probability density function (pdf) is the derivative of the CDF, or inversely, the CDF is the integral of the pdf.

made by weighting each node by the physical dimensions of the sensitive area. However, a first-order estimation of the likelihood of phase displacement values can be obtained. These simulation results and calculations illustrate that not only significant improvement in SET tolerance can be obtained by implementing the RHBD technique presented, but detailed knowledge of the complex distributions of the generated transients may be obtained by utilizing the presented analysis technique.

Experimental Validation of Analysis Technique

The probabilistic analysis and simulation techniques have been experimentally validated on a similar unhardened VCO topology designed in the IBM 130 nm CMRF8RF CMOS technology available through the MOSIS foundry. Experiments were performed on the VCO circuit using laser-induced carrier generation based on two-photon absorption (TPA) [Bo86, Mc02, Mc03, St85] for SET error signature characterization.

The TPA experimental setup is described in [Bo86, Lo07b, Mc02, Mc03, St85]. The DUT includes an unhardened VCO shown in [Lo06, Lo07b] (see Fig. II-18) designed with eleven current-starved inverter stages for a center frequency of 200 MHz and a maximum frequency of approximately 455 MHz. In order to capture SETs following a laser strike within the VCO a Tektronix-TDS6124C oscilloscope sampling at 20 GS/s was used. The oscilloscope was set to trigger on the rising edge of the laser pulse, and the FastFrame™ feature of the oscilloscope was utilized to capture 100 transients per strike location. Furthermore, 2000 SETs were captured following laser strikes within the input-bias circuit and current-starved inverter stages. All experiments

were performed at incident laser energy of 12 nJ and at the VCO's maximum frequency of approximately 455 MHz[2].

Figs. VII-11 and VII-12 illustrate the pdf and CDF of the phase displacement values following the laser strikes within the VCO. In Fig. VII-11 (a) the bins of the histogram (normalized to represent the discrete pdf) are color-coded by the region of the laser strike. For example, the phase displacement values resulting from strikes in the input-bias circuit are colored red and occupy the upper portions of each bin. Phase displacement values resulting from strikes between the input-bias circuit and the current-starved inverter stages are colored yellow, and the blue portions represent phase displacement values resulting from strikes in the current-starved inverters. The color bar indicates the colors and the corresponding circuit components. As previously described, the distribution of phase displacement values includes a near-Gaussian distribution on the left portion of the pdf and represents the peak expected phase error due to noise. To further emphasize this, Fig. VII-11 (b) illustrates the portion of the distribution representing the peak phase error due to noise. The mean value of this near-Gaussian distribution is approximately 1.55 ns (4.3 radians) and was verified by removing the laser and measuring the peak jitter of the VCO due to noise. Additionally, strikes in the input-bias circuit resulted in a secondary peak in the right-hand side of the overall distribution of phase displacements, as indicated by the red-yellow portion. For this particular VCO at 455 MHz, laser strikes in the current-starved inverters resulted in the worst-case response.

[2] See Chapter IX: Operating the PLL at the VCO's maximum frequency will result in worst-case negative frequency modulations and will minimize positive frequency modulations.

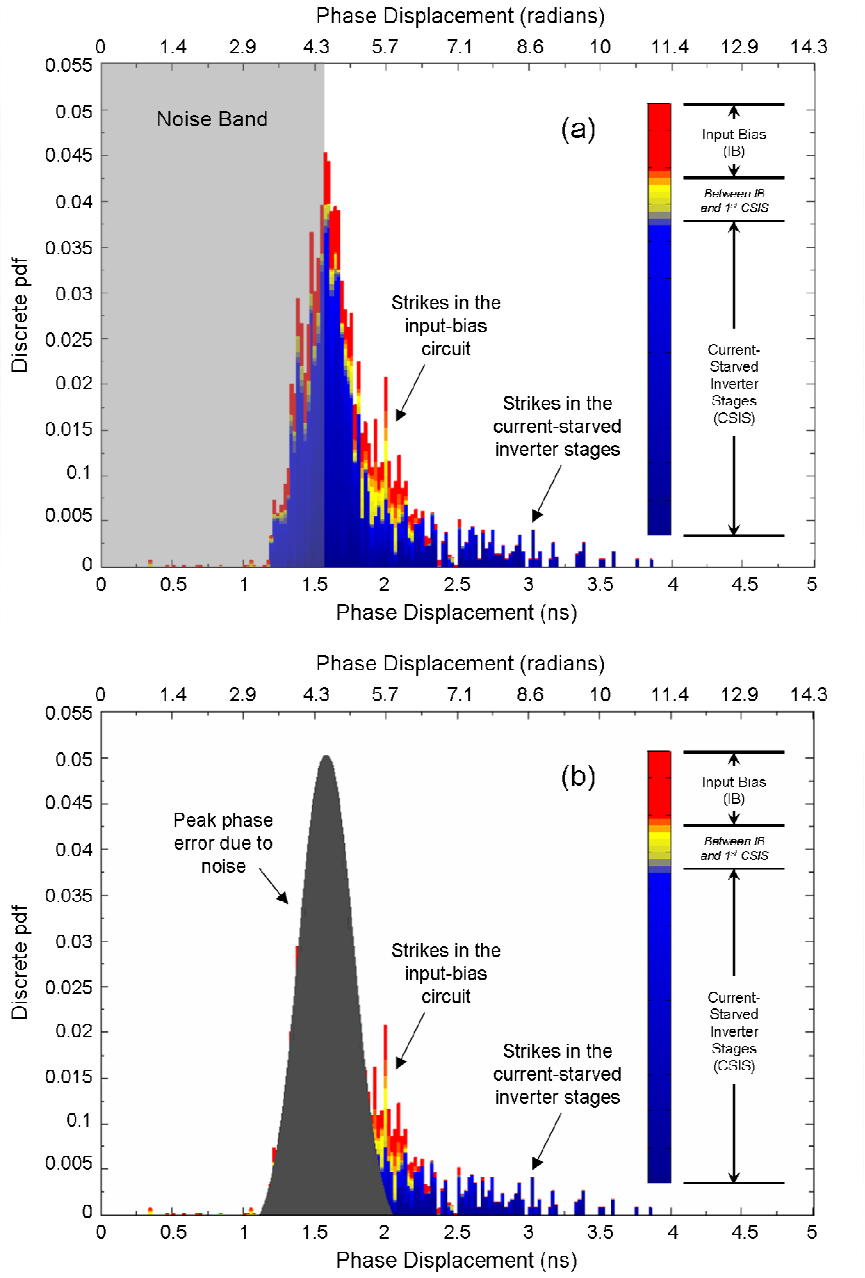


Fig. VII-11. (a) Histogram of phase displacement (radians) obtained from TPA laser experiments at incident energy 12 nJ for the 130 nm unhardened VCO. The histogram is normalized so that the total area is 1, so as to represent the discrete probability density function (pdf) of phase displacement. (b) Histogram identifying the contributions due to noise and laser strikes in the VCO.

The CDF of phase displacement values following laser strikes is shown in Fig. VII-12. Similar to the curves in Fig. VII-10 the CDF increases rapidly at

approximately the noise floor value of 1.55 ns (4.3 radians). Slight break-points in the CDF curve occur at approximately 1.8 ns and 2.5 ns and indicate the contributions of strikes in input-bias stage and current-starved inverter stages to the overall distribution of phase displacement values, respectively. Furthermore, the CDF indicates that approximately 95% of all strikes will result in phase displacements of 2.6 ns (7.3 radians) or less.

While validating the simulation and analysis techniques subsequently presented, these experimental results show the complex nature of the distribution of SETs within the VCO and highlight the importance of a full characterization of the SETs in order to determine the SE response of the circuit.

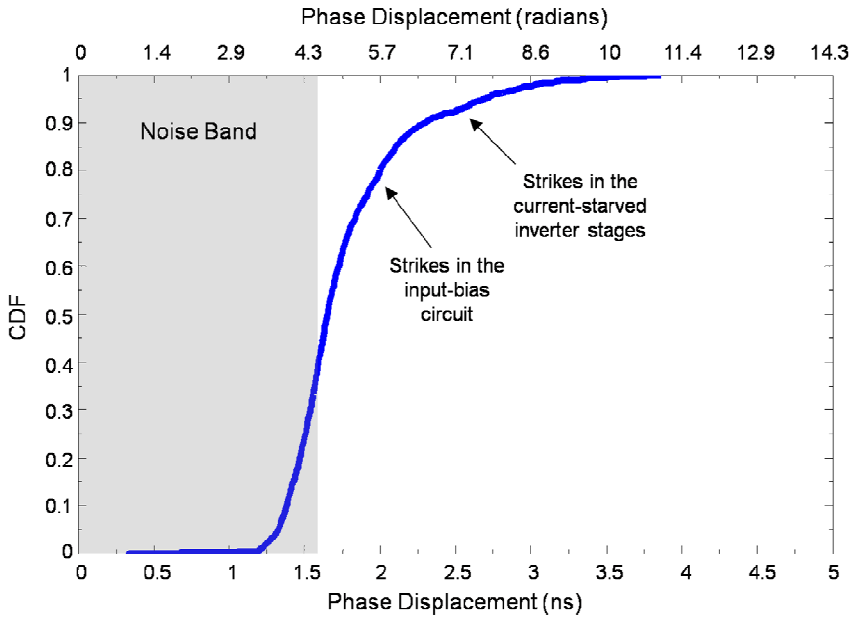


Fig. VII-12. Cumulative Distribution Function (CDF) of phase displacement (radians) obtained from TPA laser experiments at incident energy 12 nJ for the 130 nm unhardened VCO.

Design Tradeoffs

Though implementing the RHBD technique as described throughout this chapter can result in a maximum improvement in SET susceptibility and performance, certain electrical performance and design tradeoffs such as area and power must be considered. As the VCDL for the VCO is implemented in a triple-modular redundancy scheme, the area and average power dissipation for the VCDL portion of the VCO will be tripled. Also, the addition of the buffers and majority voting circuit will also add a power and area penalty depending on the number of extra buffers and the dimensions of the majority voter chosen. Therefore, the area penalty of the RHBD VCO design will be slightly greater than three times the original specifications. The power, however, due to the addition of the buffers and majority voter will dominate the overall power of the VCO as the combinational logic used in the circuits contains full drive strength and dissipates a much greater current over the current-starved inverters. The actual dynamic power dissipation of the RHBD design implemented in this paper at 1.75 GHz operation is approximately 876 μW, whereas the unhardened VCO dissipates approximately 70 μW of power.

Moreover, the power and area penalty of the hardening scheme may also vary depending on the application for which it is implemented. For example, in a PLL application with an on-chip loop filter, the overall area penalty of implementing the RHBD VCO will not be significant when compared to the total area of the passive components necessary for the loop filter. The primary tradeoff will therefore be the increased power dissipation, as the VCO circuit typically dominates the overall power dissipation of the PLL.

Conclusion

A probabilistic analysis technique has been presented and experimentally verified that effectively identifies the origins of a variety of transients generated within a circuit topology. Specific details of the transients generated throughout the circuit may also be extracted from the measurements and can provide a circuit designer with insight into where and when to apply hardening schemes within a topology. The analysis technique provides a first-order estimation of the likelihood of the various transients occurring. All techniques can be readily applied to all analog topologies.

Using the analysis technique presented, an RHBD voltage-controlled oscillator has been presented for SET mitigation that maximally reduces the output phase displacement following strikes in the VCO to below the normal operating noise floor. Although the RHBD VCO increases the required area and power, the phase jitter due to supply noise and device variations/mismatch is reduced. The RHBD technique can be readily implemented within any mixed-signal PLL and DLL application.

CHAPTER VIII

ANALYSIS OF SINGLE-EVENT TRANSIENTS IN INTEGER-N FREQUENCY DIVIDERS AND IMPACTS ON PHASE-LOCKED LOOP PERFORMANCE

Introduction

In practice most PLL topologies include a variation of the basic topologies presented thus far; common PLL variants include frequency dividers in various locations including the feedback path for frequency synthesis and multiplication applications, as well as at the PLL output and input [Ba08, Be98, Ga79, Ga05]. Therefore, examining SETs in frequency dividers is essential for the understanding of SET generation and propagation in PLLs. In fact, Hafer *et al.* recently showed data indicating that both the location and gain of the frequency divider(s) in the PLL configuration strongly influence the predicted error rate of PLLs [Ha08].

This chapter analyzes the SET signatures of an integer-*N* frequency divider topology in a 90 nm CMOS bulk process. A single divide-by-*2* circuit is analyzed for various input frequencies ranging from 31 MHz to 2 GHz in order to establish the SET vulnerability of each stage within the divide-by-*N* topology. Also, an analytical analysis of SET propagation through the divider network is provided, and identifies the SET bottleneck of the integer-*N* frequency divider from a probabilistic point-of-view. The impacts of feedback and input/output (I/O) frequency dividers on the SET vulnerability of the PLL are also discussed. Finally, experimental measurements on a programmable PLL designed in a commercial 250 nm CMOS technology are provided and corroborate the discussed analyses.

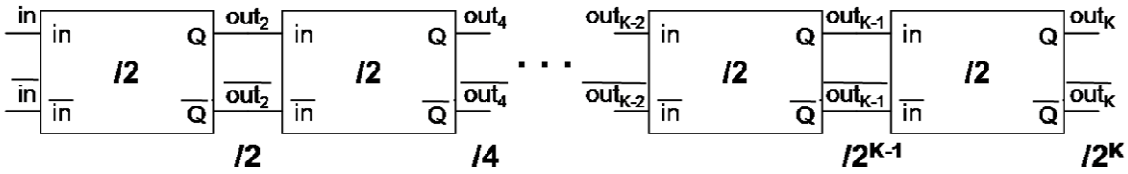


Fig. VIII-1. Integer-*N* frequency divider achieving divisors of $N = (2, 2^2, \ldots, 2^i, 2^{i+1}, \ldots, 2^K)$.

Integer-*N* Frequency Divider Topology

The integer-*N* frequency divider used in this chapter consists of a cascade of *K* divide-by-*2* circuits as shown in Fig. VIII-1. The circuit accepts an oscillatory signal (and its compliment) and divides the frequency of the signal by factors of two; thus the divisor (*N*) is 2^K for *K* divide-by-*2* stages. Each divide-by-*2* stage is achieved by implementing two D-Flip-Flops (DFF) in the fashion shown in Fig. II-21 (Chapter II), where the complementary output of the second DFF is connected to the D input of the first DFF [Ra95]. The first DFF in the divide-by-*2* circuit functions as a master stage, latching the D input (complementary Q output signal) on the rising edge of the input signal. The second DFF operates as a slave stage latching the output of the master stage (XDFF1[3]) on the falling edge of the input signal (rising edge of the complementary input signal). Therefore, node XDFF1 changes state (from logic-low to logic-high, or vice versa) at each rising edge of the input signal (in) and the Q output of the second DFF changes state each time the rising edge of the complementary input signal arrives, achieving a frequency division of exactly two. Each DFF is implemented using CMOS NAND gates, as shown in Fig. VIII-2; however, the single-event analysis presented in

[3] As a convention we will denote the output node of the first DFF in each divide-by-*2* stage as XDFF{*K*}, where {*K*} is the number of the divide-by-*2* circuit in the divide-by-*N* chain. For example, the node will be labeled XDFF1 within the first divide-by-*2* circuit and XDFF2 within the second divide-by-*2* circuit.

this work is applicable to all divide-by-*2* circuit topologies and is not restricted to the particular configuration illustrated in Figs. II-21 and VIII-2.

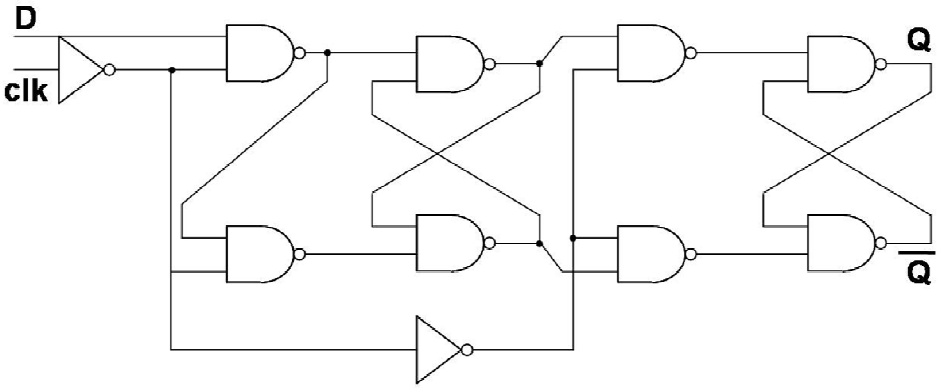


Fig. VIII-2. Schematic of the CMOS DFF used in the divide-by-*2* topology.

Single-Event Transient Simulations and Measures

The integer-*N* frequency divider was designed using the IBM 90 nm 9SF PDK and consists of seven divide-by-*2* stages such that divisors of 2, 4, 8, 16, 32, 64, and 128 may be achieved. Simulations were performed using the CADENCE EDA tool suite, the Spectre Environment, and the ACCRE computing cluster at Vanderbilt University [ACCRE]. Ion strike current profiles were obtained from 3D-TCAD simulations on device models calibrated to the 9SF PDK [Da07b]. All simulation techniques have been experimentally calibrated using laser two-photon absorption (TPA) on PLL and VCO topologies [Lo08, Lo07b]. In fact, through identical techniques, Loveless *et al.* predicted and experimentally measured a 2.3 orders of magnitude improvement in SET response by a radiation-hardened-by-design (RHBD) charge pump PLL over its conventional counterpart [Lo06, Lo07b].

SET simulations were performed on a stand-alone divide-by-*2* circuit across four parameters, requiring a total of 12,936 simulations: the input frequency, the node of the simulated ion strike, the temporal location of the strike with respect to the input/output signal, and the simulated ion strike's linear-energy-transfer (LET) value. Input frequencies ranging from 2 GHz to 31 MHz by factors of two were used in order to establish frequency dependencies on the SET vulnerability (analogous to the divide-by-*2* stage number within the divider chain). Also, for pMOS and nMOS transistors connected to a common node, simulations were performed for strikes on the pMOS and nMOS diffusion areas separately. Finally, eleven temporal locations of the ion-strike (at four LET values of 1, 10, 20, and 80 MeV-cm^2/mg) spanning the period of the output signal (consequently spanning the period of the input signal) were chosen. The output phase displacement (Φ_{disp}) following the ion strike was measured for each simulation.

Single-Event Transient Response of a Stand-Alone Divide-by-2 Circuit

Phase Transients in a Divide-by-2 Circuit

SEs in a divide-by-*2* circuit can result in latched upsets at the outputs of either DFF. Assuming the ion-induced voltage pulse is shorter in duration than the pulse width of the input signal, the latched upset will remain on the outputs of the DFF(s) until the state of the input signal changes allowing for the latches to be reset. For cases where the ion-induced voltage pulse is longer in duration than the input signal's pulse width, consecutive latched upsets may be present in the output signal. This temporary latching behavior results in an apparent stretching or compression in the output signal. The

resulting phase transient, or change in output phase displacement versus time, at the output of the divider stage may be quantified by calculating the maximum Φ_{disp}.

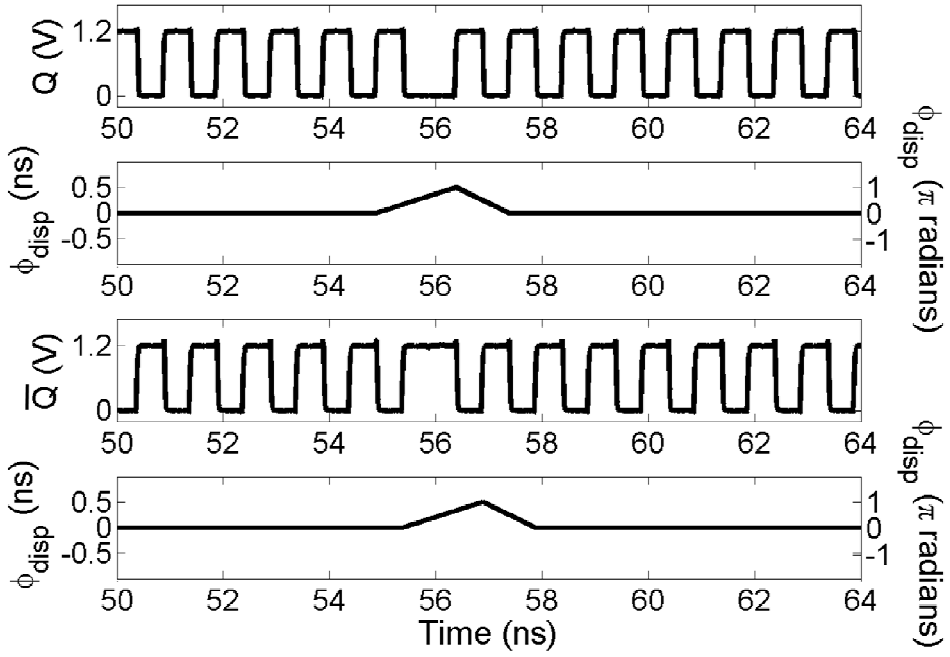


Fig. VIII-3. An example of two identical phase transients on the outputs of a single divide-by-*2* circuit. Input frequency is 2 GHz resulting in an output frequency of 1 GHz. Peak of transient reaches a Φ_{disp} of 500 ps (π radians).

One example of two such phase SETs resulting from a single strike within the divide-by-*2* circuit is shown in Fig. VIII-3, along with the measured Φ_{disp} versus time (in units of ns and π-radians). The input and output frequencies are 2 GHz and 1 GHz, respectively. The SETs on the Q output and its compliment are a result of a single pMOS strike on XDFF1 (indicated in Fig. II-21) with an LET of 20 MeV-cm^2/mg. The ion strike results in latched events on both outputs that are reset after 500 ps (one half of the output signal's period of 1 ns). The peak of the measured phase displacement is 500 ps (π radians) for both outputs.

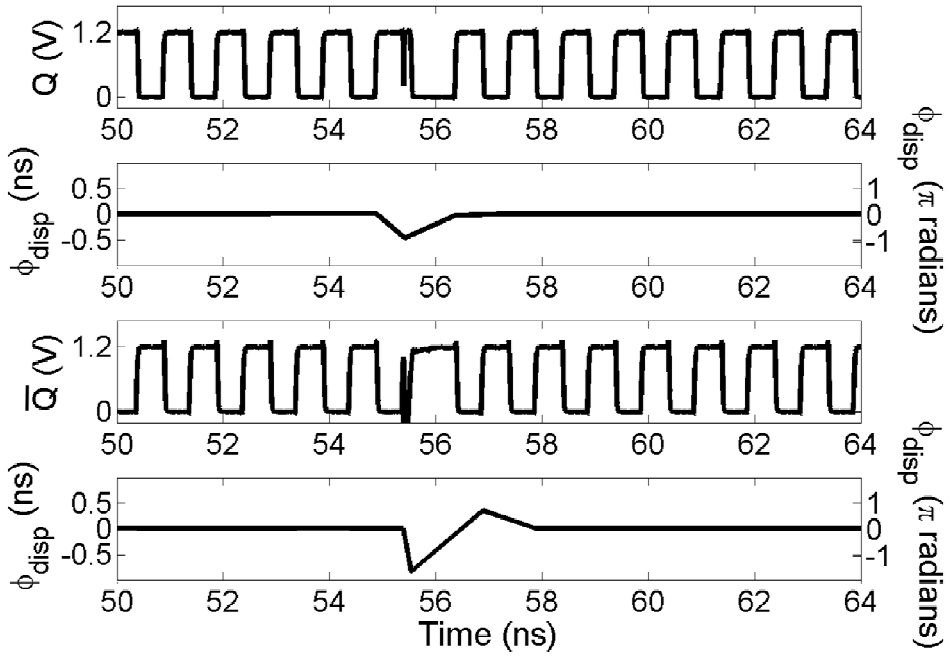


Fig. VIII-4. An example of two non-identical phase transients on the outputs of a single divide-by-*2* circuit. Input frequency is 2 GHz resulting in an output frequency of 1 GHz. Peak of transient approaches a Φ_{disp} of -1 ns (-2π radians).

Single-events in the divide-by-*2* circuit can also result in non-identical transients on the Q and complementary-Q outputs, as shown in Fig. VIII-4. The transients illustrated in Fig. VIII-4 result from a single strike (LET of 20 MeV-cm^2/mg) on an nMOS device connected to the complementary-Q output node. The strike causes an initial glitch on the complementary-Q output, followed by a latched upset. The output phase is modulated from approximately -2π radians to π radians.

A Probabilistic Analysis of Single-Event Phase Transients in a Divide-by-2 Circuit

In order to quantify the transients and to provide an indication of the probability of the generation of the transients, cumulative distribution functions (CDFs) of the absolute value of the maximum phase displacement ($|\Phi_{disp}|$) were calculated empirically from the

simulations of strikes on every node within the divide-by-*2* circuit. As shown in [Lo08], high-performance mixed-signal topologies may have extremely complex transient distributions. CDFs provide an estimate of the likelihood of a particular range of values occurring, as well an illustration of the distribution(s) of phase-displacement values under various operating conditions. The CDF represents the probability of an ion strike resulting in a given phase displacement value or less.

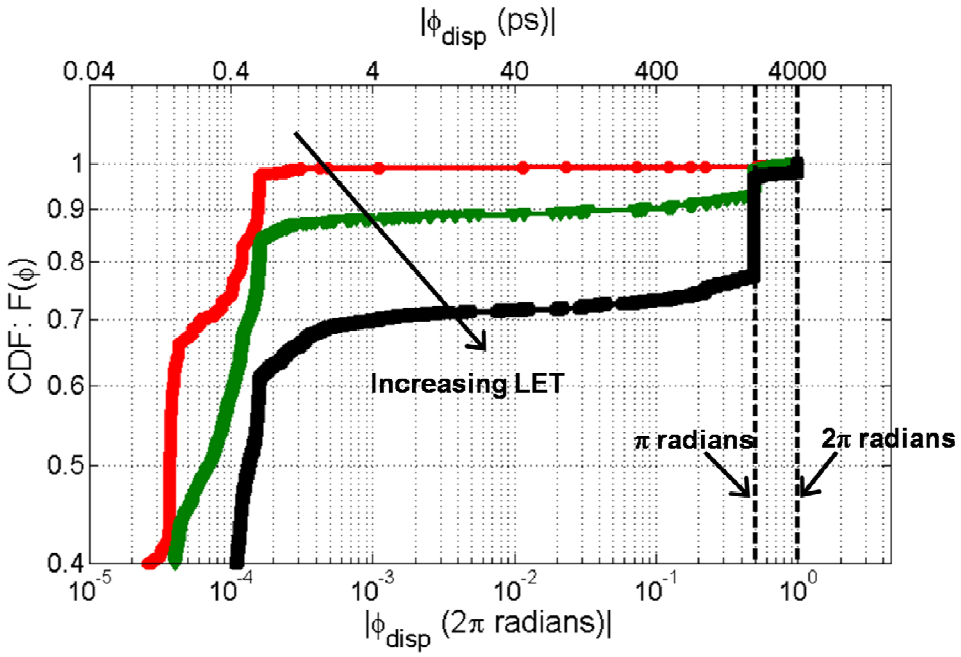


Fig. VIII-5. Empirical CDFs of the $|\Phi_{disp}|$ (units of 2π radians and ps) for strikes (LETs of 1, 20, and 80 MeV-cm^2/mg) in the divide-by-*2* circuit. Input and output frequencies are 500 MHz and 250 MHz, respectively.

Fig. VIII-5 shows the simulated CDF curves for SE hits at three different LET values (1, 20, and 80 MeV-cm^2/mg) and at an input frequency of 500 MHz. First, as the LET value increases the CDF translates down, as expected, indicating an increased likelihood of obtaining larger phase displacement values. Second, there exists a sharp increase in

the CDF curves as $|\Phi_{disp}|$ approaches π radians (2 ns for an output frequency of 250 MHz). The majority of strikes that result in a phase displacement of exactly π radians are due to strikes in the first DFF.

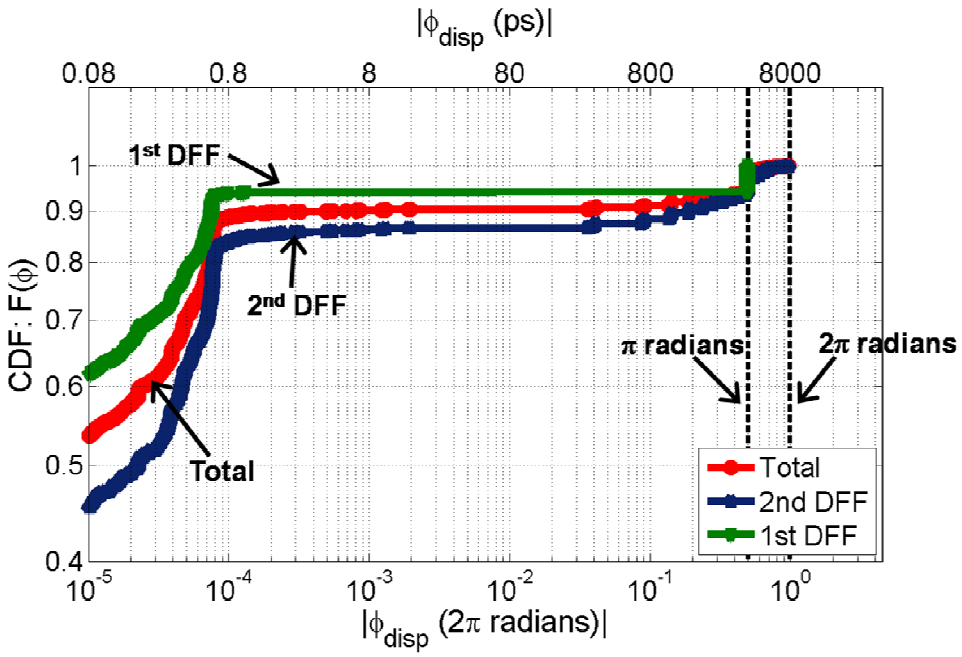


Fig. VIII-6. Total empirical CDF of the $|\Phi_{disp}|$ (units of 2π radians and ps) for strikes (LET of 20 MeV-cm^2/mg) in the divide-by-*2* circuit. Empirical CDFs for strikes in the 1st and 2nd DFF stages are also shown. Input and output frequencies are 250 MHz and 125 MHz, respectively.

In fact, as shown in Fig. VIII-6 where the CDF curves for strikes (LET of 20 MeV-cm^2/mg) in individual DFF components are constructed individually for an input frequency of 250 MHz, no strikes in the first DFF result in Φ_{disp} values of greater than π radians. This is due to the fact that XDFF1 is always reset at the period of the input signal, which is one-half the period of the output signal, or π radians. Moreover, for all LET values simulated (Fig. VIII-5), the phase displacement has an upper bound of 2π, meaning that the ion-induced current never perturbs more than a single clock period (two

pulse widths). The CDF upper bound indicates that the ion-induced current pulses (at the LET values simulated) do not deposit enough charge to incorrectly latch data for more than the period of the output signal with a frequency of 250 MHz.

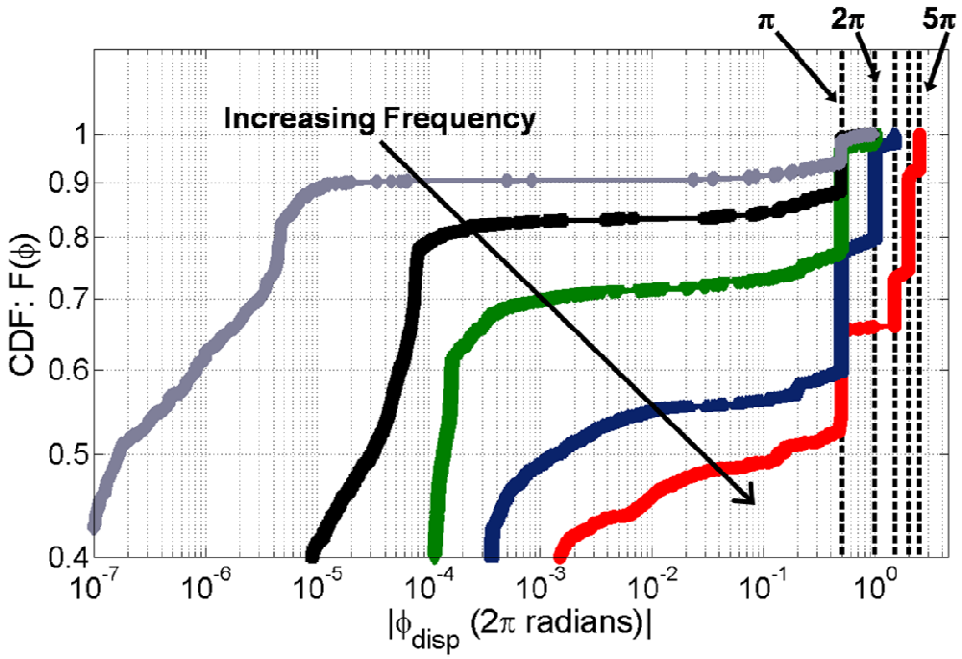


Fig. VIII-7. Empirical CDFs of phase displacement (units of 2π radians) for strikes (LET of 80 MeV-cm^2/mg) in the divide-by-2 circuit for input frequencies of 31 MHz, 250 MHz, 500 MHz, 1 GHz, and 2 GHz.

Fig. VIII-7 shows the CDF curves for various input frequencies (62 MHz, 250 MHz, 500 MHz, 1 GHz, and 2 GHz) at an LET of 80 MeV-cm^2/mg. As the input frequency increases, the CDF curve translates to the right and down indicating an increased probability of a given range of phase displacement values for higher operating frequencies. This result is consistent with a window-of-vulnerability approach for determining the probability of a SET being latched. Although this result provides no indication of how an SET will propagate through a divider network (a cascade of divide-

by-*2* stages), it does suggest that the smallest possible divisor of a divide-by-*N* circuit will result in the largest probability of an ion strike resulting in a given range of phase displacement values.

Additionally, Fig. VIII-7 shows that the phase displacement for all input frequencies simulated at 500 MHz and less are upper-bounded by 2π radians. As frequency increases, the time-width of the cycles decreases while the pulse width of the ion-induced voltage remains constant. Therefore, the results indicate that the width of the ion-induced voltage pulse is no greater than the period at 500 MHz. At 1 GHz and above, however, the phase displacement is bounded by 3π and 5π, respectively, indicating that the ion-induced current pulse deposits enough charge to incorrectly latch data over multiple data pulses (or clock cycles).

Impacts of Frequency Dividers on the SET Response of the Phase-Locked Loop

General PLL Topology

Fig. VIII-8 illustrates the general block diagram of a common PLL configuration including the phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), feedback frequency divider (β=1/*N*), and output divider (1/*M*). As detailed in Chapter II, charge pumps are typically used in conjunction with PFDs to detect and convert a phase and/or frequency difference between the input reference signal (V_{REF}) and the PLL's feedback signal (V_{FB}) into an electrical current. The PFD generates a pulse on the UP/DOWN signal lines whenever V_{FB} lags/leads V_{REF} in phase. The generation of a signal on the UP/DOWN line will activate the CP to

source/sink current to/from the LPF, adjusting the voltage, V_{inVCO}, applied to the input of the VCO, thus modifying the output frequency of the VCO [Ba08, Be98].

The rate at which the PLL can track and lock an input signal (i.e., acquisition time) depends on the natural frequency, damping factor, and input frequency step [Ga05]. Although the feedback factor affects the natural frequency and damping factor, the internal loop characteristics (voltage and frequency step per loop cycle) change proportionally; therefore, the acquisition time of the PLL is independent of the feedback divisor. However, increasing the feedback divisor does decrease the damping factor of the loop, thus modifying the settling characteristics and increasing the jitter during the lock state.

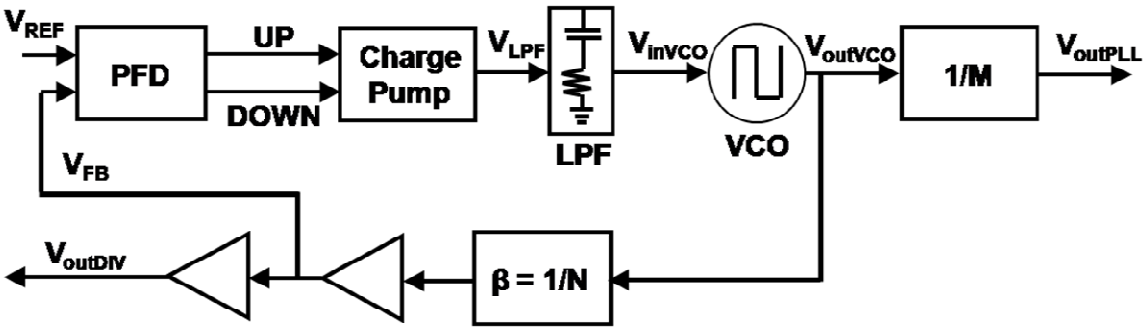


Fig. VIII-8. General block diagram of the PLL circuit including the phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO), feedback frequency divider (β=1/N), output frequency divider (1/M), and buffers.

SET Propagation through a Stand-Alone Divide-by-N Circuit (I/O Frequency Divider)

1) Theoretical and Simulation Analyses

As the output frequency (ω_{out}) of a divider network equals the input frequency (ω_{in}) divided by the divisor (M), the relationship between the instantaneous output phase and input frequency/phase may be established (Eqn. (VIII-1)).

$$\phi_{\text{out}}(t) = \frac{1}{M}\int_0^t \omega_{in}(\tau)d\tau = \frac{\phi_{in}(t)}{M} + \phi_{out}(0) \qquad \text{(VIII-1)}$$

Assuming $\Phi_{out(0)}$ is small, Eqn. (VIII-1) states that the output phase is merely the input phase divided by M. For a divisor (M) of 16, for example, the output phase will be $1/16^{\text{th}}$ that of the input phase.

The results presented in Fig. VIII-7 indicate that frequency dividers are more vulnerable for increasing frequencies, suggesting that the first output divider stage will produce the largest phase displacement. However, Eqn. (VIII-1) states that phase is divided as the signal propagates through the divider chain. Depending on the desired divisor ($M=2^K$), an erroneous transient generated within the i^{th} divide-by-*2* stage (assuming $i < K$) must propagate through the remaining K-i stages. Thus, the phase error at the output of the divider may be determined by Eqn. (VIII-2), where Φ_i is the phase error generated at the i^{th} divide-by-*2* stage and Φ_K is the resulting phase displacement at the output of the K^{th} stage.

$$\phi_K(t) = \frac{\phi_i(t)}{2^{K-i}} + \phi_K(0) \qquad \text{(VIII-2)}$$

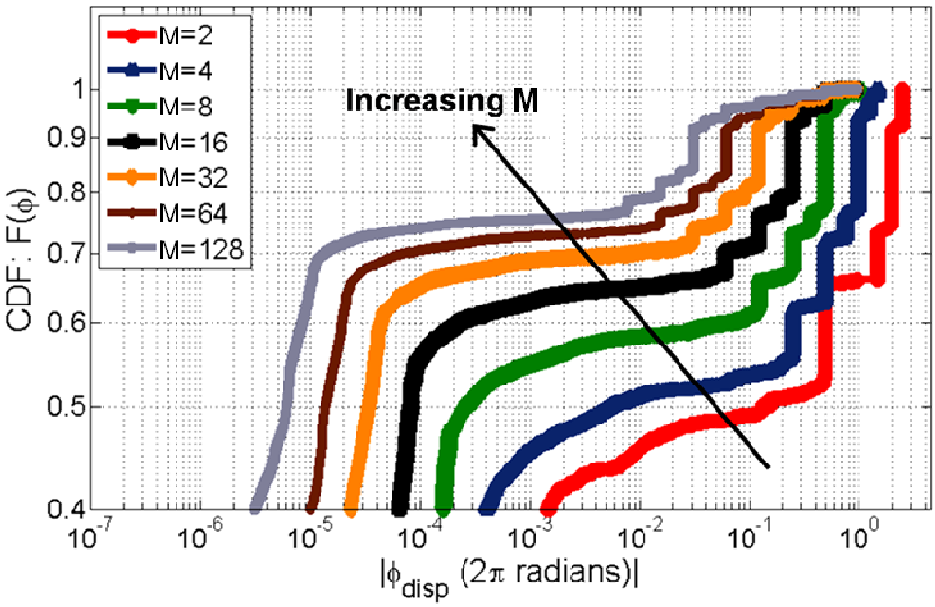


Fig. VIII-9. Empirical CDFs of phase displacement (units of 2π radians) for strikes (LET of 80 MeV-cm^2/mg) in the divide-by-*M*.

This phenomenon is illustrated in Fig. VIII-9 where the CDF of phase displacement values for various divisors (*M*) in a divide-by-*M* circuit are displayed for ion strikes with an LET of 80 MeV-cm^2/mg. The input frequency is 2 GHz for each case, resulting in output frequencies given by 2/*M* GHz. The CDF curves were generated by projecting the simulation results for a single divide-by-*2* circuit over various operating frequencies to the analogous stage number in the divide-by-*M* circuit, and utilizing Eqn. (VIII-2) to describe the propagation of transients through the divider chain. For an *M* equal to 4, for example, there are two active divide-by-*2* stages. The input frequency to the first stage is 2 GHz whereas the input frequency to the second stage is 1 GHz, resulting in an output frequency of 500 MHz. Therefore, the simulation results for a divide-by-*2* circuit for input frequencies of 2 GHz and 1 GHz represent the phase displacements at the outputs of the first and second stages, respectively. Moreover, the phase displacements generated

within the first stage must propagate through the remaining stage and are therefore divided by 2 before reaching the output.

The results presented in Fig. VIII-9 indicate that increasing the divisor (*M*) decreases the probability of strikes in the divider chain resulting in a given range of phase errors at the divider's output. Therefore, for stand-alone frequency dividers such as those that are external to the closed-loop PLL (I/O dividers), increasing *M* is expected to decrease the probability of an ion strike resulting in a given range of phase displacements. This result is consistent with data presented in [Ha08] showing a decreasing error rate for increasing output divisors.

2) Experimental Analysis

Single-event effects (SEE) testing was performed in order to illustrate and quantify the impacts of the PLL configuration (output and feedback dividers) on the SET vulnerability of the topology. The PLL was designed and manufactured by Aeroflex Colorado Springs using a commercial 250 nm CMOS technology [Ha05a, Ha08]. The general PLL topology is identical to that shown in Fig. VIII-8 and has an oscillation range of 48 MHz to 100 MHz. Additionally, the PLL consists of programmable output and frequency dividers with selectable divisors (*M* and *N*) between 1 and 32.

Testing was performed using the K500 cyclotron at Texas A&M University's (TAMU) Cyclotron Institute. Xenon and argon 25 MeV/amu heavy ions were used at incident angles between 0º (normal to surface) and 60º in order to achieve effective LET values between 10 and 109 MeV-cm^2/mg. All testing was performed at a nominal power supply voltage of 3.0 V and at room temperature. Errors were recorded when the output

signal was out of phase with the reference signal by 90º (π/2 radians of phase displacement) or more.

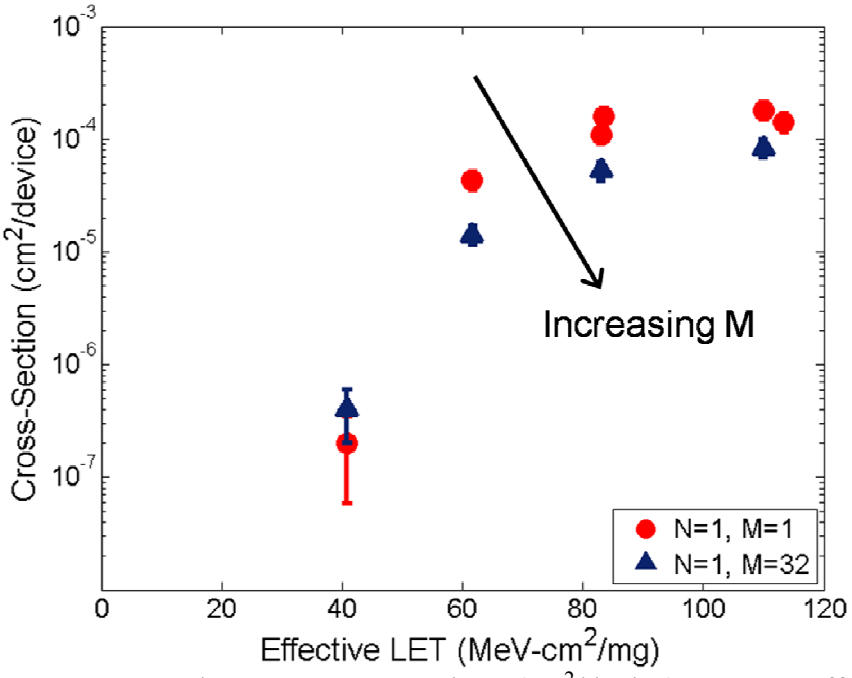


Fig. VIII-10. Measured event cross-section (cm^2/device) versus effective LET (MeV-cm^2/mg) for the programmable Aeroflex PLL discussed in the text. Two different PLL configurations (constant feedback divider) are illustrated at an operating frequency of 100 MHz. Increasing the output divisor, *M*, decreases the measured cross-sections.

Fig. VIII-10 illustrates the event cross-section (cm^2/device) versus LET (MeV-cm^2/mg) for two PLL configurations (*N, M*) at an operating frequency of 100 MHz. Both (1, 1) and (1, 32) configurations (constant feedback divisor) have identical LET thresholds of approximately 40 MeV-cm^2/mg. However, the cross-sections decrease for increasing output divisor *M*, indicating a decreased probability of upset. This result is consistent with that illustrated in Fig. VIII-9. Perhaps surprising is that the cross-section decreases although the total chip area increases (more divider stages are being utilized as *M* increases). As described in the previous sub-section, this phenomenon results from the

competing effects of the fundamental propagation nature of phase transients through the divider, and the individual vulnerabilities of the PLL and divider circuits. The end result of this competing effect is that the overall probability of PLL upset following an ion strike may be reduced by increasing the output divisor *M* due to the dominating effect of the transient division through the circuit.

Impacts of the Feedback Divider on the SET Propagation in the PLL

1) Theoretical and Simulation Analyses

Though the previous analysis states that decreasing the output divisor (M=1 being the smallest possible, $M \geq 1$) increases the probability of strikes in the output frequency divider resulting in a given range of phase error values, this result does not indicate how the presence of a feedback divider impacts SETs generated from the additional PLL sub-circuits. In order to examine the impacts (if any), SET simulations for strikes in each PLL sub-circuit were performed for various feedback divisors, *N* (see Fig. VIII-8). As the purpose of this study is to illustrate the effect of the divider on the propagation of phase SETs through the PLL, only strikes on nodes characteristic of the typical sub-circuit responses (as defined in previous works [Bo05, Bo06, Lo06, Lo08 Lo07c]) were chosen for this study. For example, strikes on nodes UP and DOWN were chosen as the representative 'worst-case' conditions for the PFD sub-circuit. Similarly, strikes on nodes V_{inVCO}, V_{outVCO}, and XDFF{K} represent the CP, VCO, and feedback divider sub-circuits, respectively.

Additionally, the charge deposition representative of the ion-induced current pulse was simulated by injecting a piece-wise linear current pulse for various integrated charge

amounts (250 fC, 500 fC, 1 pC, and 2 pC). The PLL circuit shown in Fig. VIII-8 was simulated with feedback divisors of N=1, N=2, N=4, and N=8 at an output frequency of 1.1 GHz (the center frequency of the VCO). As in the previous analysis, the temporal location of the strike with respect to the PLL's input frequency was varied in order to span the operating periods of the input/output signals. For each simulation, the PLL's maximum output phase displacement and the loop's recovery time were measured. The maximum output phase displacement was determined by finding the peak of the phase error as shown in Figs. VIII-3 and VIII-4. The recovery time (time required for the PLL to regain phase lock) was measured as the time for which the output phase displacement was greater than 50 ps (0.35 radians). A threshold of 50 ps was chosen in order to discriminate between any errors generated by the circuit's characteristic noise and numerical errors in the calculations. Fig. VIII-11 shows the mean values of (a) output phase displacement and (b) recovery time for various PLL configurations (N) and for a deposited charge of 50 fC. Error bars represent one standard deviation.

The results shown in Fig. 13(a) suggest that the feedback factor has little impact on the phase magnitude (Φ_{disp}) of the transients, where a slight increase in Φ_{disp} was measured for increasing N. This is partly due to the fact the output frequency is constant regardless of the feedback divisor. As the output frequency (ω_{out}) is unchanged, the input frequency (ω_{in}) must decrease with increasing feedback divisors (N) in order to satisfy the relationship $\omega_{out} = N \cdot \omega_{in}$. Therefore, the natural frequency must decrease proportionally with increasing N, thereby increasing only the response time of the loop [Ga05].

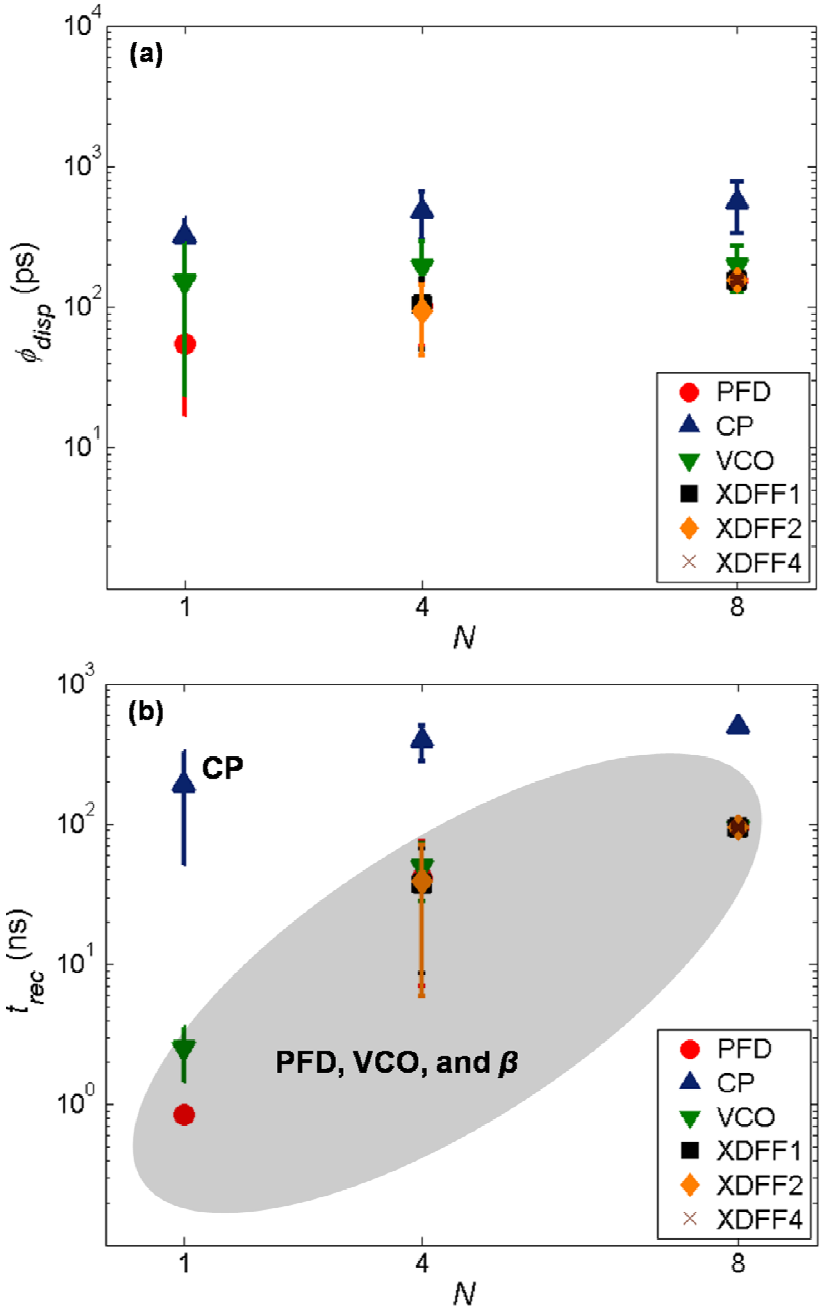


Fig. VIII-11. Mean (a) Φ_{disp} and (b) t_{rec} vs. N for SET simulations of strikes in the PFD (nodes UP and DOWN), CP (node V_{inVCO}), VCO (node V_{outVCO}), and Frequency Divider (nodes XDFF1, XDFF2, and XDFF4) within the PLL. Simulations were for a deposited charge of 50 fC. All simulations were performed for a constant output frequency of 1.1 GHz.

The previous observations that the input and natural frequencies must decrease proportionally with increasing N indicates that the relative change within the loop (the

frequency adjustment per loop cycle) must be constant for any feedback divisor. For example, PLLs with smaller feedback divisors can respond to perturbations with finer adjustments per loop cycle (greater time resolution), and can make more adjustments for a given amount of time (due to the increased natural frequency) when compared to PLLs with large feedback divisors.

Fig. 13(b) indicates that the feedback divisor chiefly impacts the PLL's recovery time following a strike. Moreover, the nature of the PLL recovery strongly depends on the location of the initial perturbation. Further details of the observed phenomena are explained in the following sub-sections, highlighting details for strikes in the PFD, CP, VCO, and feedback frequency divider.

a) Strikes in the PFD:

For perturbations due to strikes in the PFD, the recovery time of the PLL increases for increasing feedback divisors. Strikes in the PFD will result in an erroneous pulse at either the UP or DOWN node, thus 'tricking' the charge pump into sourcing/sinking charge due to the incorrectly detected phase error. Ideally, the PLL can correct this perturbation by activating the charge pump (in an opposite manner of the strike) for exactly the amount of time of the initial perturbation. However, the PLL cannot correct this internal change until the rising edges of the subsequent reference and feedback signals arrive at the PFD. Therefore, as the input frequency is greater for smaller feedback divisors, the rate at which the PLL can correct itself following the PFD perturbation is also greater for smaller feedback divisors. Thus, the recovery time increases approximately proportional to a decrease in input frequency.

b) Strikes in the CP:

Strikes in the CP sub-circuit deposit/deplete charge to/from the capacitive load in the loop filter, thus adjusting the input voltage to the VCO. The frequency perturbation at the output of the VCO is therefore directly proportional to the change in stored charge in the loop filter. The recovery of the output frequency and phase begins once the PFD detects the resulting phase error and is thus dependent on the fundamental acquisition properties of the PLL. As the acquisition properties of the PLL and output frequency remain constant versus feedback divisor, the recovery time and phase displacement of the PLL due to strikes in the charge pump is loosely dependent (independent, for practical purposes) on the feedback divisor. The slight increases in output phase displacement and recovery time are due to the decreased loop stability, increased jitter, and increased loop response time with increasing feedback divisor, *N*.

c) Strikes in the VCO:

SETs occurring within the VCO sub-circuit propagate directly to the output of the PLL, thus the magnitude of the transient depends on the nature and location of the strike within the sub-circuit [Bo05, Lo07c]. The recovery time, however, is determined by two factors: the removal of charge within the oscillator, and the feedback response of the PLL to the change in the VCO output. Once the phase error present in the VCO output signal propagates and is divided through the feedback divider, any phase error present at the output of the divider is detected by the PFD, thus activating the charge pump. Furthermore, as the VCO is not likely to immediately return to its initial phase lock with respect to the reference signal, the PLL will subsequently require some period of time to settle back into phase lock. The recovery time therefore depends on the initial transient

perturbation and the PLL settling characteristics (which depends on the loop's response time and damping). As in the case of strikes in the PFD, the recovery time following strikes in the VCO will increase with increasing feedback divisors, as the fundamental response time of the loop increases.

d) Strikes in the Frequency Divider:

As previously stated, strikes in the frequency divider can result in a phase perturbation at the output of the divider. As in the case of strikes in the VCO sub-circuit, the phase error at the output of the divider is detected by the PFD, thus causing the loop to adjust its operating condition. The magnitude of the phase error at the output of the PLL is a result of the initial 'false' phase error detected by the PFD which activates the CP to modify the VCO's control voltage. As in the case for strikes in the PFD and VCO, the recovery time depends on the detected phase error and the loop response time. Therefore, as the loop response time increases due to increases in the feedback divisor, the recovery time increases proportional to increases in the feedback divisor (decreases in input frequency).

2) Implications of PLL Feedback Factor

The results presented specify that for increasing feedback divisors (N), the recovery time increases following SETs originating in the PLL sub-circuits. Additionally, as the output phase displacement increases slightly with increasing N, the feedback divider is shown to have little impact on the magnitudes of the phase displacement values resulting from strikes within any PLL sub-circuit. Although the PLL specification for phase lock is entirely application dependent, the trends illustrated in Fig. VIII-11 suggest that

increasing the feedback divisor increases the SET vulnerability of the PLL. Moreover, assuming that the PLL area is dominated by the primary sub-circuits (PFD, CP, LPF, and VCO), the saturated event cross-section can be expected to remain relatively constant for increasing *N*. These observations are consistent with data presented in [Ha08] indicating that the calculated error rate increases with increasing feedback divider, *N*. It is important to note the feedback divider will not change the probabilities of strikes in additional PLL sub-circuits resulting in output phase transients.

3) Experimental Analysis

Fig. VIII-12 illustrates the event cross-section (cm^2/device) versus LET (MeV-cm^2/mg) for two PLL configurations (*N, M*) at a VCO operating frequency of 48 MHz. All experiments utilize the parameters discussed in the previous experimental sub-section. First, both (1, 1) and (32, 1) configurations (constant output divisor) have similar saturated cross-sections. However, the LET thresholds decrease for increasing feedback divisor *N*. This result is a consequence of the increasing transient magnitudes and recovery times for increasing feedback divisors (illustrated in Fig. VIII-11). In essence, the feedback divisor magnifies the generated transients within the PLL such that the resulting output phase displacement and loop recovery is greater for increasing *N*. As a result the minimum LET required for PLL upset (in this case, a phase displacement of π radians) decreases for increasing *N*.

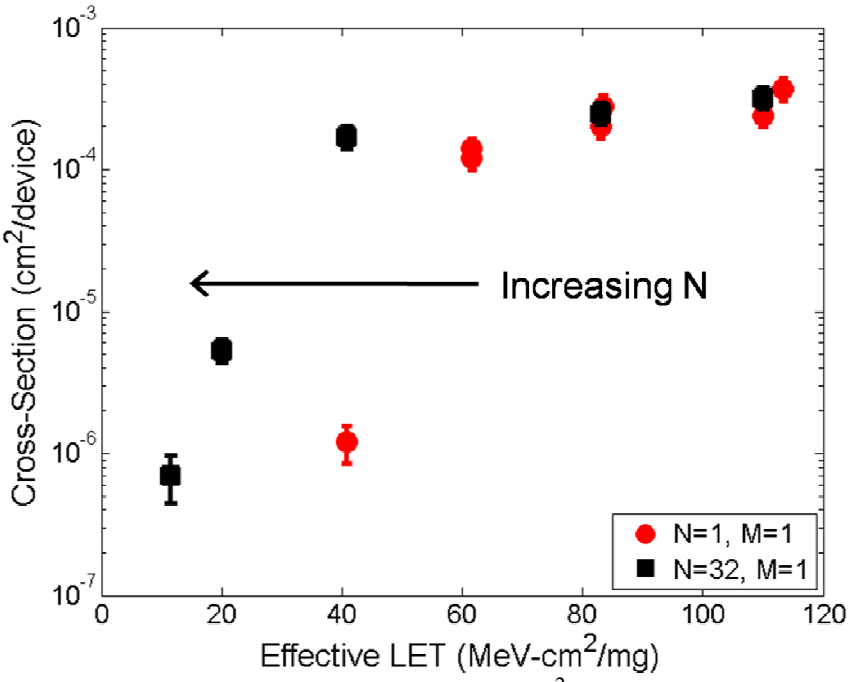


Fig. VIII-12. Measured event cross-section (cm^2/device) versus effective LET (MeV-cm^2/mg) for the programmable Aeroflex PLL discussed in the text. Two different PLL configurations (constant output divider) are illustrated at an operating frequency of 48 MHz. Increasing the feedback divisor, *N*, decreases the LET threshold.

Conclusion

Single-event transients have been analyzed in integer-*N* divider networks for the use in PLL circuits. Simulations on a single divide-by-*2* stage show that SETs within the divider can result in phase transients at the outputs bounded by multiples of the output signal's period. Moreover, the probability of an ion-strike resulting in a given range of phase displacement values increases with increasing input frequency, therefore decreasing the probability of obtaining a given phase displacement for increasing divider factors. Also, as phase transients propagate through stand-alone divider networks, such as the I/O frequency divider, they are attenuated through the chain, indicating that strikes in the final stage will most likely result in the largest phase displacement values at the

outputs of the divide-by-*N* circuit. Moreover, increasing the divisor of the I/O divider network in PLL circuits will decrease the probability of strikes in the divider chain resulting in PLL upsets. This result is corroborated with heavy-ion data illustrating a decrease in event cross-section for increasing output divisors.

Although increasing the I/O divisor decreases the probability of PLL upset due to large output phase displacements, increasing the divisor of the feedback divider increases the SET vulnerability of the PLL circuit. Consequently, the LET threshold decreases for increasing feedback divisors. Therefore, the optimal PLL configuration (in terms of SET vulnerability) requires maximizing the output frequency divider while minimizing the feedback frequency divider. This result indicates the importance of characterizing the SET response of the PLL under the worst case configuration (maximum *N* and minimum *M*). The individual impacts of *N* and *M* on the calculated error rates may subsequently be assessed by analyzing the SET performance for a variety of configurations.

CHAPTER IX

A GENERALIZED LINEAR MODEL FOR SINGLE TRANSIENT PROPAGATION IN PHASE-LOCKED LOOPS AND GUIDELINES FOR ERROR REDUCTION

Introduction

Numerous simulation, experimental, and analytical analyses have been presented thus far in an attempt to characterize the fundamental nature of SET generation in the PLL sub-circuits and the propagation of SETs through the PLL closed-loop. This chapter presents an analytical model for transient effects in PLLs, unifying all of the discussed results and observations, in a general closed-form.

Although this dissertation primarily discusses PLLs in the context of on-chip clock generation and skew reduction in the presence of single ionizing particles, it is the goal of this work to present a generalized model for single transient propagation through PLL topologies for a variety of applications and environments. The transient model is formulated from a conventional linear PLL model commonly used in a variety of noise analyses [Ha04, He04, Kr82, Me02]. However, the model is unique in that the resulting fundamental design equations are derived in closed-form under the assumption that transients are a result of single transient impulses applied to the various sub-circuits rather than continuous nondeterministic sources. This approach vastly simplifies the analysis and provides insight into the closed-loop parameters that directly influence the generation and propagation of transients through the PLL. As a result, a list of design guidelines is developed that can be applied to all PLL topologies. The set of principles may be applied for analytical transient mitigation to reduce the sensitivity of PLLs to

single transients resulting from extrinsic noise sources such as single-event radiation and crosstalk noise.

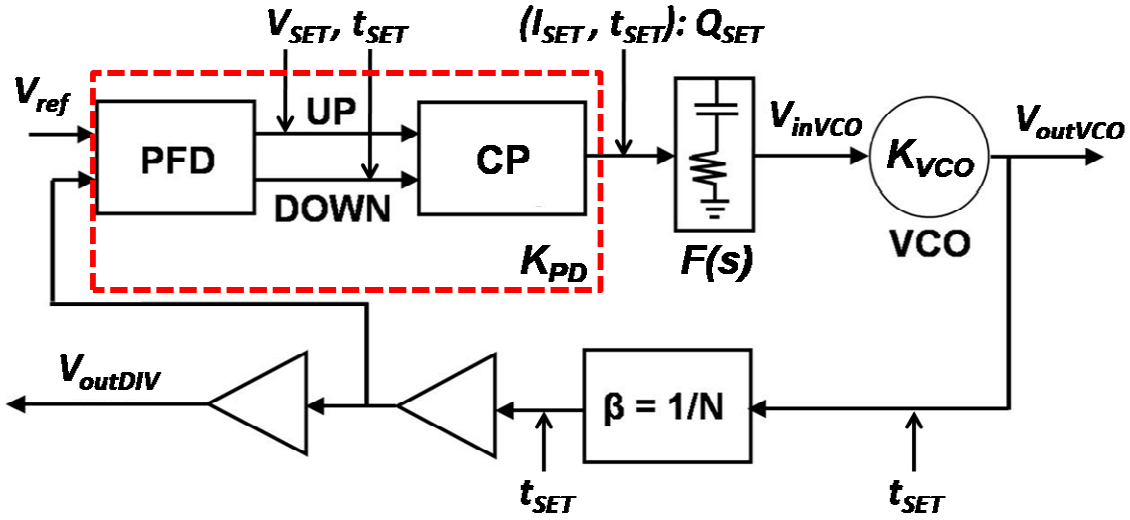


Fig. IX-1. PLL model for single transient propagation.

Transient Propagation

The model for transient propagation in the PLL is shown in Fig. IX-1. The parameters V_{SET}, I_{SET}, and Q_{SET} represent the cases where the input perturbation has the form of a voltage, current, and charge, respectively. Additionally, the parameter t_{SET} represents the length of time of the initial extrinsic perturbation. All transient perturbations are assumed to be a result of extrinsic noise and are generated by a single impulse perturbation at either the outputs of the PFD, conventional CP, VCO, or frequency divider. In regards to transients resulting from single ionizing radiation, recent works discussed throughout this dissertation have characterized the SET response of each sub-circuit in terms of the voltage perturbation (V_e) at the input to the VCO, the recovery

time (t_{rec}) of the loop, and the output phase displacement (Φ_{disp}) [Bo06, Lo06, Lo07a, Lo08, Lo07b, Lo07c]. Therefore, a set of equations will be derived in order to estimate each parameter following single perturbations in each sub-circuit.

TABLE IX-1
PLL-90NM AND *PLL-130NM* DESIGN PARAMETERS
(DESIGNED USING IBM CMOS9SF AND CMRF8RF PROCESSES)

Parameter	*PLL-90NM*	*PLL-130NM*
V_{DD}	1.2 V	1.2 V
I_{CP}	2 μA	2 μA
C_1	2.14 pF	770 fF
K_{VCO}	$2.5 \cdot 10^{10}$ rad/(s·V)	$4.82 \cdot 10^{9}$ rad/(s·V)
ω_n (β=1)	$6.1 \cdot 10^{7}$ rad/s	$1.4 \cdot 10^{8}$ rad/s
ζ	~1	~1

This chapter considers Φ_{disp} as a measure discussed in [Lo08] for measuring the phase error in a signal without the need for an ideal reference. Phase displacement, in units of radians, is calculated by measuring the time-difference between the local erroneous operating period (T_e) containing the phase perturbation and the nominal operating period of the output signal (T_{lock}), normalized by T_{lock} and multiplied by 2π, as given by Eqn. (IX-1) [Lo08]. An illustration of T_e required to measure Φ_{disp} is presented in Chapter VII (Fig. VII-6).

$$\phi_{\text{disp}} = \frac{2\pi \left| T_e - T_{\text{lock}} \right|}{T_{\text{lock}}} = \left| T_{\text{e}} - T_{\text{lock}} \right| \omega_{\text{lock}} \text{ (radians)} \qquad \text{(IX-1)}$$

The following sub-sections discuss transient generation within each sub-circuit and the transient's closed-loop propagation. All illustrations utilize the PLL design parameters described in Table IX-I and illustrated in Figs. II-6 and II-10 (Chapter II).

Loop Recovery

Following an impulse perturbation resulting in a frequency/phase shift at the output, the closed-loop transfer function (Chapter II) suggests that the PLL will re-track the input such that the output frequency is equal to that of the input frequency divided by the feedback factor. Assuming the PLL can respond instantaneously to a loop perturbation, the ideal recovery time (t_{rec}) of the loop will depend on the resulting frequency shift and will follow Eqn. (II-18) for the acquisition time. The recovery (re-acquisition) time, however, only occurs following the arrival of the next rising edge of the input or feedback signal. Thus, at most there will be a time T_{REF} (period of reference signal) before re-acquisition can occur. Therefore, the actual recovery time (t'_{rec}) is at most the ideal recovery time (t_{rec}) time plus T_{REF} and some settling time, t_s (Eqn. (IX-2)).

$$t'_{rec} \leq t_{rec} + T_{REF} + t_s \tag{IX-2}$$

Table IX-II shows the equations for the ideal recovery time following transients in each sub-circuit as derived in APPENDIX A where t_{SET} represents the length of the initial transient pulse, Q_{SET} is the amount of charge in/out of the CP sub-circuit as a result of the perturbation, T_c is the cycle time error at the output of the VCO, and $T_{c,DIV}$ is the cycle time error at the output of the frequency divider. Following the perturbation, the PLL

will reacquire the input signal by activating the CP sub-circuit in an opposite fashion of the initial perturbation. Assuming a linear response of the closed-loop PLL and a constant CP current, the ideal recovery times following transient perturbations originating within the PFD, VCO, or frequency divider sub-circuits is exactly the length of time of the original transient.

TABLE IX-2
IDEAL RECOVERY TIMES FOR TRANSIENT PERTURBATIONS
GENERATED WITHIN EACH PLL SUB-CIRCUIT

Sub-Circuit	t_{rec}
PFD	t_{SET}
CP	$Q_{SET}/I_{CP} + t_{SET}$
VCO	$\|T_c\|$
β	$\|T_{c,DIV}\|$

Following a transient perturbation, t_{SET} represents the length of the transient pulse, Q_{SET} is the amount of charge in/out of the CP sub-circuit as a result of the perturbation, I_{CP} is the nominal CP current, T_c is the cycle time error at the output of the VCO, and $T_{c,DIV}$ is the cycle time error at the output of the frequency divider.

However, the ideal recovery time following transient perturbations within the CP sub-circuit is not only dependent on the original perturbation time. As a perturbation at the output of the CP will abruptly alter the voltage applied to the input of the VCO, causing a prompt shift in the output frequency, the closed-loop PLL will reacquire the input frequency as determined by the transfer equations. Therefore, the recovery time will follow the initial acquisition characteristics as determined by Eqn. (II-18), where the amount of voltage perturbation, V_e, depends directly on the amount of charge, Q_{SET}, deposited or depleted from the LPF, as shown by the equation in Table IX-II. Fig. IX-2 illustrates an example of a voltage transient on V_{inVCO} and corresponding frequency transient resulting from an initial perturbation at the output of the CP sub-circuit. The

simulation was performed on a PLL designed using the IBM CMOS 9SF PDK using the parameters in Table IX-I (*PLL-90nm*). Moreover, the initial perturbation was induced by injecting 300 fC of extraneous charge at the output node of the CP sub-circuit (charge collected on LPF capacitor, C_1). As indicated in Fig. IX-2, the simulated recovery time ignoring any settling effects is approximately 140 ns. Utilizing the equation in Table IX-II for calculating t_{rec} following CP perturbations, the estimated recovery time is 150 ns, a 7% deviation from the simulated t_{rec}.

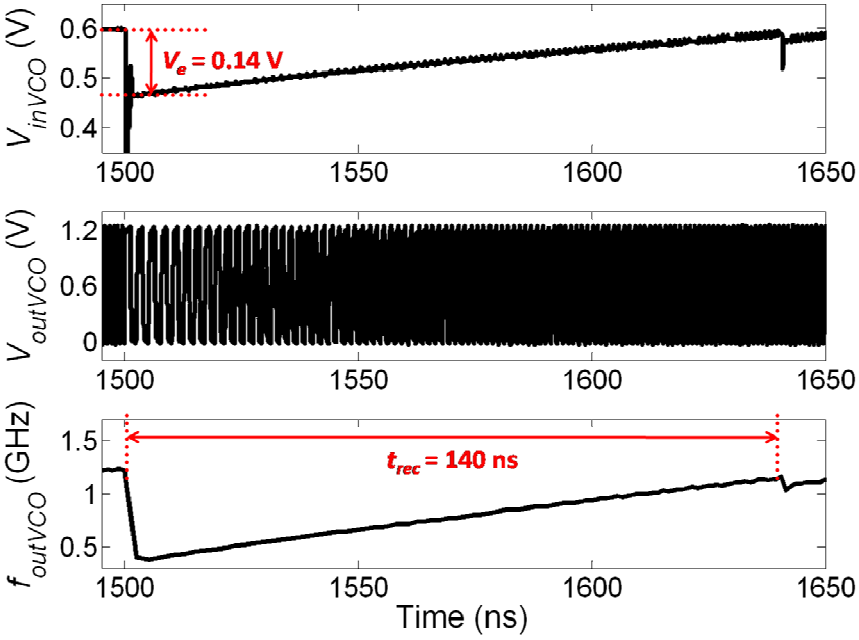


Fig. IX-2. An example of a voltage transient on V_{inVCO} and corresponding frequency transient resulting from an initial perturbation at the output of the CP sub-circuit. The simulation was performed on a PLL designed using the IBM CMOS 9SF PDK. The initial perturbation was induced by depositing 300 fC of extraneous charge at the output node of the CP sub-circuit.

Voltage Transient Generation

As the PLL output frequency is equal to the input frequency divided by the feedback factor when in phase lock, it is useful to think of the phase transfer function in terms of output frequency rather than phase (also discussed in detail in Chapter II). Also, since a change in output frequency must be accompanied by a change in the VCO control voltage, the relationship shown in Eqn. (IX-3) may be derived. Thus, the response of the closed-loop system can be obtained by monitoring the variations in the VCO's control voltage, V_{inVCO} [Ra01].

$$H(s) = \frac{\phi_{out}}{\phi_{REF}}(s) = \frac{\omega_{out}}{N \cdot \omega_{REF}}(s) = \frac{V_{ctrl} \cdot K_{VCO}}{N \cdot \omega_{REF}}(s) \qquad \text{(IX-3)}$$

For example, a perturbation occurring within the PFD sub-circuit may cause a corrupted bit which can propagate through the combinational logic blocks and appear at either the UP or DOWN signal lines. The resulting signal on node UP or DOWN will have a voltage V_{SET} over time t_{SET}. Assuming the CP is perfectly matched (sink current equals source current) and V_{SET} is large enough to engage the CP, the activation of the CP sub-circuit will perturb V_{inVCO} by some voltage V_e. Similarly, transient perturbations in the CP sub-circuit may directly activate the CP to source/sink current to/from the LPF, or deposit/deplete charge directly to/from the LPF, thus adjusting V_{inVCO}. Further, perturbations occurring within either the VCO or frequency divider sub-circuits may result in phase error that is detected by the PFD. The resulting phase error will appear at the output of the PFD and ultimately perturb V_{inVCO} in an identical fashion as previously discussed.

Assuming the VCO is linear, Eqn. (IX-3) indicates that the frequency transient will precisely follow the voltage transient as shown in Fig. IX-2. Moreover, as derived in APPENDIX A, it is shown that the maximum voltage perturbation at V_{inVCO} following transient perturbations in each sub-circuit is given as Eqn. (IX-4) where K_{PD} is the gain of the phase detector, t_{rec} is the ideal recovery time given in Table IX-II, and C_1 is the loop filter's primary capacitance. Consistent with the results illustrated in Fig. IX-2, the calculated V_e resulting from 300 fC of extraneous charge at the output of the CP is 0.14 V. Further, Eqns. (A-1), (B-2), (C-4), and (D-2) located in APPENDIX A represent simplified expressions for V_e following perturbations in the PFD, CP, VCO, and β sub-circuits, respectively.

$$V_e = \frac{2\pi K_{PD} t_{rec}}{C_1} \tag{IX-4}$$

Although V_{inVCO} is directly proportional to the output frequency and accurately represents the frequency error following perturbations within the PFD, CP, and frequency divider sub-circuits, it is important to note that voltage transients resulting from perturbations within the VCO do not directly correspond to the frequency transient appearing at the output of the VCO. As the initial VCO perturbation manifests as a phase/frequency transient, the voltage error, V_e, is a secondary effect that occurs as a result of the detected phase error. Thus, the transient on V_{inVCO} represents only the output frequency during the PLL recovery and not the initial VCO perturbation and resulting recovery. Conversely, output frequency transients resulting from perturbations originating in every other sub-circuit may be completely described by the voltage

transient on V_{inVCO}, as discussed and displayed in Fig. IX-2. This observation suggests that examining only the voltage transient on V_{inVCO} is not adequate for completely describing the transient behavior of the PLL.

Output Phase Displacement

The output phase displacement, Φ_{disp}, may be utilized in order to absolutely describe the phase/frequency transient resulting from an initial perturbation in any sub-circuit. The maximum Φ_{disp}, for example, describes the peak of the phase shift accrued, whereas Φ_{disp} quantified versus time may be used to describe the loop's recovery time and resulting number of erroneous output pulses [Lo08, Lo07b, Lo07c].

As derived in APPENDIX A, it follows that the voltage error, V_e, will modify the output frequency, thus resulting in an instantaneous frequency error (f_e) at V_{outVCO} given by Eqn. (IX-5).

$$f_e = \frac{V_e K_{VCO}}{2\pi} = \frac{K_{PD} K_{VCO} t_{rec}}{C_1} = \frac{\omega_n{}^2 t_{rec}}{\beta} \tag{IX-5}$$

The notation used in Eqns. (IX-4) and (IX-5) will always result in positive values for V_e and f_e; in other words, Eqns. (IX-4) and (IX-5) represent the magnitudes of the voltage and frequency shifts. However, a decrease/increase in V_{inVCO} will subsequently decrease/increase f_{outVCO}. The subsequent text will denote positive frequency modulations (increases in f_{outVCO}) by stating that $\Delta f_{outVCO} > 0$, whereas negative frequency modulations (decreases in f_{outVCO}) will be stated as $\Delta f_{outVCO} < 0$. Consequently, as derived in APPENDIX A, the output phase displacement following perturbations in the PFD, CP,

and β sub-circuits is given as Eqn. (IX-6) where t_{rec} is the ideal recovery time given in Table IX-II, ω_n is the PLL natural frequency, β is the feedback factor, and f_{lock} is the steady-state output frequency in phase lock. The plus sign in the denominator is used when estimating the response for transients on UP, sourcing current to C_1, or those resulting in a positive frequency modulation. The negative sign in the denominator is used for transients on node DOWN, depleting charge from C_1, or those resulting in a negative frequency modulation. Note that for negative frequency modulations, Eqn. (IX-6) is only valid for $t_{rec} < \beta f_{lock}/\omega_n^2$ as it assumed that the output frequency cannot be reduced further than f_0 as described by the linear approximation of the VCO transfer characteristics shown in Fig. II-6.

$$\phi_{disp} = \frac{2\pi\omega_n^2 t_{rec}}{\beta f_{lock} \pm \omega_n^2 t_{rec}} \tag{IX-6}$$

In contrast to perturbations originating in the PFD, CP, or frequency divider, perturbations within the VCO sub-circuit initially affect the output phase regardless of the loop characteristics. In this case, the initial phase displacement following transient perturbations in the VCO is given merely as Eqn. (IX-1). However, following the initial phase displacement in the VCO, the phase error propagates through the closed-loop, thus perturbing the steady-state loop conditions. As a result, the output phase of the VCO is further modified resulting in a secondary phase displacement as determined by Eqn. (IX-9). Moreover, Eqns. (A-6), (B-4), (C-1), and (D-3) located in APPENDIX A represent simplified expressions for the phase displacements following perturbations in the PFD, CP, VCO, and β sub-circuits, respectively.

The following observation can be made regarding the output phase displacement:

$$\lim_{t_{rec}\to\infty} \phi_{disp} = \begin{cases} 2\pi & \Delta f_{outVCO} > 0 \\ \infty & \Delta f_{\text{outVCO}} < 0 \end{cases}$$

Hence, transients resulting in positive frequency modulations will always be upper-bounded by 2π whereas transients resulting in negative frequency modulations have no upper bound. Thus, the most severe loop perturbation occurs when V_{inVCO} is reduced to 0 V, subsequently reducing the output frequency to f_0. Conversely, for transients resulting from positive frequency modulations, the output frequency approaches a maximum dependent on the VCO transfer curve. From the definition of T_e in Eqn. (IX-1), T_e approaches 0 for increasing t_{rec}. Consequently, according to Eqn. (IX-1), Φ_{disp} approaches 2π for increasing t_{rec}.

The PLL Critical Time Constant

Fig. IX-3 illustrates Φ_{disp} vs. t_{rec} for perturbations resulting in (a) positive and (b) negative frequency modulations. The phase displacement is calculated using Eqn. (IX-6) for the design parameters shown in Fig. II-10 and Table IX-I (*PLL-90nm*). Results from five lock frequencies (f_{lock}) within the VCO linear operating range are displayed and indicate that Φ_{disp} decreases slightly with increasing f_{lock} (signified by the horizontal translation of the Φ_{disp} vs. t_{rec} curve). This decrease in sensitivity with increasing lock frequencies (for a given VCO design) is due to the increase in the steady-state V_{inVCO} required to achieve larger values of f_{lock}. Larger V_{inVCO} values require either longer CP

activation times or larger charge depletions in order to reduce the nodal voltage to equivalent values.

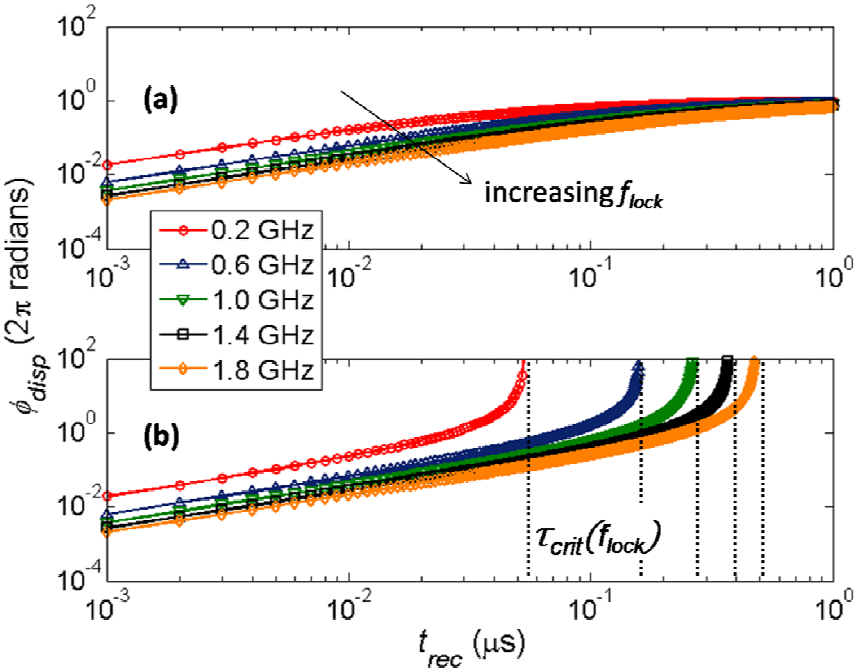


Fig. IX-3. Output phase displacement versus t_{rec} for (a) positive and (b) negative frequency modulations as determined by Eqn. (IX-6) and the PLL parameters provided in Table IX-I (*PLL-90nm*). The critical time constant, τ_{crit}, corresponds to the vertical asymptote on t_{rec} and is determined by Eqn. (IX-7) for various lock frequencies.

The results displayed in Fig. IX-3 also show that Φ_{disp} increases for increasing t_{rec}. Initially, Φ_{disp} tends to increase pseudo-linearly versus t_{rec} for both positive and negative frequency modulations. However, as discussed in the previous sub-section, Φ_{disp} resulting from positive frequency modulations asymptotically approaches 2π for increasing t_{rec} (Fig. IX-3 (a)). Conversely, for negative frequency modulations, each curve for a given f_{lock} consists of a unique vertical asymptote on t_{rec} such that Φ_{disp} approaches infinity for increasing t_{rec} (Fig. IX-3 (b)). This asymptote on t_{rec}, denoted as

the PLL critical time constant (τ_{crit}), increases linearly with increasing frequency, and is described by Eqn. (IX-7) where β is the feedback factor, f_{lock} is the steady-state output frequency in phase lock, and ω_n is the PLL natural frequency. For the PLL design parameters in Fig. II-10 and Table IX-1 (*PLL-90nm*) at a f_{lock} of 1 GHz, for example, τ_{crit} is approximately 200 ns. For perturbations resulting in $t_{rec} > \tau_{crit}$, it can be expected that $\Phi_{disp} \rightarrow \infty$ for increasing t_{rec}.

$$\tau_{crit} = \frac{\beta f_{lock}}{\omega_n^2} \tag{IX-7}$$

Conceptually, τ_{crit} corresponds to the minimum time constant of the initial perturbation required to maximally disturb the closed-loop PLL. Utilizing the equations for t_{rec} in Table IX-II (*PLL-90nm*), the perturbation characteristics for each sub-circuit may be examined and compared to a given τ_{crit} in order to estimate the ease with which the perturbation will affect the closed loop. For perturbations originating in the PFD sub-circuit, for example, transients with time-widths, t_{SET}, of close to 200 ns or greater are required before phase displacement values can be expected to rapidly increase. In the case of single ionizing particle disturbances, transient widths of 200 ns or greater are highly improbable as typical transient distributions at sub-100 nm technology nodes are reported between picoseconds and nanosecond values [Be06, Ga04, Na07]. Therefore, the PFD sub-circuit is likely to have little impact in the overall transient vulnerability. For perturbations originating in the CP sub-circuit, however, a Q_{SET} of 400 fC or greater (much more likely in the case of single ionizing particles) will result in t_{rec} values of τ_{crit} or greater. These observations are consistent with previous simulation and experimental

works identifying the CP sub-circuit as the dominant contributor to the transient vulnerability of the PLL [Bo06, Lo06, Lo07a, Lo07b].

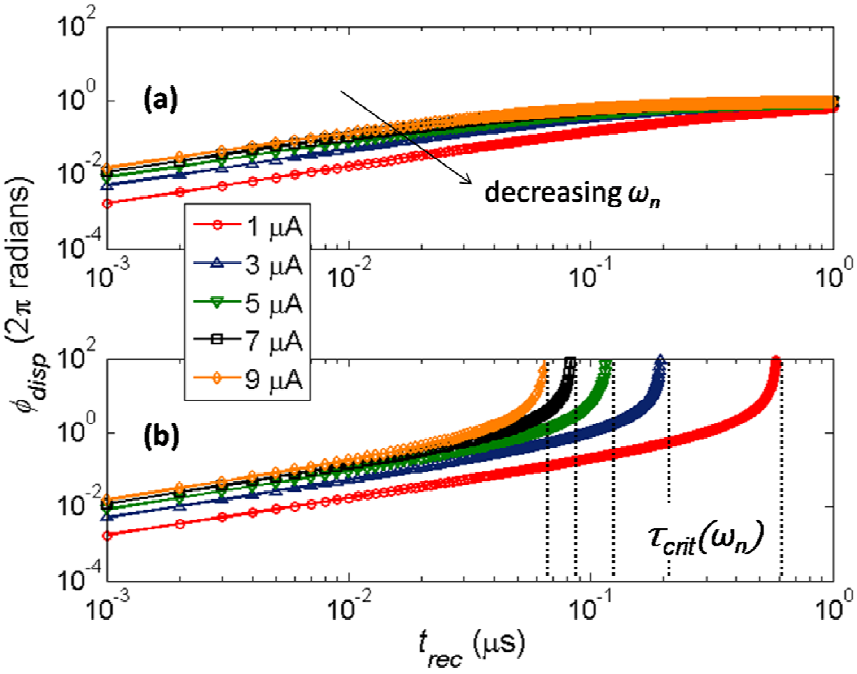


Fig. IX-4. Output phase displacement versus t_{rec} for (a) positive and (b) negative frequency modulations as determined by Eqn. (IX-6) and the PLL parameters provided in Table IX-I (*PLL-90nm*). The critical time constant, τ_{crit}, corresponds to the vertical asymptote on t_{rec} and is determined by Eqn. (IX-7) for various natural frequencies achieved by modifying the charge pump current I_{CP}.

Eqns. (IX-6) and (IX-7) also suggest that the output phase displacement and critical time constant are highly dependent on the PLL natural frequency. Fig. IX-4 shows the output phase displacement versus recovery time at various natural frequencies for (a) positive and (b) negative frequency modulations as determined by Eqn. (IX-6) and the PLL parameters provided in Table IX-I (*PLL-90nm*). Results for five natural frequencies achieved by modifying the CP current are displayed and indicate a decrease in Φ_{disp} for decreasing ω_n at a given t_{rec} (signified by the horizontal translation of the Φ_{disp} vs. t_{rec}

curve). This decrease in sensitivity is due to the loop's increased response time for decreasing natural frequency. In other words, for a given perturbation, the transient will propagate slower through the loop for smaller natural frequencies, thus reducing the impact on the output phase. Also indicated in Fig. IX-4 is the increase in τ_{crit} for decreasing ω_n. Moreover, the results suggest that the critical time constant increases as a quadratic with decreasing natural frequency, thereby decreasing the PLL ease of propagating extrinsically induced transients.

Principles for Transient Reduction

Conventional PLL design guidelines typically suggest designing the PLL with as large a natural frequency as possible [Ba08]. However, the results presented in the previous section suggest that increasing ω_n also increases the ease at which transients ensuing in large Φ_{disp} values propagate through the closed-loop. This observation indicates that when considering extrinsic single transient perturbations, there should be an upper bound for the natural frequency as given by Eqn. (IX-8).

$$\omega_n \leq \omega_{n,crit} = \sqrt{\frac{\beta f_{lock}}{\tau_{crit}}} \tag{IX-8}$$

By ensuring that $\omega_n << \omega_{n,crit}$, the magnitudes of the output phase displacement values following transient perturbations can be minimized. For example, assuming typical Q_{SET} and t_{SET} values of 500 fC and 1 ns for CP perturbations (which may be estimated from the operating environment), the maximum calculated t_{rec} (Table IX-II) is approximately 250 ns for the PLL parameters provided in Table IX-I (*PLL-90nm*). According to Fig.

IX-4, transient perturbations in the CP are likely to result in extremely large Φ_{disp} values for I_{CP} values of 3 μA and greater. In other words, the PLL critical time constant for I_{CP} values of 3 μA and greater is much less than the expected t_{rec}. However, for an I_{CP} of 1 μA, τ_{crit} is approximately 600 ns and the estimated Φ_{disp} for an expected t_{rec} of 250 ns is approximately 2π radians.

The discussed results and observations lead us to define a list of design guidelines, or principles, for analytical mitigation of single transient propagation through PLL circuits.

1. First, τ_{crit} should be as large as possible. Consequently, ω_n must be upper bounded by $\omega_{n,crit}$.
2. The gain of the VCO, K_{VCO}, should be minimized, thus decreasing the bandwidth of the VCO. Decreasing K_{VCO} also decreases the output jitter; however, K_{VCO} may not be entirely adjustable for a given application with particular output frequency requirements. Accordingly, applications requiring large output frequencies should be designed with low bandwidth VCOs.
3. The PLL lock frequency should be greater than the center frequency of the VCO while remaining within the linear operating region. Increasing f_{lock} for a given VCO has the effect of increasing τ_{crit}.
4. The CP source/sink current, I_{CP}, should be minimized in accordance with the application's lock-time specifications and the design equations presented in this work. As decreasing I_{CP} increases the lock time, the recovery time following transient perturbation also increases. Therefore, the estimated output recovery times should be weighed against the calculated critical time constant, as in Figs. IX-3 and IX-4.

5. The loop filter's capacitance, C_1, should be maximized in accordance with the application's lock-time specifications and area requirements. Increasing C_1 has the same effect as decreasing I_{CP}.

As a design example, assume a given application can tolerate up to 2π radians of phase displacement. According to Fig. IX-4, the PLL with an I_{CP} of 1 μA (τ_{crit} = 600 ns) ensures that transients resulting in t_{rec} values of up to 300 ns can be tolerated. If we assume that $t_{SET} << Q_{SET}/I_{CP}$, it appears that a good "rule of thumb" is that for every 1 ns of desired tolerance in t_{rec}, the CP can tolerate up to 1 fC of charge perturbation. Similarly, if I_{CP} is 3 μA, the CP can tolerate up to 3 fC of charge perturbation for every 1 ns of desired tolerance. Thus, for a maximum t_{rec} value of up to 300 ns for an I_{CP} = 1 μA or 100 ns for I_{CP} = 3 μA, the CP can tolerate a Q_{SET} of up to 300 fC of charge perturbation in order to ensure that the output phase displacement will be less than 2π radians.

Model Validation

The transient model has been validated through simulations and experiments on two PLL designs. The first (denoted as *PLL-90nm*), was designed using the IBM 90 nm 9SF PDK and the design parameters listed in Table IX-I. *PLL-90nm* is utilized for all simulations in order to validate the discovery of the PLL critical time constant. The second PLL (*PLL-130nm*), designed using the IBM 130 nm 8RF PDK and the parameters listed in Table IX-I, was fabricated through the MOSIS foundry [MOSIS]. Experiments validate the analytical model and all simulation results.

Simulation Results

The simulations on *PLL-90nm* (Table IX-I) were performed using the CADENCE EDA tool suite, the Spectre Environment, and the ACCRE computing cluster at Vanderbilt University [ACCRE]. All simulations were performed over four design parameters: the circuit node of the injected perturbation, the length of the initial transient perturbation and/or the amount of deposited/depleted charge, the temporal location of the perturbation within the clock period, and the PLL operating frequency. All voltage transient perturbations were induced by injecting a piecewise linear (rectangular) voltage source for a length of time, t_{SET}, and a maximum voltage of V_{DD}. Similarly, all charge perturbations were induced by injecting a rectangular current source for a length of time, t_{SET}. The maximum current was varied in order to set the total amount of deposited charge over time t_{SET}.

Following the simulated transient perturbation, the output phase displacement was directly measured using Eqn. (IX-1). Fig. IX-5 illustrates the output phase displacement (Φ_{disp}) versus deposited charge (Q_{SET}) resulting from simulated charge perturbations at the output of the CP sub-circuit in *PLL-90nm*. Also displayed is the Φ_{disp} versus t_{rec} characteristic (and corresponding Q_{SET} as determined from Table IX-II) as calculated from Eqn. (IX-6). Both the simulations and model indicate that the PLL critical time constant is 300 ns. Note that no calibration of the model is necessary in order to accurately predict the critical time constant. Thus, for CP perturbations, the corresponding critical charge (the charge, Q_{crit}, at which $t_{rec}=\tau_{crit}$) is 600 fC. Similarly, transient perturbations originating in the PFD (t_{SET}), VCO ($|T_c|$), and frequency divider

($|T_{c,DIV}|$) sub-circuits require 300 ns of time perturbation in order to result in t_{rec} equal to τ_{crit}.

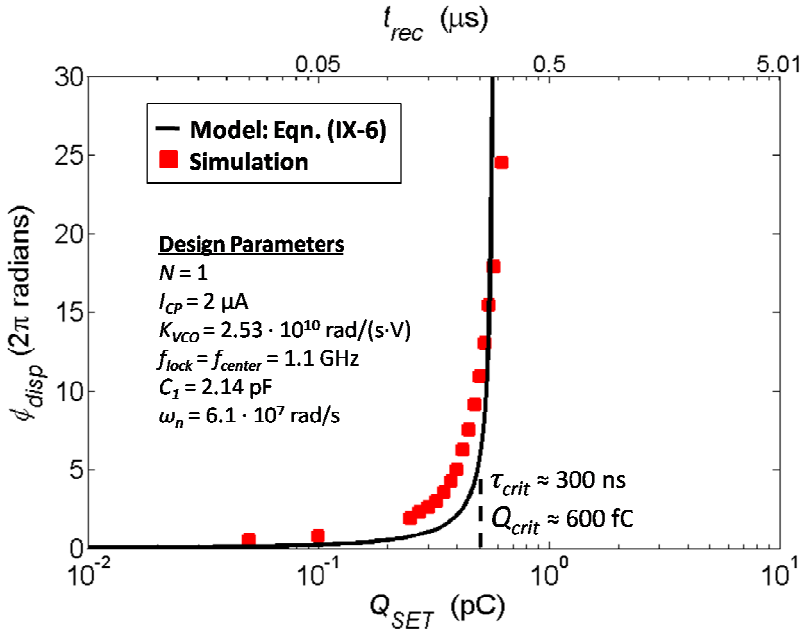


Fig. IX-5. Simulated output phase displacement (Φ_{disp}) versus deposited charge at the output of the CP sub-circuit (Q_{SET}) and corresponding t_{rec} value following single transient perturbations. The estimated τ_{crit} and Q_{crit} values resulting from the simulation results and model are approximately 300 ns and 600 fC, respectively.

Although the model accurately predicts τ_{crit}, the Φ_{disp} values deviate from the model slightly as Q_{SET} decreases from Q_{crit}. As the first-order model does not take into account any settling effects (loop damping), it is expected that for $t_{rec} < \tau_{crit}$ the model under-predicts the output response as it does account for additional time required by the loop to reacquire the input signal. Additionally, for large $t_{rec} > \tau_{crit}$ ($Q_{SET} > Q_{crit}$), the model will over-predict the output response. The model states that the output phase will approach infinity as the output frequency is reduced to 0 Hz; realistically, the output frequency is

only temporarily reduced to f_{min} as given by the VCO transfer curve. Thus, the output phase displacement will eventually reach a maximum value dependent on f_{min} and f_{lock}.

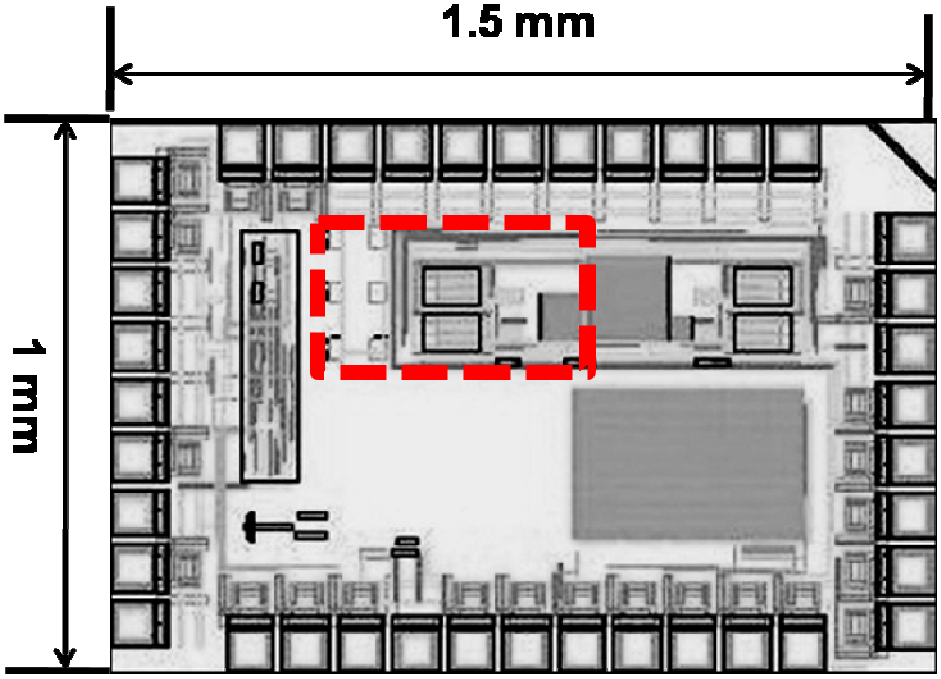


Fig. IX-6. Layout view of the *PLL-130nm* test chip indicating the PLL sub-circuit.

Experimental Results

The analytical model, determination of τ_{crit}, and the simulation results have been experimentally validated on the PLL topology illustrated in Fig. II-11 for the parameters in Table I (*PLL-130nm*). The PLL was designed using the IBM 130 nm 8RF CMOS technology and fabricated through the MOSIS Service [MOSIS]. Fig. IX-6 illustrates the layout of the test chip (*PLL-130nm*) and indicates the location of the PLL. Fig. IX-7 shows the VCO measured transfer characteristics for two *PLL-130nm* test chips, the PLL operating region, and the linear approximation used for the transient model calculations.

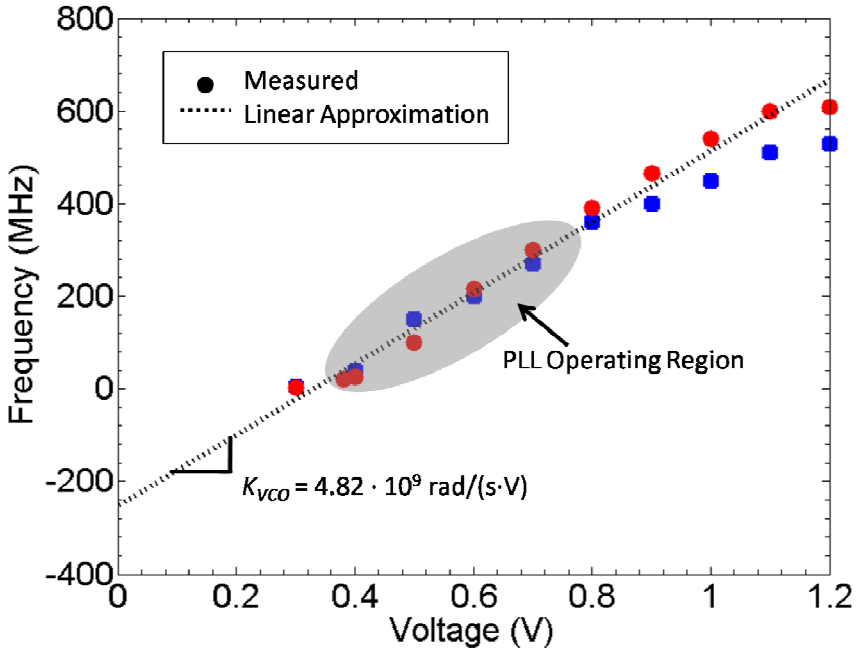


Fig. IX-7. Measured VCO transfer characteristics for two *PLL-130nm* test chips and linear approximation for transient model calculations.

Single transient perturbations were injected into the PLL circuit using laser-induced carrier generation based on two-photon absorption (TPA) using high peak power femtosecond pulses at sub-bandgap optical wavelengths [Mc02, Mc03]. Described in detail in previous chapters, the TPA technique has proven effective in interrogating transient phenomena through the wafer using backside irradiation [Lo08, Lo07b, Mc02, Mc03]. This eliminates interference from the metallization layer stacks that are prevalent in modern devices, and circumvents many of the testing issues associated with flip-chip-mounted parts.

The TPA experimental setup is described in previous chapters and in [Lo07b, Mc02]. The device under test (DUT) was mounted on a motorized xyz translation platform with 0.1 µm resolution. Optical pulses are focused through the wafer onto the front surface of the DUT with a 100x microscope objective, resulting in a near-Gaussian beam profile

with a typical diameter of approximately 1.6 μm at focus [Mc02]. Because the carrier deposition varies as the square of the irradiance (I^2) [Bo86, Mc02, St85], this corresponds to a Gaussian carrier density distribution with an approximate diameter of 1.1 μm (full-width-at-half-maximum). All experiments were performed at room temperature.

In order to characterize output transients following laser strikes within the PLL a Tektronix-TDS5104 oscilloscope sampling between 250 MS/s and 1.25 GS/s was used. The oscilloscope was set to trigger on the rising edge of the pulsed laser sync pulse, and the FastFrame™ feature was utilized to capture multiple transients per injection location. All experiments were performed at multiple incident laser energies for various operating frequencies within the PLL operating region.

Previous works indicate that the largest output phase transients are most likely a result of initial perturbations occurring within the CP sub-circuit [Bo06, Lo06, Lo07a, Lo07b]. In order to determine the most sensitive node within the CP sub-circuit, the through-wafer TPA technique was utilized to generate a map of the sensitive regions in the CP. The map displays the 2-dimensional (2D) spatial dependence of the PLL transient signatures by scanning the laser through the CP sub-circuit and recording the output phase transients following strikes in each location. In contrast to the 2D SEU maps displayed in Chapter V where only the x-y coordinates of laser strikes resulting in SEUs (as defined by a pre-defined threshold) were identified, multiple transients were recorded for each x-y location. This technique is expected to reduce the noise in the measurements and more accurately display the SET sensitive regions. Fig. IX-8 displays an image of the scanned CP sub-circuit captured by an Indigo Alpha NIR focal plane array.

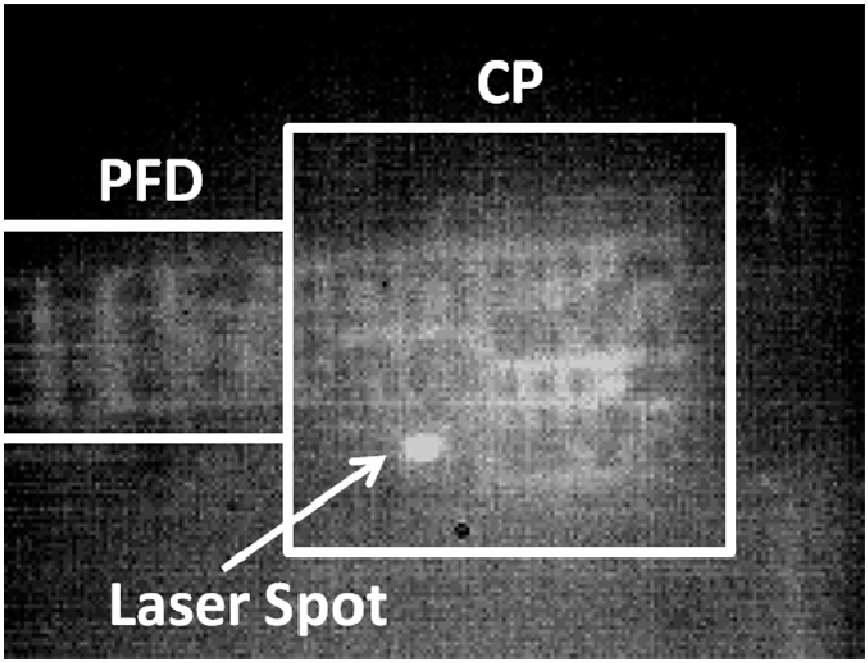


Fig. IX-8. Image of the CP sub-circuit captured by an Indigo Alpha near infrared (NIR) focal plane array.

The 2D-mapping was performed as a function of x-y location using a step size of 0.2 μm. The incident laser pulse energy was 3.5 nJ and the PLL was operated at 200 MHz. Fig. IX-9 illustrates an image of the output phase displacement versus x-y location fused to the layout image of the CP sub-circuit. Each x-y point represents the average phase displacement for 10 transient perturbations. Additional 2D sensitivity maps are provided in APPENDIX C.

According to Fig. IX-9, the most sensitive region of the CP is the NMOS portion of the output switch. Therefore, laser-induced perturbations on the NMOS device at the output of the CP sub-circuit are used in order to characterize the worst-case transients and to validate the models presented in this paper. Fig. IX-10 shows an example of a captured transient following a laser perturbation in the CP sub-circuit. The PLL output frequency in steady-state is approximately 200 MHz. Following the laser strike of

incident energy 5.4 nJ (occurring at approximately 250 ns in Fig. IX-10), the output frequency is reduced to ~50 MHz, subsequently increasing the output phase displacement to ~15 radians. The peak output phase error versus time is measured for each experimental condition as the output phase displacement.

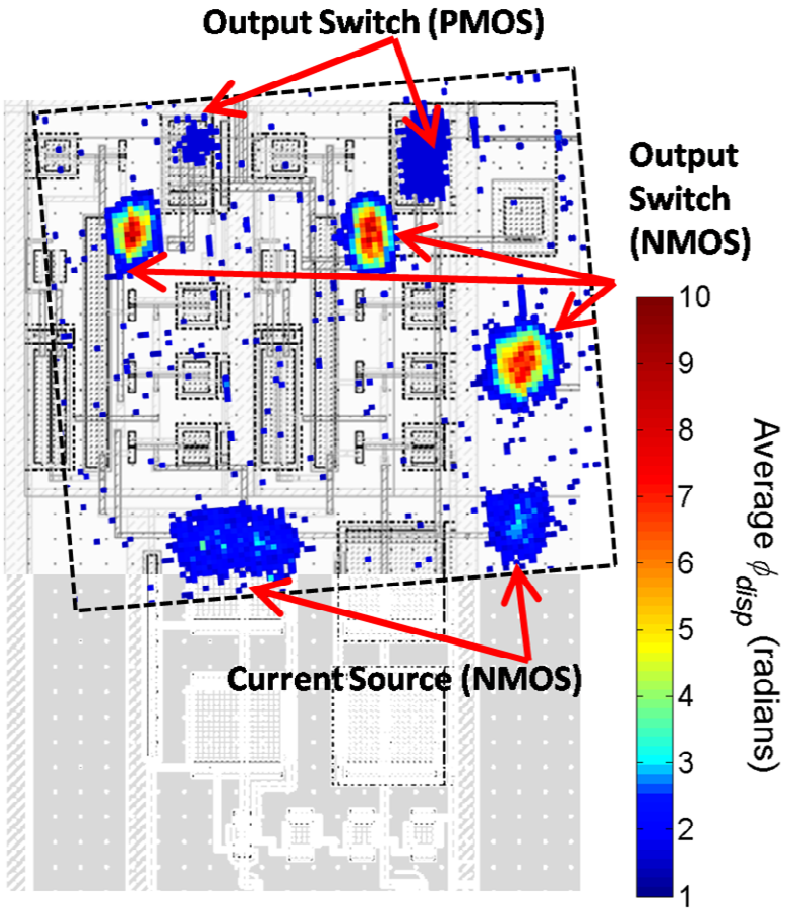


Fig. IX-9. An image of the output phase displacement versus x-y location fused to the layout image of the CP sub-circuit. The laser, with incident pulse energy of 3.5 nJ, was scanned through the CP using a step size of 0.2 μm. The PLL operating frequency was 200 MHz. Each x-y point represents the average phase displacement for 10 transient perturbations.

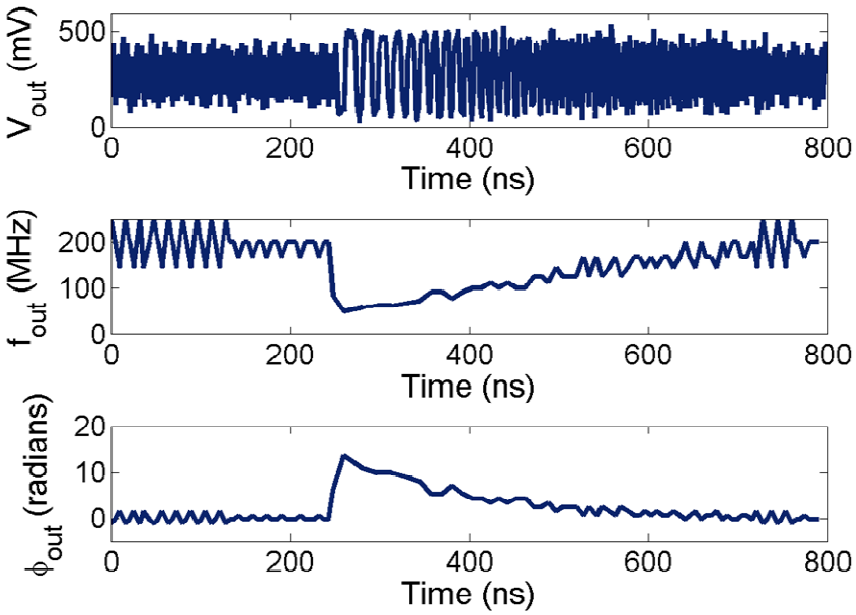


Fig. IX-10. Example of a measured output frequency/phase transient following a laser perturbation in the CP sub-circuit. The PLL was operating at 200 MHz. Following the laser strike with incident energy of 5.4 nJ, the output frequency was reduced to approximately 50 MHz, thus increasing the output phase displacement to approximately 15 radians. The recovery time of the PLL was over 200 ns.

Quantifying the results as discussed, Fig. IX-11 illustrates the average phase displacement in units of radians versus the squared laser energy. Note that the laser energies are squared because TPA carrier deposition increases linearly with the energy squared [Bo86, St85, Mc02]. Each point represents the average of 100 transients with the error bars representing the standard deviation. Multiple data points per energy value are displayed for separate sets of data acquisition and indicate a high degree of repeatability. Also displayed is the analytical solution to Eqn. IX-6 for the design parameters listed in the figure. The data indicates that the critical laser energy (the energy, E_{crit}, at which $\Phi_{disp} \rightarrow \infty$ for increasing $E > E_{crit}$) is approximately 5.4 nJ. Although the exact amount of charge deposition from TPA is difficult to determine from the incident laser energy, the

analytical model suggests that the critical time constant (τ_{crit}) and corresponding Q_{crit} are ~325 ns and ~650 fC, respectively.

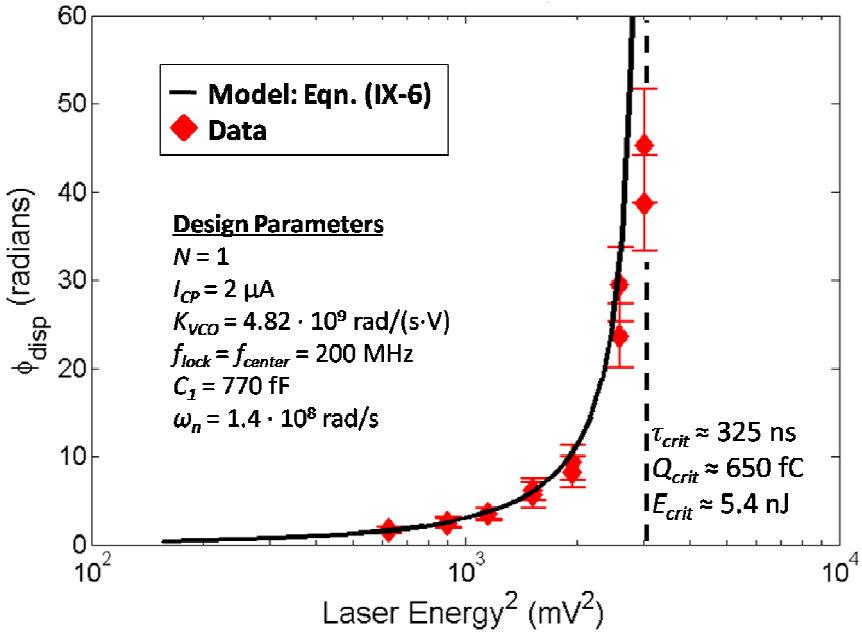


Fig. IX-11. Average measured phase displacement versus the squared laser energy. Also displayed is the analytical solution to Eqn. IX-6 for the design parameters listed in the figure.

The model presented in section IV specifies that increasing the operating frequency increases the critical time constant, thus increasing the length (or deposited charge) of the initial perturbation required to induce equivalent output phase displacements. In order to illustrate this effect, Fig. IX-12 shows the average phase displacement in units of radians versus operating frequency. Again, each point represents the average of 100 transients with the error bars representing the standard deviation. Moreover, multiple data points per frequency value are displayed for separate sets of data acquisition in order to examine repeatability in the measurements. Also displayed by the dashed line is the analytical solution to Eqn. IX-6 for the design parameters listed in the figure. The model predicts

that the output phase displacement should approach infinity for decreasing f_{lock}. However, the output frequency can only be temporarily reduced to the VCO characteristic f_{min}. Therefore, as the frequency error is at most $f_{lock} - f_{min}$, the output phase displacement reaches a maximum proportional to $f_{lock} - f_{min}$ when $t_{rec} > \tau_{crit}$.

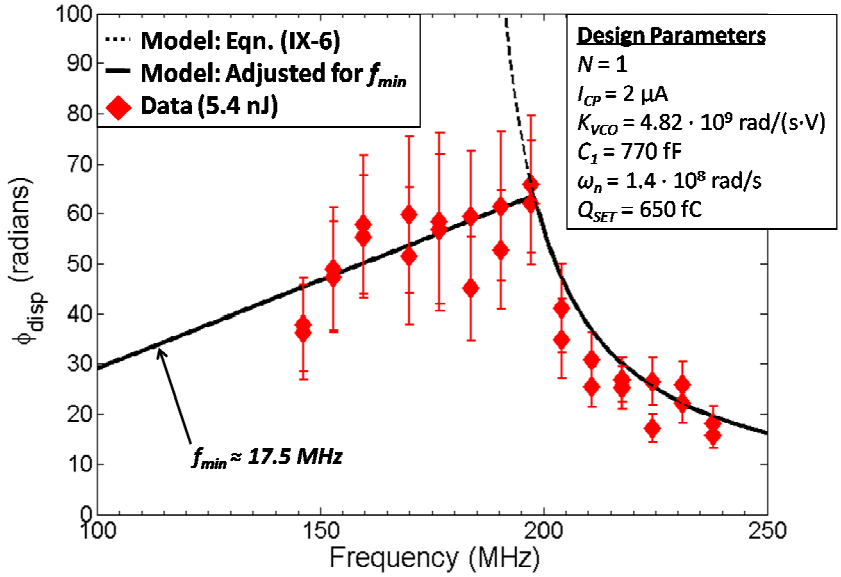


Fig. IX-12. Average phase displacement versus lock frequency within the PLL operating region for incident laser energy of 5.4 nJ. Also displayed is the analytical solution to Eqn. IV-6 for the design parameters listed in the figure assuming a Q_{SET} of 650 fC.

For a given laser energy (analogous to Q_{SET} or t_{rec}), τ_{crit} increases as the frequency increases. Therefore, eventually t_{rec} will be less than τ_{crit}, causing the output phase displacement to decrease with increasing frequency. As shown in Fig. IX-12, this phenomenon occurs at an operating frequency of approximately 200 MHz.

Conclusion

A linear model has been presented for the examination of single transient propagation through phase-locked loops (PLL). Using the first-order model, a set of equations is formulated in closed-form under the assumption that transients are a result of single impulses applied to the various sub-circuits rather than continuous nondeterministic sources. As a result, the critical time constant of the PLL (τ_{crit}) is identified as the primary motivator for single transient propagation through the PLL. Initial perturbations with characteristic time constants greater than τ_{crit} result in output phase transients orders of magnitude greater than initial perturbations with characteristic time constants less than the τ_{crit}. Moreover, utilizing the equations presented, the critical time constant may be maximized (thus reducing the impacts of single loop perturbation) by modifying the designed loop characteristics of the PLL such as the loop gain and natural frequency. In fact, this result indicates that all PLL systems should be designed with an upper bound to the natural frequency in order to reduce the effects of single loop perturbations.

In addition, various simulations and experiments have been performed on PLLs designed in 130 nm and 90 nm technology nodes. Using the described simulation and laser two-photon absorption (TPA) techniques, the generalized model is shown to accurately predict the output phase displacements and critical time constant of the PLL following transient perturbations, validating the analytical results independent of technology. Moreover, no calibration parameters are necessary in order to estimate the characteristic time constants.

CHAPTER X

CONCLUSION

A phase-locked loop (PLL) reliability concern of profound interest is the unavoidable effect of ionizing radiation. In particular, single events (SE) – single particles which can penetrate semiconductor material leaving ionized charge in their wake – can cause information corruption and transient system failure. Single events are ubiquitous – this radiation exists in the environment external to a circuit, and emanates from processing and packaging material integral to a circuit. Once only the concern of space-bound systems, integrated circuit density and power scaling have propelled this issue to the forefront of reliability concerns at current technology nodes in ground-based and space-deployed electronic systems.

In mixed-signal systems, SEs present unique challenges for the characterization and analyses of the device-, circuit-, and system-level effects. Mitigation of these effects requires exceptional understanding of the generation and propagation nature of the transients through the variety of integral circuits within the system. In recent years, there has been a particular interest in the effect of single-event transients (SET) on the PLL because of the propensity to cause loss of frequency lock, and the resultant wide-spread impact on high-performance systems.

This dissertation addresses these fundamental reliability concerns for PLL circuits, and mixed-signal topologies in general, by:

1) Characterizing the SET signatures of a general PLL topology, including the individual sub-circuits such as the phase-frequency detector, charge pump, voltage-controlled oscillator, and frequency divider.
2) Providing various hardening alternatives (if necessary) for the PLL at the sub-circuit level.
3) Identifying the specific closed-loop parameters that directly influence the generation and propagation of SETs in the PLL.
4) Developing a set design guidelines for the analytical mitigation of SETs in PLL circuits.

The following are the important contributions provided by this dissertation:

1) Output phase displacement has been introduced as a single-event transient metric to quantify the portion of a dynamic output signal perturbed by a single-event. The phase displacement is useful for quantifying all dynamic signals, and is the essential parameter (all other performance metrics are shown to be derivatives) for quantifying the erroneous response due to single particles in PLLs.
2) A novel probabilistic analysis technique, applicable to numerous analog topologies, has been demonstrated for SET characterization. The technique allows for a full characterization of complex transient distributions for circuits in noisy environments, without the need to independently characterize system noise. The technique has been shown practical in simulation and experimental analyses.

3) For the first time, various experimental techniques for SET characterization have been performed on mixed-signal PLL circuits at native operating frequencies. The techniques show the feasibility in achieving statistical significance in the transient characterization of complex analog structures. Also illustrated is the ability to map the spatial dependence of the multifaceted nature of transient generation and propagation.
4) Non-conventional, targeted RHBD is shown to be effective for complex mixed-signal topologies. RHBD techniques for various PLL sub-circuits are provided and applicable to a variety of PLL applications.
5) A generalized closed-form model for single transient propagation in all PLL topologies is developed. Accordingly, the specific closed-loop parameters that directly influence the generation and propagation of SETs in PLLs are identified. Moreover, a novel design parameter, the PLL critical time constant, is discovered to be the fundamental factor determining the ease at which transients influence the output phase displacement.
6) A comprehensive list of design guidelines for analytical transient mitigation is developed and applicable to all PLL topologies subject to single transient phenomena.

APPENDIX A

DERIVATIONS FOR THE GENERALIZED LINEAR MODEL FOR SINGLE TRANSIENT PROPAGATION IN PHASE-LOCKED LOOPS

A) Transient Generation in the PFD

A perturbation occurring within the PFD sub-circuit may cause a corrupted bit which can propagate through the combinational logic blocks and appear at either the UP or DOWN signal lines. The resulting signal on node UP or DOWN will have a voltage V_{SET} over time t_{SET}. Assuming the CP is perfectly matched (sink current equals source current) and V_{SET} is large enough to engage the CP, the resulting voltage error (V_e) on V_{inVCO} is given by Eqn. (A-1), which states that V_e increases linearly with increasing t_{SET} and is independent of operating frequency.

$$V_e = \frac{I_{CP} t_{SET}}{C_1} = \frac{2\pi K_{PD} t_{SET}}{C_1} \tag{A-1}$$

It follows that V_e will modify the output frequency of the VCO, thus resulting in an instantaneous frequency error at V_{outVCO} given by Eqn. (A-2).

$$f_e = \frac{V_e K_{VCO}}{2\pi} = \frac{K_{PFD} K_{VCO} t_{SET}}{C_1} = \frac{\omega_n{}^2 t_{SET}}{\beta} \tag{A-2}$$

Then, the worst-case output frequency during the error is given by Eqn. (A-3), where $f_e \geq 0$ for t_{SET} on UP and $0 \leq f_e < f_{lock}$ for t_{SET} on DOWN.

$$f'_{outVCO} = \begin{cases} f_{lock} + f_e \;\; if \;\; t_{SET} \;\; on \text{ UP} \\ f_{lock} - f_e \;\; if \;\; t_{SET} \;\; on \text{ DOWN} \end{cases} \tag{A-3}$$

For the calculation of output phase displacement, it is necessary to determine the worst-case cycle time error (portion of the output signal that is erroneous, T_c=T_e-T_{lock}), as given by Eqns. (A-4) and (A-5). Again, $f_e \geq 0$ for t_{SET} on UP and $0 \leq f_e < f_{lock}$ for t_{SET} on DOWN.

$$T_c = T'_{outVCO} - T_{lock} = \frac{1}{f'_{outVCO}} - \frac{1}{f_{lock}} = \frac{f_{lock} - f'_{outVCO}}{f'_{outVCO} f_{lock}} \tag{A-4}$$

$$T_c = \begin{cases} \dfrac{-f_e}{f_{lock}\left(f_{lock} + f_e\right)} \;\; if \;\; t_{SET} \;\; on \text{ UP} \\ \dfrac{f_e}{f_{lock}\left(f_{lock} - f_e\right)} \;\; if \;\; t_{SET} \;\; on \text{ DOWN} \end{cases} \tag{A-5}$$

Note that for t_{SET} on DOWN, the equation for T_c is not valid for $f_e = f_{lock}$ as T_c would approach infinity. This condition corresponds to the case where the VCO output frequency is reduced to f_0. Finally, the worst-case phase displacement at the PLL output is given as Eqn. (A-6).

$$\phi_{disp} = \frac{2\pi|T_c|}{T_{lock}} = \begin{cases} \dfrac{2\pi\omega_n^2 t_{SET}}{\beta f_{lock} + \omega_n^2 t_{SET}} \;\; if \;\; t_{SET} \;\; on \text{ UP} \\ \dfrac{2\pi\omega_n^2 t_{SET}}{\beta f_{lock} - \omega_n^2 t_{SET}} \;\; if \;\; t_{SET} \;\; on \text{ DOWN} \end{cases} \tag{A-6}$$

Assuming the PLL can respond instantaneously to an error, the re-acquisition time of the PLL is given by Eqn. (A-7), which states simply that the ideal recovery time following the transient perturbation will be the length of time of the transient.

$$t_{rec} = \frac{V_e}{m} = \frac{2\pi K_{PD} t_{SET}}{I_{CP}} = t_{SET} \tag{A-7}$$

The re-acquisition time, however, only occurs during the period of time following the arrival of the next rising edge of the input signal up until the arrival of the next rising edge of the feedback signal. Thus, at most there will a time T_{REF} before re-acquisition can occur. Therefore, the actual recovery time (t'_{rec}) is at most the transient perturbation time plus T_{REF} and some settling time, t_s (Eqn. (A-8)). Note that Eqn. (A-8) is not valid for $\beta = 0$ as this would be an open-loop condition for the PLL.

$$t'_{rec} \leq t_{rec} + T_{REF} + t_s = t_{SET} + \frac{T_{lock}}{\beta} + t_s \tag{A-8}$$

B) Transient Generation in the CP

A transient occurring within the CP can temporarily activate the CP source or sink current sources, thus modifying the voltage on V_{inVCO}. Moreover, it has been shown that perturbations such as those resulting from ionizing particles on the CP output node can deposit/deplete charge directly to/from C_1, thus modifying V_{inVCO} [Bo06, Lo06, Lo07a, Lo07b].

Assuming that Q_{SET} is the amount of charge collected over time t_{SET} at the output of the charge pump, the total charge in/out of the charge pump during time t_{SET} is given by Eqn. (B-1).

$$\Delta Q_e = Q_{SET} + I_{CP} t_{SET} \tag{B-1}$$

As shown by Eqn. (B-2), the resulting voltage error on V_{inVCO} is given merely as the change in total charge in/out of the charge pump during time t_{SET} divided by the loop filter capacitance, C_1. V_e increases linearly for increasing Q_{SET} and/or increasing t_{SET}, and results in an instantaneous output frequency error as shown by Eqn. (B-2).

$$V_e = \frac{\Delta Q_e}{C_1} = \frac{Q_{SET} + I_{CP} t_{SET}}{C_1} \tag{B-2}$$

$$f_e = \frac{V_e K_{VCO}}{2\pi} = \frac{K_{VCO}\left(Q_{SET} + I_{CP} t_{SET}\right)}{2\pi C_1} = \frac{\omega_n^2}{\beta}\left(\frac{Q_{SET}}{I_{CP}} + t_{SET}\right) \tag{B-3}$$

$$\phi_{disp} = \frac{2\pi\left|T_c\right|}{T_{lock}} = \begin{cases} \dfrac{2\pi\omega_n^2\left(\dfrac{Q_{SET}}{I_{CP}} + t_{SET}\right)}{\beta f_{lock} + \omega_n^2\left(\dfrac{Q_{SET}}{I_{CP}} + t_{SET}\right)} & \text{for } Q_{SET} \text{ source} \\ \dfrac{2\pi\omega_n^2\left(\dfrac{Q_{SET}}{I_{CP}} + t_{SET}\right)}{\beta f_{lock} - \omega_n^2\left(\dfrac{Q_{SET}}{I_{CP}} + t_{SET}\right)} & \text{for } Q_{SET} \text{ sink} \end{cases} \tag{B-4}$$

Utilizing Eqns. (A-3), (A-4), and (A-5), it can be shown that the resulting output phase displacement is given by Eqn. (B-4), where $f_e \geq 0$ for Q_{SET} deposited (source) and $0 \leq f_e < f_{lock}$ for Q_{SET} depleted (sink).

The ideal recovery time of the PLL following single transient generation within the CP sub-circuit is determined by Eqn. (B-5), assuming that the PLL can respond instantaneously to an error. Thus, the ideal recovery time following the transient perturbation depends on the amount of charge deposited/depleted and the CP current. Although Φ_{disp} may be reduced by increasing C_1, t_{rec} is independent of C_1.

$$t_{rec} = \frac{V_e}{m} = \frac{\Delta Q_e}{I_{CP}} = \Delta Q_e \left(\frac{\beta K_{VCO}}{2\pi\omega_n^2 C_1} \right) = \frac{Q_{SET}}{I_{CP}} + t_{SET} \tag{B-5}$$

Assuming $t_{SET} << Q_{SET}/(I_{CP})$, the recovery time can be approximated as Eqn. (B-6). As the recovery time follows the acquisition properties of the PLL as defined by Eqn. (13) and cannot occur instantaneously as in the case of the PFD, the actual recovery time (t'_{rec}) is at most t_{rec} plus the period of the reference signal and some settling time (Eqn. (B-7)). However, if $t_{rec} >> T_{REF}$ and $t_{rec} >> t_s$, Eqn. (B-6) is suitable for estimating the recovery time following transients generated within the CP.

$$t_{rec} = \frac{Q_{SET}}{I_{CP}} \tag{B-6}$$

$$t'_{rec} \leq \frac{Q_{SET}}{I_{CP}} + T_{REF} + t_s \tag{B-7}$$

Similar to transients occurring in the PFD, the recovery time following CP transients increases approximately linearly with increasing deposited/depleted charge. In contrast, the recovery time following CP perturbations is weakly dependent on β. Assuming that $Q_{SET}/I_{CP} >> T_{REF}$, the recovery time will follow Eqns. (B-5) or (B-6). Additionally, as the fundamental acquisition time of the PLL was found to be independent of β, the recovery time of the PLL following large V_{inVCO} perturbations must also be independent of β.

C) Transient Generation in the VCO

Transient generation within the VCO sub-circuit is a complex phenomenon and has been analyzed for a variety of oscillator types [Bo05, Ch03, Ch06a, Ch07, Lo08, Lo07c]. In general, oscillator perturbations can result in amplitude modulation, frequency modulation, and temporary oscillation failures. As the phase error resulting from single transients is the predominant concern in this work, we consider only cases of frequency modulation and oscillation failures, both of which can be quantified by output phase displacement [Lo08]. For single ionizing particles, detailed trends on the SET vulnerability of the current-starved VCO are presented in [Bo05, Lo08, Lo07c] and indicate that the vulnerability is a result of complex interdependencies of device biasing, currents, and operating frequency. As it is the goal of this work to understand the impacts of the closed-loop on the transient propagation, it is assumed for this work that the VCO type has been characterized.

Let T_e be the measured maximum erroneous operating period of the output of the VCO. Then the worst-case cycle time-error (T_c), which represents the portion of the operating period that is erroneous, is given as $T_c = T_e - T_{lock}$. In contrast to the PFD and

CP cases where the Φ_{disp} values resulting from PFD and CP transients are secondary effects resulting from loop perturbations, the VCO transient results in an instantaneous phase displacement given as Eqn. (C-1).

$$\phi_{disp} = \frac{2\pi|T_c|}{T_{lock}} = \frac{2\pi|T_e - T_{lock}|}{T_{lock}} = 2\pi\left|\frac{T_e}{T_{lock}} - 1\right| \tag{C-1}$$

Following the initial phase perturbation in the VCO, the transient propagates through the frequency divider to the input of the PFD. Eqn. (C-2) shows the relationship between the divider's output phase (Φ_{out}) and input phase (Φ_{in}), where ω_{in} and $\Phi_{out}(0)$ are the input frequency and initial output phase, respectively. As the frequency divider preserves the time error present in the input signal, the phase error (which is normalized to the operating period) is modified as the signal propagates through the divider.

$$\phi_{\text{out}}(t) = \beta\int_0^t \omega_{in}(\tau)d\tau + \phi_{out}(0) = \beta\phi_{in}(t) + \phi_{out}(0) \tag{C-2}$$

Assuming $\Phi_{out(0)}$ is small, Eqn. (C-2) states that the output phase is merely the input phase multiplied by the feedback factor, β=1/N. For a division factor (N) of 16, for example, the output phase will be 1/16$^{\text{th}}$ that of the input phase. Thus, the phase displacement at the output of the frequency divider is determined as $\Phi_{disp,DIV} = \Phi_{disp}\cdot\beta$. Then, the cycle time-error at the output of the frequency divider detected by the PFD is also $T_c = T_e$-T_{lock} such that the relationship is Eqn. (C-3) holds true.

$$\phi_{disp,DIV} = \frac{2\pi|T_c|}{T_{REF}} = \frac{2\pi\beta|T_c|}{T_{lock}} = \phi_{disp}\beta \tag{C-3}$$

As the PFD detects $\Phi_{disp,DIV}$, $|T_c|$ is the length of a voltage pulse at either the UP ($T_c >$ 0) or DOWN ($T_c <$ 0) output of the PFD. By following the analysis of transients generated in the PFD, the voltage error at the input to the VCO and resulting secondary frequency error and phase displacement can be determined. In an iterative fashion, the process of determining the feedback adjustments of the loop indicates that the output phase displacement approaches zero for increasing iterations, signifying that the PLL is re-acquiring phase lock. Consequently, the secondary phase displacement following the initial transient perturbation at the output of the VCO will always be less than the initial phase displacement.

Similar to the case of transients generated in the PFD, it follows that V_e resulting from the transient at the output of the VCO is given by Eqn. (C-4). Additionally, the actual recovery time is given by Eqn. (C-5) where the ideal recovery time is simply $t_{rec} = |T_c|$. As for the PFD, t_{rec} and V_e increase linearly with increasing transient perturbation at the output of the VCO.

$$V_e = \frac{I_{CP}|T_c|}{C_1} = \frac{2\pi K_{PD}|T_c|}{C_1} \tag{C-4}$$

$$t'_{rec} \leq |T_c| + T_{REF} + t_s \tag{C-5}$$

D) Transient Generation in the Frequency Divider

Similar to the transient manifestations observed in the VCO, a transient can perturb the output phase of the frequency divider (although transients in the divider cannot result in frequency modulation as in the VCO sub-circuit) [Lo09]. Therefore, if $T_{e,DIV}$ is the measured erroneous operating period of the output of the divider, the initial phase displacement at the output of the divider is given by Eqn. (D-1). It is shown in [Lo09] that transients in the frequency divider are bounded by multiples of the input frequency; therefore it is useful in this case to consider the input transient in terms of phase rather than time.

In contrast to transients in the VCO, the divider transient does not directly affect the output phase of the PLL and must propagate through the closed loop. Note that Eqn. (D-1) is determined in an identical fashion as Eqn. (C-1) except that the phase is determined with respect to the output frequency of the divider (f_{REF}) rather than f_{lock}.

$$\phi_{disp,DIV} = \frac{2\pi\left|T_{c,DIV}\right|}{T_{REF}} = \frac{2\pi\left|T_{e,DIV} - T_{REF}\right|}{T_{REF}} = 2\pi\left|\frac{T_{e,DIV}}{T_{REF}} - 1\right| \tag{D-1}$$

As the divider's output phase error is detected by the PFD, it follows that V_e, t'_{rec}, and Φ_{disp} may be determined by following the procedure outlined in sub-section (A) for determining the parameters following PFD transient generation. Thus, it can be shown that that V_e, Φ_{disp}, and t'_{rec} are given by Eqns. (D-2), (D-3), and (D-4), respectively.

$$V_e = \frac{I_{CP}\left|T_{c,DIV}\right|}{C_1} = \frac{2\pi K_{PD}\left|T_{c,DIV}\right|}{C_1} \tag{D-2}$$

$$\phi_{disp} = \frac{2\pi|T_c|}{T_{REF}} = \begin{cases} \dfrac{2\pi\omega_n^2|T_{c,DIV}|}{\beta f_{lock} + \omega_n^2|T_{c,DIV}|} & if \;\; T_{c,DIV} \;\; on \text{ UP} \\ \dfrac{2\pi\omega_n^2|T_{c,DIV}|}{\beta f_{lock} - \omega_n^2|T_{c,DIV}|} & if \;\; T_{c,DIV} \;\; on \text{ DOWN} \end{cases} \tag{D-3}$$

$$t'_{rec} \leq |T_{c,DIV}| + T_{REF} + t_s \tag{D-4}$$

General Observations from Transient Model

The equations derived in the previous sections lead to a general observation regarding the propagation of transients resulting from erroneous impulses in the various PLL sub-circuits. By substituting the ideal recovery times (Eqns. (A-7), (B-5), and (C-5)) into the equations for the output phase displacements (Eqns. (A-6), (B-4), and (D-3)) following transients in the PFD, CP, and frequency divider, respectively, Eqn. (IX-6) can be derived to represent the output phase displacement independent of the sub-circuit of the original perturbation.

APPENDIX B

BASIC SPICE NETLIST FOR THE UNITY GAIN PHASE-LOCKED LOOP CIRCUIT

This appendix details the general SPICE netlist for the unity gain PLL used throughout this work, excluding the specific PDK parameters and the netlist for the frequency dividers. This particular netlist represents a PLL designed for a center frequency of 1.2 GHz.

```
// Design cell name: BASIC PLL NETLIST
// Design view name: schematic
simulator lang=spectre
global 0 vdd!

///////////////// BEGIN BASIC PLL TOPOLOGY /////////////////
// Cell name: CPLL_1.2GHz
I14 (VinVCO VoutVCO) _sub11
I2 (VinVCO) CLPF_generic
I12 (Down Up VinVCO) CP_2uA
I11 (VoutPLL VoutBuff) bufferx3_8
I13 (VoutVCO net14 VoutPLL) bufferx2
I0 (Vclock VoutPLL Down Up) PDF_BuffX4
V0 (Vclock 0) vsource type=pulse val0=0 val1=1.2
period=909p delay=0 \
        rise=80p fall=80p width=375p
///////////////// END BASIC PLL TOPOLOGY /////////////////

////////////// BEGIN BASIC PLL SUB-CIRCUITS //////////////
// PHASE-FREQUENCY DETECTOR (PFD)
// Cell name: PDF_BuffX4
// View name: schematic
subckt PDF_BuffX4 Data Dclock Down Up
    I0 (net49 Data vdd! 0) invx4
    I45 (net011 net0121 net058 vdd! 0) nor2x1
    I79 (net037 net036 net0150 vdd! 0 net052) nand3x1
    I36 (net9 net067 net078 vdd! 0 net036) nand3x1
    I80 (net048 net069 vdd! 0) invx1_schematic
    I81 (net052 net048 vdd! 0) invx1_schematic
    I46 (net036 net011 vdd! 0) invx1_schematic
    I34 (net071 net064 vdd! 0) invx1_schematic
    I35 (net067 net071 vdd! 0) invx1_schematic
    I77 (net083 net036 net0150 vdd! 0) nand2x1
    I82 (net069 net068 net037 vdd! 0) nand2x1
    I78 (net058 net069 net0150 vdd! 0) nand2x1
    I44 (net0121 net078 net064 vdd! 0) nand2x1
    I74 (net082 net078 net036 vdd! 0) nand2x1
```

```
    I76 (net0150 net083 net069 vdd! 0) nand2x1
    I73 (net078 net064 net082 vdd! 0) nand2x1
    I33 (net064 net9 net49 vdd! 0) nand2x1
    I37 (Up net9 vdd! 0) invx4_schematic
    I83 (Down net037 vdd! 0) invx4_schematic
    I84 (net068 Dclock vdd! 0) invx4_schematic
ends PDF_BuffX4
// End of subcircuit definition.
// END PHASE-FREQUENCY DETECTOR


// CHARGE-PUMP (CP)
// Cell name: CP_2uA
// View name: schematic
subckt CP_2uA ChDown ChUp Vcap
    I0 (net42 Vcap ChUp) _sub0
    I32 (Vcap net27 ChDown) _sub0
    T5 (net27 vnbias 0 0) nfet w=30u l=3u
    T2 (vpbias vnbias 0 0) nfet w=30u l=3u
    T9 (vdd! vdd! n1 0) nfet w=900n l=900n
    T13 (n1 n1 vnbias 0) nfet w=900n l=900n
    T15 (0 vnbias vnbias 0) nfet w=720.0n l=720.0n
    T1 (net42 vpbias vdd! vdd!) pfet w=30u l=3u
    T0 (vpbias vpbias vdd! vdd!) pfet w=30u l=3u
ends CP_2uA
// End of subcircuit definition.

// Cell name: p_switch_1.2
// View name: schematic
subckt _sub0 SW0 SW1 in
    I13 (net039 net021 vdd! 0) invx1
    IP1 (net015 net019 vdd! 0) invx1
    I14 (net019 in vdd! 0) invx1
    I12 (net051 net015 vdd! 0) invx1
    T0 (SW0 net051 SW1 vdd!) pfet w=5.6u l=240.0n
    TN2 (net021 0 net019 vdd!) pfet w=1.83u l=80n
    T3 (SW0 net039 SW1 0) nfet w=1.6u l=240.0n
    TN1 (net021 vdd! net019 0) nfet w=915.00n l=80n
ends _sub0
// End of subcircuit definition.
// END CHARGE-PUMP

// LOW-PASS FILTER (LPF)
// Cell name: CLPF_generic
// View name: schematic
subckt CLPF_generic lpf_in
    R1 (net8 0) resistor r=500.0
    C0 (lpf_in net8) capacitor c=2.14p
    C1 (lpf_in 0) capacitor c=210f
ends CLPF_generic
// End of subcircuit definition.
// END LOW-PASS FILTER

// VOLTAGE-CONTROLLED OSCILLATOR (VCO)
// Cell name: vco_1.2_fc1.2GHz
// View name: schematic
subckt _sub11 n_bias v_out_11
```

```
    I30 (n_bias p_bias) _sub9
    I72 (net104 n_bias net112 p_bias) _sub10
    I102 (net68 n_bias v_out_11 p_bias) _sub10
    I103 (net100 n_bias v_out_7 p_bias) _sub10
    I95 (net112 n_bias net96 p_bias) _sub10
    I101 (net84 n_bias net68 p_bias) _sub10
    I98 (net108 n_bias net100 p_bias) _sub10
    I97 (net92 n_bias net108 p_bias) _sub10
    I100 (net76 n_bias net84 p_bias) _sub10
    I31 (v_out_11 n_bias net104 p_bias) _sub10
    I99 (v_out_7 n_bias net76 p_bias) _sub10
    I96 (net96 n_bias net92 p_bias) _sub10
ends _sub11
// End of subcircuit definition.

// Cell name: vco_input_stage_fc1.2GHz
// View name: schematic
subckt _sub9 n_in p_out
    T8 (p_out n_in 0 0) nfet w=230.0n l=80n
    T14 (p_out p_out vdd! vdd!) pfet w=540.0n l=80n
ends _sub9
// End of subcircuit definition.

// Cell name: vco_stage_fc1.2GHz
// View name: schematic
subckt _sub10 _net0 n_in out p_in
    T1 (out _net0 net20 0) nfet w=200n l=80n
    T27 (net20 n_in 0 0) nfet w=230.0n l=80n
    T40 (net050 p_in vdd! vdd!) pfet w=540.0n l=80n
    T0 (out _net0 net050 vdd!) pfet w=480.0n l=80n
ends _sub10
// End of subcircuit definition.
//END VOLTAGE-CONTROLLED OSCILLATOR
///////////////// END BASIC PLL SUB-CIRCUITS ///////////////

/////////////// BEGIN BASIC DIGITAL LIBRARY ///////////////
// Cell name: invx1
// View name: schematic
subckt invx1 O1 i1 vdd_avt vss_avt
    T0 (O1 i1 vss_avt vss_avt) nfet w=200n l=80n
    T1 (O1 i1 vdd_avt vdd_avt) pfet w=480.0n l=80n
ends invx1
// End of subcircuit definition.

// Cell name: invX128_1.2
// View name: schematic
subckt _sub1 in out
    T1 (out in 0 0) nfet w=25.68u l=80n
    T0 (out in vdd! vdd!) pfet w=61.44u l=80n
ends _sub1
// End of subcircuit definition.

// Cell name: invX64_1.2
// View name: schematic
subckt _sub2 in out
    T1 (out in 0 0) nfet w=12.84u l=80n
    T0 (out in vdd! vdd!) pfet w=30.72u l=80n
```

```
ends _sub2
// End of subcircuit definition.

// Cell name: invX32_1.2
// View name: schematic
subckt _sub3 in out
    T1 (out in 0 0) nfet w=6.42u l=80n
    T0 (out in vdd! vdd!) pfet w=15.36u l=80n
ends _sub3
// End of subcircuit definition.


// Cell name: invX16_1.2
// View name: schematic
subckt _sub4 in out
    T1 (out in 0 0) nfet w=3.21u l=80n
    T0 (out in vdd! vdd!) pfet w=7.68u l=80n
ends _sub4
// End of subcircuit definition.

// Cell name: invX8_1.2
// View name: schematic
subckt _sub5 in out
    T1 (out in 0 0) nfet w=1.6u l=80n
    T0 (out in vdd! vdd!) pfet w=3.84u l=80n
ends _sub5
// End of subcircuit definition.

// Cell name: invX4_1.2
// View name: schematic
subckt _sub6 in out
    T1 (out in 0 0) nfet w=800n l=80n
    T0 (out in vdd! vdd!) pfet w=1.92u l=80n
ends _sub6
// End of subcircuit definition.

// Cell name: bufferx3_8
// View name: schematic
subckt bufferx3_8 in out
    I13 (net018 out) _sub1
    I12 (net017 net018) _sub2
    I11 (net012 net017) _sub3
    I10 (net08 net012) _sub4
    I2 (net16 net08) _sub5
    I0 (in net16) _sub6
ends bufferx3_8
// End of subcircuit definition.

// Cell name: invX2_1.2
// View name: schematic
subckt _sub7 in out vdd vss
    T1 (out in vss 0) nfet w=280.0n l=80n
    T0 (out in vdd vdd!) pfet w=910.0n l=80n
ends _sub7
// End of subcircuit definition.

// Cell name: invX1_1.2
```

```
// View name: schematic
subckt _sub8 in out vdd vss
    T1 (out in vss 0) nfet w=200n l=80n
    T0 (out in vdd vdd!) pfet w=480.0n l=80n
ends _sub8
// End of subcircuit definition.

// Cell name: bufferx2
// View name: schematic
subckt bufferx2 in nout out
    I2 (nout out vdd! 0) _sub7
    I0 (in nout vdd! 0) _sub8
ends bufferx2
// End of subcircuit definition.

// Cell name: invx4
// View name: schematic
subckt invx4 O1 i1 vdd_avt vss_avt
    T0 (O1 i1 vss_avt vss_avt) nfet w=800n l=80n
    T1 (O1 i1 vdd_avt vdd_avt) pfet w=1.92u l=80n
ends invx4
// End of subcircuit definition.

// Cell name: nor2x1
// View name: schematic
subckt nor2x1 O1 A B vdd_avt vss_avt
    T1 (O1 A vss_avt vss_avt) nfet w=200n l=80n
    T0 (O1 B vss_avt vss_avt) nfet w=200n l=80n
    T3 (net8 A vdd_avt vdd_avt) pfet w=960.0n l=80n
    T2 (O1 B net8 vdd_avt) pfet w=960.0n l=80n
ends nor2x1
// End of subcircuit definition.

// Cell name: nand3x1
// View name: schematic
subckt nand3x1 O1 i1 i2 vdd_avt vss_avt i3
    T4 (net29 i2 net062 vss_avt) nfet w=600n l=80n
    T5 (net062 i1 vss_avt vss_avt) nfet w=600n l=80n
    T0 (O1 i3 net29 vss_avt) nfet w=600n l=80n
    T3 (O1 i2 vdd_avt vdd_avt) pfet w=480.0n l=80n
    T6 (O1 i1 vdd_avt vdd_avt) pfet w=480.0n l=80n
    T1 (O1 i3 vdd_avt vdd_avt) pfet w=480.0n l=80n
ends nand3x1
// End of subcircuit definition.

// Cell name: invx1
// View name: schematic
subckt invx1_schematic O1 i1 vdd_avt vss_avt
    T0 (O1 i1 vss_avt vss_avt) nfet w=200n l=80n
    T1 (O1 i1 vdd_avt vdd_avt) pfet w=480.0n l=80n
ends invx1_schematic
// End of subcircuit definition.

// Cell name: nand2x1
// View name: schematic
subckt nand2x1 O1 i1 i2 vdd_avt vss_avt
    T4 (net29 i1 vss_avt vss_avt) nfet w=400n l=80n
```

```
    T0 (O1 i2 net29 vss_avt) nfet w=400n l=80n
    T3 (O1 i1 vdd_avt vdd_avt) pfet w=480.0n l=80n
    T1 (O1 i2 vdd_avt vdd_avt) pfet w=480.0n l=80n
ends nand2x1
// End of subcircuit definition.

// Cell name: invx4
// View name: schematic
subckt invx4_schematic O1 i1 vdd_avt vss_avt
    T0 (O1 i1 vss_avt vss_avt) nfet w=800n l=80n
    T1 (O1 i1 vdd_avt vdd_avt) pfet w=1.92u l=80n
ends invx4_schematic
// End of subcircuit definition.
/////////////// END BASIC DIGITAL LIBRARY ///////////////
```

APPENDIX C

2D TRANSIENT-SENSITIVITY MAPS OF CONVENTIONAL CHARGE PUMP OBTAINED FROM LASER TWO-PHOTON ABSORPTION EXPERIMENTS

Fig. C-1 illustrates the layout view of the conventional charge pump circuit in *PLL-130nm*. Indicated by the dashed rectangular region is the approximate region of interest (nMOS portion of an output switch) corresponding to the results displayed in Fig. C-2. The TPA laser (0.2 µm resolution) was used to generate 2D transient maps of the output phase displacement (Φ_{disp}) as a function of incident laser energy at a PLL operating frequency of 150 MHz (see Chapter IX).

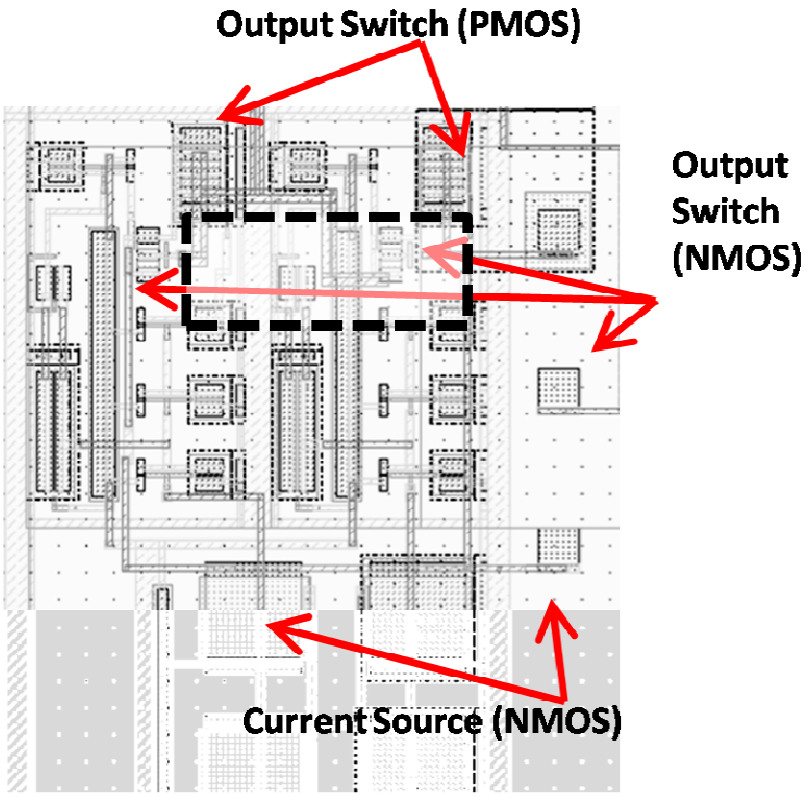


Fig. C-1. Layout view of the conventional charge pump circuit in *PLL-130nm* indicating the approximate region of interest for the results displayed in Fig. C-2.

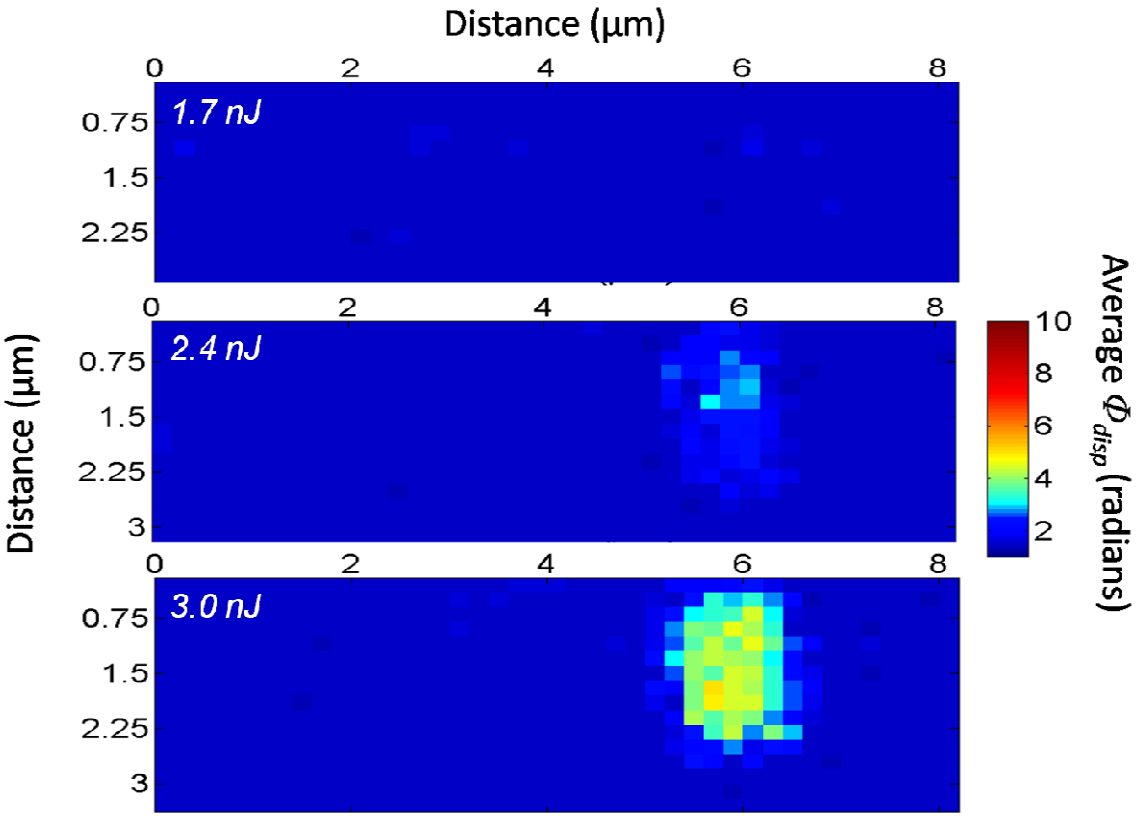


Fig. C-2. 2D transient maps (0.2 µm x-y resolution) of the output phase displacement (Φ_{disp}) as a function of incident laser energy (see Chapter IX) at a PLL operating frequency of 150 MHz.

REFERENCES

[ACCRE] ACCRE Computing Cluster, Nashville, TN, USA. [Online]. Available: http://www.accre.vanderbilt.edu/.

[Ad00] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of Single-Event Transients in Analog Circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2616–2623, Dec. 2000.

[Al03] D. R. Alexander, "Transient Ionizing Radiation Effects in Devices and Circuits," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 565–582, June 2003.

[Am06] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[Am07] O. A. Amusan, A. L. Sternberg, A. F. Witulski, B. L. Bhuva, J. D. Black, M. P. Baze, L. W. Massengill, "Single event upsets in a 130 nm hardened latch design due to charge sharing," *Proc. of the 45th Int. Reliability Physics Symp.*, Arizona, 2007, pp. 306–311.

[An06] *Lock Detect on the ADF4xxx Family of PLL Synthesizers*, Analog Devices, Inc., Norwood, MA, 2006.

[Ba84] G. Baccarani, M. R. Wordeman and R. H. Dennard, "Generalized Scaling Theory and Its Application to a ¼ Micrometer MOSFET Design," *IEEE Trans. Elect. Dev.*, vol. ED-31, no. 4, pp. 452–462, Apr. 1984.

[Ba98] J. L. Barth, "Radiation Environments," *Military and Aerospace Applications of Programmable Devices and Technologies Conference*, Greenbelt, MD, Sept. 1998.

[Ba03] J. L. Barth, C. S. Dyer, and E. G. Stassinopoulos, "Space, Atmospheric, and Terrestial Radiation Environments," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 466–482, June 2003.

[Ba05] R. Baumann, "Single-event effects in advanced CMOS," *in IEEE NSREC Short Course*, 2005, pp. II-1–II-59.

[Ba06] D. Banerjee, "PLL Performance, Simulation, and Design," Fourth Ed., Dog Ear Publishing, 2006.

[Ba08] R. J. Baker, “CMOS: Circuit Design, Layout, and Simulation,” Second Ed., Piscataway, NJ: IEEE Press, 2008.

[Be98] R. E. Best, “Phase-Lock Loops,” Second Ed., New York: McGraw-Hill, 1998.

[Be04] J. Benedetto, P. Eaton, K. Avery, D. Mavis, M. Gadlage, T. Turflinger, P. E. Dodd, and G. Vizkelethyd, “Heavy Ion-Induced Digital Single-Event Transients in Deep Submicron Processes,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3480–3485, Dec. 2004.

[Be06] J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Gadlage, and T. Turflinger, "Digital Single Event Transient Trends With Technology Node Scaling," *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 3462-3465, 2006.

[Bi95] D. J. Bird, S. C. Corbatto, H. Y. Dai, J. W. Elbert, K. D. Green, M. A. Huang, D. B. Kieda, S. Ko, C. G. Larsen, E. C. Loh, M. Z. Luo, M. H. Salamon, J. D. Smith, P. Sokolsky, P. Sommers, J. K. K. Tang, and S. B. Thomas, “Detection of a Cosmic Ray with Measured Energy Well Beyond the Expected Spectral Cutoff Due to Cosmic Microwave Radiation,” *Astrophys. Journal*, vol. 441, pp. 144–150, Mar. 1995.

[Bo86] T. F. Boggess, Jr., K. M. Bohnert, K. Mansour, S. C. Moss, I. W. Boyd, and A. L. Smirl, “Simultaneous measurement of the two-photon coefficient and free-carrier cross section above the bandgap of crystalline silicon,” *IEEE J. Quantum Electron.*, vol. 22, no. 2, pp. 360–368, Feb. 1986.

[Bo02] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, R. L. Pease, S. Buchner, J. W. Howard, D. McMorrow, M. W. Savage, and C. Poivey, “Circuit Modeling of the LM124 Operational Amplifier for Analog Single-Event Transient Analysis,” *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 3090–3096, Dec. 2002.

[Bo04a] Y. Boulghassoul, P. C. Adell, J. D. Rowe, L. W. Massengill, R. D. Schrimpf, and A. L. Sternberg, “System-Level Design Hardening Based on Worst-Case ASET Simulations,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2787–2793, Oct. 2004.

[Bo04b] Y. Boulghassoul, S. Buchner, D. McMorrow, V. Pouget, L. W. Massengill, P. Fouillat, W. T. Holman, C. Poivey, J. W. Howard, M. Savage, and M. C. Maher, “Investigation of millisecond-long analog single-event transients in the LM6144 op amp,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3529–3536, Dec. 2004.

[Bo05] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, and B. L. Bhuva, "Effects of Technology Scaling on the SET Sensitivity of RF CMOS Voltage-Controlled Oscillators," *IEEE. Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2426–2432, Dec. 2005.

[Bo06] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, B. L. Bhuva, and W. T. Holman, "Towards SET Mitigation in RF Digital PLLs: From Error Characterization to Radiation Hardening Considerations," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 4, pp. 2047–2053, Aug. 2006.

[Bu87] S. P. Buchner, D. Wilson, K. Kang, D. Gill, J. A. Mazer, W. D. Raburn, A. B. Campbell, and A. R. Knudson, "Laser Simulation of Single Event Upsets," *IEEE Trans. Nucl. Sci.*, vol. NS-34, no. 6, pp. 1228–1233, Dec. 1987.

[Bu01] S. Buchner and M. Baze, "Single-event transients in fast electronic circuits," *in IEEE NSREC Short Course*, 2001, pp. V-1–V-105.

[Bu05] S. Buchner and D. McMorrow, "Single-Event Transients in Linear Integrated Circuits," *in IEEE NSREC Short Course*, 2005, pp. IV-1–IV-77.

[Ch03] W. Chen, V. Pouget, H. J. Barnaby, J. D. Cressler, G. Niu, P. Fouillat, Y. Deval, and D. Lewis, "Investigation of single-event transients in voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2081–2087, Dec. 2003.

[Ch06a] W. Chen, V. Pouget, G. K. Gentry, H. J. Barnaby, B. Vermeire, B. Bakkaloglu, K. Kiaei, K. E. Holbert, and P. Fouillat, "Radiation Hardened by Design RF Circuits Implemented in 0.13 um CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 3449-3454, 2006.

[Ch06b] H. H. Chung, W. Chen, B. Bakkaloglu, H. J. Barnaby, B. Vermeire, and S. Kiaei, "Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3539–3543, Dec. 2006.

[Ch07] W. Chen, N. Varanasi, V. Pouget, H. J. Barnaby, B. Vermeire, P. C. Adell, T. Copani, and P. Fouillat, "Impact of VCO Topology on SET Induced Frequency Response," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2500–2505, Dec. 2007.

[Da07a] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, , O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf and L. W. Massengill, "Effect of Well and Substrate Potential Modulation on Single Event Pulse Shape in Deep Submicron CMOS," *IEEE Trans. On Nucl. Sci.*, vol. 54, no. 6, pp. 2407–2412, Dec. 2007.

[Da07b] S. DasGupta, “Trends in Single Event Pulse Widths and Pulse Shapes in Deep-Submicron CMOS,” *M. S. Thesis*, Dec., 2007.

[De74] R. H. Dennard, F. H. Gaensslen, H-N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, “Design of Ion-Implanted MOSFETs with Very Small Physical Dimension,” *IEEE J. Solid State Circuits*, vol. 9, no. 5, pp. 256–268, Oct. 1974.

[Do96] P. E. Dodd, F. W. Sexton, G. L. Hash, M. R. Shaneyfelt, B. L. Draper, A. J. Farino, and R. S. Flores, “Impact of technology trends on SEU in CMOS SRAMs,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2797–2804, Dec. 1996.

[Do99] P. E. Dodd, “Basic Mechanisms for Single-Event Effects,” *in IEEE NSREC Short Course*, 1999, pp. II-1–II-85.

[Do03] P. E. Dodd and L. W. Massengill, “Basic Upset Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–601, June 2003.

[Ec94] R. Eccofet, S. Duzellier, P. Tastet, C. Aicardi, and M. Labrunee, “Observation of Heavy Ion Induced Transients in Linear Circuits,” *IEEE Radiation Effects Data Workshop*, pp. 72–77, July, 1994.

[Fo02] A. Fox, “PLL Synthesizers,” *Analog Dialogue: Ask the Applications Engineer–30*, vol. 36, no. 3, pp. 1–4, 2002.

[Fr04] *PLL Lock Detection on the HC12 D-Family*, Freescale Semiconductor, Inc., Chandler, AZ, 2004.

[Fu85] J. S. Fu, C. L. Axness, and H. T. Weaver, “Memory SEU simulations using 2-D transport calculations,” *IEEE Electron. Device Lett.*, vol. 6, no. 8, pp. 422–424, Aug. 1985.

[Ga79] F. M. Gardner, *Phaselock Techniques*, 2nd ed. New York: Wiley, 1979.

[Ga80] F.M. Gardner, “Charge-Pump Phase-Lock Loops,” *IEEE Trans. Comm.*, vol. COM-28, no. 11., pp. 1849-1858., Nov. 1980.

[Ga96] K. F. Galloway and G. H. Johnson, “Catastrophic single event effects in the natural environment,” *in IEEE NSREC Short Course*, 1996, pp. IV-1–IV-72.

[Ga04] M. J. Gadlage, R. D. Schrimpf, J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Sibley, K. Avery, and T. L. Turflinger, “Single Event Transient Pulsewidths in Digital Microcircuits,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3285–3290, Dec. 2004.

[Ga05] F. M. Gardner, *Phaselock Techniques*, 3rd ed. Hoboken, NJ: Wiley, 2005.

[Ga08] M. J. Gadlage, R. D. Schrimpf, B. Narasimham, J. A. Pellish, K. M. Warren, R. A. Reed, R. A. Weller, B. L. Bhuva, L. W. Massengill, and X. Zhu, "Assessing Alpha Particle-Induced Single Event Transient Vulnerability in a 90-nm CMOS Technology," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 638–640, June 2008.

[Ha85] J. R. Hauser, S. E. Diehl-Nagle, A. R. Knudson, A. B. Campbell, W. J. Stapor, and P. Shapiro, "Ion Track Shunt Effects in Multi-Junction Structures," *IEEE Trans. Nucl. Sci.*, vol. NS-32, no. 6, pp. 4115–4121, 1985.

[Ha04] P. K. Hanumolu, M. Brownlee, K. Mayaram, and M. Un-Ku, "Analysis of charge-pump phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, pp. 1665-1674, 2004.

[Ha05a] C. Hafer, V. Schnathorst, J. Pfeil, T. Meade, T. Farris, and A. Jordon, "SEE and TID Results for a Commercially Fabricated Radiation-Hardened Clock Generator Circuit," *IEEE NSREC 2005 Radiation Effects Data Workshop Record*, pp. 93-97, 2005.

[Ha05b] M. Hartwell, C. Hafer, P. Milliken, and T. Farris, "Single event effects testing of a PLL and LVDS in a RadHard-by-design 0.25-micron ASIC," *Radiation Effects Data Workshop, 2005, IEEE*, pp. 98-101, Dec. 2005.

[Ha06] D. L. Hansen, P. Chu, K. Jobe, A. L. McKay, and H. P. Warren, "SEU Cross Sections of Hardened and Unhardened SiGe Circuits," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3579–3586, Dec. 2006.

[Ha08] C. Hafer, J. Pfeil, D. Bass, A. Jordan, and T. Farris, "Single Event Transient Event Frequency Prediction Model for a Next Generation PLL," *Radiation Effects Data Workshop, 2008 IEEE*, pp. 85-89, Dec. 2008.

[He99] F. Herzel and B. Razavi, "A Study of Oscillator Jitter Due to Supply and Substrate Noise," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 1, pp. 56-62, Jan. 1999.

[He04] P. Heydari, "Analysis of the PLL jitter due to power/ground and substrate noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, pp. 2404-2416, 2004.

[Ho07] G. Holman and S. Benedict, "Solar Flare Theory Educational Web Pages," Heliophysics Science Division, NASA/Goddard Space Flight Center, Solar Physics Laboratory, [Online]. Available: http://hesperia.gsfc.nasa.gov/sftheory/flare.htm, Aug. 2007.

[Hs81] C. M. Hsieh, P. C. Murley, and R. R. O'Brien, "A Field-Funneling Effect on the Collection of Alpha-Particle-Generated Carriers in Silicon Devices," *IEEE Electron Device Letters*, vol. 2, no. 4, pp. 103–105, Apr. 1981.

[Hu93] C. Hu, "Future CMOS Scaling and Reliability," *Proc. of the* IEEE, vol. 81, no. 5, pp. 682–689, May 1993.

[Id04] *PLL Lock Indicato*r, Integrated Device Technology, Inc., San Jose, CA, 2004.

[Jo96a] K. Jobe, M. Shoga, and R. Koga, "A Systems-Oriented Single Event Effects Test Approach for High Speed Digital Phase-Locked Loops," *IEEE Trans. Nucl. Sci*., vol. 43, pp. 2868-2873, 1996.

[Jo96b] A. H. Johnston, "The influence of VLSI technology evolution on radiation-induced latchup in space systems," *IEEE Trans. Nucl. Sci.,* vol. 43, no. 2, pp. 505–521, Apr. 1996.

[Jo98] A. H. Johnston, "Radiation effects in advanced microelectronics technologies," *IEEE Trans. Nucl. Sci.,* vol. 45, no. 3, pp. 1339–1354, June 1998.

[Jo00a] A. H. Johnston and S. M Guertin, "The effects of space radiation on linear integrated circuits," *in Proc. 2000 IEEE Aerospace Conference*, vol. 5, pp. 363–369, Mar. 2000.

[Jo00b] A. H. Johnston, G. M. Swift, T. F. Miyahira, and L. D. Edmonds, "A Model for Single Event Transients in Comparators," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2624–2633, Dec. 2000.

[Jo02] A. H. Johnston, T. F. Miyahira, L. D. Edmonds, and F. Irom, "Single-Event Transients in High-Speed Comparators," *IEEE Trans. Nucl. Sci.,* vol. 49, no. 6, pp. 3082–3089, Dec. 2002.

[Ke89] S. E. Kerns, L. W. Massengill, D. V. Kerns, Jr., M. L. Alles, T. W. Houston, H. Lu, and L. R. Hite, "Model for CMOS/SOI single-event vulnerability," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 6, pp. 2305–2310, Dec. 1989.

[Ko93] R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. LaLumondiere, S. J. Hansel, K. B. Crawford, and W. R. Crain, "Observation of Single-Event Upsets in Analog Microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1838–1844, Dec. 1993.

[Ko99] H. C. Koons, J. E. Mazur, R. S. Selesnick, J. B. Blake, J. F. Fennell, J. L. Roeder, and P. C. Anderson, "The impact of the space environment on space systems," *Aerospace Technical Report*, no. TR-99(1670)-1, July, 1999.

[Ko00] R. Koga, S. H. Crain, K. B. Crawford, S. C. Moss, S. D. LaLumondiere, and J. W. Howard, Jr., “Single-Event Transient (SET) Sensitivity of Radiation Hardened and COTS Voltage Comparators,” *in Proc. 2000 IEEE Radiation Effects Data Workshop Record*, Reno, Nevada, July 2000, pp. 53–60.

[Kr82] V. Kroupa, "Noise Properties of PLL Systems," *IEEE Trans. Commun.*, vol. 30, pp. 2244-2252, 1982.

[La02] S. D. LaLumondiere, R. Koga, P. Yu, M. C. Maher, and S. C. Moss, “Laser-Induced and Heavy Ion-Induced Single-Event Transient (SET) Sensitivity Measurements on 139-Type Comparators,” *IEEE Trans. Nucl. Sci.,* vol. 49, no. 6, pp. 3121–3128, Dec. 2002.

[La06] H. Lapuyade, V. Pouget, J. B. Bégueret, P. Hellmuth, T. Taris, O. Mazouffre, P. Fouillat, and Y. Deval, “A Radiation-Hardened Injection Locked Oscillator Devoted to Radio-Frequency Applications,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 4, pp. 2040–2046, Aug. 2006.

[Le04a] T. H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits,” Second Ed., New York, NY: Cambridge University Press, 2004.

[Le04b] S. Levantino, L. Romano, S. Pellerano, C. Samori, and A. L. Lacaita, “Phase Noise in Digital Frequency Dividers,” *IEEE J. Solid State*, vol. 39, no. 5, pp. 775–784, May 2004.

[Lo06] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, A. F. Witulski and Y. Boulghassoul, “A Hardened-by-Design Technique for RF Digital Phase-Locked Loops,” *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3432–3438, Dec. 2006.

[Lo07a] T. D. Loveless, “A Single-Event-Hardened Charge Pump for Phase-Locked-Loop Circuits,” *M. S. Thesis*, *Vanderbilt University*, Mar. 2007.

[Lo07b] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, R. A. Reed, D. McMorrow, J. S. Melinger, and P. Jenkins, “A Single-Event-Hardened Phase-Locked Loop Fabricated in 130 nm CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2012–2020, Dec. 2007.

[Lo07c] T. D. Loveless, L. W. Massengill, W. T. Holman, and B. L. Bhuva, “Modeling and Mitigating Single-Event Transients in Voltage-Controlled Oscillators,” accepted for publication in *IEEE Trans. Nucl. Sci.*, Dec. 2007.

[Lo08] T. D. Loveless, L. W. Massengill, B. L. Bhuva, W. T. Holman, M. C. Casey, R. A. Reed, S. A. Nation, D. McMorrow, and J. S. Melinger, "A Probabilistic Analysis Technique Applied to a Radiation-Hardened-by-Design Voltage-Controlled Oscillator for Mixed-Signal Phase-Locked Loops," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 3447-3455, 2008.

[Lo09] T. D. Loveless, B. L. Bhuva, W. T. Holman, B. D. Olson, and L. W. Massengill, "Analysis of Single-Event Transients in Integer-N Frequency Dividers and Impacts on Phase-Locked Loop Performance," *in review, IEEE Trans. Nucl. Sci.*, 2009.

[Ma93] L. W. Massengill, "SEU modeling and prediction techniques," *in IEEE NSREC Short Course*, 1993, pp. III-1–III-93.

[Ma99] P. W. Marshall and C. J. Marshall, "Proton Effects and Test Issues for Satellite Designers," *in IEEE NSREC Short Course*, 1999, pp. IV-1–IV-49.

[Ma02] J. Mazur, "The Radiation Environment Outside and Inside a Spacecraft," *in IEEE NSREC Short Course*, 2002, pp. II-1–II-69.

[Ma04] P. Marshall, M. Carts, A. Campbell, R. Ladbury, R. Reed, C. Marshall, S. Currie, D. McMorrow, S. Buchner, C. Seidleck, P. Riggs, K. Frits, B. Randall, and B. Gilbert, "A comparative study of heavy-ion and proton-induced bit-error sensitivity and complex burst-error modes in a commercially available high-speed SiGe BiCMOS," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3457-3463, Dec. 2004.

[Mc02] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Sub-bandgap laser-induced single event effects: Carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3002–3008, Dec. 2002.

[Mc03] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, Y. Boulghassoul, L. W. Massengill, and R. L. Pease, "Three-Dimensional Mapping of Single-Event Effects Using Two Photon Absorption," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2199–2207, Dec. 2003.

[Mc07] D. McMorrow, W. T. Lotshaw, J. S. Melinger, P. Jenkins, P. Eaton, J. Benedetto, M. Gadlage, J. D. Davis, R. K. Lawrence, D. Loveless, and L. Massengill, "Single-Event Effects Induced by Through-Wafer Sub-Bandgap Two-Photon Absorption," *in Nonlinear Optics: Materials, Fundamentals and Applications*, *OSA Technical Digest (CD) (Optical Society of America, 2007)*, paper WC4, 2007.

[Me74] P. Meyer, R. Ramaty, and W. R. Webber, "Cosmic Rays: Astronomy with energetic particles," *Physics Today*, vol. 27, no. 10, pp. 23–30; 32, Oct. 1974.

[Me82] G. C. Messenger, “Collection of Charge on Junction Nodes from Ion Tracks,” IEEE Trans. Nucl. Sci., vol. NS-29, no. 6, pp. 2024–2031, Dec. 1982.

[Me02] A. Mehrotra, "Noise analysis of phase-locked loops," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, pp. 1309-1316, 2002.

[MOSIS] http://www.mosis.com/, "The MOSIS Service." Marina del Rey, California.

[Mu03] R. S. Muller, T. I. Kamins, and M. Chan, “Device Electronics for Integrated Circuits,” Third Ed., John Wiley & Sons, Inc., 2003.

[Na07] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, O. A. Amusan, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, J. M. Benedetto, and P. H. Eaton, "Characterization of Digital Single Event Transient Pulse-Widths in 130-nm and 90-nm CMOS Technologies," IEEE Trans. Nucl. Sci., vol. 54, pp. 2506-2511, 2007.

[Ol03] T. R. Oldham and F. B McLean, “Total Ionizing Dose Effects in MOS Oxides and Devices,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 483–499, June 2003.

[Ol05] B. D. Olson, D. R. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. Doyle, and D. McMorrow, “Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2132–2136, Dec. 2005.

[Ol07] B. D. Olson, O. A. Amusan, S. Dasgupta, L. W. Massengill, A. F. Witulski, B. L. Bhuva, M. L. Alles, K. M. Warren, and D. R. Ball., “Analysis of parasitic pnp bipolar transistor mitigation using well contacts in 130 nm and 90 nm CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pp. 894–897, Aug. 2007.

[Pe82] E. L. Petersen, P. Shapiro, J. H. Adams, Jr., and E. A. Burke, “Calculation of Cosmic-Ray Induced Soft Upset and Scaling in VLSI Devices,” *IEEE Trans. Nucl. Sci.,* vol. 29, no. 6, pp. 2055–2063, Dec. 1982.

[Pe01] R. L. Pease, A. Sternberg, L. Massengill, R. Schrimpf, S. Buchner, M. Savage, J. Titus, and T. Turflinger, “Critical charge for single-event transients (SETs) in bipolar linear circuits,” *IEEE. Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1966–1972, Dec. 2001.

[Pe02] R. L. Pease, A. L. Sternberg, Y. Boulghassoul, L. W. Massengill, S. Buchner, D. McMorrow, D. S. Walsh, G. L Hash, S. D. LaLumondiere, and S. C. Moss, “Comparison of SETs in Bipolar Linear Circuits Generated with an Ion Microbeam, Laser and Circuit Simulation,” *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3163–3170, Dec. 2002.

[Po99] V. Pouget, D. Lewis, H. Lapuyade, R. Briand, P. Fouillat, L. Sarger, and M. C. Calvet, "Validation of Radiation Hardened Designs by Pulsed Laser Testing and SPICE Analysis," *Microelectron. Reliab.*, vol. 39, no. 6, pp. 931–935, June 1999.

[Ra95] B. Razavi, K. F. Lee, and R. H. Yan, "Design of High-Speed, Low-Power Frequency Dividers and Phase-Locked Loops in Deep Submicron CMOS," *IEEE J. Solid State*, vol. 30, no. 2, pp. 101–109, Feb. 1995.

[Ra01] B. Razavi, "Design of Analog CMOS Integrated Circuits," New York, NY: McGraw-Hill, 2001.

[Re08] R. A. Reed, "Fundamental Mechanisms for Single Particle-Induced Soft Errors," *in IEEE NSREC Short Course*, 2008, pp. I-1–I-63.

[Sa02] M. W. Savage, T. Turflinger, J. L. Titus, H. F. Barsun, A. Sternberg, Y. Boulghassoul, and L. W. Massengill, "Variations in SET pulse shapes in the LM124A and LM111," *IEEE NSREC 2002 Radiation Effects Data Workshop Record*, pp. 75–81, July 2002.

[Sa03] M. W. Savage, T. Turflinger, J. L. Titus, R. L. Pease, and C. Poivey, "Characterization of SET Response of the LM124A, the LM111, and LM6144," *IEEE NSREC 2003 Radiation Effects Data Workshop Record*, pp. 121–126, July 2003.

[SEE04] *SEE Symp. 2004*, panel discussion records.

[Si09] Brian D. Sierawski, Jonathan A. Pellish, Robert A. Reed, Ronald D. Schrimpf, Robert A. Weller, Marcus H. Mendenhall, Jeffrey D. Black, Alan D. Tipton, Michael A. Xapsos, Robert C. Baumann, Xiaowei Deng, Mark R. Friendlich, Hak S. Kim, Anthony M. Phan, and Christina M. Seidleck, "Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions" *in review, IEEE Trans. Nucl. Sci.*, Dec. 2009.

[SOHO] National Aeronautics and Space Administration's Goddard Space Flight Center, Solar & Heliospheric Observatory (SOHO) Project. [Online]. Available: http://visibleearth.nasa.gov/view_rec.php?id=1675.

[Sr03] J. R. Srour, C. J. Marshall, and P. W. Marshall, "Review of Displacement Damage Effects in Silicon Devices," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 653–670, June 2003.

[St85] E. W. Van Stryland, H. Vanherzeele, M. A. Woodall, M. J. Soileau, A. L. Smirl, S. Guha, and T. F. Boggess, "Two photon absorption, nonlinear refraction and optical limiting," *Opt. Eng.*, vol. 24, pp. 613–623, Jul./Aug. 1985.

[St88a] W. J. Stapor, P. T. McDonald, A. R, Knudson, A. B. Campbell, and B. G. Glagola, "Charge Collection in Silicon for Ions of Different Energy but Same Linear Energy Transfer (LET)," *IEEE Trans. on Nuclear Science*, vol. NS-35, no. 6, pp. 1585–1590, Dec. 1988.

[St88b] E. G. Stassinopoulos and J. P. Raymond, "The space radiation environment for electronics," *Proc. of the IEEE*, vol. 76, pp. 1423–1442, Nov. 1988.

[St02a] H. Stark, and J. W. Woods, "Probability and Random Processes with Applications to Signal Processing," Third Ed., Upper Saddle River, New Jersey: Prentice Hall, 2002.

[St02b] A. L. Sternberg, L. W. Massengill, S. Buchner, R. L. Pease, Y. Boulghassoul, M. W. Savage, D. McMorrow, and R. A. Weller, "The Role of Parasitic Elements in the Single-Event Transient Response of Linear Circuits," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3115–3120, Dec. 2002.

[Su06] A. K. Sutton, R. Krithivasan, P. W. Marshall, M. A. Carts, C. Seidleck, R. Ladbury, J. D. Cressler, C. J. Marshall, S. Currie, R. A. Reed, G. Nui, B. Randall, K. Fritz, D. McMorrow, and B. Gilbert, "SEU Error Signature Analysis of Gbit/s SiGe Logic Circuits Using a Pulsed Laser Microprobe," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3277–3284, Dec. 2006.

[Ti06] A. D. Tipton, J. A. Pellish, R. A. Reed, R. D. Schrimpf, R. A. Weller, M. H. Mendenhall, B. Sierawski, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. D. Cressler, P. W. Marshall, and G. Vizkelethy, "Multiple-Bit Upset in 130 nm CMOS Technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3259–3264, Dec. 2006.

[Va59] J. A. Van Allen, C. E. McIlwain, and G. H. Ludwig, "Radiation observations with satellite 1958 EX," *J. Geophys. Res.*, vol. 64, no. 3, pp. 271–286, 1959.

[Wa86] A. W. Waskiewicz, J. W. Groninger, V. H. Strahan, and D. M. Long, "Burnout of power MOS transistors with heavy ions of Californium-252," *IEEE Trans. Nucl. Sci.,* vol. 33, no. 6, pp. 1710–1713, Dec. 1986.

[We02] T. Weatherford, "From carriers to contacts, a review of SEE charge collection processes in devices," *in IEEE NSREC Short Course*, 2002, pp. IV-1–IV-53.

[Wo93] R. L. Woodruff and P. J. Rudeck, "Three-dimensional numerical simulation of single event upset of an SRAM cell," *IEEE Trans. Nucl. Sci*., vol. 40, no. 6, pp. 1795–1803, Dec. 1993.

[Xa06] M. Xapsos, "Modeling the Space Radiation Environment," *in IEEE NSREC Short Course*, 2006, pp. II-1–II-62.