SINGLE EVENT TRANSIENT AND TOTAL IONIZING DOSE EFFECTS ON III-V MOSFETs FOR SUB-10 NM NODE CMOS

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Chapter 1. Introduction

Ever since the invention of the transistor, the semiconductor industry has seen tremendous progress by following Moore's law, which states that the number of transistors per integrated circuit doubles approximately every 24 months. For example, Fig. 1.1 shows that the transistor count in microprocessors has been increasing for over 40 years [1]. The key to sustain Moore's law is the miniaturization of single transistors. However, conventional scaling has hit a power wall, so that it is now limited by the power consumption [2]. Therefore, low power and high performance logic devices are currently actively investigated to maintain the scaling trends.

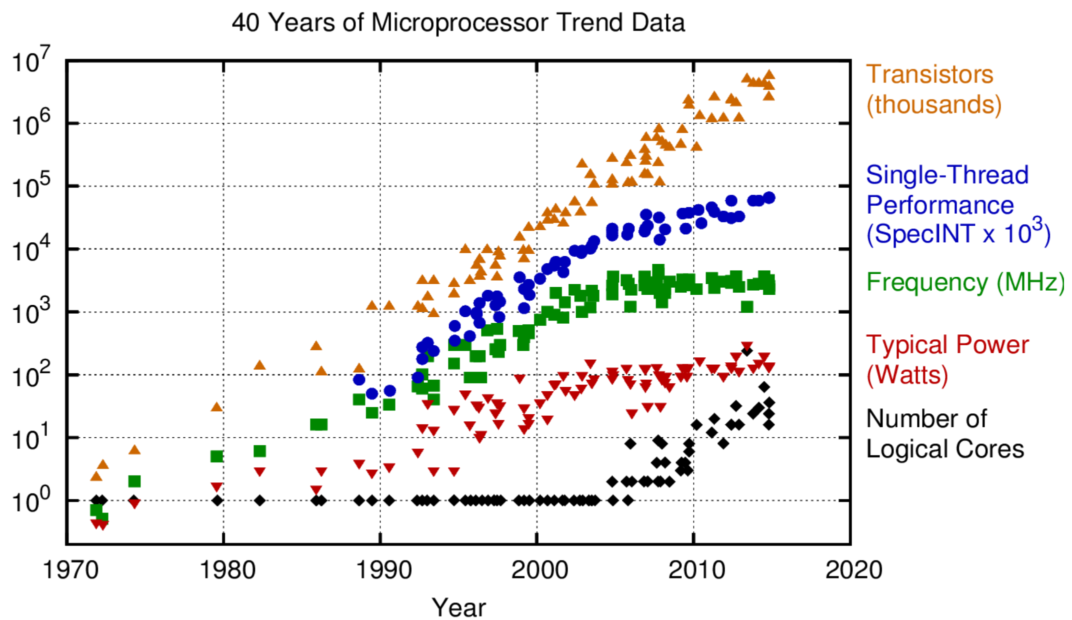

Fig. 1.1. 40 years of microprocessor trend data [1].

However, it is becoming more and more challenging to continue transistor scaling. Technology innovations are necessary to extend Moore's law. Several transformative changes have been implemented and explored to maintain the scaling, as shown in Fig. 1.2 [3]. For example, strain engineering was first introduced in the 90 nm node to increase both electron and hole mobility [4], [5]. Metal-gate/high-κ gate stacks were introduced in the 45 nm node to reduce the gate leakage and eliminate poly-silicon depletion [6], [7]. The most dramatic change was the transition from planar transistor to FinFET technology in the 22 nm node for combating short channel effects [8], [9], [10]. However, as scaling continues, current techniques are reaching their limits and new technologies are needed. Some of the leading candidates for sub-10 nm nodes are alternative

channel materials which have superior transport properties. Currently III-V/Ge materials are promising NMOS/PMOS channel materials due to their high carrier mobility and injection velocity [11], [12], [13], [14].

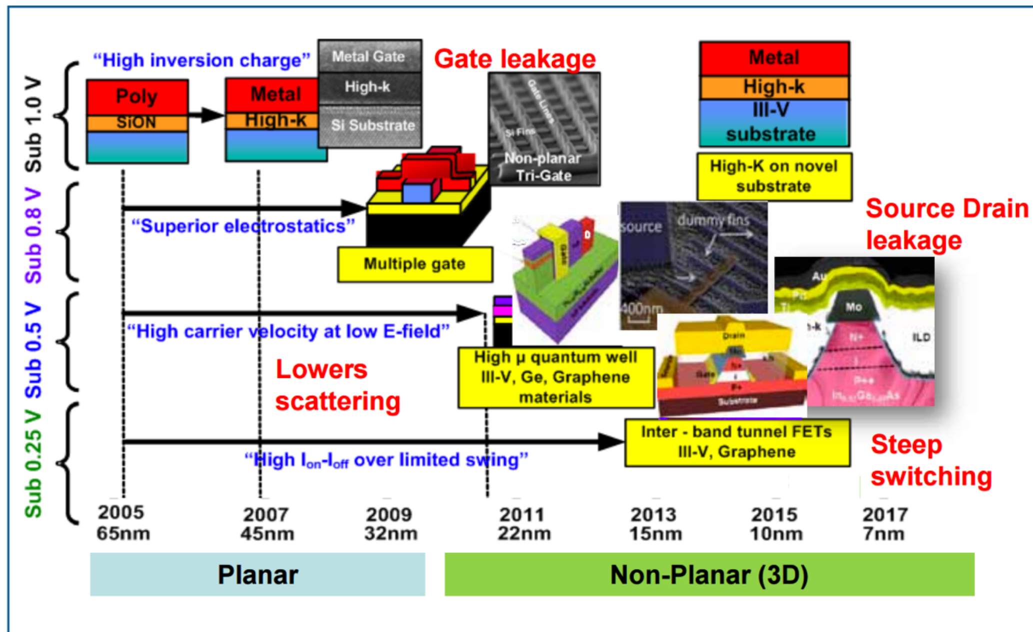

Fig. 1.2. Trend in state-of-the-art high performance (HP) CMOS transistor innovation. Transformative changes in materials (high-k dielectric, Ge, III-V channel) and the transistor architecture (3D, Tunnel FET) being implemented and explored to maintain historical rate of performance, density and power scaling [3].

1.1. III-V MOSFET

The low field carrier mobilities of typical semiconductor materials are shown in Fig. 1.3(a) [15]. The electron mobility in III-V materials, especially InGaAs, is about 10x higher than Si. This is due to the low effective mass of electrons in InGaAs compared with Si. Similarly, the hole mobility in Ge is significantly higher than Si. As a result, heterogeneous integration of InGaAs and Ge as channel materials on silicon substrates is under consideration for the next generation logic devices [11], [12], [13].

For sub-10 nm technology, transistors are operating in the quasi-ballistic region, where the electrons traveling from source to drain experience no or few scattering events [16]. In this circumstance, low field mobility is no longer a physically meaningful parameter. Instead, the injection velocity v_{inj} at the 'virtual source', where the conduction band barrier is the highest, is the right parameter to characterize the transport properties [17]. The transistor ballistic current can be expressed as [18]:

$$I_D = Q_i v_{inj} \frac{1 - \mathcal{F}_{1/2}(\eta_{F2}) / \mathcal{F}_{1/2}(\eta_{F1})}{1 + \mathcal{F}_0(\eta_{F2}) / \mathcal{F}_0(\eta_{F1})} \tag{1.1}$$

where Q_i is the charge density at the top of conduction band and $\mathcal{F}_i$ is the Fermi-Dirac integral of order *i*. The other parameters are defined as:

$$\begin{aligned} v_{inj} &= \sqrt{\frac{2k_B T}{\pi m^*}} \frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} \\ \eta_{F1} &= \frac{E_{FS} - \varepsilon_S}{k_B T} \\ \eta_{F2} &= \frac{E_{FD} - \varepsilon_D}{k_B T} \\ Q_i &= C_g (V_G - V_T) \end{aligned} \tag{1.2}$$

This model shows that the smaller the effective mass, the higher the injection velocity. Fig. 1.3(b) shows the injection velocity of InGaAs of different composition compared with silicon obtained from experiments and simulations. The injection velocity in InGaAs is at least 2x higher than that in strained Si. Therefore, it can be concluded that InGaAs has better transport properties than Si for ballistic transport.

There have been concerns over the low effective mass of InGaAs, which results in a low density of states (DOS), known as the 'density of states bottleneck' [19]. This is because the DOS is given by:

$$\begin{aligned} 2D: &\quad DOS = \frac{m^*}{\pi \hbar^2} \\ 3D: &\quad DOS = \frac{1}{2\pi^2} \left(\frac{2m^*}{\hbar^2} \right)^{3/2} \sqrt{E - E_C} \end{aligned} \tag{1.3}$$

Smaller effective mass, such as that in InGaAs, will lead to smaller density of states. For extremely scaled device with thin gate dielectrics, the gate capacitance is dominated by the quantum capacitance, not the insulator capacitance [20], [21]. The quantum capacitance includes two components, one due to the finite DOS C_{DOS}, and the other one due to the finite distance between the charge centroid and the interface C_{cent}. Both terms are proportional to the effective mass [20], [21]. The low gate capacitance corresponds to low carrier densities at a certain gate voltage. Therefore, the performance of III-V MOSFETs needs to be studied carefully, considering both mobility and DOS together.

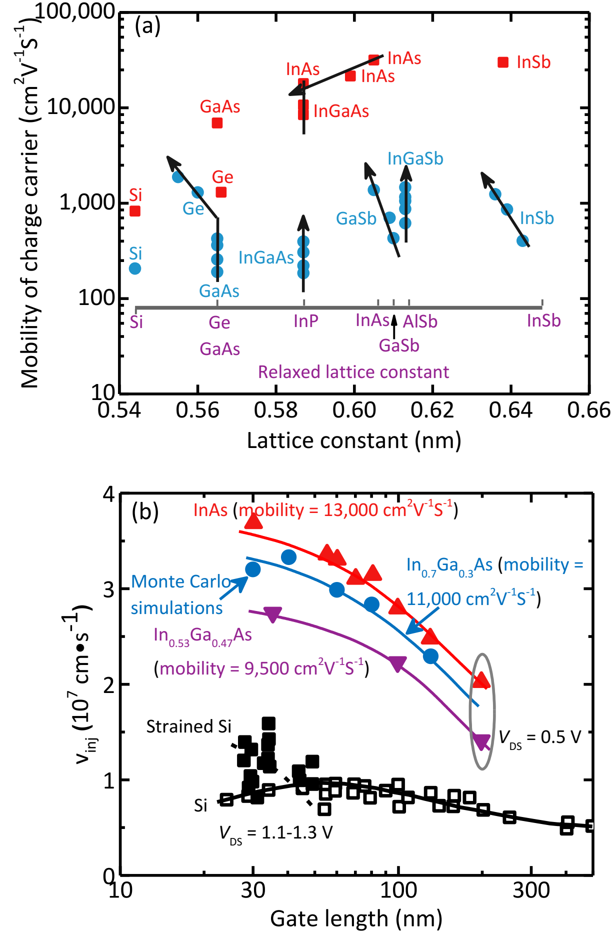

Fig. 1.3 (a) Electron and hole mobility of group III-V compound semiconductors. Electron mobility is marked red and hole mobility is in blue. The arrow indicates the increase of biaxial compressive strain. (b) Electron injection velocity in III-V materials [15].

However, studies have shown that the strong non-parabolicity of the band structure of InGaAs boosts the carrier concentration effectively compared with the simple parabolic approximation [19]. Moreover, techniques, such as use of (111) surface orientation to take advantage of large out-of-plane quantization mass and low in-plane transport mass of the L valley, have been proposed to overcome the DOS bottleneck [22], [23]. Table 1.1 shows the effective mass at different energy valleys for some typical semiconductor materials [24]. For all the III-V materials listed, the L valley is close to the Γ valley and the transverse effective mass is also very small, close to the Γ valley effective mass, suggesting superior transport properties. In addition, the longitudinal effective mass of the L valley is large. By proper design of the quantum well channel, the Γ valley and L valley will be almost at the same energy level so that both valleys participate in the carrier transport, which can boost the density of states and increase drive current. Taking all these effects

into consideration, III-V MOSFETs still outperform Si, as shown in various simulation studies [25], [26].

Table 1.1. Electron effective mass and energy separations for different valleys of different materials [24].

	Γ valley	X valley			L valley		
material	m^*/m_o	m_l/m_o	m_t/m_o	$E_X - E_\Gamma$	m_l/m_o	m_t/m_o	$E_L - E_\Gamma$
$In_{0.53}Ga_{0.47}As$	0.045	1.29	0.19	0.83 eV	1.23	0.062	0.47 eV
InAs	0.026	1.13	0.16	0.87 eV	0.65	0.05	0.57 eV
GaAs	0.067	1.30	0.22	0.47 eV	1.90	0.075	0.28 eV
Si	-	0.92	0.19	negative	-	-	-

The initial attempt to fabricate III-V MOSFETs started in 1965 [27]. It was quickly realized that a low-defect thermo-dynamically stable gate dielectric was the key to III-V MOSFETs. Unlike the nearly perfect interface between Si and SiO_2, there are no ideal native oxides for III-V materials. The oxides are not stable, generally leaky and have low dielectric breakdown strength [28]. These highly defective states will pin the Fermi-level, which prevents the formation of an inversion layer. Since then, there are decades of research on suitable dielectrics for III-V MOSFETs. But limited success has been achieved until in-situ molecular beam epitaxy (MBE) deposition of $Ga_2O_3(Gd_2O_3)$ as a gate dielectric [29] and ex-situ atomic layer deposition (ALD) of high κ dielectric on III-V materials were discovered [30]. Since the ALD process was used to deposit high κ dielectric materials on Si in commercial technology and record-high performance III-V MOSFETs were reported [31], [32], the ALD process is now most widely used.

In parallel with the surface channel III-V MOSFET development, quantum-well III-V MOSFETs, which use an InGaAs or InAs channel sandwiched between barriers, were also heavily investigated [14], [33]-[39]. Because of the good interface between the channel and barrier, the interface-related scattering is eliminated, which boosts the carrier mobility. With this structure, record high performance III-V MOSFETs were reported [40].

To control the short channel effects in the sub-10 nm node, multi-gate architecture is necessary to enhance the gate control over the channel [12], [41]. In accordance with this, multi-gate III-V MOSFETs are developed. For example, InGaAs FinFETs have been demonstrated in [42], [43], [44]. In addition, InGaAs gate-all-around nanowire transistors have also been demonstrated through both top-down and bottom-up fabrication methods [45]-[49]. To fully understand the

radiation effects in III-V MOSFETs, different device architectures are investigated, including surface channel, quantum-well channel, and FinFET.

1.2. Radiation Effects Overview

For space applications, devices or ICs have to withstand radiation exposure. The radiation comes from high energy particles, including protons, electrons, solar heavy ions, and galactic cosmic rays [50]. Radiation can have different effects on devices or ICs. In this thesis, two kinds of effects, total ionizing dose (TID) effects and single event effects (SEE), are studied.

1.2.1. Total Ionizing Dose Effects Introduction

Total ionizing dose (TID) effects refer to parametric degradation and possible functional failures in electronic devices caused by the cumulative effects of ionizing radiation [51]. Usually insulators are the most sensitive parts in MOS systems. Fig. 1.4 shows the physical processes that happen in MOS systems following ionizing radiation [51]. When radiation passes through an oxide, electron/hole pairs are created by the deposited energy. Electrons are quickly swept out of the oxide due to high mobility, while holes surviving from initial recombination remain in the oxide. The fractional yield of holes is dependent on the electric field and the generated electron/hole pair densities [51]. The remaining holes are trapped in oxide defects or transported to the oxide/semiconductor interface through hopping. Some of the holes are trapped close to the interface. Protons are liberated during hole transport and further move to the interface and create interface traps. The oxide traps and interface traps cause reliability issues.

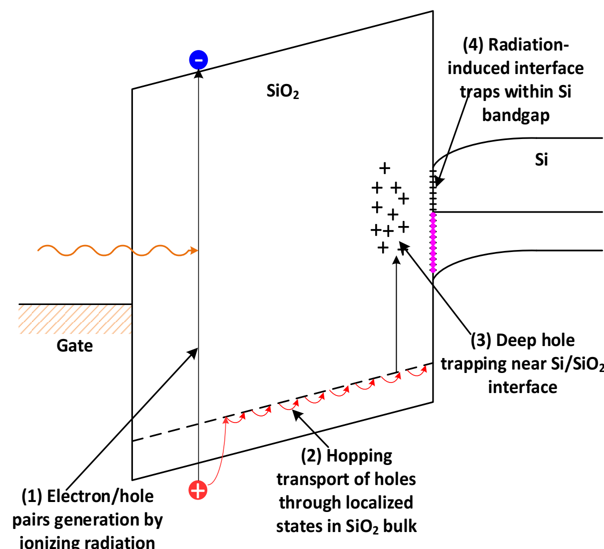

Fig. 1.4. Schematic diagram illustrating physical processes in MOS system after ionizing radiation [51].

The charges trapped in the gate oxide will cause threshold voltage shifts. The positive charge reduces threshold voltage while the negative charge increases threshold voltage. The relationship is given by:

$$\Delta V_{TH} = -\frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{x_o} x \cdot \rho_{ox}(x) dx \tag{1.4}$$

where Q_i is the interface charge, ρ_{ox} is the volumetric oxide charge density, x_o is the oxide thickness and ε_{ox} is the oxide dielectric constant.

For relatively thick oxides, the threshold-voltage shift caused by trapped holes in the oxide is described by:

$$\Delta V_{ot} \propto x_o^2 \tag{1.5}$$

This square law dependence is due to the capacitance of the gate oxide on the one hand, as illustrated in (1.4), and the number of generated electron/hole pairs [52]. This suggests that TID effects on gate oxides are becoming less significant for advanced technology nodes with the CMOS scaling. The gate oxide thickness is now approximately 1.0 nm, which is too thin to cause noticeable TID effects. Instead, the thick oxides in the device structure, for example the shallow trench isolation (STI) and the buried oxide in the silicon-on-insulator (SOI), cause reliability problems, for example leakage current increases [52].

1.2.2. Single Event Effects Introduction

SEE refers to events caused by high energy particles (protons, neutrons, electrons, heavy ions, etc.) hitting sensitive regions of a device or circuit [53]. When a particle hits a device, it may cause nondestructive effects such as single event upset (SEU) in a memory cell where the memory cell flips [54] or potentially destructive effects such as single event latchup (SEL) where parasitic pnpn junctions are triggered and form a low resistance path between the power supply and ground [55]. The physical origin of all these phenomena comes from the charge deposition by high energy particles through either direct ionization or indirect ionization, and then charge collection through carrier transport in the device [53]. Fig. 1.5 (A) shows the charge deposition by the ion and subsequent charge collection by drift and diffusion [54]. For example, for a reverse-biased pn junction, which is usually the most sensitive region in a device due to the high electric field, particle-induced electron/hole pairs in the depletion region are separated and collected efficiently by the terminal, known as drift collection.

For those carriers generated close to the depletion region, they can diffuse back to the depletion region, where they are collected by the drift process. This process is known as the diffusion process since the carriers generated outside the high-field region diffuse to the depletion region. The charge collection processes are extensively investigated through TCAD simulations [56], [57]. A representative current pulse, shown in Fig. 1.5 (B), illustrates a prompt drift and a slow diffusion component.

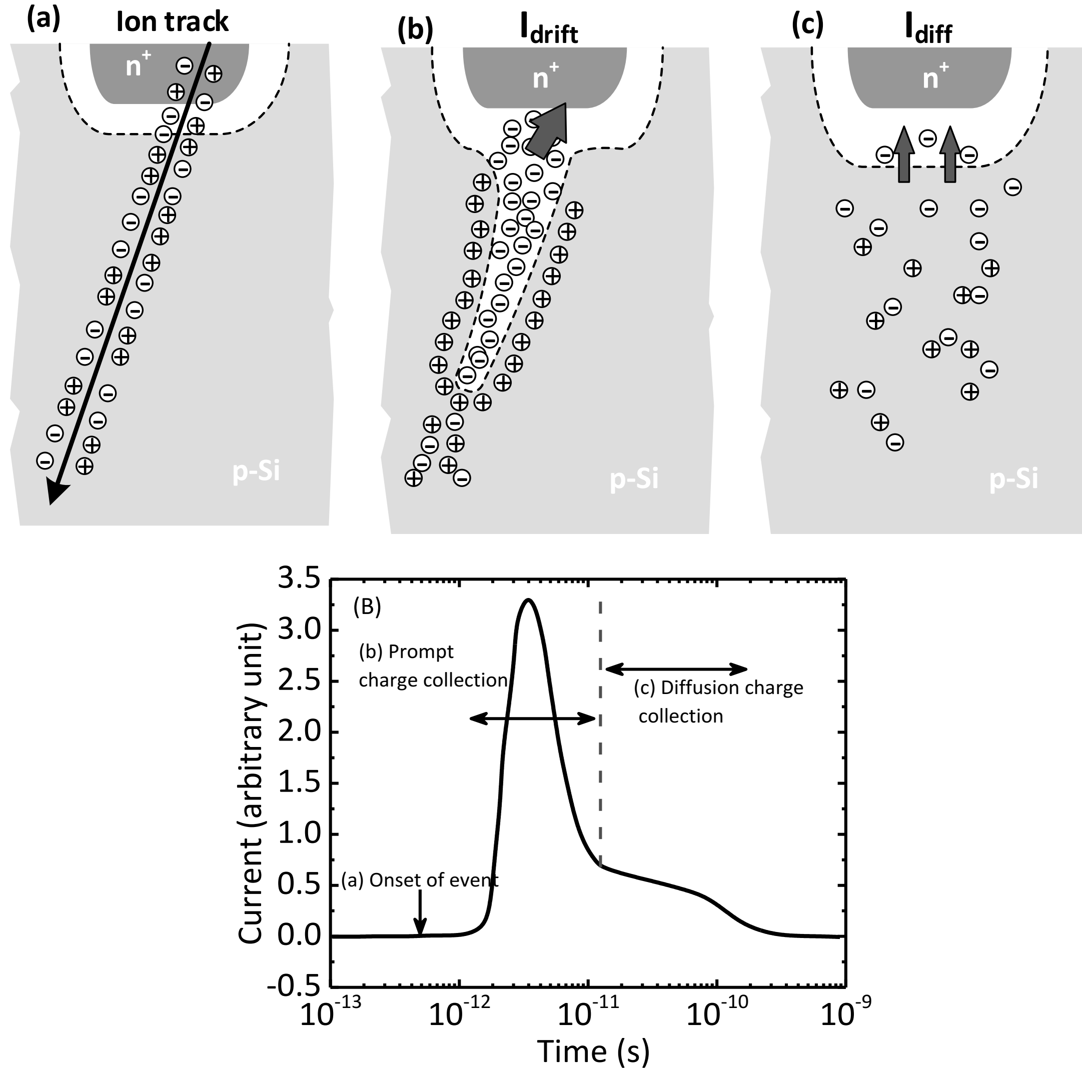

Fig. 1.5. (A) Charge generation and collection processes in a reverse biased pn junction and (B) the resultant current transient caused by the passage of a high-energy ion [54].

Different from the impact of scaling on TID effects, devices/ICs are more sensitive to SEE effects due to scaling. This is because the node capacitance and supply voltage decrease, which lead to the reduction of critical charge [59], [60]. The critical charge is defined as a threshold above

which soft errors occur when the collected charge is over the threshold. The soft error rate (SER) is approximately represented as [59], [60],

$$SER \propto A_{diff} \exp\left(-\frac{Q_{crit}}{Q_{coll}}\right) \tag{1.6}$$

where A_{diff} is the diffusion area and on average decreases 2x every technology generation as illustrated in Moore's law, Q_{crit} is the critical charge, and Q_{coll} is the collected charge. The critical charge Q_{crit} of SRAM cell for different Intel technology nodes is shown in Fig. 1.6 [59]. It shows that the Q_{crit} decreases 30% in older technology and 15% in more advanced technologies (starting from 45 nm). The decrease of Q_{crit} leads to enhanced soft error rate when it is considered independently of other factors, such as changes in the size of the transistors.

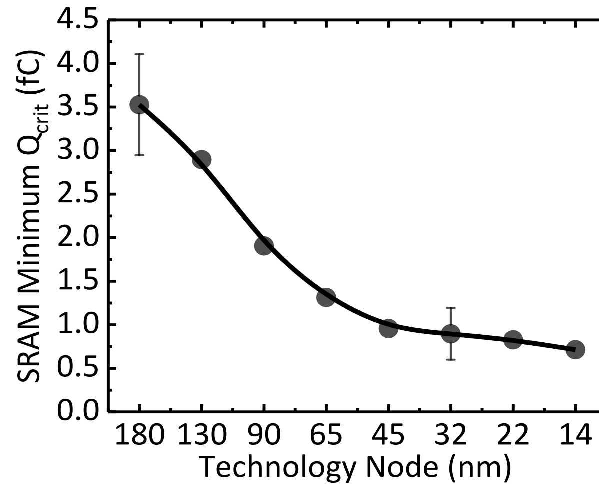

Fig. 1.6. Neutron-induced critical charges for SRAM devices at different technology nodes. Minimum critical charge refers to the minimum value of all state nodes and state transitions [59].

The overall impact of scaling on SER depends on all three factors in Eq. (1.6). For example, with the introduction of FinFET technology, the SER of a single SRAM cell decreases significantly [59]. This is because the Q_{coll} significantly decreases due to the smaller geometrical footprint of the FinFET while the Q_{crit} remains almost the same. In addition, different circuits have different dependence on scaling. For example, SRAM/latch SER decreases with scaling while the combinational logic SER exponentially increases [61]. Since III-V MOSFETs are expected to continue the scaling, it is necessary to understand the SEE effects in these devices.

To understand the device vulnerability to SEE, and further to harden the device or IC against SEE, it is very important to understand the charge collection processes, especially for new

technologies that are very different from traditional Si technology. Usually new technologies have new charge collection mechanisms. For example, CMOS scaling makes the transistor inside a well more sensitive to SEE due to the bipolar amplification mechanism caused by slow holes staying in the well, which reduces the source to substrate barrier [58]. Similar effects are also observed in silicon on insulator (SOI) technology [62]. Thus, understanding the charge collection processes in emerging III-V MOSFETs with different structures, such as surface channel, quantum-well channel, and FinFET, is important and can provide insights for their applications in radiation environments.

1.3. Radiation Effects in III-V Materials and Devices

Since the early search for suitable dielectrics on III-V materials was not successful, other types of field effect transistors that did not need an insulator were developed, such as junction gate field-effect transistors (JFETs) [63], metal-semiconductor field effect transistors (MESFETs) in 1966 [64], and high electron mobility transistor (HEMTs) in 1980 [65]. Applications of these devices included early digital IC and RF/Microwave ICs for communication [66]. Radiation effects on these devices have been investigated thoroughly from the 1970s to the 1990s because of the strong motivation of applying them in space due to their high speed and high performance [67]. Since the emergence of III-V MOSFETs, several radiation studies have also been performed [68], [69], [70], [71]. In this section, the radiation effects in III-V materials and devices are reviewed.

1.3.1. Total Ionizing Dose Effects in III-V FETs: An Overview

In early III-V FETs, including JFETs, MESFETs, and HEMTs, there is no gate dielectric in the device. This makes these devices hard against TID effects. This is because the gate oxide is usually the most critical in determining TID response since it causes charge trapping when exposed to ionizing irradiation. Therefore, for III-V FETs without gate insulators, TID effects on the threshold voltage are not a concern [72].

With the advent of III-V MOSFETs, TID effects have been studied in AlGaN/GaN MOS-HEMTs [68], InGaAs quantum-well MOSFETs [69], and InGaAs nanowire gate-all-around (GAA) MOSFETs [70]. Fig. 1.7 (a) and (b) show the threshold voltage shift as a function of irradiation dose for InGaAs quantum-well MOSFETs and GAA MOSFETs, respectively. The threshold voltage shifts about -0.35 V and shows interesting turn-around behavior for the quantum-well MOSFET, which has an equivalent oxide thickness (EOT) of 7.5 nm. However, for multi-gate

architectures, the threshold voltage shift is much smaller, less than -0.1 V, as presented in Fig. 1.7 (b). Moreover, the GAA structure shows smaller threshold voltage shift than the FinFET device. This is because the electrons are closer to the surface in FinFETs than GAA devices, which leads to higher electric field in the oxide in FinFET [70]. The large electric field means high hole yield, and hence higher hole trapping [51]. These studies show an interesting device architecture dependence of TID effects. However, all these studies focus on thick gate oxide, around 8 nm, which is impractical for advanced technology nodes. Therefore, it is necessary to study the TID response with more relevant gate oxides.

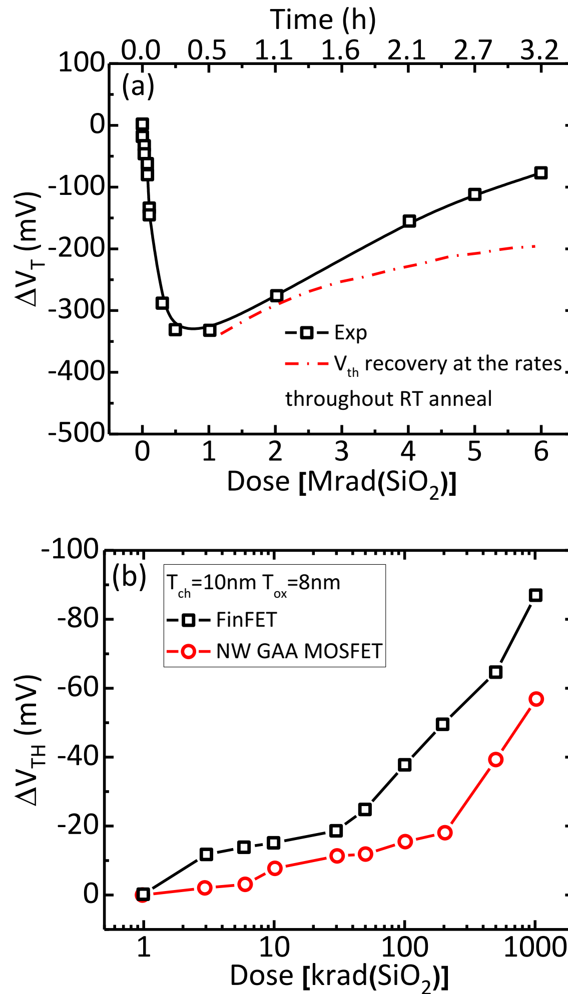

Fig. 1.7.Threshold voltage shift as a function of irradiation dose for (a) InGaAs planar quantum-well MOSFETs [69] and (b) InGaAs FinFET and nanowire GAA MOSFETs [70].

1.3.2. Single Event Effects in III-V FETs: An Overview

Since the early III-V FETs are found to be hard against TID effects, most of the research efforts have been directed toward understanding SEE in III-V FETs [67], [72]-[75]. It is found that III-V FETs are more sensitive to SEE compared with Si FETs, due to material property and device architecture differences. For example, Fig. 1.8 shows a typical cross section vs. LET for a GaAs MESFET-based direct coupled FET logic (DCFL) latch [76]. The threshold LET is low, less than 1 MeV•cm^2/mg and the saturation cross section is much higher than the sensitive area of the latch, suggesting enhancement effects in these devices and circuits. These two factors imply that III-V FETs may be relatively sensitive to SEE. In this section, the SEE in III-V FETs are briefly overviewed and the sensitivity is explained through the charge deposition, non-insulating gate, charge enhancement mechanisms, and semi-insulating substrate, which could provide insights into the SEE in III-V MOSFETs.

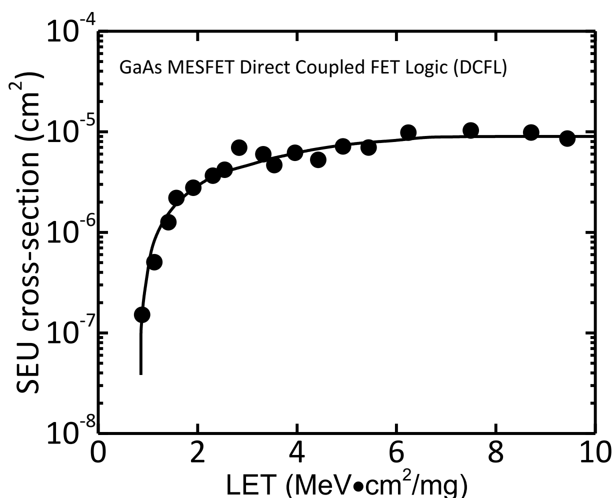

Fig. 1.8. SEU cross section vs. LET for GaAs MESFET based DCFL latch circuit [76].

1.3.2.1. Charge Deposition in III-V Materials

To understand the SEE vulnerability of III-V FETs, it is important to understand the charge deposition in III-V materials. The ionizing energy loss by an ion to the target material is characterized by linear energy transfer (*LET*), which is a measure of energy transfer per unit length of the material. It is defined as energy loss per unit length divided by the material density

$$LET = \frac{dE}{dx}\frac{1}{\rho} \tag{1.7}$$

To calculate the number of electron-hole pairs generated by an ion, another important parameter is the creation energy ε_I [77], which is the energy required to create an electron-hole pair. Then the number of electron-hole pairs generated per unit length is

$$LET\left(\frac{ehp}{\mu m}\right) = LET\left(\frac{MeV \bullet cm^2}{mg}\right) \div \varepsilon_I\left(\frac{eV}{ehp}\right) \times \rho\left(\frac{g}{cm^3}\right) \tag{1.8}$$

where the unit of each parameter is shown in the parentheses. So for a given material, there is a conversion factor from *LET* in units of $MeV \bullet cm^2/mg$ to *LET* in units of $ehp/\mu m$. Table 1.2 lists the conversion factor, ε_I, and ρ. Also listed in column four is the ionized charge per unit length for an ion having *LET* of 1 $MeV \bullet cm^2/mg$.

From the results, it could be concluded that the higher the creation energy and the smaller the mass density, the smaller the generated electron-hole pair density. Even though GaAs has higher creation energy than Si, the higher density of GaAs causes 70% more carriers generated compared with Si for the same LET. The situation is even worse for $In_{0.53}Ga_{0.47}As$, which has lower creation energy and higher density than GaAs. The charge generated in $In_{0.53}Ga_{0.47}As$ is 3x that in Si. So for III-V FETs, such as GaAs MESFETs or InGaAs MOSFETs, more charge will be generated by an ion compared with Si FETs if the ion penetrates the same thickness of Si and III-V materials and has the same LET in the materials.

Table 1.2. Ionized charge per unit length for an ion having a LET of 1MeV•cm²/mg [75]

Target Semiconductor	ε_I **(eV)**	**Density (g/cm^3)**	**$fC/\mu m$ for an LET=1 $MeV \bullet cm^2/mg$**	**Divide *LET* by X for $pC/\mu m$ deposited**
Si	3.6	2.32	10.4	97
GaAs	4.8	5.32	17.8	56
InP	4.5	4.81	17.1	58
InAs	1.8	5.68	50.5	20
$In_{0.53}Ga_{0.47}As$	2.9	5.49	30.3	33
$In_{0.52}Al_{0.48}As$	4.6	4.74	16.5	61
SiC	8.7	3.21	5.9	169
GaN	10.3	6.11	9.5	105

1.3.2.2.Non-insulating Gates

For III-V FETs that have wide application, most of them have non-insulating gates, such as the pn depletion region used in JFETs, the Schottky barrier used in MESFETs, and the barrier layer in high electron mobility transistors (HEMTs) to isolate the gate from the channel. These devices are robust against TID-induced degradation, however, the high field in the depletion region under the gate or low barrier layer will cause radiation-generated carriers to be collected in the gate, causing gate transients [78]. The gate transient-induced upset is a new upset mechanism, different from the traditional drain transient-induced upset. Fig. 1.9 shows the current path for gate to drain current transients [79]. This can discharge the stored charge on the left side and cause the upset of the SRAM cell.

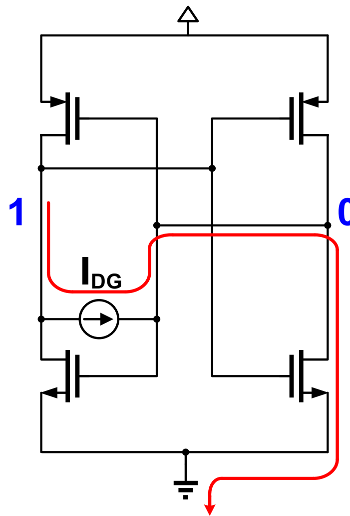

Fig. 1.9. Current path for gate to drain charge collection in a SRAM cell [79].

Different from SEUs in CMOS technology, gate transient-induced SEU is a new upset mechanism and has a lower critical charge compared with the traditional upset mechanism [80]. Besides, it is found that the gate transient biases the device and causes additional drain current [73], [81]. Furthermore, it is observed that traditional hardening techniques, such as decoupling feedback resistors, used in CMOS technology will store the collected charges in the gate node, making the circuit more susceptible to single events [67], [80]. Therefore, the non-insulating gate represents a tradeoff between TID and SEE effects.

1.3.2.3. Charge Enhancement

Another reason why III-V FETs are vulnerable to SEE is charge enhancement, which means that the charge collected at a node, usually the drain node, is higher than that deposited by an ion

[82], [83]. Charge enhancement has been observed in all different kinds of III-V FETs when exposed to ions, lasers, and e-beams, such as GaAs MESFETs [82], [83], AlGaAs/GaAs HEMTs [84], InAs HEMTs [86], InGaAs HEMTs [86], etc. The main mechanisms are illustrated in Fig. 1.10 for GaAs MESFETs [73]. The enhancement mechanisms are very similar in other types of III-V FETs.

During an ion strike, a high density of electron hole pairs is generated along the ion track. Due to highly asymmetric carrier motilities in III-V materials (electron mobility is at least 10x hole mobility), electrons are quickly collected, while the holes remain in the device, perturbing the local potential. Fig. 1.10(a) shows the parasitic bipolar mechanism. The holes in the substrate near the source reduce the potential barrier from source to substrate, causing electron injection from source to substrate, which are further collected by the drain. Fig. 1.10(b) shows the channel modulation, or backgating mechanism. The holes in the substrate act like a floating back gate and modulate the channel conductivity, causing current flow between source and drain.

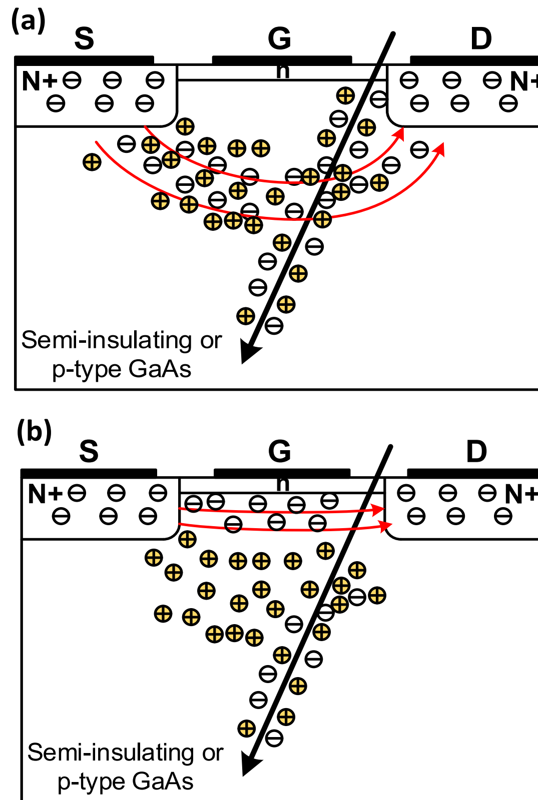

Fig. 1.10 Schematic diagram illustrating (a) the bipolar gain and (b) channel-modulation charge enhancement mechanisms that contribute to the charge collection processes of GaAs FETs [73].

The charge enhancement mechanisms contribute most of the charge collected and are the main

reason why III-V FETs are relatively vulnerable to SEE. Charge enhancement factors are typically less than 5 [83]-[89], but factors up to 60 also have been reported [74]. Therefore, the collected excess charge makes III-V FET SEU performance a serious concern for applications in radiation environments.

1.3.2.4. Semi-insulating Substrate

High resistivity semi-insulating substrates are widely used in III-V FET technology because they are ideal for isolation between transistors and also eliminate additional isolation structures. These substrates are usually made through a compensation mechanism, where the high density deep donor native defect, EL2, related to the As antisite, compensates shallow acceptors [90]. The depletion region in the semi-insulating substrate will be much larger than that in a p-type substrate. Therefore, the sensitive volume of III-V FETs on a semi-insulating substrate is very large. One related effect is the gate-edge effect [91]. At the gate edge, the gate is directly in contact with the semi-insulating substrate, creating a large depletion region underneath the gate, as shown in Fig. 1.11. The charge collection efficiency has a peak around the gate edge, about 3X of the active region of the device.

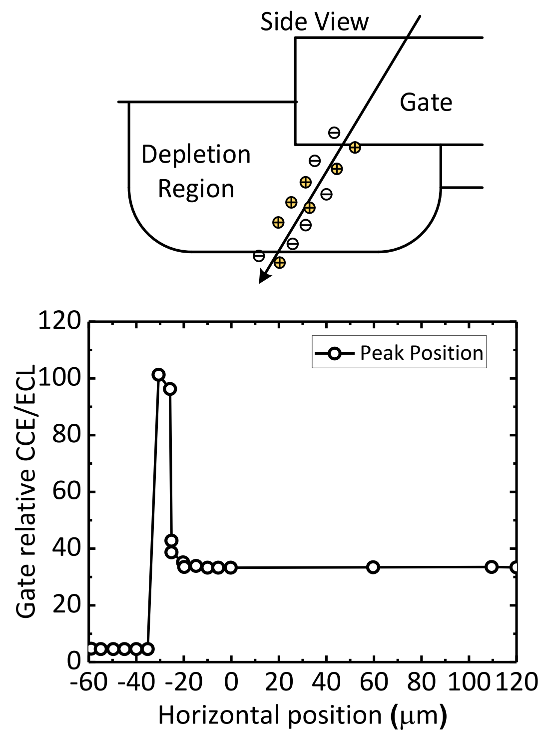

Fig. 1.11. Schematic of an ion hitting the gate edge of a GaAs MESFET device and the charge collection efficiency/effective collection length along the transistor width direction [91]. The efficiency is normalized to the maximum efficiency.

The other phenomenon related to semi-insulating substrates are the long-term transients after irradiation [92]-[96]. Recovery time on the order of 1s is observed in all kinds of devices after irradiation. It is ascribed to charge trapping in deep traps in the substrate and its subsequent thermal release. Negatively-charged traps deplete the channel and decrease the channel current, while positively-charged traps increase the channel current. Further studies show that a buried p-layer under the active region could effectively shield the channel from the charges in the substrate, and reduce the long-term transients significantly [95].

1.3.2.5. Transistor Hardening Techniques

Several transistor-level hardening techniques have been proposed against SEE and they have achieved various degrees of success. The idea behind hardening is to reduce the gain enhancement mechanisms. For example, a buried p layer under the active region, as shown in Fig. 1.12 (a), increases the source to substrate barrier and could reduce the charge collection [97]. It does not eliminate the charge enhancement completely, however.

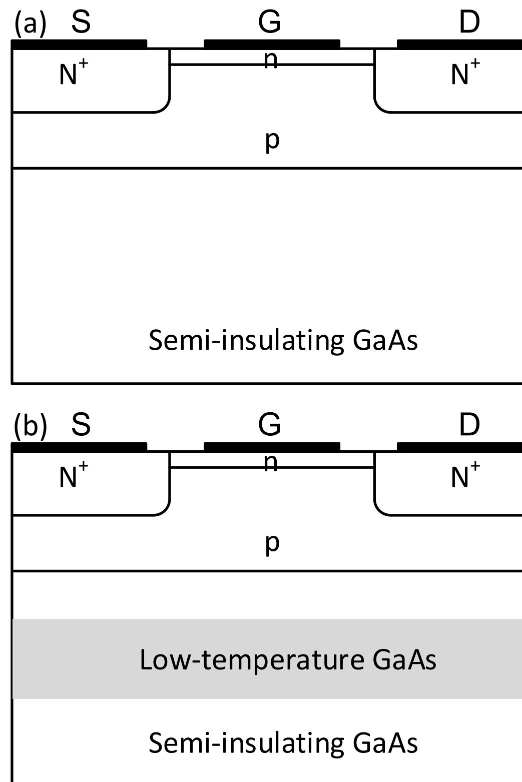

Fig. 1.12.Proposed hardening techniques. (a) Buried p layer under the active region and (b) low-temperature GaAs buffer layer.

Another effective hardening method is to reduce the hole lifetime in the substrate so that

generated holes quickly recombine before they can induce source to drain current flow [98]-[100]. A low temperature (LT) GaAs buffer layer inserted between the substrate and the active layer, as shown in Fig. 1.12 (b), could effectively reduce carrier lifetime, even down to 150 fs [73]. The LT GaAs buffer layer is grown at around 200 °C to 350 °C in an As-rich environment via molecular beam epitaxy (MBE). It contains high densities of As antisites and Ga vacancies, which increase the electron/hole trapping and recombination significantly. The generated holes are quickly recombined, so the charge enhancement is largely eliminated. Fig. 1.13 (a) and (b) show the comparison between HFETs with and without an LT buffer layer in terms of charge collection transients and collected charge, respectively, when exposed to α particles [100]. It is clear that the LT buffer layer effectively reduces the transients and collected charge.

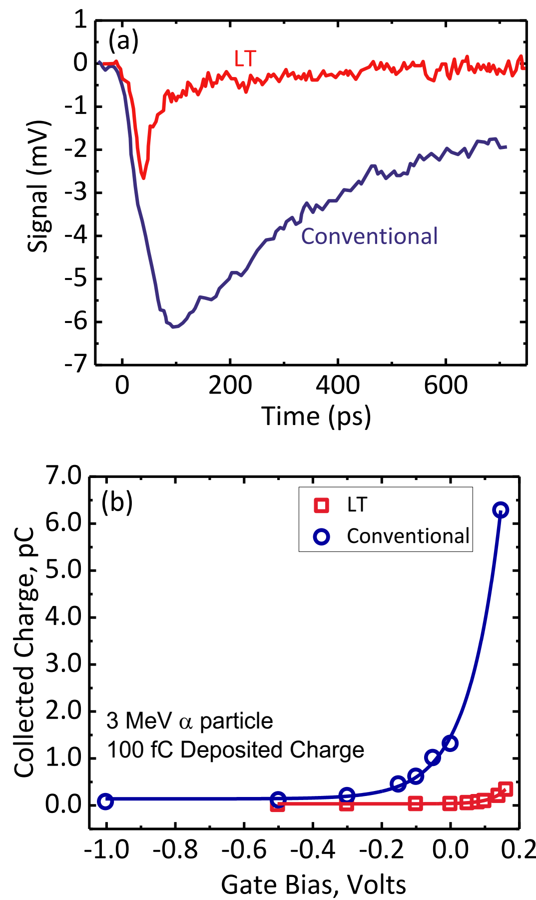

Fig. 1.13 (a) Charge collection transients and (b) collected charge measured for n-channel HFET devices with and without LT GaAs buffer layer exposed to 3 MeV α particle irradiation [100].

The aforementioned factors which lead to sensitivity of III-V FETs to SEE may or may not apply for III-V MOSFETs, depending on the device materials and architectures. The charge

deposition and charge enhancement are likely to be effective in III-V MOSFETs, since the III-V materials are present in the device. However, the effects related to non-insulating gates will disappear due to the gate insulator in III-V MOSFETs. The issues with semi-insulating substrates are complicated. For the early demonstration of III-V MOSFETs, semi-insulating GaAs or InP substrates are used. The aforementioned issues will likely be present in these substrates. However, III-V MOSFETs will eventually be integrated on Si substrates [15], [101], [102], [103]. Whether substrate-related issues exist needs further investigation. In this dissertation, these effects are discussed in III-V MOSFETs.

1.4. Overview of Dissertation

This Ph.D. dissertation focuses on the characterization and understanding of radiation effects in emerging III-V MOSFETs with different architectures, such as surface channel, quantum-well channel, and FinFET. This dissertation is organized as follows:

1. Chapter 1 introduces the background and motivation of this work. The history and advantages of III-V nMOSFETs are discussed. Moreover, the radiation effects in III-V FETs are overviewed.
2. Chapter 2 describes the transient characterization and charge collection mechanisms in GaAs surface channel MOSFETs. Similar experiments are performed as those in Chapter 2. Comparisons of charge collection mechanisms are made between surface channel and quantum-well channel devices.
3. Chapter 3 describes the single event transients in InGaAs quantum-well MOSFETs induced by heavy ion and two-photon-absorption (TPA) laser irradiation. Technology computer aided design (TCAD) simulations are applied to understand the charge collection mechanisms.
4. Chapter 4 studies the charge collection mechanisms in InGaAs FinFET devices through tunable wavelength laser irradiation and TCAD simulation. The new laser setup allows charge injection into channel layer and new insights can be obtained.
5. Chapter 5 investigates the gate bias and geometry dependence of TID effect in InGaAs quantum-well MOSFETs. Combined electrical stress and X-ray experiments are designed to understand the TID effects in these devices.
6. The last chapter is the conclusion of the dissertation and future work is described that is interesting and worth further investigation.

7. The appendix includes the tunable wavelength laser setup and several TCAD scripts that I developed during my Ph.D.

Chapter 2. Charge Collection Mechanisms in GaAs MOSFETs

2.1. Introduction

Charge collection mechanisms are investigated in surface channel GaAs MOSFETs under broadbeam heavy ion irradiation and pulsed two-photon-absorption laser irradiation. The large barrier between the gate dielectric and GaAs eliminates gate conduction current, but there is significant gate displacement current. Charge enhancement occurs because radiation-generated holes accumulate in the substrate, which increases the local electrostatic potential. The increased potential enhances the source-to-drain current, resulting in excess collected charge. The collected charge increases significantly with gate bias, due to the long tails of the charge waveforms that occur for higher gate bias. The collected charge increases with increasing drain bias.

2.2. Device Description

The devices under test are surface channel GaAs nMOSFETs with gate lengths of 2 and 4 μm; the schematic cross-section is shown in Fig. 2.1(a). Also shown is the TEM picture around the gate stack. The gate dielectric is composed of 4 nm of single crystalline La_2O_3 grown on top of a 350 μm thick semi-insulating (SI) GaAs substrate by atomic layer epitaxy (ALE), with 4 nm of Al_2O_3 on top of the La_2O_3 for protection. The distance between electrodes varies with the gate length and is given for devices with L_G = 4 μm in Fig. 1(a). The detailed process information is found in [116]. The band diagrams along a vertical cutline through the gate oxide at zero bias applied to all terminals are shown in Fig. 2.1(b). The electron and hole quasi-Fermi levels are the same in this case because zero bias is applied to all terminals. The conduction band and valence band offsets between La_2O_3 and GaAs are 2.4 eV and 2.1 eV, respectively [117].

The I_D-V_G transfer characteristic is shown in Fig. 2.2. The experimental data and simulation data agree well. To simulate the semi-insulating GaAs substrate, carbon acceptor doping and deep donor traps are included [118]. Devices with gate lengths of 2 μm and 4 μm and gate widths of 20 μm and 33 μm were tested (W/L = 20/4, 20/2, and 33/4). For both heavy ion experiments and laser experiments, at least three devices were tested. For transient capture, all the devices are mounted in custom milled high-speed packages [107]. For the laser experiments, the backsides of the DUTs were polished before mounting in high-speed packages.

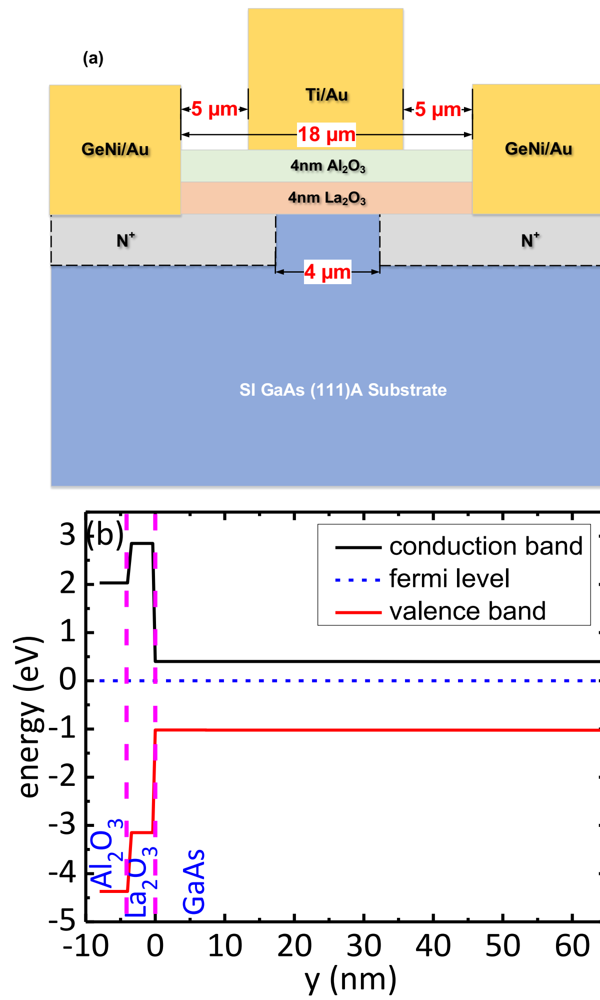

Fig. 2.1. (a) Schematic cross section of the device with $L_G = 4\ \mu$m; (b) band diagram along a vertical cutline through the gate oxide at V_G=V_D=V_S=0 V. The band diagram is generated from Sentaurus TCAD simulation.

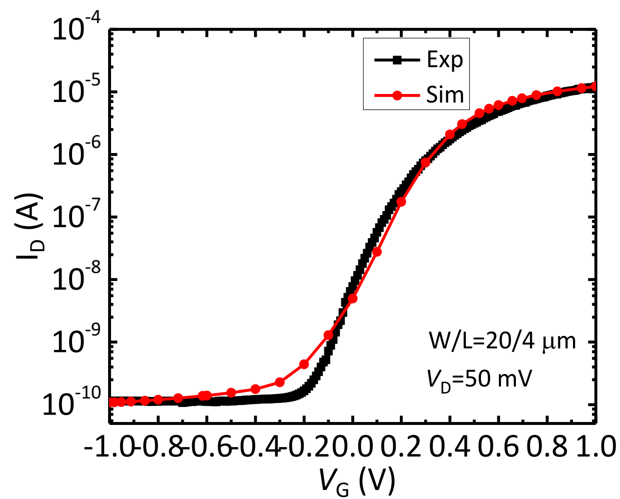

Fig. 2.2. Measured and simulated I_D-V_G transfer characteristics. V_D = 50 mV during measurement. Simulation is done with Sentaurus TCAD tools.

2D TCAD simulations, performed with Sentaurus TCAD tools, were used to understand the charge collection process during heavy ion strikes. The models used include drift and diffusion transport, inversion and accumulation layer mobility models, and electron velocity saturation models [119]. In addition, the SRH, radiative and Auger recombination models are used. Events produced by oxygen ions are simulated. The center of the strike is at 1.0 ns, and the strike center is at x = -6 μm, as shown in Fig. 2.3. The radius of the strike is 50 nm. During the simulation, V_D = 2.0 V and V_G was varied to study the gate bias dependence.

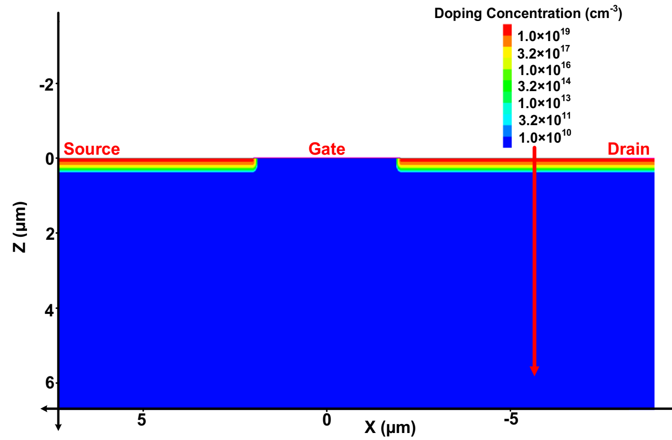

Fig. 2.3. Device model used in 2D TCAD simulation. Here the drain is in the negative x direction and source is in the positive x direction. The red arrow indicates the strike location, x = -6 μm. For the simulation, Sentaurus TCAD tools are used.

2.3. Experimental and Simulation Details

Broadbeam heavy ion irradiation was performed using 14.3 *MeV* oxygen ions in Vanderbilt's Pelletron electrostatic accelerator. *LET* of Oxygen ion in GaAs is 4.3 $MeV{\bullet}cm^2/mg$. The range is 7.5 μm. The experimental setup is the same as that shown in Fig. 3.3. TPA laser irradiation was performed at Vanderbilt University. All devices were irradiated from the backside by high peak power femtosecond laser pulses. A similar experimental setup is used as described in section 3.3. The laser photon energy is 0.98 eV, which is less than the GaAs band gap of 1.42 eV. As a result, the carriers are generated primarily through two-photon absorption [109].

Quantitative understanding of TPA laser experiments is challenging and remains an active area of research [120]. In this chapter, TPA laser experiments are used to map the sensitive areas of the devices by scanning the laser beam across the active areas with varying gate and drain biases. The transients were captured using a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20 GS/s sampling rate. Each oscilloscope channel has 50 Ω input impedance, which

is used to convert the transient current to a measurable voltage. During these tests, the source was grounded and the gate bias and the drain bias were varied. A semiconductor parameter analyzer, HP 4156B, supplied the dc biases through Picosecond Model 5542 bias tees with 50 GHz bandwidth.

2.4. Results and Discussion

2.4.1. Broadbeam Heavy Ion Results

Fig. 2.4 (a) and (b) show the transients for a device with $L_G = 4$ µm for OFF and ON gate biases under oxygen ion irradiation. For all transients, the DC current is filtered out and only AC current transients are shown. Under both bias conditions, there are strong gate transients. Positive and negative gate transients correspond to charging and discharging of the gate capacitance, respectively.

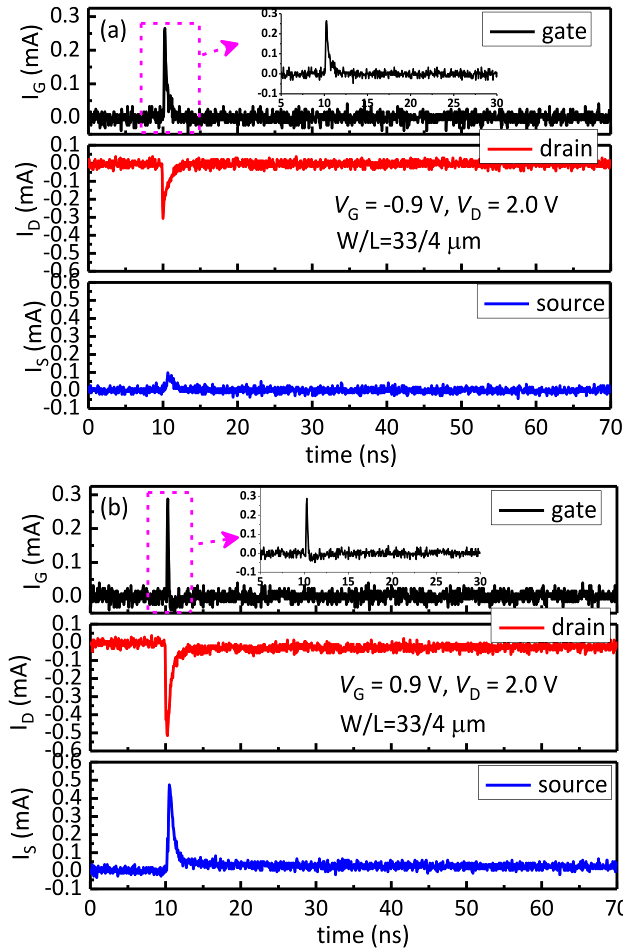

Fig. 2.4. Representative transients under oxygen ion irradiation at (a) OFF, $V_G = -0.9$ V; (b) ON bias conditions; $V_G = 0.9$ V for a device with $L_G = 4$ µm. For this device, $V_{TH} = 0.4$ V. The inset of the figure shows the zoom into the magenta box region.

After an initial positive transient, the gate current polarity changes for devices biased in the ON state (see inset in the top panel of Fig. 2.4 (b)), which is a strong indication of displacement current through the gate dielectric [121], [122]. This polarity change is not observed for devices in the OFF state (see inset of Fig. 2.4 (a)). If there is any negative gate current in the OFF state, it is obscured by the oscilloscope noise.

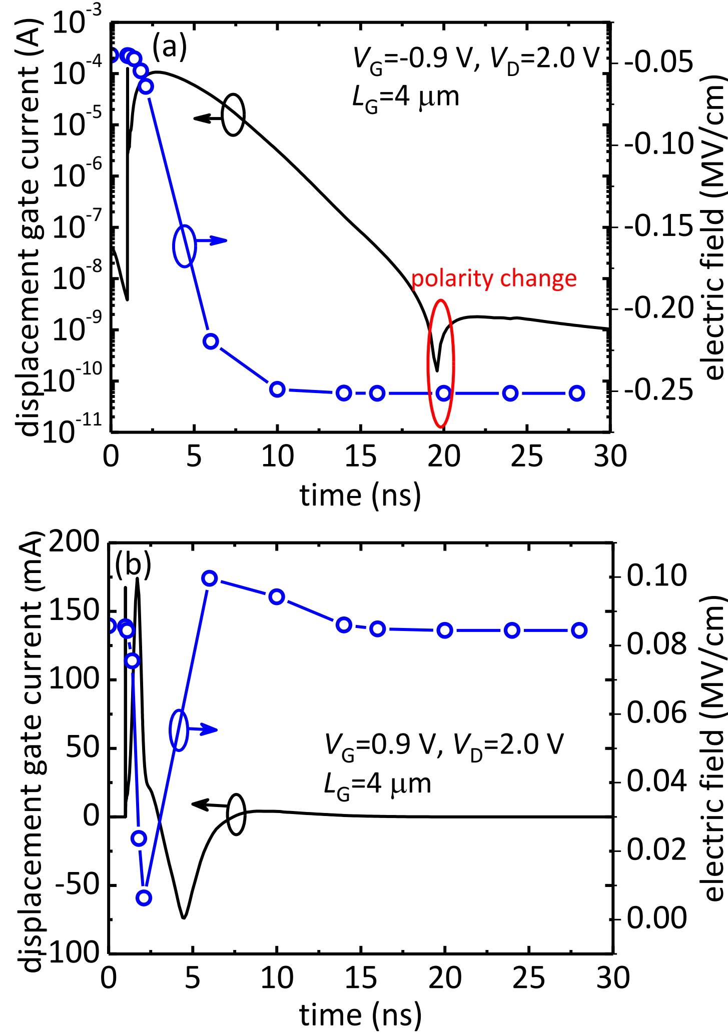

Fig. 2.5. Displacement gate current and electric field in La_2O_3 as a function of time at (a) V_G = -0.9 V; (b) V_G = 0.9 V.

Fig. 2.5 (a) and (b) show the simulated gate displacement current and electric field in the La_2O_3 as functions of time at V_G = -0.9 V and V_G = 0.9 V, respectively. The gate transient at V_G = -0.9 V is displayed on a log scale to show the polarity change more clearly. When the device is biased in the OFF state, there is a large initial positive gate transient, followed by a polarity change. The electric field in the gate dielectric increases up to 20 ns, and after that it slowly decreases. The moment the electric field reaches a peak is when the gate transient changes polarity. The negative

gate current is orders of magnitude smaller than the positive peak gate current, which explains why only positive gate transients are observed in Fig. 2.5 (a). The negative portion of the gate transient is small and likely obscured by the instrument noise.

Also, as shown in Fig. 2.5 (b), when the device is ON, there is a clear polarity change in the gate transient, consistent with the heavy ion data in Fig. 2.4. The polarity change happens quickly, at approximately 3 ns. The electric field in the gate dielectric decreases up to 3 ns, and then increases to the steady state value. Although there are large barriers between the gate oxide and semiconductor, there are displacement current in the gate, which is different from InGaAs quantum-well MOSFETs in chapter Chapter 3 and other III-V FETs introduced in section 1.3.2. The reason is likely related to the large dimensions of the tested devices, which leads to large gate capacitance and hence large displacement current. However, with the technology scaling, this phenomenon will likely disappear, like that shown in InGaAs quantum-well MOSFETs.

The source transients differ significantly between the ON and OFF states. During the OFF state, source transients are small, with peak current less than 0.1 mA, which is smaller than the gate transients. When the devices are irradiated in the ON state, the drain and the source transients are approximately equal. This is because the channel resistance is much higher in the OFF state and the source and drain are electrically isolated, which suppresses the source to drain current [123]. However, when the device is biased in the ON state, the source and drain are electrically connected, resulting in large source to drain current. This can be further confirmed with the heavy ion test results with shorter gate length, $L_G = 2$ µm, as shown in Fig. 2.6 (a). Even at strongly OFF gate bias, the source and drain current transients are approximately equal and have opposite polarity. This is because the channel resistance is smaller for shorter gate length device. This also suggests that with technology scaling to smaller gate length, the channel contribution will become stronger.

It is also interesting to compare the GaAs surface-channel MOSFET with the Si counterparts. Fig. 2.6 (b) shows the current transients for a Si device with dimension of W/L=20/0.25 μm, irradiated by 35 MeV Chlorine ion [124]. It has a LET of approximately 16 MeV●cm^2/mg. Even though the Si device has a much smaller gate length and is exposed to ions with higher LET, the current transients is less than half that of GaAs MOSFET. Moreover, the source current is smaller than the drain current for Si device. This is because that the parasitic bipolar amplification is much smaller in Si device, so that the drain junction collection dominates the transient response. Amplification factor of around 2 is found for this device [124]. Therefore, it can be concluded that

the GaAs surface-channel MOSFET is much more sensitive to the ionizing radiation compared with the Si counterparts.

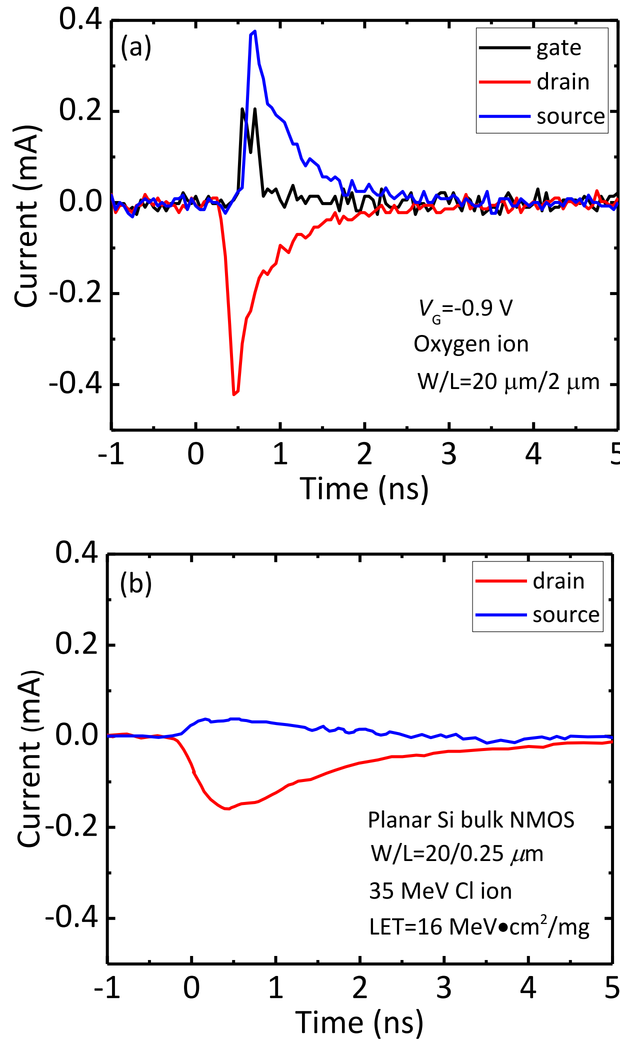

Fig. 2.6. Current transients for (a) GaAs surface channel MOSFET with W/L=20/2 μm due to oxygen ion irradiation and (b) planar Si bulk NMOS with W/L=20/0.25 μm due to Cl ion irradiation [124].

The simulated transients are shown in Fig. 2.7 biased at $V_G = 0.9$ V. The gate transient, showing the polarity change, is displacement current as discussed in Fig. 2.5(b). The source and drain transients are approximately equal and opposite, meaning the current comes from the electrons traveling from source to drain. The simulated transients also illustrate charge enhancement, since the charge deposition is 0.58 pC while the drain collected charge is about 8.5 pC. These simulations are not quantitative, however, primarily because they are conducted with 2D rectangular coordinates. In addition, the parasitic capacitance and inductance of the device and the

experimental setup are not included. While the simulation results are qualitative, they do illustrate the key characteristics.

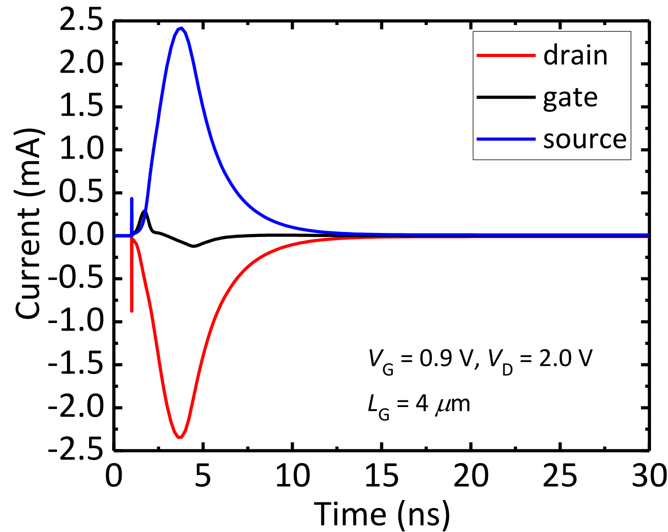

Fig. 2.7. Simulated current transients at $V_G = 0.9$ V, $V_D = 2.0$ V when striking at x = - 6 μm. The current is scaled by the width of 33 μm.

The OFF state bias allows radiation-generated holes to stay under the gate dielectric because the electric field attracts the holes. In the ON state, however, holes are repelled from the gate. Consequently, the ON state has a stronger restoring force, restoring the pre-strike steady state quickly, and leading to larger displacement current. For the OFF state, in contrast, it takes a longer time to remove radiation-generated holes to recover the pre-strike steady state, so the displacement current lasts for a longer time. The high resistivity and deep traps in the semi-insulating GaAs inhibit hole transport to the substrate contact. Such long-lasting displacement current is typically not observed in Si nMOSFETs because the substrate is quite conductive.

For irradiation in the ON state, source and drain transients have long tails that may last microseconds. This behavior is repeatable both in heavy ion and laser irradiation. The collected charge is obtained by integrating the recorded transient. For transients without long tails, the integration time window used is the region where the transient is larger than 1% of the peak current value, which reduces the noise contribution. For transients with long tails, the end of the integration time is selected to be 200 ns, which is the sampling window during the experiment. The collected charge is shown as a function of gate bias in Fig. 2.8. Again when the device is ON, there is a long tail in the transient, which contributes a large amount of collected charge. As a result, the collected charge increases with the gate bias. As the oxygen ion generates about 0.58 pC of charge,

approximately 3 pC of collected charge corresponds to a charge enhancement factor of 5. This is consistent with the results reported in other types of GaAs FETs [73], [84].

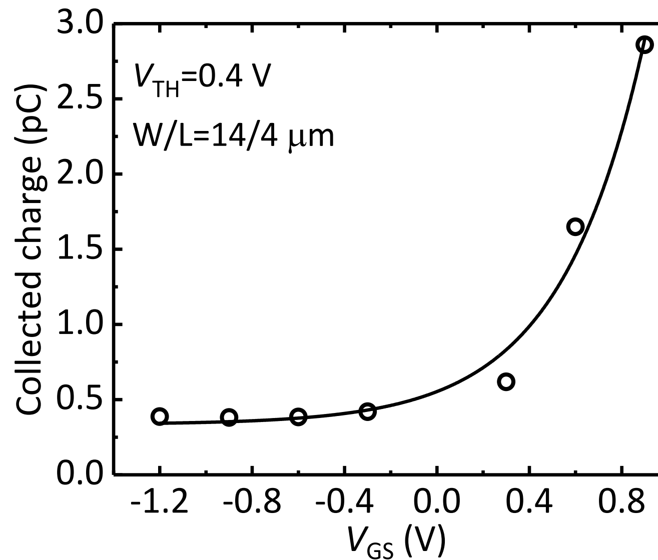

Fig. 2.8. Drain collected charge as a function of gate bias under oxygen ion irradiation. V_D = 2 V during irradiation.

Both positive and negative long-tail transients (compared with the DC terminal current) have been observed in irradiated GaAs FETs [92]-[96], [125]-[127]. Deep traps in the substrate close to the channel are responsible for the long transients. Negatively-charged traps deplete the channel and decrease the channel current, while positively-charged traps increase the channel current. This process lasts until the trapped electrons/holes are emitted from the deep traps, which may require microseconds or even seconds. For the GaAs MOSFETs examined here, the effects appear to be due to holes trapped in deep traps in the substrate, which backgate the channel and induce long term transients, similar to the results described in [125]-[127].

The properties of the traps depend on the device structure, material, and process. Electron traps with activation energy in the range of 0.7 to 0.9 eV have been reported in previous work, which are related to Cr impurities or EL2 traps in the GaAs substrate [92], [93], [95], [96]. Similar energy levels are reported for hole traps. Shallower traps with activation energies of 0.57 eV, 0.37 eV and 0.14 eV also have been reported in GaAs MESFETs/MODFETs [95], [96]. The specific type of trap responsible for the long tail in the GaAs MOSFETs evaluated here remains to be determined, but the traps likely are also deep levels in the substrate. Hardening techniques to reduce the long-term transients, such as including a buried p-layer under the active region and AlGaAs buffer [95], [96], may therefore also be applicable to these GaAs MOSFETs.

To understand the charge enhancement process, Fig. 2.9 (a) shows the simulated electrostatic potential (colors) and hole density difference between post-strike (4.0 ns) and pre-strike conditions (contour lines). Holes accumulate in the substrate and the channel, due to their long lifetime in the substrate [98], [99], which leads to an increase in the local electrostatic potential. This potential increase backgates the channel and also produces bipolar amplification, which leads to source to drain current [82], [83]. Fig. 2.9 (b) shows the conduction band along a horizontal cutline in the channel located 50 nm below the gate dielectric. The conduction band energy drops about 0.37 eV at 4.0 ns, which is the peak of the transient, due to an increase in the electrostatic potential. Although the source to channel barrier remains high, about 0.7 eV, the source to drain current flows outside the depletion region, where the gate has little control, as shown later.

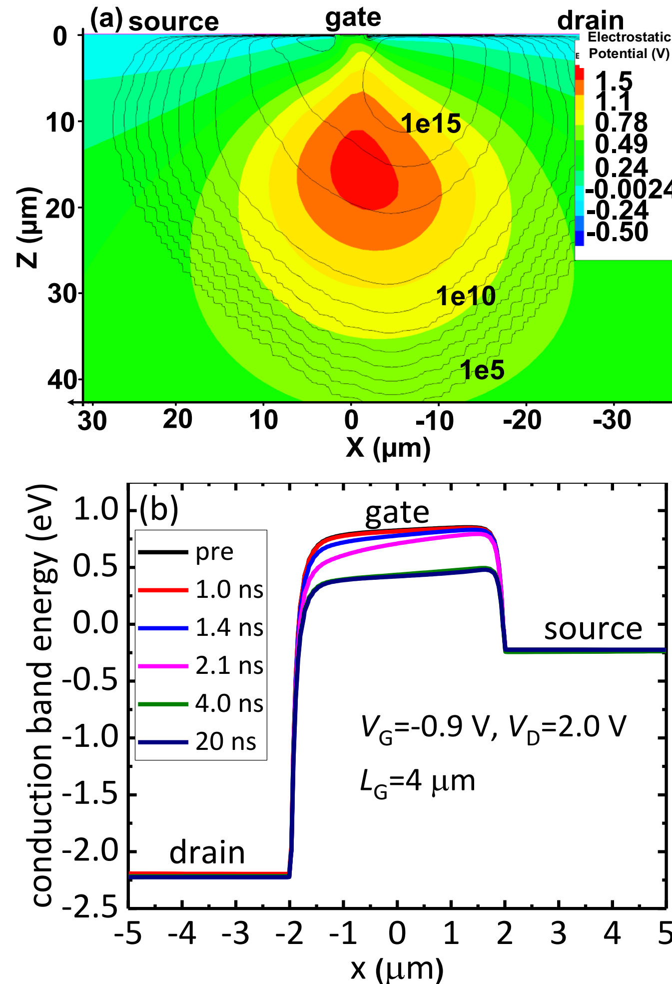

Fig. 2.9. (a) The color map shows the electrostatic potential difference and the contour plot shows the hole density difference between post-strike (4.0 ns) and pre-strike at V_G = -0.9 V. (b) The conduction band energy is plotted along a horizontal cutline at z = 50 nm at different times.

Devices were also tested at LBNL for different heavy ions. The ion details, LET and range in GaAs, are given in Table 2.1.

Table 2.1. Details of heavy ions used to test GaAs surface channel MOSFETs.

Ions	**Energy (MeV)**	**LET (GaAs) (MeV•cm^2/mg)**	**Range (GaAs)(μm)**
Oxygen	14.30	4.3	7.5
Neon	89.95	3.9	35.6
Krypton	387.08	26.6	32.8
Xeon	602.90	47.0	33.0

The cross section as a function of LET is shown in Fig. 2.10. Here two different kinds of cross sections are shown. The first is the event cross section, which is the total number of recorded events divided by total fluence. An event is triggered and recorded in the oscilloscope when the current is higher than 0.12 mA. However not all the recorded events would cause an upset in real applications. To illustrate the effects that may occur in a particular application, a cross section based on the number of recorded events with a peak drain current over 2 mA is also plotted (called the over-threshold cross section).

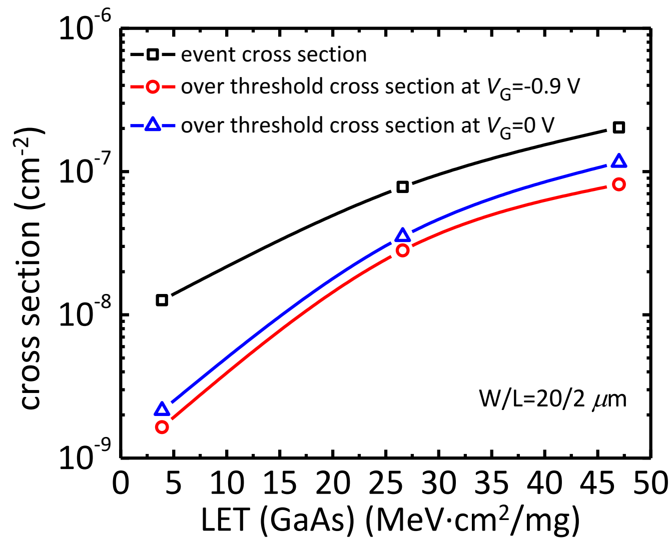

Fig. 2.10. The event cross section and the over threshold cross section at V_G = -0.9 V and V_G = 0 V as a function of LET. V_D = 2 V during irradiation.

The over-threshold cross section is plotted for two different gate biases. The event cross section is the largest, as it considers every event that is recorded. All cross sections increase with LET.

Moreover, the over-threshold cross section at $V_G = 0$ V is slightly larger than the cross section at $V_G = -0.9$ V. This is because the peak drain current increases slightly with the gate bias, as discussed below.

2.4.2. TPA Laser Results

A line scan from drain to source, parallel to the channel, was performed at different bias conditions, shown as the white and red dots in the inset of Fig. 2.11. Fig. 2.11 (a) and (b) show the transients at x = -22 μm (red dot located in the drain and referenced to x-axis scale in Fig. 2.9 (a)) of a line scan for devices in the OFF and ON bias conditions, respectively.

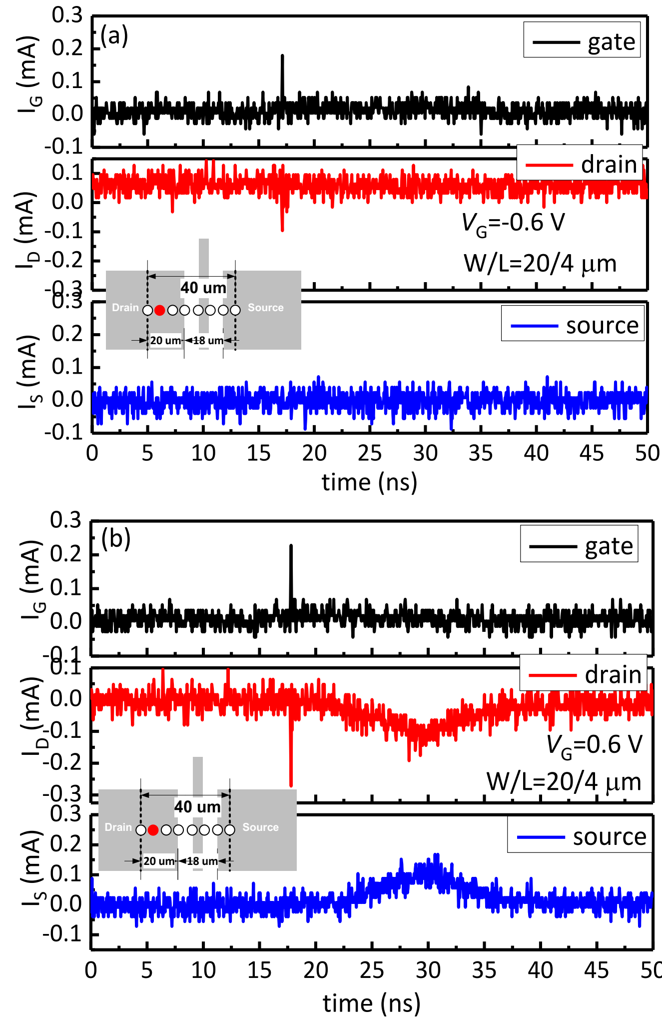

Fig. 2.11. Transients during pulsed laser irradiation for biases (a) $V_G = -0.6$ V; (b) $V_G = 0.6$ V. $V_{TH} = 0.3$ V, $V_D = 2.0$ V. The inset shows the line scan across the device during the laser irradiation. The white circles represent the possible scan points. The red circle represents the current strike point. For this transient, the strike location is x = -22 μm. The center of the gate is taken as the origin, and the drain is in the negative x direction. The laser pulse energy is 0.51 nJ.

In the OFF state, there is no source transient, and only the gate and the drain transients are present. However, when the device is ON, at the same strike location, there are source transients that are approximately equal to the drain transients. This behavior is consistent with the heavy ion results in which it was seen that in the OFF state, the source transients are quite small.

Two peaks are observed for drain transients in the ON state, similar to those shown in [73], [84]. Following the strike, there is charge collection at very short times that relaxes so fast that it is limited by the instrument resolution. This is due to collection of the generated electrons close to the drain. The peak in the gate transients corresponds to the change of electric field in the gate dielectric during carrier generation, as shown in the simulated results in Fig. 2.5. This peak is due to displacement current, consistent with the heavy ion data and accompanying simulations. The second peak is due to the generated holes moving toward the source, which backgate the channel and/or induce the bipolar amplification. The time difference between the two peaks is related to the time required for holes to move toward the gate.

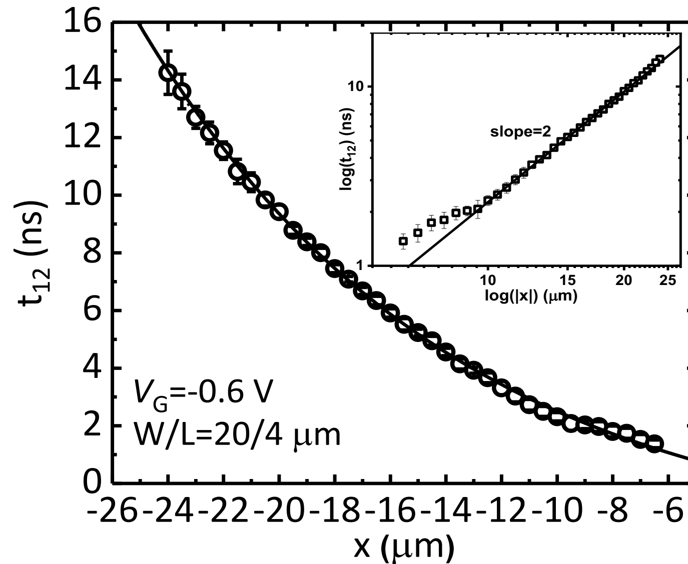

Fig. 2.12. The time difference between the first peak and second peak of the drain transients versus the strike location. Here the center of the gate is taken as the origin and the drain is in the negative x direction. The error bar represents one standard deviation of the transients taken at a single location. The inset plots the same data on a log-log scale.

Fig. 2.12 shows the time difference between the two peaks as a function of strike location. The farther the strike location is from the gate, the longer it takes for the second peak to show up. The inset shows the data in a log-log plot, in which the slope is very close to 2, which suggests that the time it takes for holes to move toward the gate is the diffusion time.

The source and drain collected charge and peak drain current along a line scan at different gate biases are shown in Fig. 2.13 (a) and (b), respectively. On the drain side, the peak drain current increases with gate bias, indicating the sensitive area moves deeper into the drain with higher gate bias. This is consistent with the results shown in Fig. 2.11. The source and drain collected charge are approximately equal and increase with the gate bias. The region between the gate and the drain has the largest collected charge. This spatial dependence is similar to that shown in planar Si bulk technology [124]. However, the drain collected charge is more than the source collected charge for Si technology, different from the GaAs MOSFET studied here.

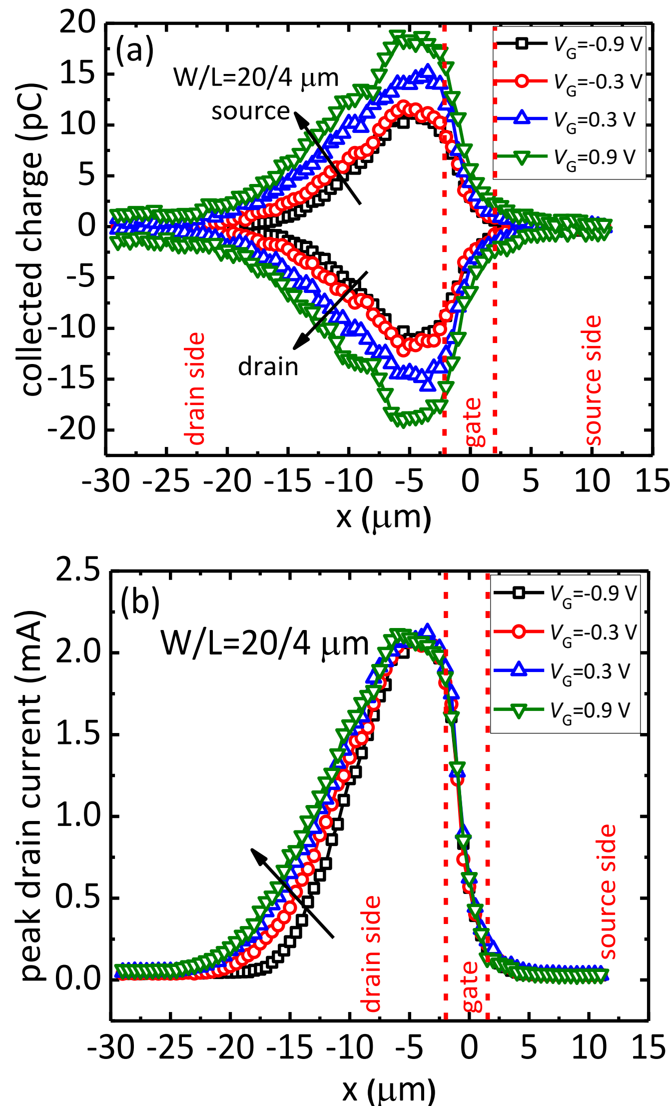

Fig. 2.13. (a) Collected charge; (b) peak drain current along a line scan at different gate biases. V_{TH}=0.3 V, V_D=2.0 V. In (a), the positive collected charge corresponds to the source and the negative collected charge corresponds to the drain. The arrows in both figures show the increase direction with the gate bias.

The increase of the collected charge with gate bias is partially due to the increase of the peak current with the gate bias. The greater contribution to the collected charge comes from the long tails in the ON state, as shown in Fig. 2.14. The peak drain current has little gate bias dependence; however, the tail current increases with the gate bias, also observed in GaAs MESFETs [125]. From V_G = -0.6 V to V_G = 0.9 V, the tail current increases by almost 0.05 mA, which can contribute as much as 3 pC to the total collected charge in a time window of 60 ns.

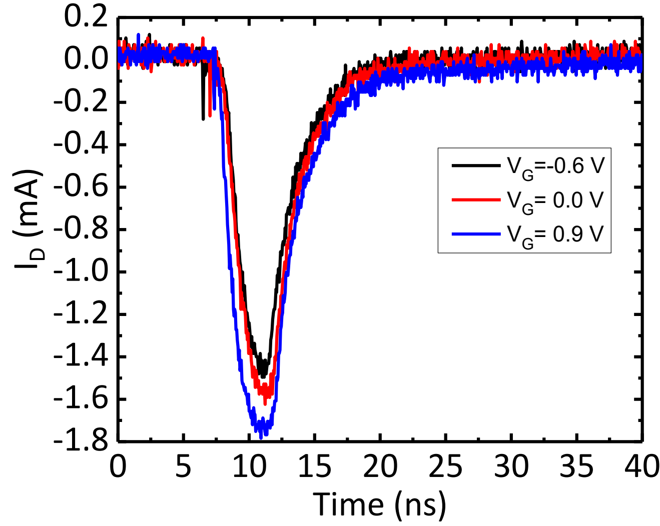

Fig. 2.14. Drain transients at different gate biases at a location of x=-9 μm. V_{TH} = 0.3 V, V_D = 2.0 V.

The peak drain current in these GaAs MOSFETs does not vary significantly with gate bias, which contrasts with results reported for several other types of devices. The peak drain current in InGaAs quantum-well MOSFETs shown in chapter Chapter 3, and AlSb/InAs HEMTs [88] reached a maximum around the threshold or pinch-off voltage. For GaAs HFETs [84] and InP HEMTs [128], due to the limited bias range reported, such roll-off behavior at higher gate biases was not observed. In both devices, however, the peak drain current varied strongly with the gate bias. The peak drain current in these surface channel GaAs MOSFETs is relatively insensitive to gate bias because of the vertical band-structure of the device. Devices that are sensitive to gate bias usually have quantum-well channels, which confine the radiation-generated carriers. The gate has control over the quantum-well, which in turn controls the charge collection. However, for surface channel GaAs MOSFETs, significant current flows outside the gate control region, as shown below.

To study the gate bias dependence of the charge collection, simulated electron current density differences between post-ion-strike (4.0 ns) and pre-ion-strike at V_G = -0.9 V and V_G = 0.9 V are

shown in Fig. 2.15 (a) and (b), respectively, like that shown in [129]. In the OFF state, the current flows outside the depletion region, where the gate has little influence. The current is due to the source to substrate barrier lowering, as shown in Fig. 2.9 [129], [130]. In the ON state, the current density is higher compared with the OFF state, which explains the increase of the peak drain current with gate bias at the same strike location, as shown in Fig. 2.13 (b). The current flows closer to the channel because there is no depletion region in the ON state. The current density is higher in the ON state because the depletion region in the OFF state pushes the current flow farther away from the channel. In the ON state, the current flows in the channel in addition to those regions away from the channel.

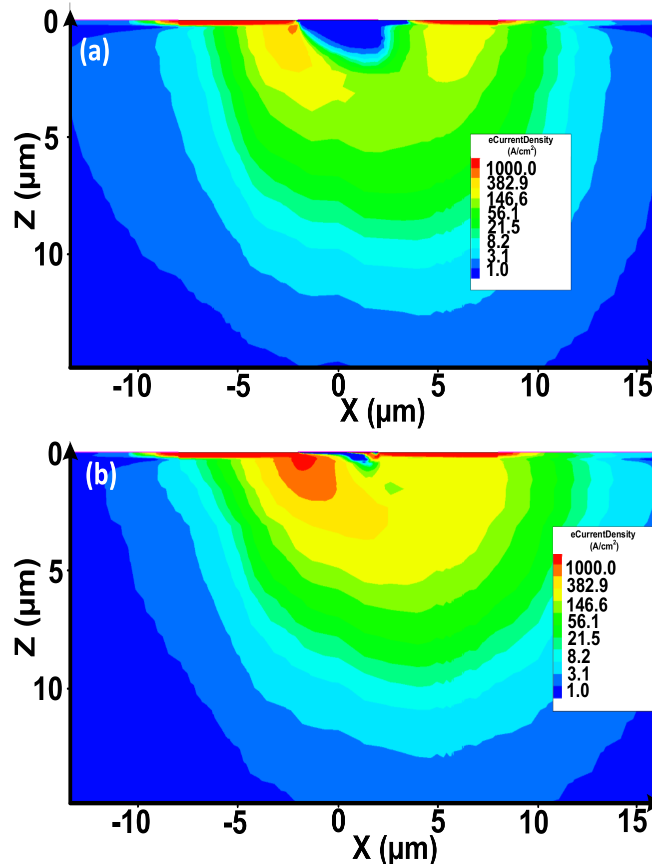

Fig. 2.15. Electron current density difference between post-strike (4.0 ns) and pre-strike at (a) V_G = -0.9 V; (b) V_G = 0.9 V.

To understand the spatial dependence of the charge collection, a horizontal line scan similar to the TPA laser experiment is also simulated in TCAD. Fig. 2.16 shows the simulated peak drain current along a horizontal cutline at V_G = -0.9 V and V_G = 0.9 V. The peak drain current increases with gate bias. The simulation results are qualitatively consistent with the TPA laser results of Fig.

2.13. These results show that the area between the gate and drain has the highest sensitivity, due to higher electric field in those regions.

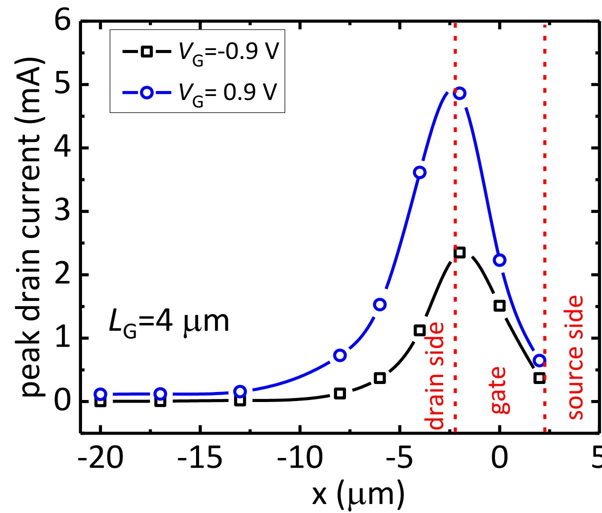

Fig. 2.16. Simulated peak drain current along a horizontal cut line at two different gate biases.

Fig. 2.17 shows the peak drain current along a line scan at three different drain biases. The collected charge follows the same behavior as the peak drain current. The drain side is the most sensitive to the drain bias, while the areas below the gate and the source do not show drain bias dependence. The peak drain current increases with drain bias, similar to results in [84], [85], due to the higher electric field on the drain side when the drain bias is higher. The higher electric field leads to higher electron velocity, which means higher drain current for the same amount of charge generation. These results suggest that the sensitive volume increases with both drain and gate bias.

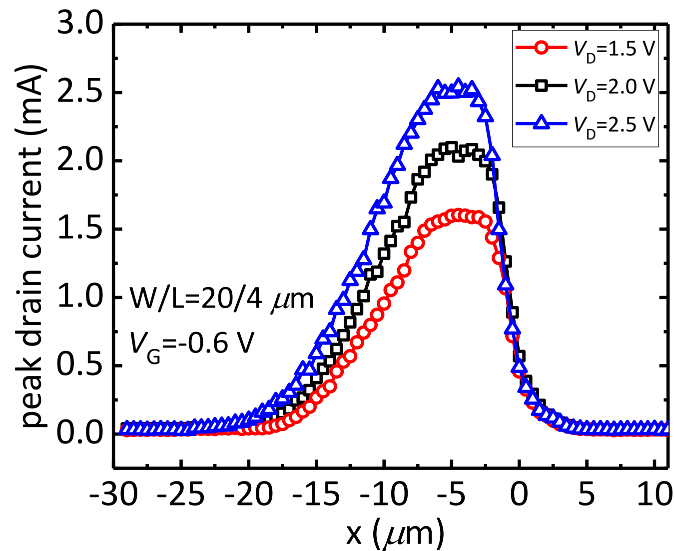

Fig. 2.17. Peak drain current along a line scan vs. drain biases. V_{TH} = 0.3 V.

TPA laser irradiation also allows the three dimensional mapping of the sensitivity of the device. Fig. 2.18 shows the peak drain current and drain collected charge at two different laser pulse energies. When the carriers are generated away from the active region, the peak current and the collected charge drop, indicating that charge collection efficiency decreases with depth. When the laser pulse energy increases so that high level injection conditions exist, the charge collection efficiency is constant in the sensitive volume and is reduced outside of the sensitive volume. However, in this case, 0.75 nJ is still in low level injection, so the collection efficiency keeps decreasing and follows approximately linear behavior.

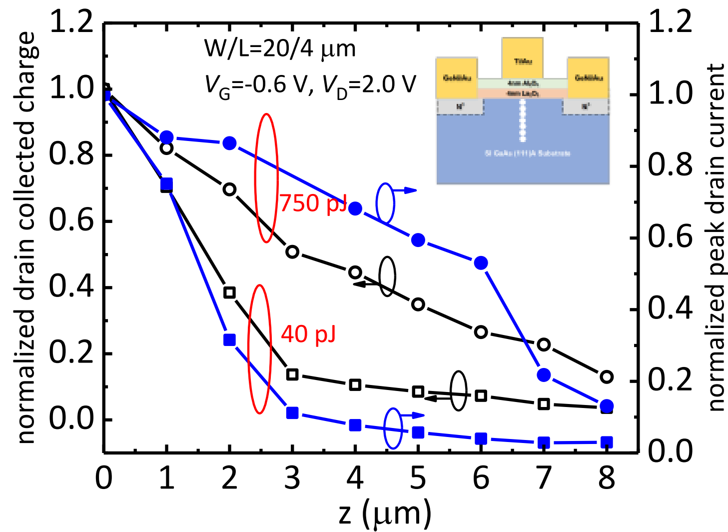

Fig. 2.18. Normalized drain collected charge and normalized peak drain current as a function of depth of the device at two different laser pulse energies. Z = 0 μm represents the front surface of the device. The normalization is based on the collected charge and peak current from the front surface strike. The white circles in the inset represent the strike location during the depth scan. V_{TH} = 0.3 V.

Fig. 2.19 shows the peak gate current obtained during an XZ area scan. The scan area is indicated in the inset of the figure. The gate current is most significant in the area between the gate and the drain. When the carriers are generated 10 μm away from the front surface, the gate current is approximately the same as when they are generated at the front surface. The carrier density in the channel is orders of magnitude smaller when the carriers are generated 10 μm away from the front surface compared with generation on the front surface. The currents are approximately the same in the two cases, however, which is consistent with gate displacement current, but not carrier transport through the gate dielectric.

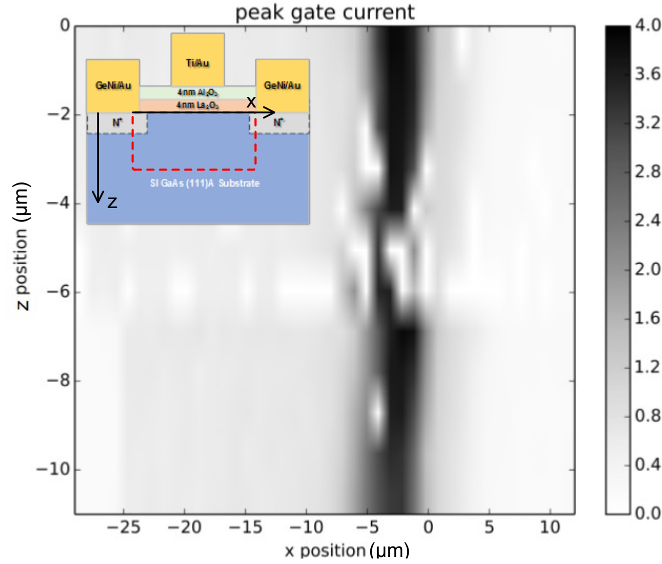

Fig. 2.19. Peak gate current under the XZ area scan. The origin of the XZ plane is at the center of the gate and the front surface of the device. For this scan, V_G = -0.6 V, V_D = 2.0 V, V_{TH} = 0.3 V. Laser pulse energy is 0.75 nJ. The white block in the center of the figure is due to loss of the data during experiment. The red box in the inset shows the scan area.

2.5. Conclusion

The single event transient response of surface channel GaAs MOSFETs is investigated through broadbeam heavy ion irradiation and TPA laser irradiation. 2D TCAD simulations are used to understand the charge collection mechanisms. There are significant gate transients, even though the barriers between the gate dielectric and GaAs are large enough and the gate dielectric is thick enough to remove the possible conduction current through tunneling. Experimental results and TCAD simulations confirm that the transients come from displacement current. The presence of deep traps in the semi-insulating substrate lead to long-lasting tails in the displacement current.

For long channel device, the channel resistance is large enough to suppress the source transients in the OFF state. With the increase of the gate bias, the source transients becomes equal to the drain transients since the source and drain region are not isolated anymore. The source transients are associated with the charge enhancement processes, such as backgating and bipolar amplification. These processes occur because the radiation-generated holes accumulate in the substrate and increase the local electrostatic potential, which backgates the channel and causes bipolar amplification. The long tails in the source/drain transients in the ON state are likely due to holes trapped in deep levels in the semi-insulating GaAs substrate, which can modulate the channel. In addition, experimental results suggest that the sensitive volume increases with the drain bias.

Because of charge enhancement effects, the soft error rate of GaAs MOSFET circuits may be higher than that of their silicon counterparts. For example, critical LET values lower than 1 MeV/mg/cm^2 [73] have been reported for GaAs MESFET logic. Hardening techniques mentioned in section 1.3.2.5 could be used to reduce the charge enhancement effect by reducing the hole lifetime in the substrate. Since GaAs MOSFET grows on the semi-insulating substrate and the holes in the substrate is the reason for charge enhancement, similar methods are also likely to be successful for these devices.

Chapter 3. Single Event Transient Response of InGaAs Quantum-Well MOSFETs

3.1. Introduction

In this chapter, the single-event-transient response of InGaAs MOSFETs exposed to heavy-ion and laser irradiations is investigated. The large barrier between the gate oxide and semiconductor regions effectively suppresses the gate transients compared with other types of III-V FETs. After the initial radiation-induced pulse, electrons and holes flood into the channel region at short time. The electrons are collected efficiently at the drain. The slower moving holes accumulate in the channel and source access region and modulate the source-channel barrier, which provides a pathway for transient source-to-drain current lasting for a few nanoseconds. The peak drain transient current reaches its maximum when the gate bias is near threshold and decreases considerably toward inversion and slightly toward depletion and accumulation. 2D TCAD simulations are used to understand the charge collection mechanisms.

3.2. Device Description

The device under test (DUT) is a self-aligned InGaAs quantum-well MOSFET. Detailed device information is described in [40]. Fig. 3.1 shows the schematic cross section of the device (not drawn to scale) and TEM cross section of the device. A 0.4 μm $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm semi-insulating InP substrate. An 8 nm high-mobility $In_{0.7}Ga_{0.3}As$ quantum-well channel enhances the device conductance. A HfO_2 gate dielectric sits directly on top of the channel. The inverted Si delta doping in the buffer layer is used to reduce source/drain access resistance and increase the channel carrier density [104].

The band diagram cut through the gate vertically is shown in Fig. 2. For this band diagram, all the terminals of the device are biased at 0 V. The device has a type-I heterostructure, which means that both the electrons and holes are confined in the channel region. This has a significant impact on the charge collection mechanisms. For the devices examined here, the $In_{0.7}Ga_{0.3}As/HfO_2$ conduction band offset is 2.2 eV and the valence band offset is 2.9 eV [105]. This band alignment is similar to SOI technology. However the carriers deposited in the buffer and substrate can flow back to the quantum-well, unlike the SOI technology. Therefore, the sensitive volume of this type of device is larger compared with the SOI technology.

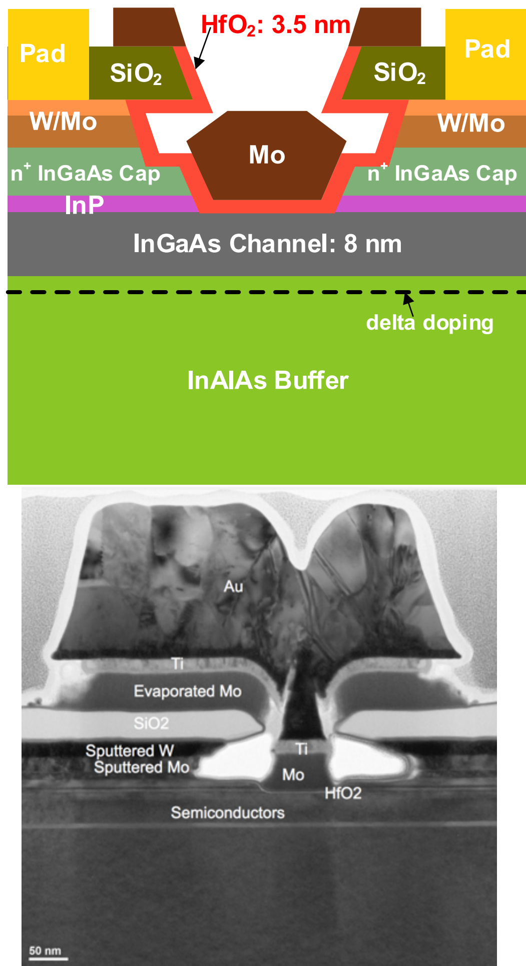

Fig. 3.1. Schematic cross section (Not drawn to scale) of devices under test (left) and TEM cross section of the device (right).

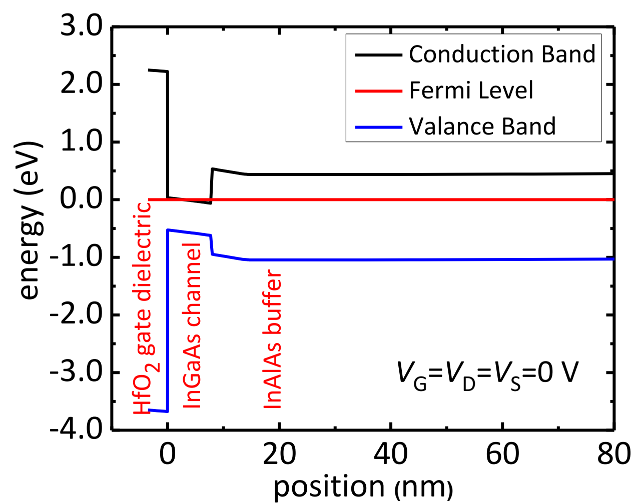

Fig. 3.2. Vertical band diagram of the device (all terminals are biased at 0 V for this band diagram).

3.3. Experimental Details

For transient capture, all the devices are mounted in custom-milled metal packages with microstrip transmission lines and Precision 2.92 mm K connectors [106], [107]. The transients were captured using a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20GS/s-sampling rate. Each oscilloscope channel has 50 Ω input impedance, which is used to convert the transient current to a measurable voltage. During these tests, the source and substrate were grounded, the drain bias was 0.5 V, and the gate bias was varied. A semiconductor parameter analyzer, HP 4156B, supplied the DC biases through Picosecond Model 5542 bias tees with 50 GHz bandwidth.

A. Broadbeam Ion Tests

For the broadbeam test, the devices were irradiated with 14.3 MeV oxygen ions in Vanderbilt's Pelletron electrostatic accelerator. Fig. 3.3 shows the schematic diagram of the experiment setup. From SRIM calculations, the ions have LETs of 3.9 MeV-cm^2/mg, 4.1 MeV-cm^2/mg, and 4.2 MeV-cm^2/mg, respectively, in $In_{0.7}Ga_{0.3}As$, $In_{0.52}Al_{0.48}As$, and InP. The corresponding ion ranges are 6.9 μm, 7.4 μm, and 8.5 μm. Considering that the channel and buffer layer thicknesses are much smaller than the ion range, carriers are generated primarily in the InP substrate. In addition, the overlayer thickness is about 0.4 μm, which is much smaller than the ion range, about 3.6 μm, indicating very small energy loss in those materials.

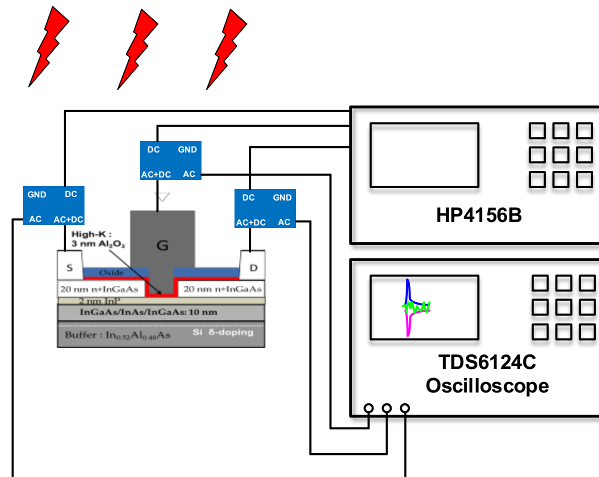

Fig. 3.3. Schematic diagram of the broadbeam heavy ion experiment setup.

B. Two-Photon-Absorption (TPA) Laser Test

The pulsed laser technique has been widely used for SEE testing [108]-[111]. High peak power

femtosecond laser pulses at sub-bandgap optical wavelengths have been used as a viable alternative to conventional single-photon excitation to investigate the single event transient response of various devices based on two-photon absorption (TPA) [109]-[111]. In two-photon absorption, the laser wavelength is chosen to be less than the bandgap of the semiconductor material such that no carriers are generated at low light intensities and at sufficiently high intensities, however, the material can absorb two photons simultaneously to generate a single electron–hole pair [109]. This allows the carriers to be generated only in the high field intensity focal region. As a result, charge can be injected at any depth, allowing 3D mapping of the sensitive volume of the device [109]. Since laser irradiation avoids the radiation damage introduced by heavy ion irradiation and is easy to operate, it is becoming a valuable method to investigate charge collection mechanisms.

Laser irradiations were performed at Vanderbilt University. The experimental setup is the same as Fig. 3.3 except that the laser pulse irradiation is from the backside. The detailed experimental setup is described in [111]. The laser wavelength is 1.26 μm and the nominal pulse width is approximately 150 fs. The DUT was fixed on an automated precision linear stage with a resolution of 0.1 μm. The stage jitter is about 0.2 μm. The optical pulses were focused onto the DUT using a 100× (NA 0.5) microscope objective with a charge generation spot size of approximately 1.2 μm in InGaAs.

The photon energy of the laser is 0.98 eV, which is greater than the bandgap of the channel material, $In_{0.7}Ga_{0.3}As$ (0.58 eV) [112]. For the laser experiment, the irradiance is approximately 2 $\times 10^8$ W/cm^2 . Considering that the linear absorption coefficient (~ 10^4 cm^{-1}) is much larger than the TPA coefficient (~ 50 cm/GW [113]), the two-photon absorption in the channel region of these devices is much smaller than the single-photon absorption. This means that single-photon absorption dominates in the channel region. However, the photon energy is less than the band gap of the other materials, InP (1.35 eV) and $In_{0.52}Al_{0.48}As$ (1.45 eV) [112]. In these materials, TPA occurs, but the density of generated carriers is much smaller than that in the channel. Because both InP and $In_{0.52}Al_{0.48}As$ have a TPA coefficient of ~ 30 cm/GW [114], the depth at which the beam intensity decays to half of the original value is ~ 3000 μm, which is larger than the buffer and substrate thickness. Considering the Gaussian beam profile, the high irradiance region extends ~ 10 μm [109]. This is about a thousand times larger than the channel thickness, which compensates for the difference between the linear absorption coefficient in the channel and the TPA coefficient

in the buffer and substrate. As a result, the buffer and substrate together have a comparable number of generated carriers with the channel layer.

3.4. Results and Discussions

3.4.1. Heavy Ion Results

A typical current transient is shown in Fig. 3.4. The source and drain transients have nearly the same magnitude but opposite polarity, which suggests that the transient current comes from the channel conduction. This is different from the traditional junction collection in Si devices [54]. The gate transients, if any, are indistinguishable from the background noise.

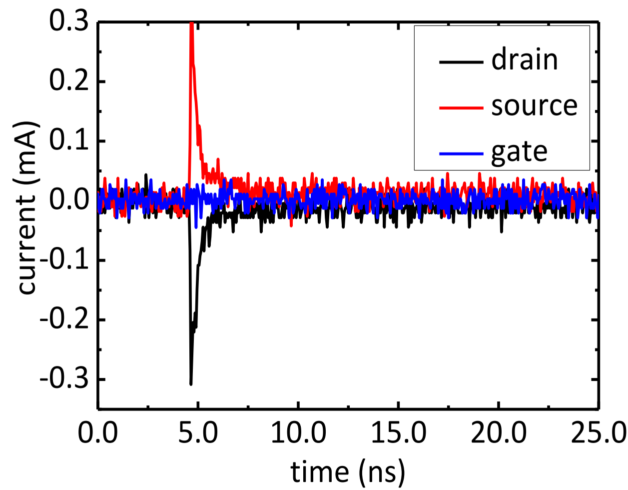

Fig. 3.4. Current transient for a device biased at V_{GS}-V_{TH} = -0.2 V, V_{DS} = 0.5 V with source grounded. W/L=10 μm/0.07 μm.

Since the barrier between semiconductor and HfO_2 for both types of carriers (2.2 eV for electron and 2.9 eV for hole) in these devices is much larger than that for the AlGaN/GaN MOS HEMTs studied in [106], the gate oxide effectively suppresses the gate transients. This is different from the previously investigated III-V FETs, which have significant gate transients, as described in section 1.3.2.2.

The shapes of the source and drain transients are similar to those reported in [86]. Following the strike, the source and drain currents increase sharply. After reaching the peak, they start to decay. The relaxation is related to processes with two distinct time constants. The fast collection is fairly rapid, with a time constant of approximately 300 ps or less. This fast collection is caused by the generated electrons that are collected by the drain. The longer-time portion of the transient comes from a source-to-drain current pathway, which extends for about 3-5 ns. This results from the more slowly transporting holes. Following the ion strike, the generated electrons and holes

under the channel layer flood into the channel region, because of the type-I band alignment. The electrons are rapidly swept toward the drain, but the slower holes (the electron mobility is around 50 times greater than the hole mobility) pile up in the channel and the source access region, lowering the source-channel barrier. As a result, electrons are injected from the source into the channel, and subsequently collected by the drain. This is illustrated in the following TCAD simulations. This bipolar enhancement is similar to that shown in other III-V FETs, as mentioned in section 1.3.2.3.

The gate-bias dependence of peak drain current was also investigated. In these tests, the drain bias voltage was 0.5 V, while the gate voltage was varied according to the pseudo-random sequence of 0 V, -0.4 V, 0.4 V, -0.8 V, 0.2 V, -1 V, -0.2 V, -0.6 V. This special sequence was selected to reduce any potential effects of device degradation on the measurement trends. Fig. 3.5 shows the peak drain current versus gate bias of one of the devices. The smooth curve is a spline fit to aid the eye.

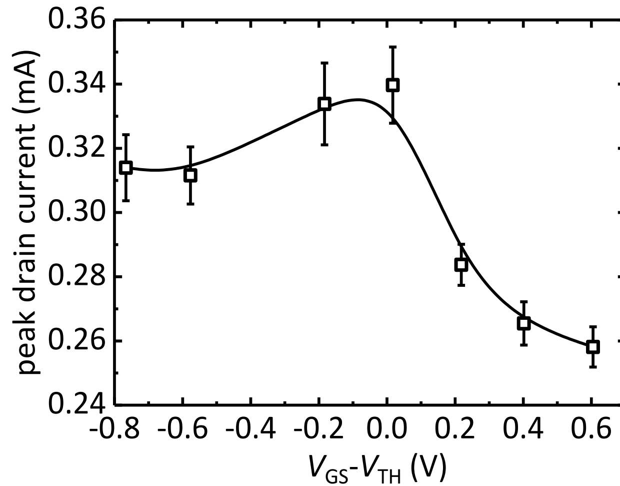

Fig. 3.5. Peak drain current vs. gate bias of at V_{DS} = 0.5 V. The average flux is 1×10[8] particles/s•cm[2]. The error bars indicate the standard error of the mean. W/L=10 μm/0.07 μm.

The peak drain current of the device decreases slightly in depletion and accumulation. Transients occur in inversion because the carrier density generated by radiation is higher than the carrier density induced by the applied gate bias. Moreover, the peak drain current decreases considerably in inversion. This gate bias dependence is similar to that reported in III-V HEMTs [88]. This strong gate bias dependence is different from the GaAs surface-channel MOSFET. This is mainly because the transient current flows through the quantum-well, instead of the bulk region outside the depletion region in GaAs MOSFET. The quantum-well is in close proximity to the gate,

so that the gate has a good control over the current flow. The mechanisms are illustrated by TCAD simulations in section IV.

Heavy ion tests were also conducted at Lawrence Berkeley National Laboratory (LBNL) with different heavy ions. Table 3.1 shows the ion LETs and ranges in the channel material, InGaAs, and substrate, InP. Since the channel layer is very thin, only 8 nm, most of the charges are generated in the InP substrate. Fig. 3.6 (a) and (b) show the transients due to Ar ion strikes biased at V_G = -0.6 V, V_G = 0.0 V, and V_G = 0.6 V, respectively. The peak drain current dependence on the gate bias is consistent with the oxygen ion data, as shown in Fig. 3.5. It decreases significantly in the inversion region, and reaches a maximum around the threshold voltage. Another feature shown in the transients of Fig. 3.6 (b) is the long tails. The tail current is about 0.05 mA and lasts for μs. Such tails become evident when the device turns ON. It is probably related to the semi-insulating substrate, as described in section 1.3.2.4.

Table 3.1. Details of ions used in experiment

Ions	**Energy (MeV)**	**LET (InGaAs) (MeV•cm^2/mg)**	**Range (InGaAs)(μm)**	**LET (InP) (MeV•cm^2/mg)**	**Range (InP)(μm)**
Oxygen	14.30	3.9	6.9	4.16	8.53
Neon	89.95	3.73	32.57	3.80	42.45
Argon	180.00	9.28	29.95	9.45	38.90
Krypton	387.08	25.34	29.99	25.70	28.81
Xeon	602.90	44.54	30.14	45.31	38.95

Comparison can also be made between the InGaAs quantum-well MOSFET with the Si device. Due to the limited report of Si device in literature, direct side by side comparison with Si device at the same experimental conditions is difficult. But meaningful comparison can still be made. Fig. 3.6 (c) shows the drain current transients of FDSOI and Si planar device with similar or larger size. The ion LET for these devices are much larger compared with the Ar ion in InGaAs quantum-well MOSFET. However, it shows that the drain current is much smaller in FDSOI technology, due to small sensitive volume. The current is much larger in Si bulk device, but it is still smaller than InGaAs quantum-well MOSFET. This suggests that the InGaAs quantum-well MOSFET is more sensitive compared with both the Si SOI and planar technology.

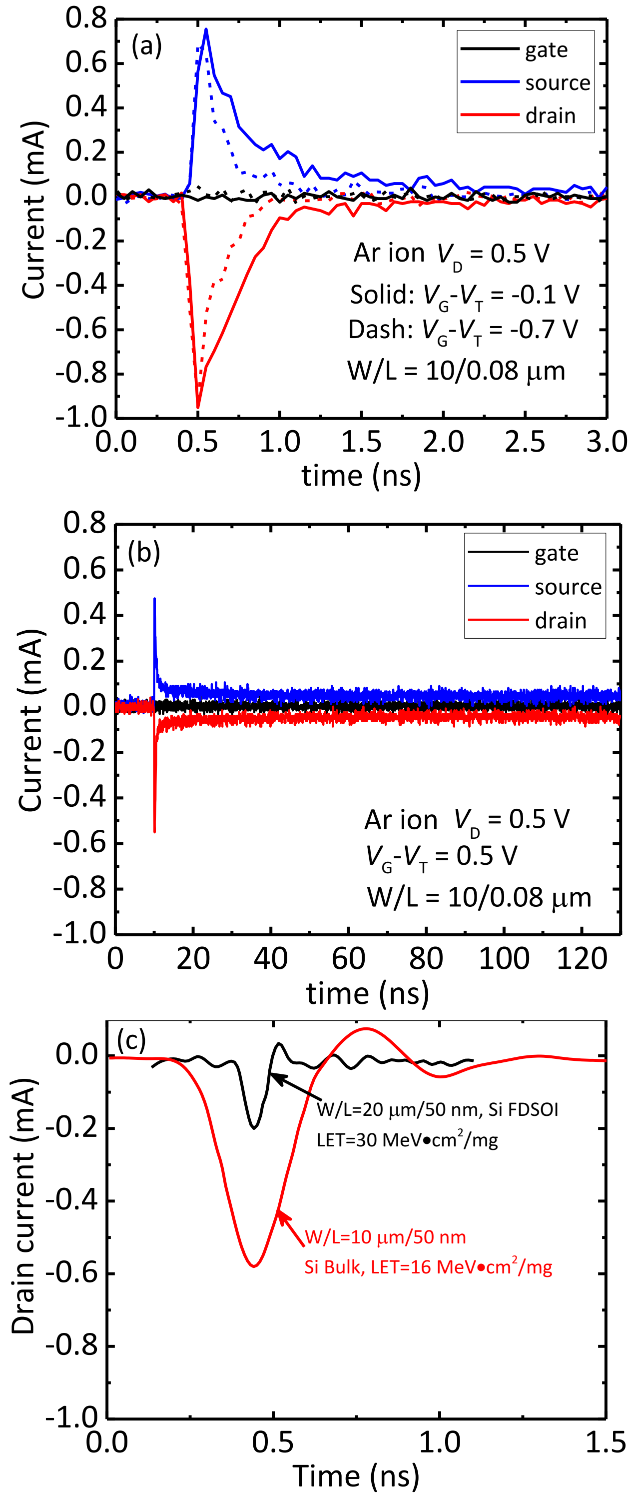

Fig. 3.6. Transients due to Ar ion strike for device biased at (a) V_G = -0.6 V and V_G = 0.0 V, and (b) V_G = 0.6 V. V_T = 0.1 V. (c) Drain current transients of Si FDSOI with size of W/L=20 μm/50 nm and body thickness of 11 nm, exposed to 808 MeV Kr ion with LET=30 MeV● cm^2/mg [131] and Si planar bulk device with size of W/L=10 μm/50 nm exposed to 35 MeV Cl ion with LET=16 MeV● cm^2/mg [132].

The peak drain current and drain collected charge as a function of LET are shown in Fig. 3.7 (a) and (b), respectively. Both the peak current and the collected charge increase with the LET, as expected, irrespective of the applied gate bias. The peak drain current gate bias dependence is the same among all the ions tested. Besides, the collected charge is one order of magnitude higher at $V_G = 0.6$ V compared with OFF state gate biases, similar to that shown in Fig. 1.13. This is due to the tail current at $V_G = 0.6$ V, which contributes most of the collected charge.

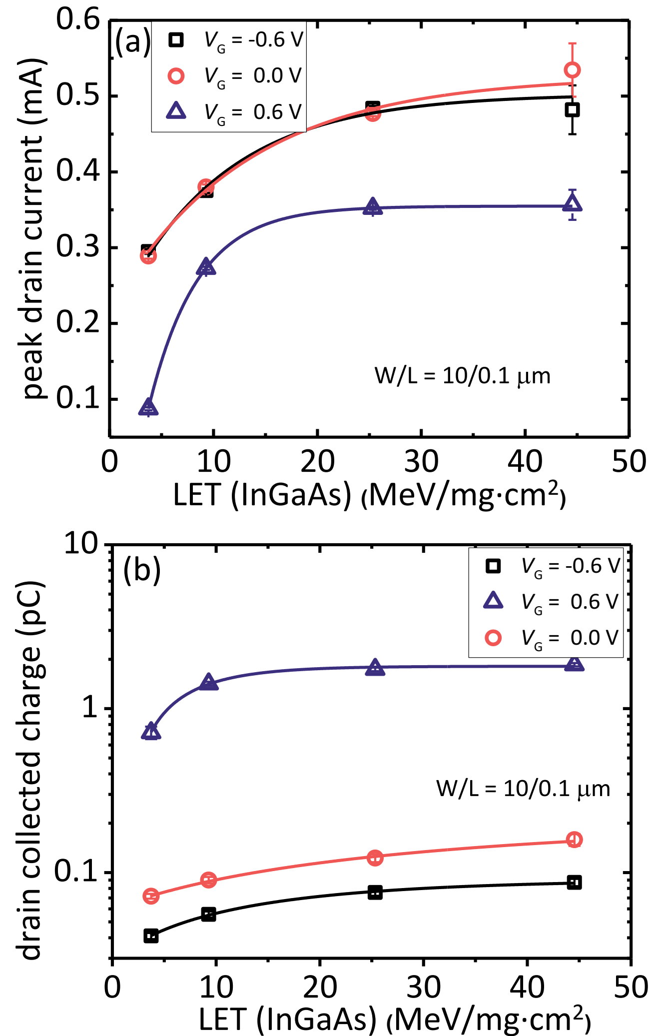

Fig. 3.7. (a) Peak drain current and (b) drain collected charge as a function of LET. Each data point represents an average of 100 transients recorded. The error bar represents the standard deviation of the mean. The drain collected charge is obtained by integrating the drain current transients within a time window of 30 ns. This is to restrict the tail current contribution at $V_G = 0.6$ V.

3.4.2. TPA Laser Results

For the laser test, line scans were performed, so the position dependence of the induced transients could be evaluated. Fig. 3.8 inset shows the schematic diagram of the experiment used to obtain the line scan of the devices. The line scan XX' was from -2 μm to 2 μm horizontally. The center of the device is regarded as the origin.

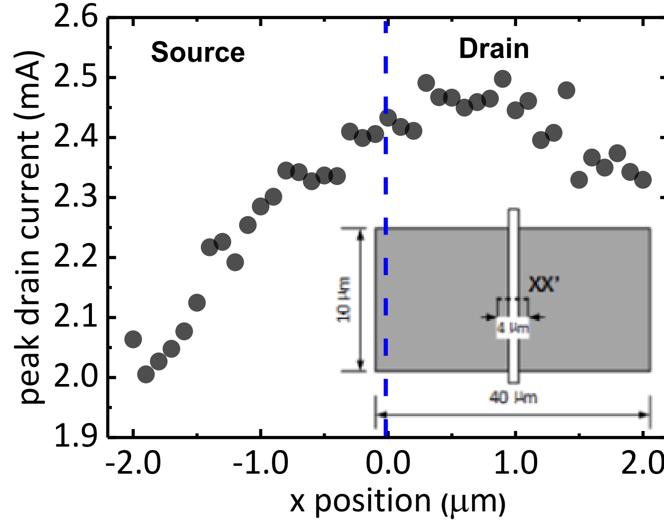

Fig. 3.8. Peak drain current along the line scan XX' at bias V_{GS}-V_{TH}=0 V, V_{DS}=0.5 V. The laser pulse energy is around 0.55 pJ. The source side has a negative x coordinate while the drain side is positive.

The drain side strike has a higher peak current compared with the source side strike. This is consistent with the applied bias between the drain and source contact, V_{DS} = 0.5 V. Consequently, the electric field on the drain side is larger than the source side. The carriers generated by the laser pulses move at a higher velocity in the drain side, which leads to larger peak current. Thus the drain side has a higher sensitivity to the irradiation.

The transients were investigated under different gate biases. Fig. 3.9 shows the peak drain current under different gate biases. Each data point is taken by averaging the drain peak current along a line scan XX', as shown in Fig. 3.8. The statistical standard error of the mean for each bias point is less than 5%. The peak drain current reaches a maximum around the threshold voltage. Furthermore, the current decreases considerably in inversion and decreases slightly in depletion and accumulation. This result is consistent with the broadbeam heavy ion data.

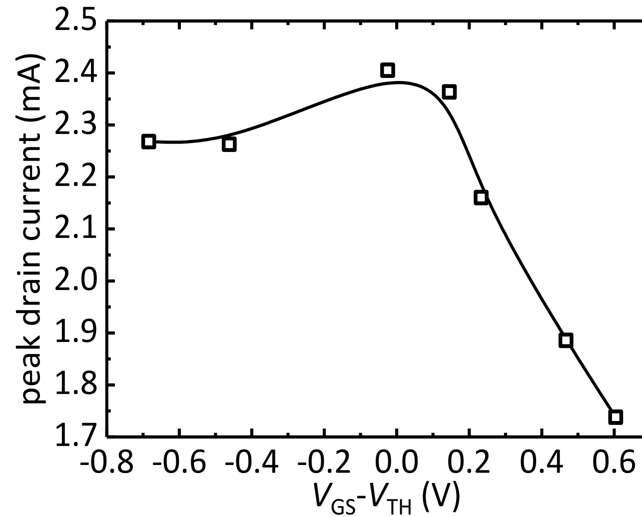

Fig. 3.9. Drain peak current vs. gate bias at V_{DS}=0.5 V (each data point is taken as the average of a line scan). The small error bar is neglected.

3.4.3. 2D TCAD Simulation Results

In this section, 2D TCAD simulations are used to illustrate the mechanisms of charge collection in these devices. Fig. 3.10 shows the structure used for the TCAD simulations. The gate length is 70 nm. The ion strikes are defined to be Gaussian both in time and space. The Gaussian heavy ion model has a characteristic width of 10 nm in space and 2 ps in time.

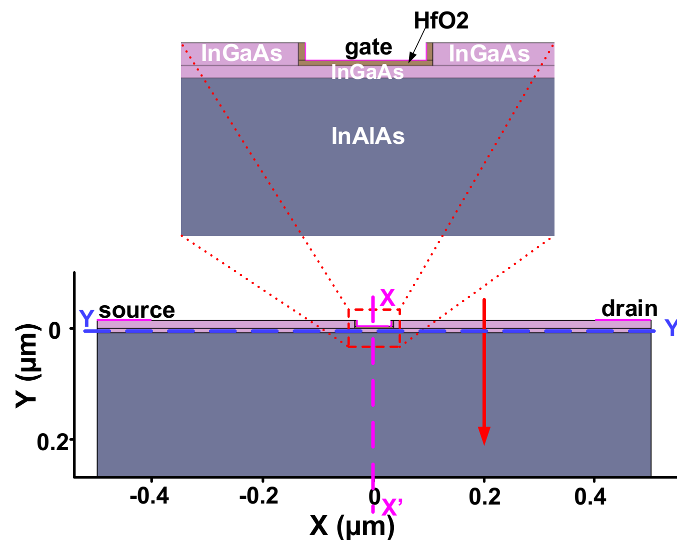

Fig. 3.10. Device model that is used in the 2D TCAD simulation (red arrow indicates the center of strike location). Synopsys Sentaurus TCAD tools are used here for simulation.

The linear energy transfer (LET) used to illustrate the mechanisms corresponds to charge

deposition of 0.1 pC/μm, approximately the LET used in the broadbeam heavy ion experiment. The red arrow indicates the center of the strike location for the simulation (between the gate and drain), which is x = 0.2 μm. The time center of the strike is t = 1.0 ns.

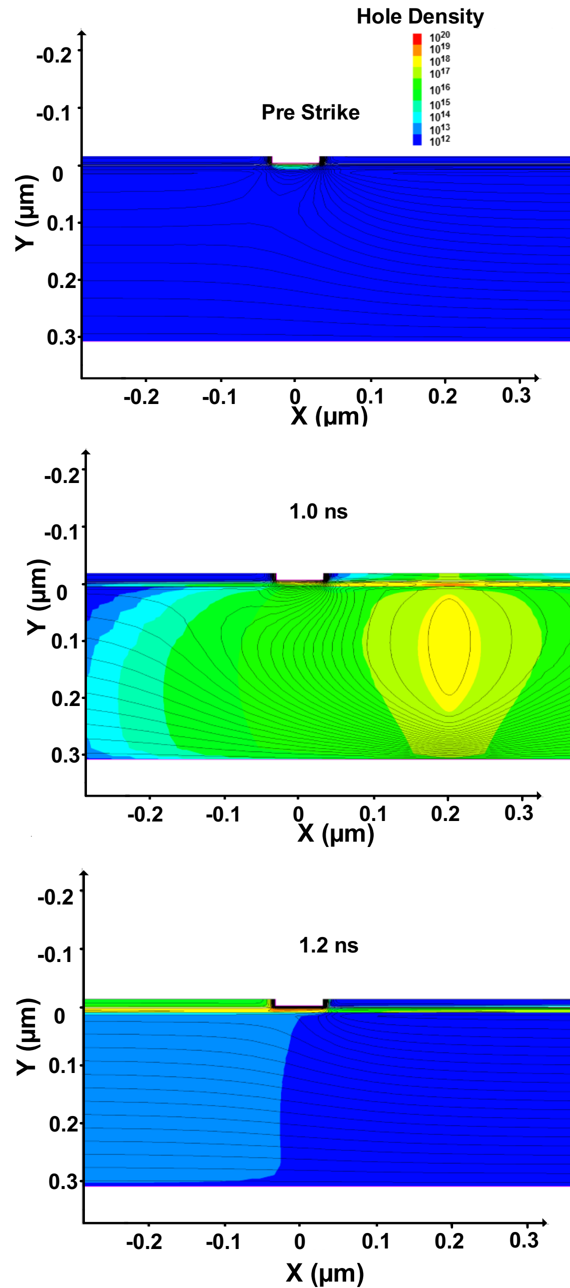

Fig. 3.11. Hole density and electrical potential plotted at 1.0 ps (pre-strike), 1.0 ns and 1.2 ns. The hole density is shown as color map and the electrical potential is shown as the equipotential line. The device is biased at V_{GS}-V_{TH}=-0.2 V, V_{DS}=0.5 V. Only the region around the channel is shown for clarity.

Fig. 3.11 shows the hole density and the electric potential in the device at t = 1.0 ps (pre-strike),

1.0 ns (center of strike) and 1.2 ns (post-strike), respectively. At the time of the strike, a large number of electron hole pairs are created around the strike location. As a result, the electric potential is strongly distorted compared with the pre-strike condition (t = 1.0 ps). At 1.2 ns, the potential in the thick buffer layer has almost recovered and the holes in the buffer are mostly collected, especially at the drain side. This confirms that the generated electrons and holes soon move into the channel layer because of the type-I heterostructure.

After 1.2 ns, only the channel region is strongly perturbed as a large number of electrons and holes are collected there. The process of collecting these carriers lasts for a few nanoseconds as illustrated in Fig. 3.4. To understand this process, Fig. 3.12 shows the time evolution of the conduction band along the horizontal cut, YY'. At 1.0 ns, the electrostatic potential around the strike location is strongly distorted by the generated carriers. Soon after the strike, the conduction band recovers on the drain side at 1.2 ns. This confirms that the generated electrons are collected quickly by the drain. Following the strike, the source channel barrier is lowered from 0.52 eV to 0.03 eV at 1.2 ns as holes pile up in the channel layer right under the gate and the source access region. The barrier keeping the electrons from being injected from the source to channel is quite small. The transistor turns ON and current flows between source and drain. As holes reach the source where they recombine, the electric potential recovers to the pre-strike value. Eventually, the source channel barrier returns to 0.52 eV.

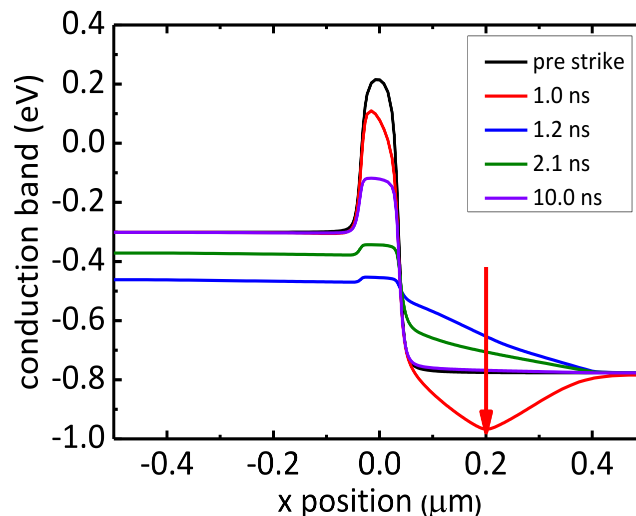

Fig. 3.12. Conduction band along the horizontal cut,YY', shown in Fig. 3.10, at different time. The bias condition is the same as shown in Fig. 3.11.

Fig. 3.13 (a) shows the conduction band along the horizontal cut YY' under different gate biases at 1.2 ns. The source channel barriers preventing carriers from being injected from the source are small under all gate biases. The potential drop along the channel region is reduced with increasing gate bias. This leads to a smaller horizontal electric field along the channel, which translates into smaller electron velocity at higher gate bias.

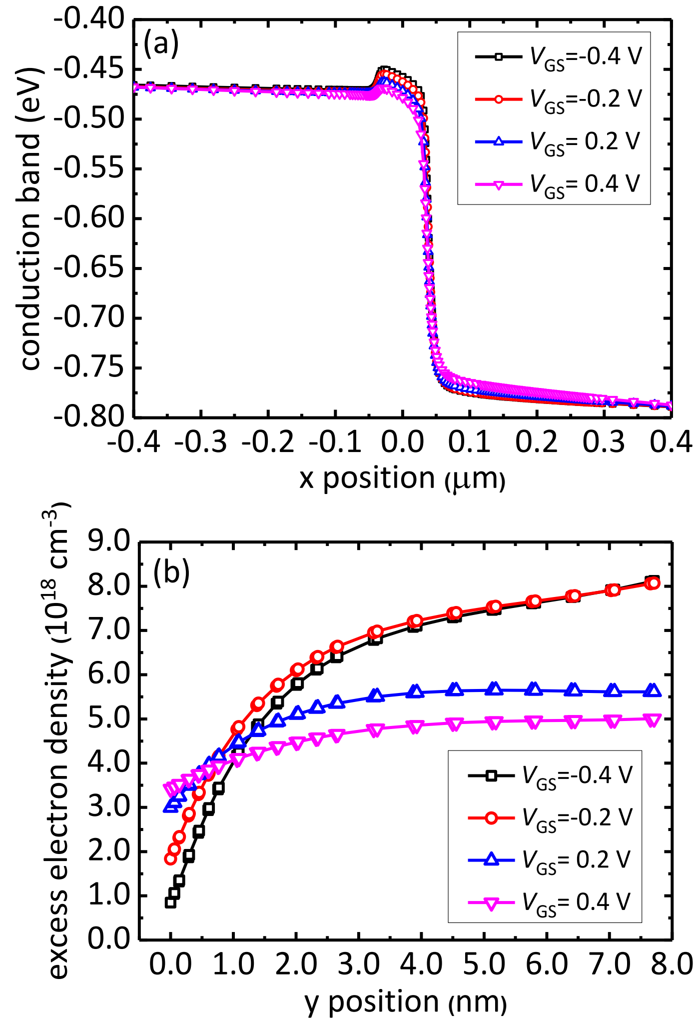

Fig. 3.13. (a) Conduction band along the horizontal cut YY' in the channel layer and (b) Electron density along the vertical cut XX' under different gate biases at 1.2 ns (200 ps after the center of the strike). Here for clarity, only the electron density in the channel layer is shown.

Fig. 3.13 (b) presents the excess electron density, the absolute electron density difference between the post-strike and pre-strike conditions, along the vertical cut XX' under different gate biases at 1.2 ns. As the gate bias increases, the excess electron density in the channel reaches a maximum for gate voltages near the threshold, and decreases slightly in depletion and considerably

in inversion. Although there is a slight increase in the post-strike electron density with the gate bias, the increase with gate bias is small. This is because for a given amount of generated carriers, most of them will be collected in the channel layer, irrespective of the gate bias. The gate bias does not have a large effect on the post-strike electron density in the channel due to the electric potential distortion caused by the large number of carriers. As a result, the higher the pre-strike electron density, the smaller the excess electron density will be. Thus, for gate biases in inversion, the reduced excess electron density and the reduced electron velocity cause a significant decrease in peak drain current. For gate biases in depletion and accumulation, the excess electron density is slightly smaller than the density in threshold, which causes a slight decrease of the peak current.

The normalized peak drain current for the heavy ion experiment, the laser experiment, and the 2D TCAD simulations is shown in Fig. 3.14. Each set is normalized by its own maximum peak current, which occurs near $V_{GS} - V_{TH} = 0$ V. The TCAD simulations describe trends in the gate bias dependence of the peak drain current quite well, showing that the peak drain current decreases considerably in inversion and decreases slightly in depletion and accumulation.

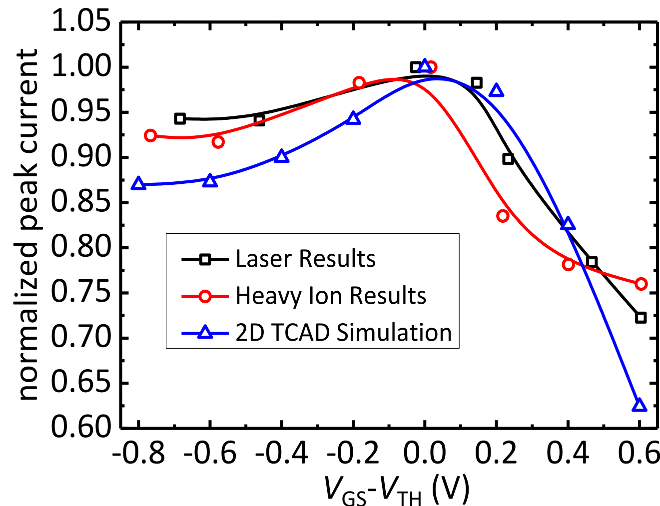

Fig. 3.14. Normalized peak drain current of heavy ion experiment, laser experiment and 2D TCAD simulation. The maximum peak drain currents are 2.4 mA, 0.34 mA, and 48 mA for laser, heavy ion, and TCAD simulation respectively. The quantitative differences in peak current result from parasitic capacitance and inductance that exist in the experimental configuration that are not replicated in the simulations. But the trends in peak current are replicated well via simulation.

3.5. Conclusion

The single-event-transient response of InGaAs MOSFETs is investigated through broadbeam heavy ion and laser irradiation. The large conduction band offset and valence band offset between the gate dielectric and semiconductor regions effectively suppress the gate transients. The deep type-I heterostructure strongly affects the charge collection process. The generated carriers are collected in the quantum well (channel layer). The slow holes pile up under the gate and the source access region, which reduces the source channel barrier height. More electrons are injected from the source to the drain, enhancing the collected charge. The peak drain current reaches a maximum near the threshold voltage and decreases considerably in inversion and slightly in depletion and accumulation. These results, coupled with previous work, show that the charge collection in MOSFETs can vary strongly with channel technology and gate stack materials. Depending on the application and the opportunities for remediation, these transient responses may impose limitations on the use of some types of alternative-channel materials in space applications.

Chapter 4. Understanding Charge Collection Mechanisms in InGaAs FinFETs Using High-Speed Pulsed-Laser Transient Testing with Tunable Wavelength

4.1. Introduction

A tunable wavelength laser system and high resolution transient capture system are introduced to characterize transients in high mobility MOSFETs. The experimental configuration enables resolution of fast transient signals and new understanding of charge collection mechanisms. The channel layer is critical in the charge collection process for the InGaAs FinFETs examined here. The transient current mainly comes from the channel current, due to shunt effects and parasitic bipolar effects, instead of the junction collection. The charge amplification factor is found to be as high as 14, which makes this technology relatively sensitive to transient radiation. The peak current is inversely proportional to the device gate length. Simulations show that the parasitic bipolar effect is due to source-to-channel barrier lowering caused by hole accumulation in the source and channel. Charge deposited in the channel causes prompt current, while charge deposited below the channel causes delayed and slow current.

Pulsed-laser testing has become a valuable testing method to study SEE in devices and circuits [133], [134]. Although the charge generation mechanisms and charge profile induced by laser irradiation are different from heavy ion irradiation, laser testing provides a complementary nondestructive, convenient, and low-cost method to identify mechanisms responsible for SEE. Pulsed laser testing is generally divided into two categories: single-photon absorption (SPA) and two-photon absorption (TPA), depending on the electron-hole pair generation mechanism [109].

SPA refers to above-band gap optical excitation, where each absorbed photon generates an electron-hole pair. Due to the exponential decay of light intensity traveling through the material, the penetration depth of the laser is limited. To generate charge tracks with various depths, usually the laser wavelength is varied [135]. For SPA irradiation, however, it is often difficult or impossible to inject charge into a device, due to the presence of metal over-layers. This challenge is addressed by TPA, which is produced by irradiation with high peak power femtosecond laser pulses at sub-band gap wavelength. Electron-hole pairs are only generated in the focal region of the laser beam, where the optical field intensity is high enough to stimulate the absorption of two photons simultaneously. This enables backside irradiation, thus addressing the problem of metal over-layers [110].

Typically, the TPA laser wavelength is set to be around 1260 nm for conventional CMOS, at which the photon energy is slightly smaller than the Si band gap. However, with CMOS scaling

continuing to sub-10 nm nodes, high mobility channel materials, such as InGaAs and Ge, are likely to be introduced [12], [15]. The integration of these new materials will also necessitate other relevant materials, creating a complex multi-layer structure. There are multiple band gaps in these advanced devices compared with Si. Therefore, a single laser wavelength tuned for Si is not sufficient for characterizing SEE in these new materials. Charge generation at a wavelength of 1260 nm will lead to mixed SPA and TPA in different layers, depending on material band gaps, such as shown in [123], [136]. In studying the charge collection mechanisms in these multi-layer structure devices, it is both necessary and difficult to identify the roles of different layers. Thus a laser with tunable wavelength is helpful to inject charge primarily into a specific layer, e.g., the channel.

Time-resolved measurements are usually conducted with digital sampling oscilloscopes. For fast transients or fast edges characterization, it is desirable to have enough time resolution to resolve signals on the same timescale as the device response. The highest bandwidth oscilloscope reported is a 70 GHz superconducting sampling oscilloscope, which has sub-10 ps resolution [137]. However, this oscilloscope needs additional cooling and can only capture limited time window transients, so it is not practical for most testing. Almost all the other transient capture experiments that have been reported are conducted with oscilloscopes with bandwidths less than or approximately equal to 20 GHz [123], [136], [138]. These have limited capability to resolve fast transient signals.

In this chapter, we describe a tunable wavelength laser system that can inject charge into a specific layer in the device and capture transients with a 36 GHz bandwidth oscilloscope. We show that these new capabilities lead to enhanced insight into charge collection mechanisms in advanced devices.

4.2. Device Description

The device under test is a double-gate InGaAs FinFET. The cross-sectional and side-view schematic diagrams of the device are shown in Fig. 4.1(a) and (b), respectively. The detailed fabrication process is presented in [44]. A 0.4 μm thick $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm thick semi-insulating InP substrate. A 40 nm thick $In_{0.53}Ga_{0.47}As$ channel is grown on top of the buffer layer. The fin height is 220 nm. On top of the fin, there is a SiO_2 hard mask about 40 nm thick. A 5 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition. The thick hard

mask electrostatically decouples the top gate from the channel. As a result, this device is only controlled by the two side gates.

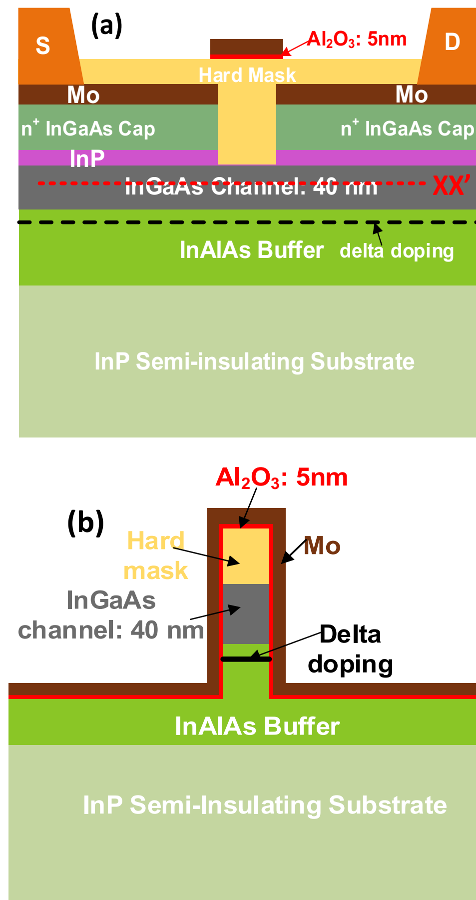

Fig. 4.1. (a) Cross-sectional and (b) side-view schematic diagrams of InGaAs double-gate FinFETs.

Fig. 4.2 (a) and (b) shows the band diagram cut through the fin along fin width and fin height direction, respectively. Along the fin width direction, the InGaAs channel and Al_2O_3 gate dielectric form a deep type I quantum-well. The barrier height is more than 2.0 eV for both electron and hole. Along the fin height direction, the InGaAs channel, InAlAs buffer and SiO_2 also form a type I quantum-well, similar to planar InGaAs quantum-well MOSFETs. Thus, carriers are effectively confined in the channel layer, making the channel layer critical to the charge collection process. In this chapter, devices with different gate lengths and fin widths are studied with a pulsed-laser at different wavelengths. There are 11 parallel fins in each tested device. For transient capture, all the devices are mounted in custom-milled metal packages with microstrip transmission lines and Precision 2.92 mm K connectors [123].

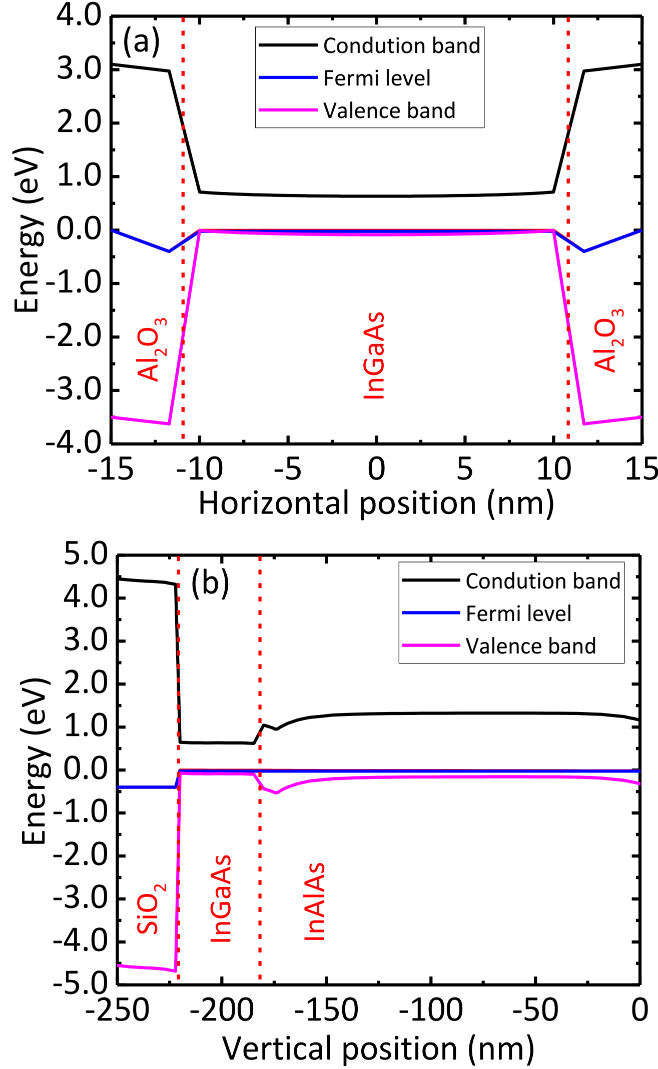

Fig. 4.2. Band diagram cut through the fin structure along (a) fin width direction and (b) fin height direction. For the band diagram, V_G=V_D=V_S=0 V.

4.3. Experimental Setup

Pulsed-laser testing experiments were performed at Vanderbilt University. The laser system setup is shown schematically in Fig. 4.3 [139]. It utilizes a titanium-sapphire (Ti/S) pumped Optical Parametric Generator (OPG). The OPG is pumped at a 1 kHz repetition rate with 1 mJ, 150 fs pulses centered at 800 nm from a chirped-pulse amplifier. The amplifier is seeded with a passively mode-locked Ti/S oscillator. The OPG uses non-linear parametric frequency conversion in a Beta Barium Borate (BBO) crystal to generate and amplify signal and idler wavelengths that are continuously tunable from ~1200 nm to ~2400 nm. Using harmonic, sum, and difference frequency-generating crystals outside the OPG, wavelengths from ~200 nm to ~10 µm can be

generated with average pulse energies varying from 1μJ/pulse to 100μJ/pulse, depending on the wavelength. A prism is used to isolate the desired wavelength from the output of the laser system. Optics currently installed on the beam line allow for component testing at wavelengths from 300 nm to 2600 nm.

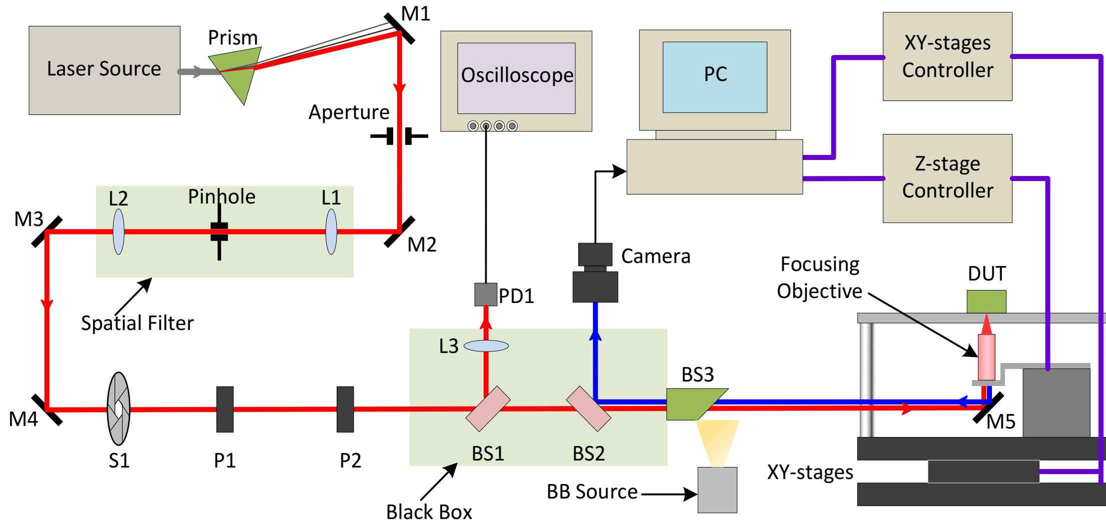

Fig. 4.3. A simplified block diagram of TPA test setup. In the figure, 'L' stands for lens, 'M' stands for mirror, 'S' stands for shutter, 'P' stands for polarizer, 'BS' stands for beam splitter, 'PD' stands for photodiode, and "BB" represents the broadband light source. The red line indicates the optical path traveled by the laser beam. The blue line indicates the reflected light that is imaged by the near infrared camera.

The selected wavelength is spatially filtered and variably attenuated using holographic wire-grid polarizers before reaching the test bench. The laser beam passes through a series of beam splitters before reaching the target. The first beam splitter diverts a fraction of the beam to a calibrated photodiode. Each pulse from the detector is captured and measured individually. Another beam splitter sends light reflected from the target to an infrared (IR) camera for imaging and positioning of the laser spot. A third splitter couples a broadband near-IR light source onto the beam axis for illuminating the target. Finally, the laser is focused through the back-side of the target using either a 50X or 100X microscope objective mounted to a customized high-precision z-stage used to change the depth at which the laser focuses inside the die.

The laser wavelengths used in this experiment are 1260 nm and 2200 nm. The photon energy and carrier generation mechanisms are listed in Table 4.1 for different materials in the device. For a wavelength of 1260 nm, charge will be generated in all of the semiconductor materials, either through SPA or TPA. In contrast, for a wavelength of 2200 nm, charge can only be generated in

the $In_{0.53}Ga_{0.47}As$ channel. No charge will be generated in $In_{0.52}Al_{0.48}As$ or InP, since the photon energy is less than half of the material band gap so that neither SPA nor TPA can take place. Therefore, charge can be generated in a specific layer, allowing the response of that specific layer to be isolated from all the surrounding layers.

Transients are captured using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36 GHz front-end bandwidth and 80 GS/s sampling rate. As mentioned above, transients of planar InGaAs quantum-well MOSFETs are also shown as captured by a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20 GS/s sampling rate for comparison. During these tests, the source was grounded, and the drain and gate biases were varied. A semiconductor parameter analyzer, HP 4156B, supplied the dc biases through Picosecond Model 5542 bias tees with 50 GHz bandwidth.

Table 4.1. Materials parameters and carrier generation mechanism at two different wavelengths

Material	Bandgap (eV)	λ=1260 nm (E=0.98 eV)	λ=2200 nm (E=0.56 eV)
$In_{0.53}Ga_{0.47}As$	0.75 eV	**SPA**/TPA	TPA
$In_{0.52}Al_{0.48}As$	1.46 eV	TPA	NONE
InP	1.35 eV	TPA	NONE

(For materials where both SPA and TPA happen, the dominant mechanism is marked as bold.)

4.4. Results and Discussions

4.4.1. System Validation

Fig. 4.4 (a) and (b) show the transients captured by the TDS6124C and LabMaster 10-36Zi-A oscilloscopes, respectively. Transients were generated by a 1260 nm laser. The rise time of the transients is very short, on the order of 100 ps. As a result, only a single data point is recorded on the rising edge for the TDS6124C oscilloscope, which has 50 ps resolution. It is hard to predict the rising edge shape based on such limited data. However, for the LabMaster 10-36Zi-A oscilloscope, the time resolution is 12.5 ps, which is short enough to resolve the rising edge. By fitting the rising edge with an exponential curve, the rise time constant is estimated to be around 39 ps. This illustrates both the benefit and the need to use a higher bandwidth system to characterize fast signals with more accuracy and precision.

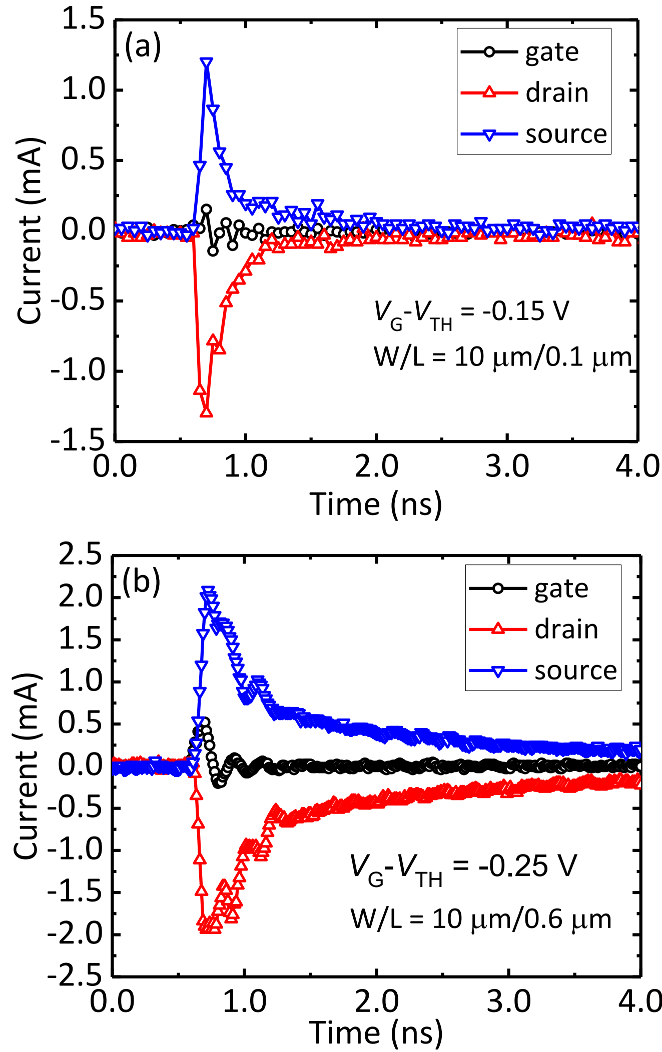

Fig. 4.4. Typical transients captured by (a) Tektronix TDS6124C oscilloscope and (b) Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope. The strike point is at the center of the device, on top of the gate. The laser wavelength used is 1260 nm. Peak currents differ as a result of different laser energies. V_D=0.5 V.

Another feature of the transients shown in Fig. 4.4 (b) is the oscillation signal appearing in the transients. The oscillation period is 0.2 ns. There are many possible reasons for this oscillation, including impedance mismatch and extrinsic RLC oscillation associated with bond wires [126]. Since the bond wire used for this device is relatively long, a few mm, here the oscillation is likely related to circuit RLC parameters [126].

Charge collection in InGaAs FinFET devices is compared with two different wavelengths, 1260 nm and 2200 nm, in Fig. 4.5 (a) and (b). Two typical transients are shown, for a device biased in the ON state. The difference in the transient magnitude is due to the laser energy difference at the two wavelengths. The rising edge is well resolved and the relevant time constant is about 40 ps,

similar to the planar device. The oscillation is still present in the gate transients, with a period of 0.15 ns. This likely results from the shorter bond wires used in the FinFET, as compared with the planar device.

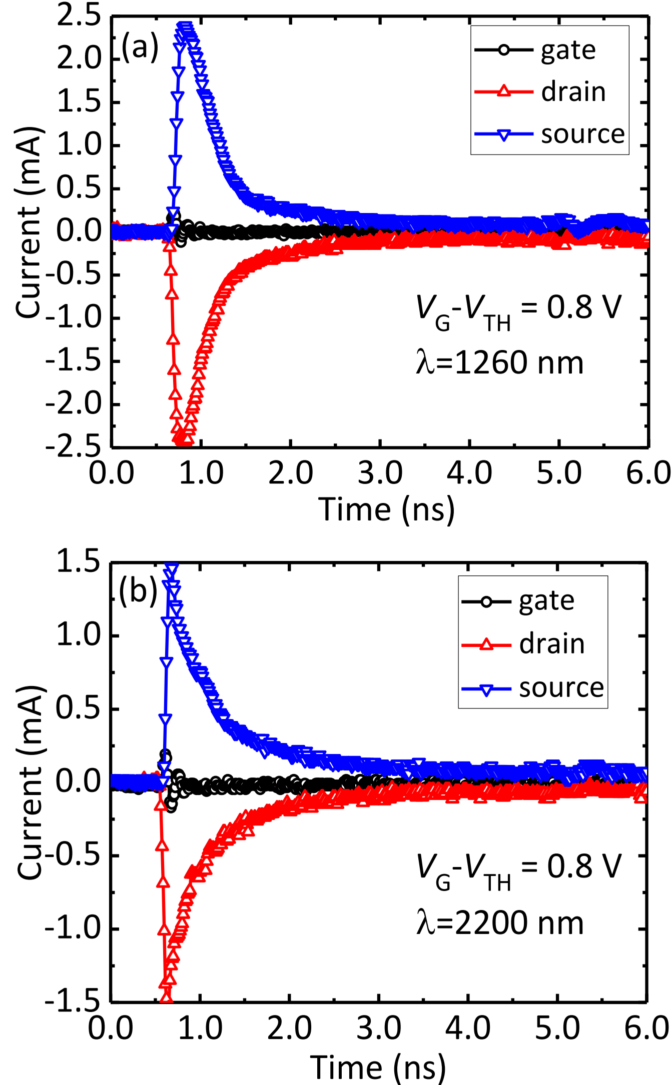

Fig. 4.5. Typical transients captured by Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope at (a) λ=1260 nm and (b) λ=2200 nm at V_G-V_{TH}=0.8 V, V_D=0.5 V. The laser strike is at the center of the gate. W_{FIN}=20 nm.

4.4.2. Charge collection in InGaAs FinFETs

The transient shapes at the two wavelengths are very similar, indicating that the channel layer is critical to the charge collection process. The transient fall times are faster at a wavelength of 2200 nm than at 1260 nm. The time constants obtained by fitting the transients with double exponentials at 2200 nm, 0.14 ns and 0.66 ns are less than half of those at 1260 nm, 0.28 ns and

1.50 ns. This is probably because charges are only generated in the channel at 2200 nm, so they can quickly get collected.

Fig. 4.6 (a) and (b) show the drain current transients at different gate biases and drain biases, respectively. The transient peak does not vary with the gate bias, in contrast to the planar III-V MOSFETs, shown in chapter Chapter 3 and Chapter 2. This is because the device is controlled by the two side gates, which has little effect on the substrate below the fin. The tail current increases 53% (evaluated at 2.0 ns) with the gate bias, which is consistent with the response of planar III-V MOSFETs. In contrast, the drain current is significantly dependent on the applied drain bias. The peak drain current increases approximately 5X when V_D changes from 0.1 V to 0.5 V. This is consistent with the increase of the channel electric field with increasing drain bias.

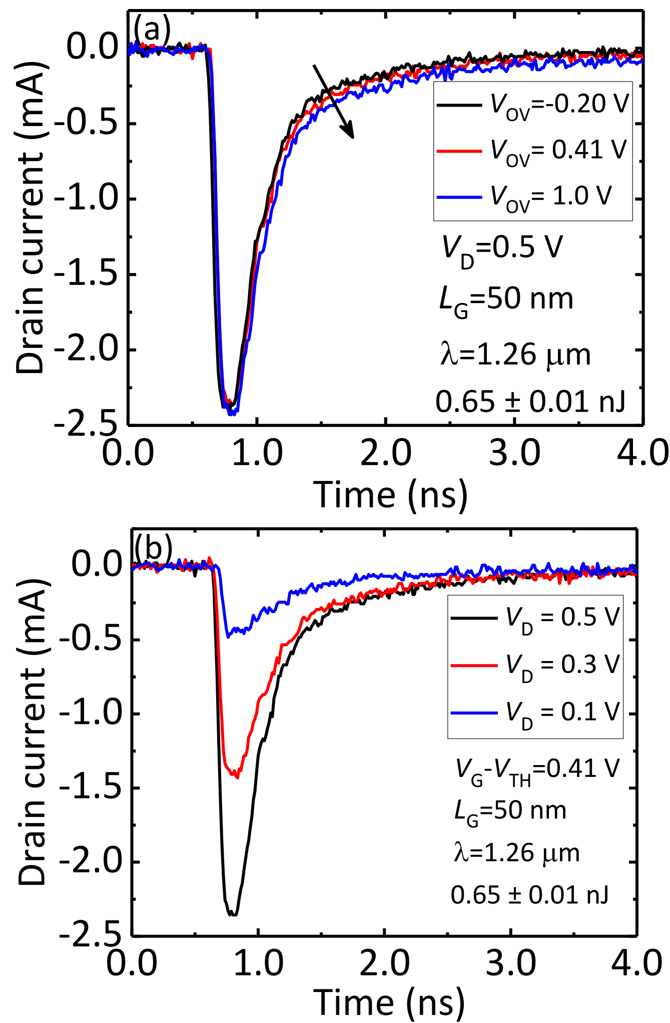

Fig. 4.6. Drain current transients at different (a) gate bias, and (b) drain bias. The laser strike is at the center of the gate. W_{FIN}=20 nm.

Fig. 4.7 (a) shows the source and drain current transients at different laser strike points along a line scan. The source transients are approximately the inverse of the drain transients (similar magnitude, opposite polarity), no matter whether the strike point is on the source side or drain side. This suggests that the transient current mainly comes from the channel current.

There is little contribution from the junction collection, which is different from traditional Si devices [54]. In addition, the transient current decreases more rapidly in the source side than the drain side, which is related to the higher electric field in the drain region than the source region. This is also observed in the planar III-V MOSFETs, as shown in chapter Chapter 3 and Chapter 2.

The comparison between the channel current and junction current can also be seen in Fig. 4.7 (b), which shows the peak drain current along a line scan at different gate biases. Two groups of curves are shown, which correspond to two bias conditions V_S= 0 V and $V_S = V_D$. The case with equal source and drain bias represents junction collection, since there is no electric field along the channel, while the grounded source represents the situation where the channel current makes a significant contribution. The drain current is almost zero on the source side with $V_S = V_D$. This is because the source collects most of the charge at the source side. With the junction collection, the peak drain current is very small, less than 0.3 mA. However, the channel current is much higher, suggesting that the channel current contributes the most significant charge.

The mechanisms of channel current are also investigated. At the center of the gate, the peak drain current is maximum. This is similar to the ion-shunt mechanism observed in Si devices [140], [141]. When an ion track size is comparable to the device gate length, the high density of electron-hole pairs will short the source and drain, contributing to a large prompt current. Similarly, in our laser system, the laser spot size is approximately 1.2 μm, much larger than the gate length. Therefore, it should be expected that the peak drain current is maximum around the gate center. The shunt mechanism alone, however, cannot explain the channel current when the laser strikes away from the gate, for example x = ±5 μm. This increase is due to parasitic bipolar effects, as illustrated in section 1.3.2.3, which become active when radiation-induced holes accumulate beneath the gate, perturbing the local electrostatic potential, lowering the source to channel barrier, and inducing a source-to-drain current pathway. This will be further illustrated below by TCAD simulations.

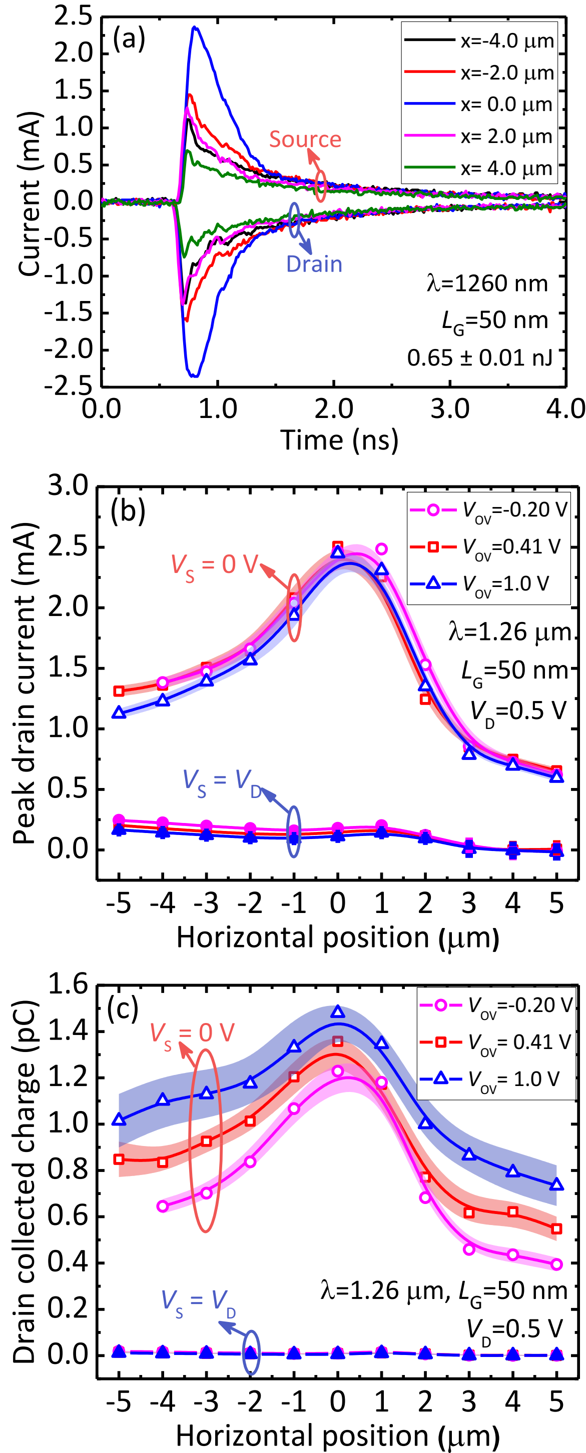

Fig. 4.7. (a) Source and drain current transients at different laser strike positions along a line scan. (b) and (c) show the peak drain current and drain collected charge, respectively, along a line scan at different gate biases. Here the center of the gate is taken as x=0 μm. The negative x coordinate represents the drain side and the positive x coordinate represents the source side. The laser wavelength λ=1260 nm. The shadow in (b) and (c) represents the standard deviation among the 50 transients recorded at each position. W_{FIN}=20 nm.

The collected charge along a line scan is shown in Fig. 4.7 (c). The charge is obtained by integrating the captured transients within a time window of 30 ns. The collected charge increases with the gate bias when the source is grounded. This is because the tail current increases with gate bias, as shown in Fig. 4.6 (a). When integrated, the tail current contributes a significant amount of charge. In comparison, the junction-collected charge is much smaller, around 10 fC. However, there is no clear evidence that the deposited charge correlates with the junction collected charge, when the deposited charges are distributed in the channel, buffer, and substrate, as shown in Table I. Therefore, no quantitative conclusions can be drawn. The spatial dependence of the collected charge is very different from the Si bulk FinFET [142]. For Si bulk FinFET, the collected charge increases toward the drain region and saturates as the strike location moves deep into the drain [142]. This is because that most of the collected charge is due to the drain junction collection for the Si bulk FinFET. There is very small contribution from the channel conduction. However, for the InGaAs FinFET device, most of the collected charge comes from the channel current, as illustrated in Fig. 4.7. The most sensitive region is the gate for the InGaAs FinFET.

However, for the laser wavelength λ=2200 nm, charge is generated only in the channel layer, similar to SOI technology. It has been shown in Si SOI technology that the deposited charge can be empirically estimated from the source/drain transients with the source and drain at the same bias [143]. In our case, this methodology is also applicable at λ=2200 nm.

Fig. 4.8 (a) and (b) show the peak drain current and drain collected charge, similar to Fig. 4.7 (b) and (c), at different drain biases for λ=2200 nm. Both the peak drain current and the drain collected charge increase with the drain bias, as illustrated also in Fig. 4.6 (b). The current gain is approximately 6 for V_D=0.5 V at x=0 μm. In addition, the deposited charge is twice the drain collected charge at equal source and drain bias, about 60 fC at x=0 μm. This corresponds to charge enhancement factors of 14, 10, and 4 for V_D = 0.5, 0.3, and 0.1 V, respectively. Similar charge enhancement factors have also been reported in other types of III-V FETs [84], [85]. These results demonstrate the advantage of a tunable wavelength laser system, which allows quantitative analysis of these important device responses.

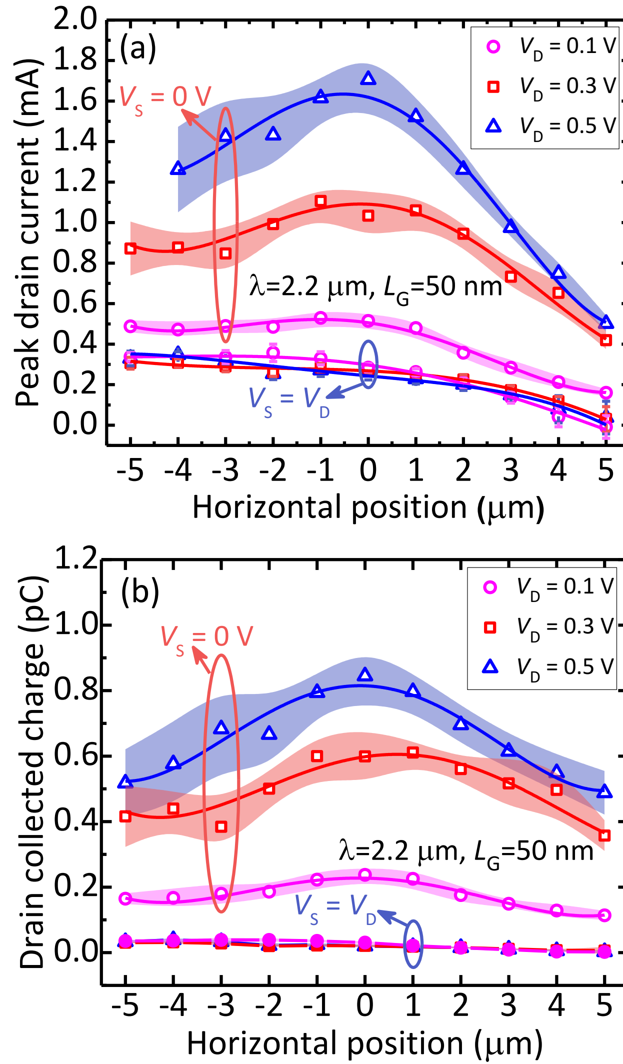

Fig. 4.8. (a) and (b) show the peak drain current and drain collected charge, respectively, along a line scan at different drain biases. The negative x coordinate represents the drain side and the positive x coordinate represents the source side. The laser wavelength λ=2200 nm. The shadow represents the standard deviation among the 50 transients recorded at each position. V_G-V_{TH}=0.5 V. W_{FIN}=20 nm.

Parasitic bipolar effects are also observed in the excess OFF-state leakage current in InGaAs quantum-well MOSFETs; the gain is typically inversely proportional to the gate length [144]. Fig. 4.9 shows the peak drain current along a line scan for different gate lengths. Two groups of curves are shown, one with source grounded and the other with equal source and drain voltages. The peak drain current decreases with gate length, as expected. For L_G = 420 nm, the peak drain currents are approximately equal in the drain side for the two bias conditions, suggesting that the parasitic bipolar action is fully suppressed in the longer channel device. In addition, the sensitive area

broadens with decreasing gate length. These results imply that sensitivity to transient radiation effects may increase in these types of devices with technology scaling, which is important to understand for space applications.

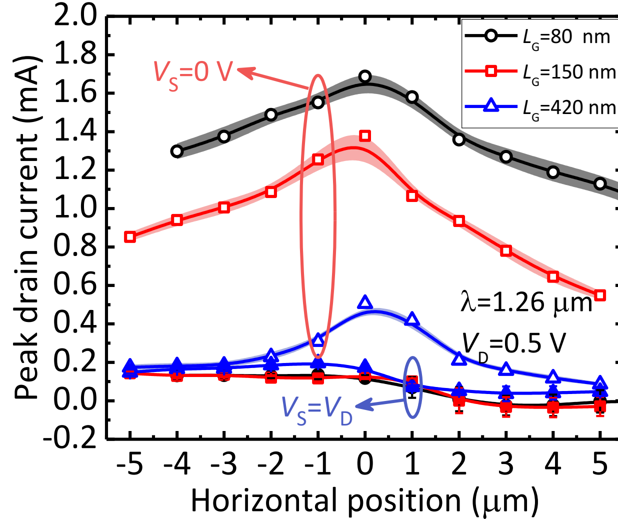

Fig. 4.9. Peak drain current along a line scan for different gate lengths. The laser wavelength λ=1260 nm. The shadow represents the standard deviation among the 50 transients recorded at each position. V_G-V_{TH}=0 V. W_{FIN}=30 nm.

The peak drain current dependence on laser energy is investigated in Fig. 4.10. The peak drain current increases with the laser pulse energy, with a relationship of approximately $I_{DP} \propto E^{0.5}$, where E is the laser pulse energy and I_{DP} is the peak drain current. This sublinear dependence may be related to the complex charge injection profile at λ = 1260 nm on the one hand, but may also be related with the parasitic bipolar effect which induces the channel current. Further experiments are needed, for example laser energy dependence at λ = 2220 nm, to elucidate the dependence.

An area mapping of the sensitive region is also performed. The results are shown in Fig. 4.11 (a) and (b) for L_G = 600 nm and L_G = 50 nm, respectively. There is amplification only around the gate region for L_G = 600 nm, consistent with Fig. 4.9. In the drain region, only the drain junction collects charge; while in the source region, the charge collection is greatly suppressed. However, for L_G = 50 nm, the sensitive region is much larger, extending deep into the source and drain regions.

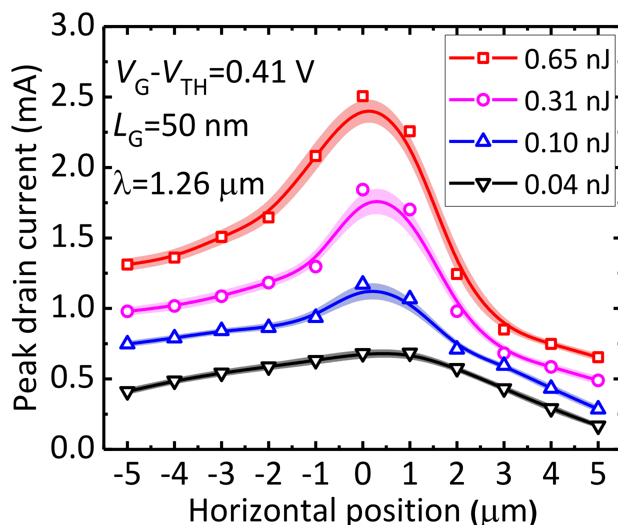

Fig. 4.10. Peak drain current along a line scan for different laser pulse energies. The shadow represents the standard deviation among the 50 transients recorded at each position. W_{FIN}=20 nm.

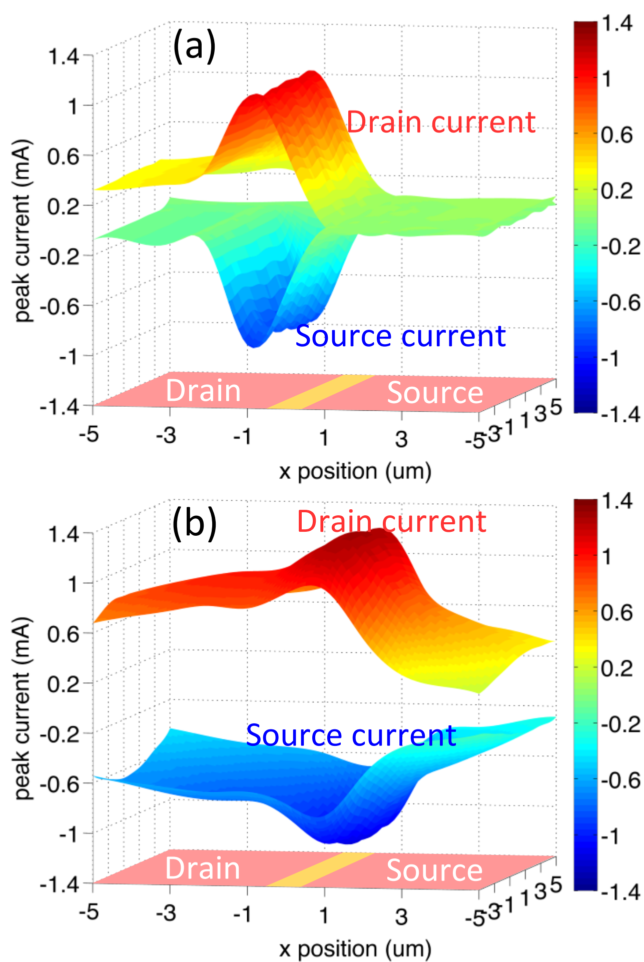

Fig. 4.11. Peak source and drain current area map for (a) L_G=600 nm and (b) L_G=50 nm. The source current is the top and the drain current is at the bottom. For the area scan, the origin is chosen to be the center of the gate. W_{FIN}=20 nm.

4.4.3. TCAD Simulations

To gain more understanding of the above charge collection processes, 3D TCAD simulations are performed with Sentaurus TCAD tools. Fig. 4.12 shows the TCAD model of the device. The simulated device has a gate length of 50 nm. For the simulation, charges caused by an oxygen ion strike are introduced into the device at different locations. The injected charge has a Gaussian distribution in both space and time. The center of the strike is 1.0 ns and the characteristic length of the Gaussian distribution is 50 nm. The amount of deposited charge is 76 fC/μm for 8 μm. Although the charge distribution used in simulation is different from the laser irradiation, these results provide qualitative understanding of the charge collection process.

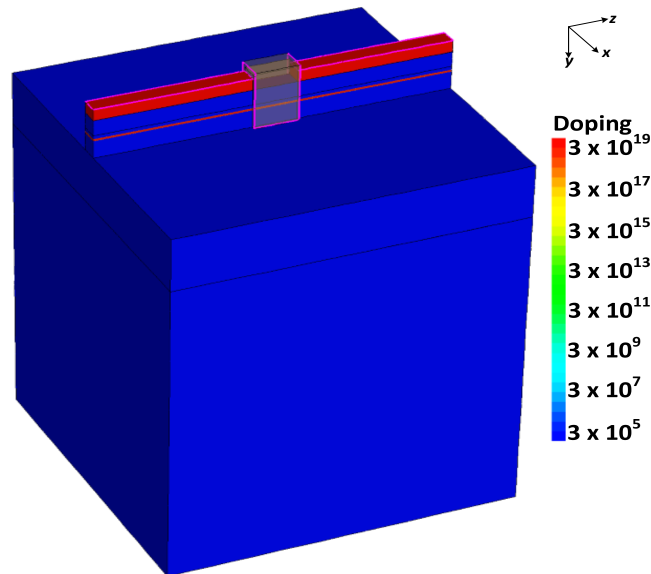

Fig. 4.12. 3D TCAD model of InGaAs double-gate FinFET device. L_G=50 nm, W_{FIN}=20 nm.

Fig. 4.13 shows the electron density evolution as a function of time due to an ion strike at a cut plane of x=0 μm. It shows that a very high density of electron/hole pairs is generated around the strike location. After the strike, the electron/hole pairs quickly diffuse away and spread out. The carriers in the substrate do not directly lead to transient currents, however, as shown in the simulation below, they can move to the channel layer and induce source-to-drain current. The deeper the charge generation in the substrate, the longer it takes for the carriers to move into the channel. Therefore, most of the carriers generated in the substrate contribute to the transient tails.

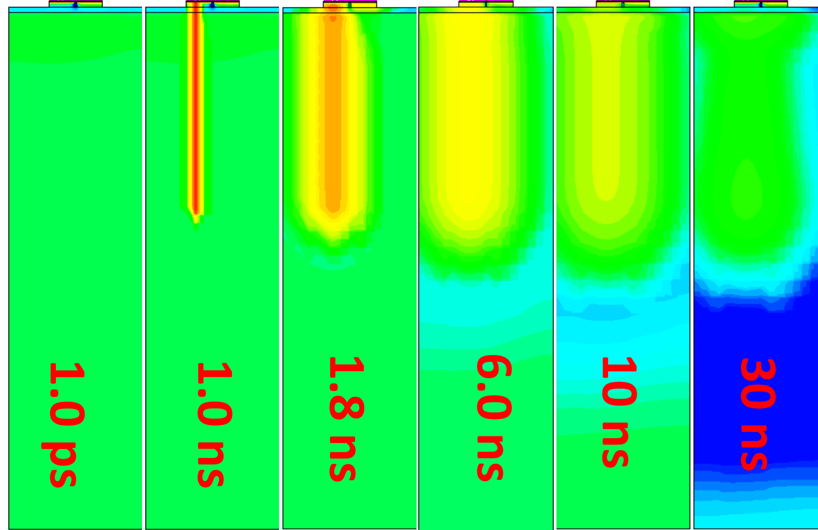

Fig. 4.13. Electron density evolution as a function of time at a cut plane of x=0 μm after an ion strike. 1.0 ps represents the pre-strike condition and 1.0 ns represents the center of the strike.

To illustrate the parasitic bipolar effect, Fig. 4.14 (a) shows the hole density inside the fin at different times for charge injection at z = 0.63 μm, in the drain side. Following the charge injection at 1.0 ns, a large number of electrons and holes are collected in the InGaAs channel within 100 ps, due to the type I heterostructure quantum-well. The hole density remains high for a long time and does not recover to the steady state value even at 30 ns. The accumulated holes close to the source and channel reduce the barrier between source and channel, which can cause additional electrons to be injected from the source and collected by the drain [84], [86].

This is further illustrated in Fig. 4.14 (b), which shows the conduction-band time-evolution along a horizontal cut line, XX', as defined in Fig. 4.1 (a), from the source to drain. The barrier between the source and channel is as high as 0.6 eV before charge injection. However, 200 ps after the strike, the barrier is temporarily removed so that electrons can flow from source to drain. This causes the channel current observed in the experiment. The barrier only partially recovers to 0.1 eV after 28 ns, implying that the perturbation can last for a long time, probably due to the highly confined FinFET structure. This long lasting transient can increase the sensitivity to radiation.

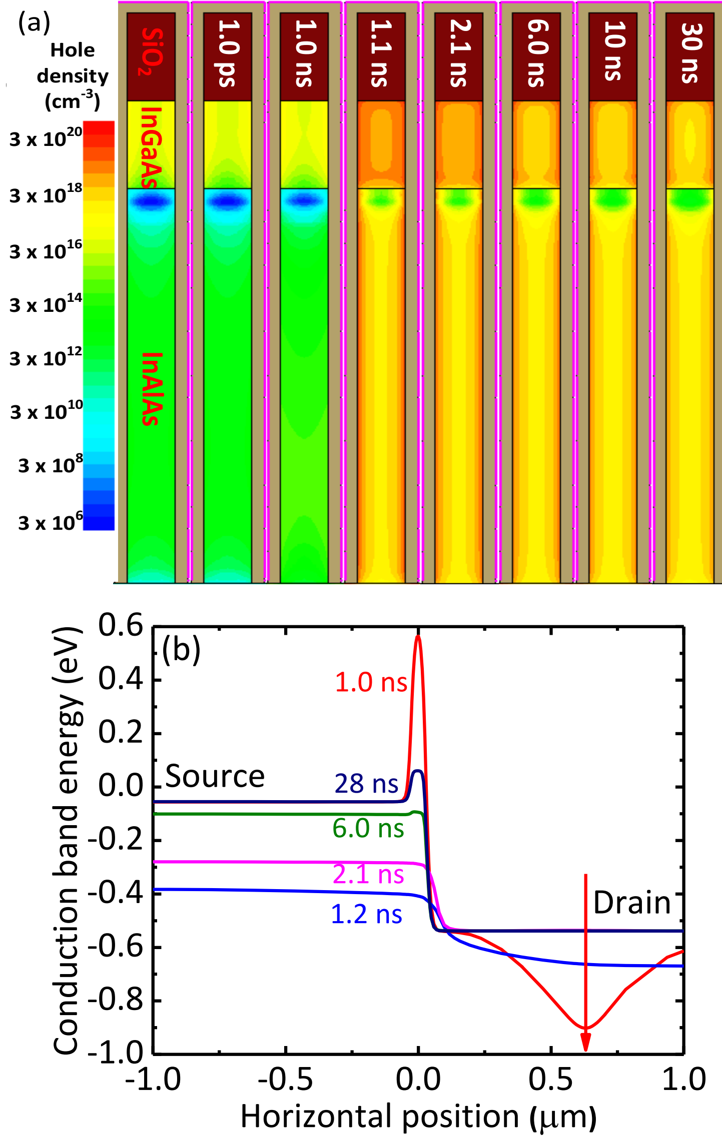

Fig. 4.14. (a) Hole density inside the fin structure at different times. Shown is a cut plane of the device at z=0 μm, the center of the gate. There are three layers in the fin structure, the top SiO_2, the middle InGaAs channel and the bottom InAlAs buffer. (b) Conduction band along a horizontal cut line, XX' shown in Fig. 4.1 (a), from source to drain. V_G=-0.6 V, V_D=0.5 V, V_S=0 V. The red arrow indicates the location of charge injection.

To understand the role of different layers in the charge collection process, Fig. 4.15 (b) shows the simulated drain current transients for different charge injection volumes, as schematically shown in Fig. 4.15 (a). The current is maximum for the 'full' case (defined in the figure caption), where the charge is injected from the top surface of the device and extends 8 μm. This result is as expected since the charge injection for the other cases is only a segment of the 'full' condition. For

charge injection only in the channel layer, the current increases promptly but also decays quickly. Thus, the charge deposited in the channel layer will mainly be promptly collected.

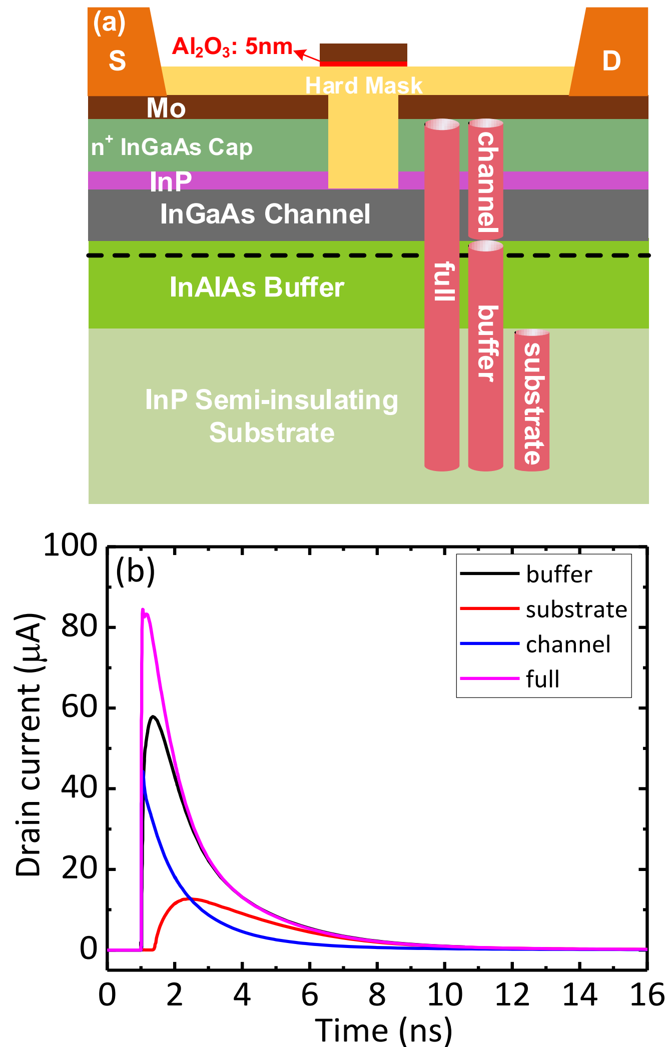

Fig. 4.15. (a) Different charge injection volumes in the simulation. (b) Drain current transients as a function of time for these areas. Here 'full' represents charge injection from the top surface of the device and extends 8 μm, 'channel' represents charge injection in the channel layer only, 'buffer' represents charge injection starting from the buffer layer and extending 7.9 μm, and 'substrate' represents charge injection starting from the substrate. The charge injection profiles in the other three conditions are just segments of the 'full' condition. Here different charge injection cases are displaced from each other for clear demonstration. In the simulation they overlap; that is, the charge is injected at the same point when projected into the horizontal plane.

For the charge injection starting from the buffer layer, the transient peak is delayed 0.3 ns compared with the 'channel' case. This delay is caused by the time required for the generated electrons and holes to move to the channel. The current almost overlaps with the 'full' case after

2.0 ns, suggesting that the slow portion comes from the deposited charge below the channel layer. This is different from the diffusion process observed in Si devices [54], since the current comes from the channel current caused by parasitic bipolar effects. The current for the 'full' case is approximately equal to the sum of the 'channel' and 'buffer' cases. For the charge injection in the substrate, the transient rises slowly and the peak is delayed 1 ns compared with the 'buffer' case because of the larger distance for carriers to diffuse into the channel layer. After 6.0 ns, the current overlaps with the 'full' case, indicating that the charge deposited in the substrate mainly contributes to the tail currents.

Drain current transients due to strikes at different locations from source to drain are shown in Fig. 4.16. The position dependence is similar to Fig. 4.7 (a); the current decreases as the strike location moves away from the center of the gate.

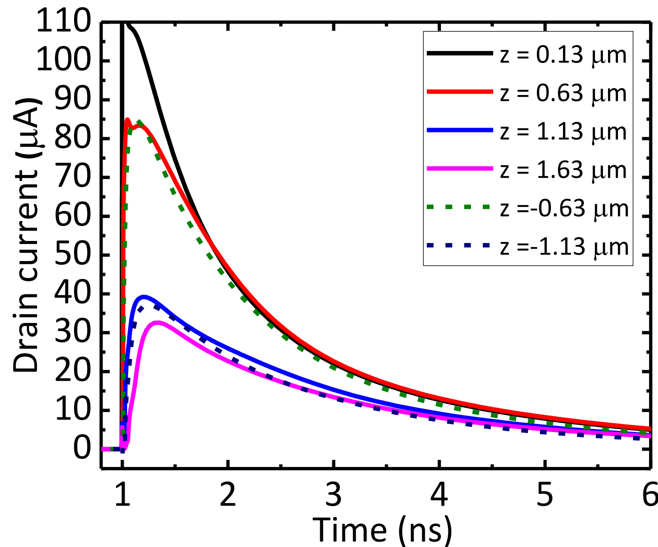

Fig. 4.16. Drain current transients as a function of time for different strike locations. Here *z*=0 is at the center of the gate, the positive z coordinate is at the drain side, and the negative z coordinate is at the source side. The solid curves represent strikes in the drain side while the dashed curves represent strikes in the source side.

4.5. Conclusion

A tunable wavelength laser system and high resolution transient capture system are introduced for high mobility MOSFETs. The system has high time resolution, and transient features such as fast edges and oscillations are well resolved. The tunable wavelength laser provides a method to generate charge only in a specific layer of interest, usually the channel layer, since the lowest band gap typically occurs in the channel of high mobility MOSFETs. This enables the response of the

channel layer to be distinguished from that of the surrounding layers, providing a valuable tool to understand charge collection mechanisms in advanced devices.

The transient current in InGaAs double-gate FinFET device mostly comes from the channel current, instead of junction collection. The channel current is attributed to the shunt effect around the gate and parasitic bipolar effects. Charge amplification factors as high as 14 are found. The tunable wavelength laser system allows empirically quantitative analysis of the results. In addition, parasitic bipolar effects are shown to be inversely proportional to the device gate length, making scaled devices highly sensitive to radiation.

From TCAD simulations, it is found that the parasitic bipolar effect in these devices is due primarily to radiation-generated holes accumulating in the source and channel, which reduce the source to channel barrier and cause additional electrons to be injected from the source and collected by the drain. Further simulations also show that the charge deposited in the channel layer contributes to the prompt current, while the charge deposited in the buffer layer contributes to a delayed and longer-lasting current. The channel layer is critical in determining the charge collection. Therefore, considering both the geometrical footprint and the charge amplification, the two factors compete with each other in determining the sensitivity of InGaAs FinFETs to single event effects. Hence, this chapter presents important and early insights into charge collection mechanisms in InGaAs FinFETs. Further circuit level analysis will be needed to determine the ultimate sensitivity of this technology, for eventual space application.

Chapter 5. Gate Bias and Geometry Dependence of Total-Ionizing-Dose Effects in InGaAs Quantum-Well MOSFETs

5.1. Introduction

The effects of total-ionizing-dose irradiation are investigated in HfO_2/InGaAs quantum-well MOSFETs. Radiation-induced hole trapping is higher for irradiation under positive gate bias than under negative gate bias. Electrical stress-induced electron trapping compensates radiation-induced hole trapping during positive gate-bias irradiation. Stress-induced hole trapping adds to the effects of radiation-induced hole trapping under negative gate bias. Radiation-induced charge trapping increases with the channel length.

As mentioned in section 1.1, the oxide/III-V interface is far from perfect. There is a high density of defect states at the interface and in the bulk of the oxide. These defects will cause positive bias temperature instability, especially in InGaAs MOSFETs, when electrically stressed with positive gate bias [145], [146]. For example, Fig. 5.1 (a) and (b) show the threshold voltage shift and degradation of peak transconductance, respectively, when stressed at different gate biases [145]. These results show significant degradation of device performance. Hence, it is important to separate the TID response from effects produced by electrical bias in these structures. On the other hand, TID effects in III-V MOSFETs have been introduced in section 1.3.1. But those studies focus on devices with thick gate oxide, around 8 nm, which is impractical for advanced technology nodes. In this work, we investigate total-ionizing-dose (TID) effects in InGaAs quantum-well MOSFETs with a thin (physical thickness of 2.5 nm) HfO_2 gate dielectric, which is more relevant for future CMOS applications.

5.2. Device Description and Experimental Setup

The devices tested are very similar to those tested in chapter 3, except for the difference of oxide thickness and InGaAs channel thickness. The schematic is shown in Fig. 5.2 (a) (not drawn to scale). A 0.4 μm thick $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm thick semi-insulating InP substrate. A 5 nm thick $In_{0.7}Ga_{0.3}As$ channel is grown on top of the buffer layer. A silicon delta doping layer (*n*-type) in the buffer just below the channel is used to enhance the channel electron density. 2.5 nm HfO_2 is deposited by atomic layer deposition on top of the channel. The device is mesa isolated instead of using oxide isolation, which means that there should not be a leakage current increase caused by hole trapping in the field oxide. Fig. 5.2 (b) shows the measured capacitance from 300 kHz to 5 MHz. The capacitance equivalent thickness (CET) in these devices

is approximately 1.7 nm. The vertical energy band alignment through the gate is shown in Fig. 3.2. The channel, the buffer, and the gate dielectric form a type-I heterostructure.

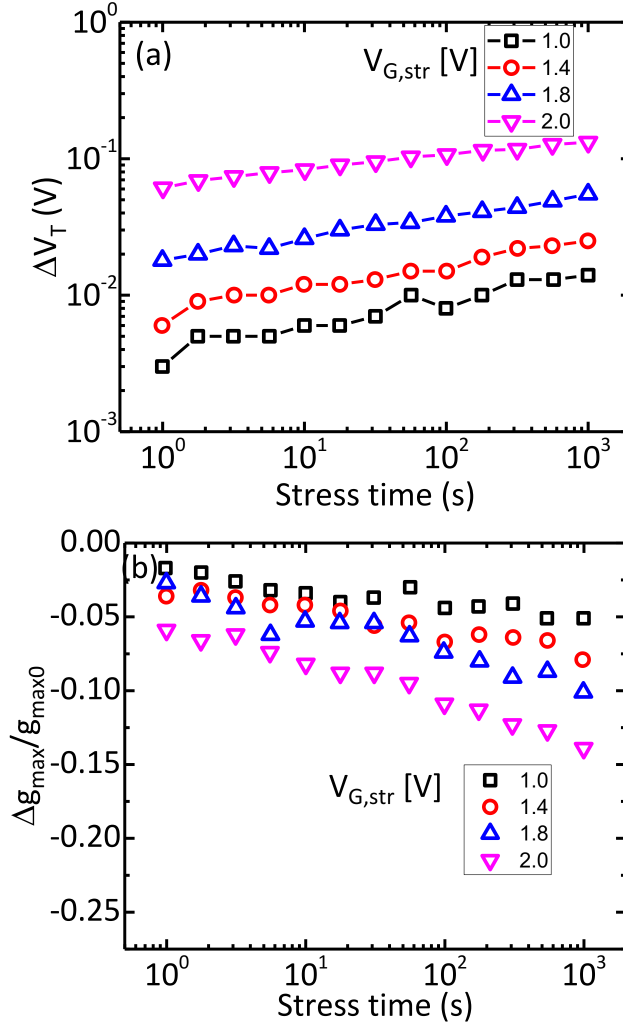

Fig. 5.1. Time evolution of threshold voltage shift and peak transconductance degradation for different $V_{G,str}$ [145].

The irradiation is performed in a 10-keV ARACOR X-ray source at a dose rate of 31.5 krad(SiO_2)/min at room temperature. Irradiations and stresses were performed with gate voltages (V_{GS}) of +1.0 V or -1.0 V, with all the other terminals grounded. All the tested devices have an initial threshold voltage of approximately 0.1 V. There is a relatively high density of pre-existing traps in the gate oxide of these devices, which cause charge trapping due to electrical stress. To account for this, the electrical stress-induced degradation without irradiation is also measured at biases and times comparable to those used in the irradiation experiments. Current-voltage (I-V) characteristics are measured using an Agilent 4156 parameter analyzer. Devices with three different channel lengths are studied. At least three devices of each channel length are tested for

each bias condition with and without exposure to X-ray irradiation. After irradiation, the devices are annealed with all terminals grounded at room temperature and I-V characteristics are re-measured after different annealing times.

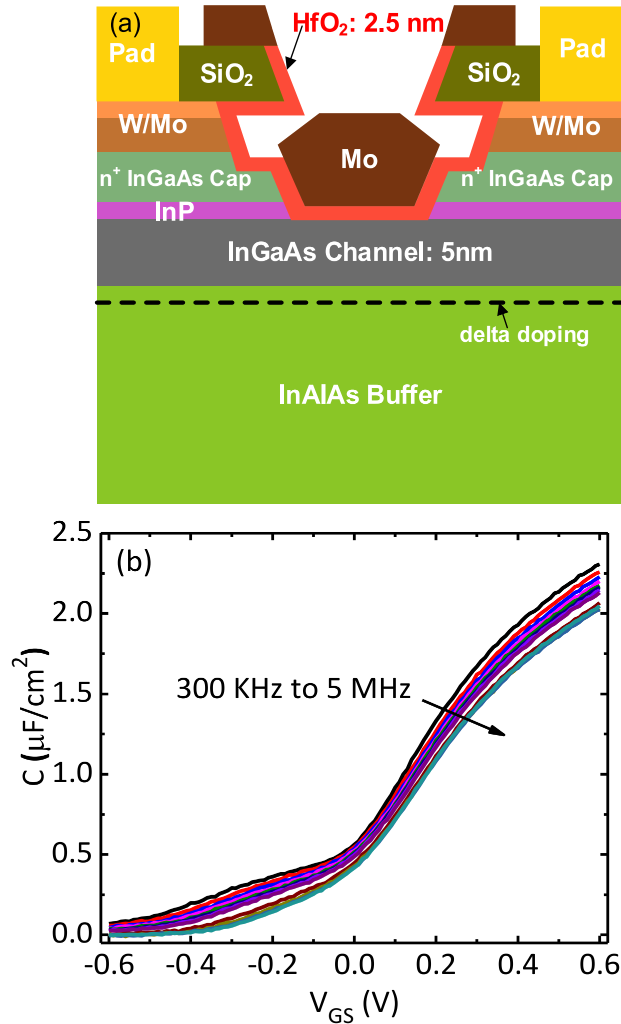

Fig. 5.2. (a) Schematic cross section of the device under test (not drawn to scale); (b) measured capacitance as a function of frequency from 300 kHz to 5 MHz. The arrow indicates the direction of increasing frequency. The tested device has a dimension of W/L = 10 μm/2 μm.

5.3. Results and Discussions

Fig. 5.3 (a) and (b) show I_D (drain current) vs. V_{GS} and g_m (transconductance) vs. V_{GS} measured with V_{DS} = 50 mV as a function of dose for devices biased at V_{GS} = +1.0 V and V_{GS} = -1.0 V, respectively, during irradiation. The threshold voltage shifts positively for V_{GS} = +1.0 V, indicating net electron trapping during positive-bias irradiation. But for V_{GS} = -1.0 V, the threshold voltage shifts negatively, suggesting net hole trapping. For both conditions, the devices have an excellent

ON/OFF ratio, above 10^4 after a total dose of 2 Mrad(SiO_2), indicating excellent gate control. Due to variations among devices, the leakage currents are at different levels for different devices. The leakage current mechanisms have been illustrated in [144].

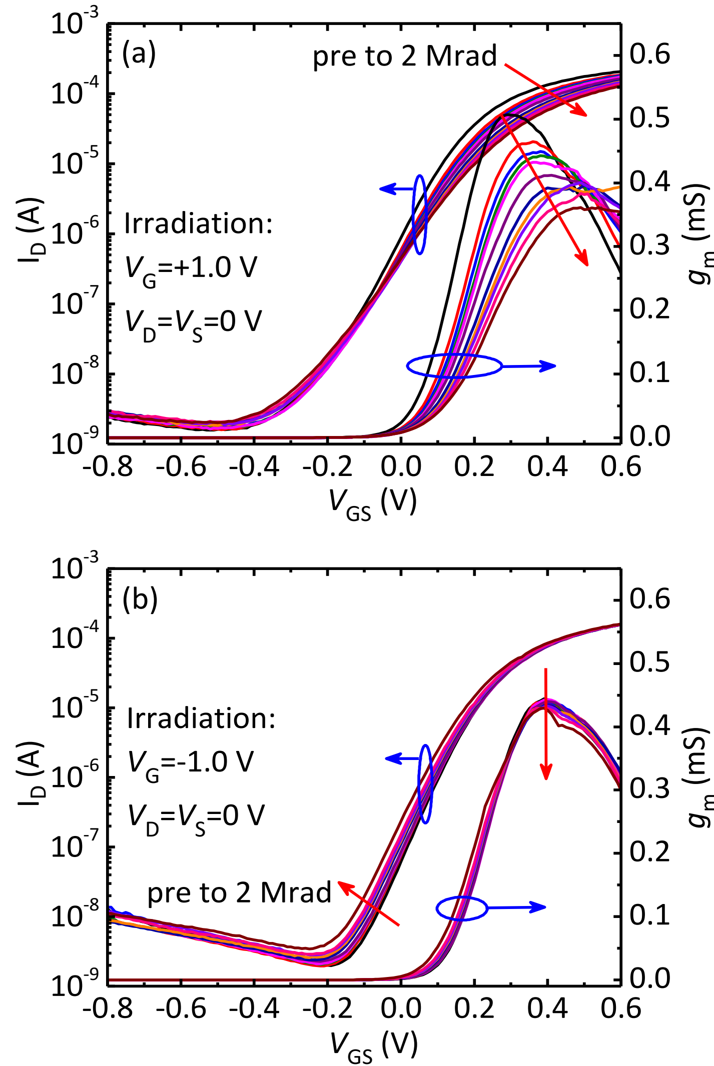

Fig. 5.3. I_D versus V_{GS} (left) and g_m versus V_{GS} (right) at different irradiation doses for a device with dimensions of W/L = 10 μm/2 μm at (a) V_{GS} = +1.0 V and (b) V_{GS} = -1.0 V during irradiation. Measurements are made with V_{DS} = 50 mV. The red arrow indicates the direction of increasing dose.

Fig. 5.4 (a) and (b) shows the subthreshold swing (SS) and normalized peak transconductance, extracted from Fig. 5.3, as a function of total dose and anneal time for V_{GS} = +1.0 V and V_{GS} = -1.0 V irradiation bias conditions, respectively. The average SS increases approximately 40 mV/decade at V_{GS} = +1.0 V, which would correspond to the generation of 2.5×10^{13} cm^{-2}eV^{-1} interface traps, if interface traps were solely responsible for the increase of SS. The SS increase at

V_{GS} = -1.0 V is half that of positive biased irradiation. Similarly, the peak-g_m degradation at V_{GS} = -1.0 V (10%) is less than half of V_{GS} = +1.0 V (30%). Fig. 5.5 (a) and (b) show the correlation between peak-transconductance degradation and threshold voltage shift and subthreshold swing degradation, respectively. That the peak-g_m degradation correlates well with the subthreshold swing increase suggests that there are interface and/or near interface oxide (border) traps generated during irradiation [146]. The partial recovery in SS and peak-g_m during annealing is likely related to electron/hole detrapping from the border traps. Some of the remaining degradation may be due to interface traps, but a significant percentage may also be due to border traps.

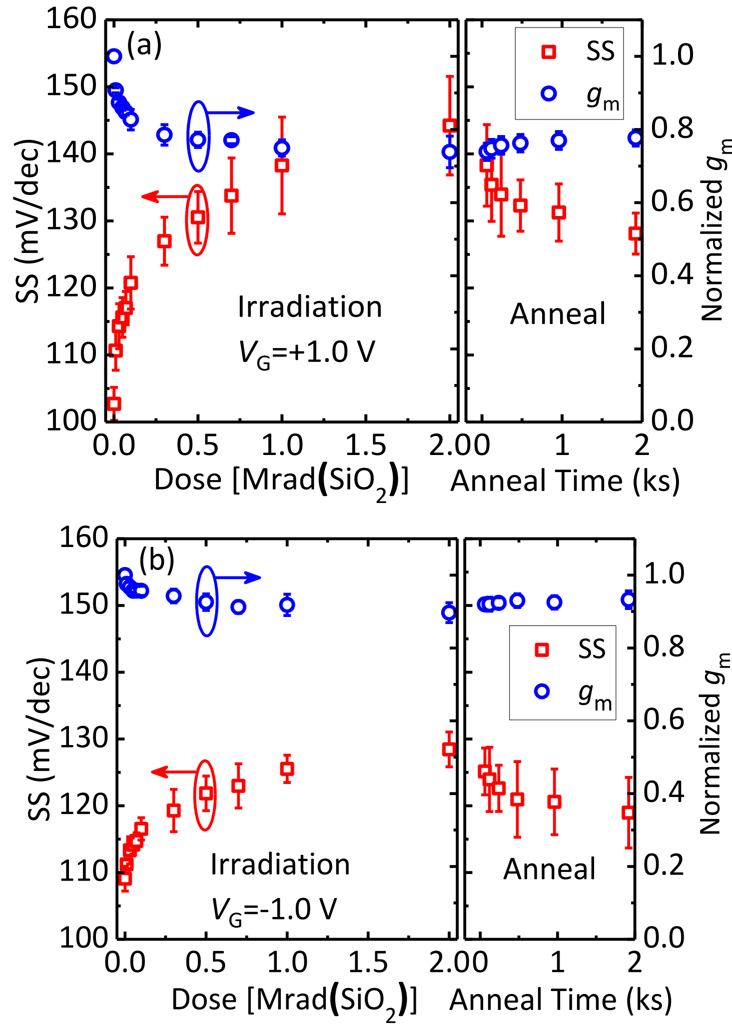

Fig. 5.4. Subthreshold swing (left) and normalized peak transconductance (right) as a function of irradiation dose and annealing time for (a) V_{GS} = +1.0 V and (b) V_{GS} = -1.0 V. The normalization is based on the pre-irradiation peak transconductance. The error bars represent standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV. All the tested devices have dimensions of W/L = 10 μm/2 μm.

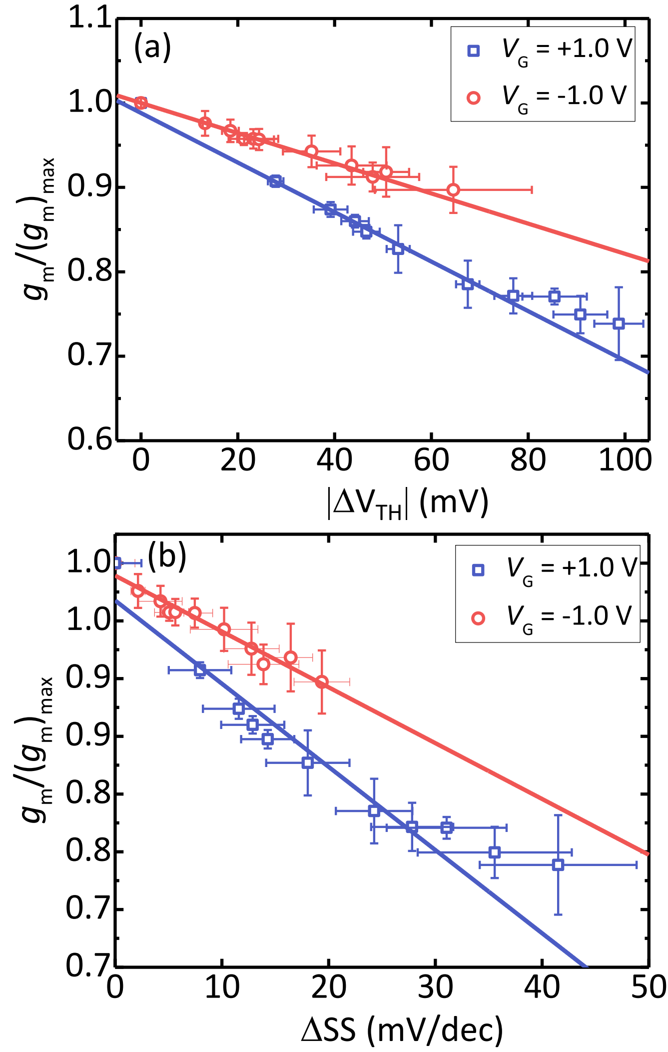

Fig. 5.5. Peak transconductance degradation correlation with (a) threshold voltage shift and (b) subthreshold swing degradation. The approximately linear relationship suggests good correlation among all the degradations of device characteristics.

The degradation under the two bias conditions in Fig. 5.3 is quite different. At V_{GS} = +1.0 V, the ON current (at V_{GS} -V_{TH} = 0.5 V) decreases by 26% after 2 Mrad(SiO_2) exposure, and the subthreshold current increases 6% (at V_{GS} = -0.2 V). However, for V_{GS} = -1.0 V, the ON current decreases 4% and the subthreshold current increases by 2x. These differences occur because devices irradiated under positive bias capture tunneling electrons very near the interface during irradiation. These more than offset the trapped positive charge, and efficiently scatter the channel carriers [147], [148], [149], [150]. In contrast, the irradiation- and tunnel-injected holes captured under negative-bias irradiation do not scatter the channel electrons as efficiently.

To separate the pure TID response from the combined response, the bias-induced degradation was separately measured at biases and times comparable to those used during irradiation. Fig. 5.6 (a) and (b) show the threshold voltage shift as a function of equivalent dose for (1) TID irradiation, (2) bias only, and (3) the pure TID response, adjusted for charge trapping due to the simultaneous bias-stress at V_{GS} = +1.0 V and V_{GS} = -1.0 V, respectively. The adjustment is made by subtracting (2) bias only results from (1) TID irradiation results. For the bias-only condition at V_{GS} = +1.0 V, there is a positive threshold-voltage shift of about 200 mV, indicating an areal density of 7.5×10^{12} cm^{-2} trapped electrons when projected to the interface. These trapped charges cause Coulomb scattering to channel carriers and decrease the carrier mobility, as discussed above. However, for V_{GS} = -1.0 V, there is a negligible negative threshold voltage shift (less than -10 mV) due to bias only. This suggests that InGaAs MOSFETs are more sensitive to positive bias stress than negative bias stress.

Subtracting the bias-induced threshold-voltage shift from the biased irradiation-induced threshold-voltage shift in Fig. 5.6 (a), there is a negative threshold voltage shift of about 100 mV at V_{GS} = +1.0 V, which corresponds to an areal density of 3.6×10^{12} cm^{-2} trapped holes when projected to the interface. That net electron trapping is observed shows that less TID-induced hole trapping occurs than bias-induced electron trapping under the selected irradiation and bias conditions, consistent with the response of some Si-gate devices with HfO_2 gate dielectrics [151]. Hence, the combined positive-bias response of the devices biased at V_{GS} = +1.0 V during irradiation is dominated by electron trapping due to the applied bias alone, i.e., positive-bias instability [145].

Similar analysis shows that the threshold voltage shift is approximately -60 mV for the V_{GS} = -1.0 V gate-bias irradiation in Fig. 5.6 (b), corresponding to 2.2×10^{12} cm^{-2} hole trapping in the HfO_2. The threshold voltage shifts under both bias conditions are larger than silicon devices with similar gate dielectric [151]. This is related to the high density of interface defects between the high κ dielectric and InGaAs, such as Ga or As dangling bonds, as well as Ga-Ga or As-As like-atom bonds, which leads to enhanced hole and electron trapping [152].

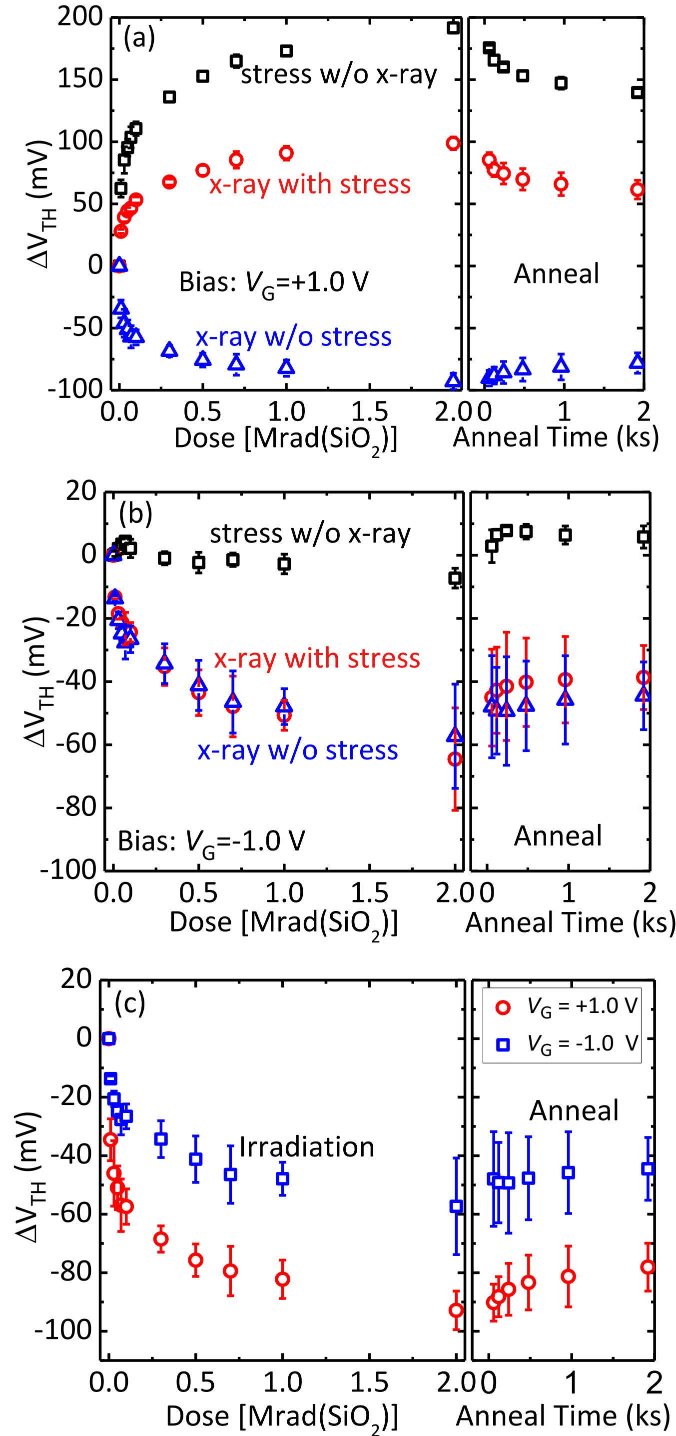

Fig. 5.6. Threshold voltage as a function of irradiation dose and annealing time for irradiation, bias only, and bias-stress-adjusted irradiation conditions for (a) V_{GS} = +1.0 V and (b) V_{GS} = -1.0 V during irradiation; (c) threshold voltage shift as a function of dose and annealing time for bias-stress-adjusted irradiation at two bias conditions. The error bars represent the standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV. All the tested devices have dimensions of W/L = 10 μm/2 μm.

Fig. 5.6 (c) shows the pure TID-induced threshold-voltage shift at irradiation bias of V_{GS} = +1.0 V and V_{GS} = -1.0 V. These results show that the threshold voltage shift due to irradiation alone is greater under positive gate bias during irradiation than negative gate bias, similar to what is observed in Si MOSFETs with HfO_2 gate oxides [153], and contrary to what is observed in InGaAs gate-all-around MOSFETs [70].

TCAD simulations were also performed. Fig. 5.7 shows the simulated and measured I_D vs. V_G for a device with dimension of W/L=10 μm/2 μm. It shows that the simulation is well calibrated to the measurement. Simulation shows that the electric fields in the HfO_2 at V_{GS} = +1.0 V and V_{GS} = -1.0 V are approximately 0.8 MV/cm and -0.8 MV/cm, respectively. Hence, the charge yield in both bias conditions should be approximately equal, which suggests that the charge yield cannot explain this bias dependence.

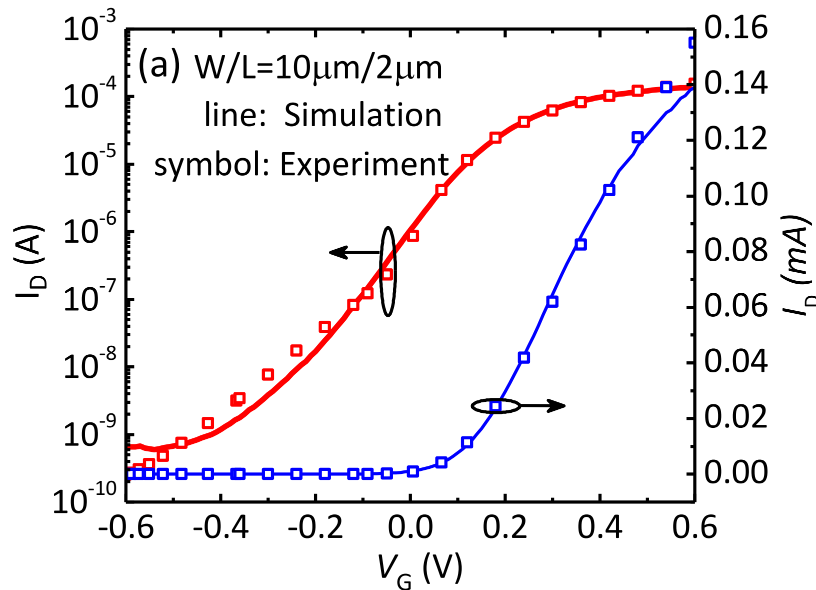

Fig. 5.7. Simulated and measured I_D vs. V_{GS} on the log scale (left) and linear scale (right) for device with dimension of W/L=10 μm/2 μm.

One plausible explanation for the difference in threshold voltage shift under the two bias conditions is that the trapped hole centroid at V_{GS} = +1.0 V is closer to the HfO_2/InGaAs interface than at V_{GS} = -1.0 V, due to the electric field polarity difference between the two bias conditions, as illustrated in Fig. 5.8. The closer to the interface the charge centroid, the charge would cause

larger threshold voltage shift, as shown in equation (1.4). This result is similar to what is typically observed for charge trapping in SiO_2 [154].

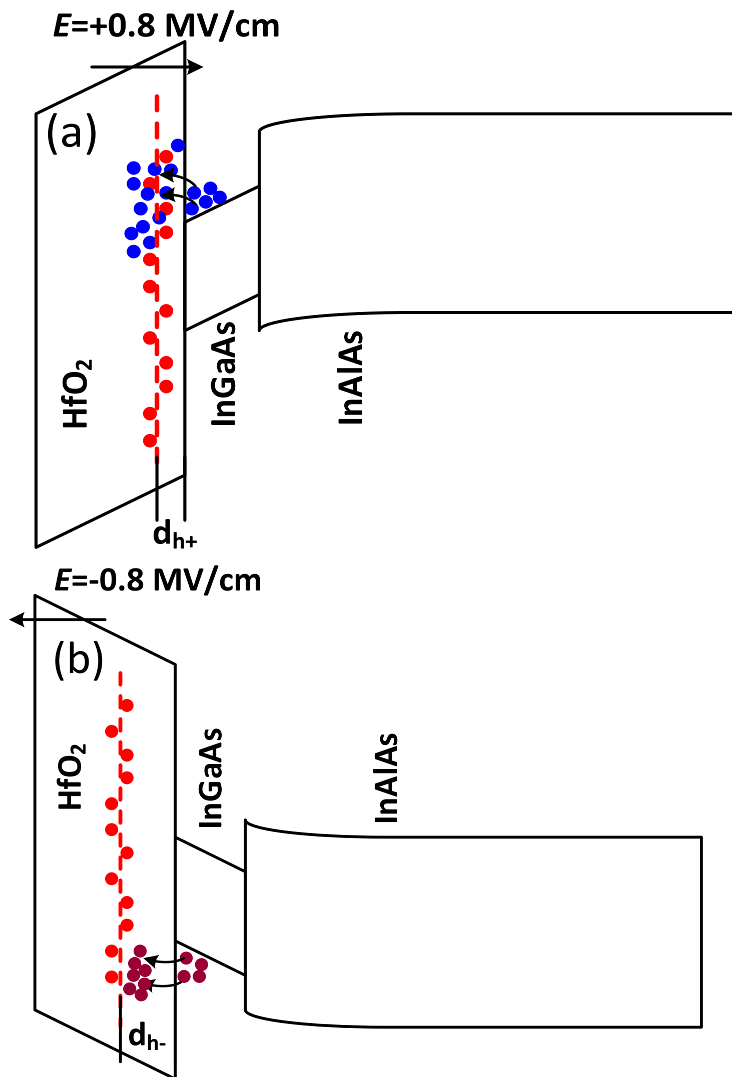

Fig. 5.8. Schematic illustrating charge trapping during biased irradiation at (a) V_{GS} = +1.0 V and (b) V_{GS} = -1.0 V. The blue circle represents electrical stress induced electron trapping; the red circle represents radiation induced hole trapping; and the dark red circle represents electrical stress induced hole trapping. The red dash line in the figure represents the hole centroid. The label d_{h+} and d_{h-} represents the distance between the hole centroid and the HfO_2/InGaAs interface at V_{GS} = +1.0 V and V_{GS} = -1.0 V, respectively. $d_{h-} > d_{h+}$.

Fig. 5.9 (a) shows the transfer characteristics before irradiation and after 2 Mrad(SiO_2) exposure for devices with different gate lengths. The device is biased with V_{GS} = +1.0 V during irradiation. Devices with different gate lengths have similar irradiation response, namely positive threshold-voltage shift, negligible leakage-current increase, and ON-current degradation. After 2

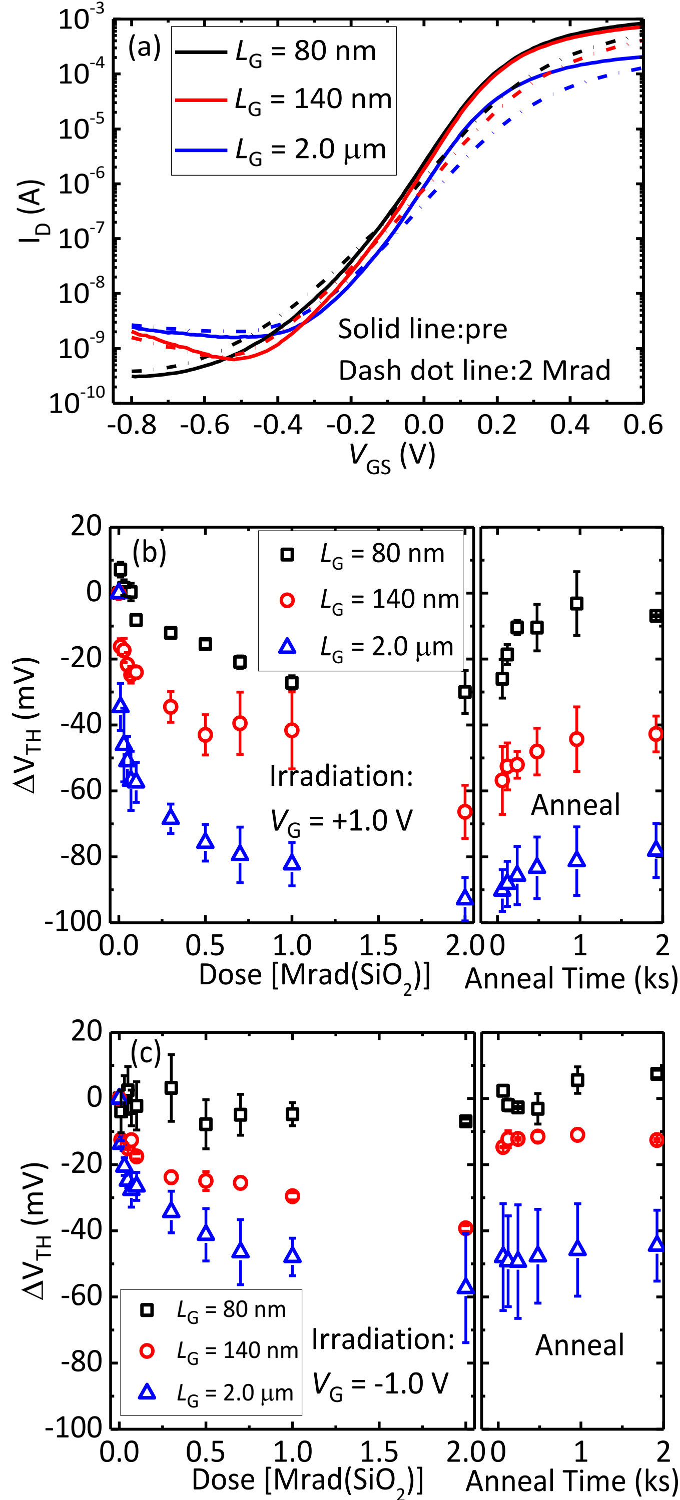

Fig. 5.9. (a) I_D versus V_{GS} before and after 2 Mrad(SiO_2) irradiation for devices with different gate lengths. During irradiation, V_{GS} = +1.0 V. The bias-stress-adjusted TID-induced threshold voltage shift is shown as a function of dose and anneal time for different gate lengths for bias at (b) V_{GS} = +1.0 V, and (c) V_{GS} = -1.0 V. The error bars represent standard deviations among different devices tested. Measurements are made with V_{DS} = 50 mV.

Mrad(SiO_2) exposure, the devices still have ON/OFF ratios over 10^5, even for the devices with L_G = 80 nm. The bias-stress-adjusted TID response as a function of dose and annealing time for different gate lengths are shown in Fig. 5.9 (b) and (c) under irradiation bias of V_{GS} = +1.0 V and V_{GS} = -1.0 V, respectively. The results indicate that larger threshold-voltage shifts are observed for devices with longer channels, for both positive and negative gate bias during irradiation. This suggests there is more hole trapping for the longer devices than the shorter devices.

A typical cause of length and width variation in TID response is electric field variation in the gate dielectric as a function of channel length, which can strongly influence the amount of hole trapping [155], [156]. Fig. 5.10 (a) and (b) show the vertical electric field in the gate oxide along a horizontal cut line for devices with different gate lengths biased at V_{GS} = +1.0 V and V_{GS} = -1.0 V, respectively. The electric field is higher for device with shorter gate length, due to the corner effect. However, the results show that the electric field in the HfO_2 differs by less than 1% among all these devices and gate lengths. Therefore, electric field variations cannot explain the large TID-induced threshold voltage shift difference at different gate lengths.

Another possibility is that the mechanical strain in the gate oxide may vary with gate length, which in turn can impact the hole trapping in the oxide significantly. This has been evaluated for SiO_2/Si devices [157], [158], [159], [160], but not for devices with high-K gate stacks. In previous work, it has been shown that radiation-induced hole trapping tends to decrease if the interfacial Si tensile stress decreases. As a result, the radiation-induced hole trapping is larger for narrow width [157], and thick gate metal devices [158], due to more compressive stress. This is consistent with the trends we observe, but more work is required to evaluate the effects of stress on charge trapping in devices with high-κ gate stacks.

5.4. Conclusion

The gate bias and geometry dependence of TID effects on InGaAs quantum-well MOSFETs with thin HfO_2 gate oxide have been evaluated. Positive gate bias during irradiation leads primarily to bias-stress-induced electron trapping that exceeds radiation-induced hole trapping, leading to a net positive threshold-voltage shift under the conditions of this study. Negative gate bias during irradiation results in additive hole trapping from irradiation and bias-stress. The shift produced by the irradiation alone is negative and larger with positive gate bias than that observed under negative gate bias. In addition, the bias-stress-adjusted radiation-induced hole trapping increases with the channel length for both positive and negative bias irradiations. These results provide important,

early insight into the mechanisms and magnitude of the combined bias-stress and TID responses of InGaAs quantum-well MOSFETs with thin HfO_2 gate oxides.

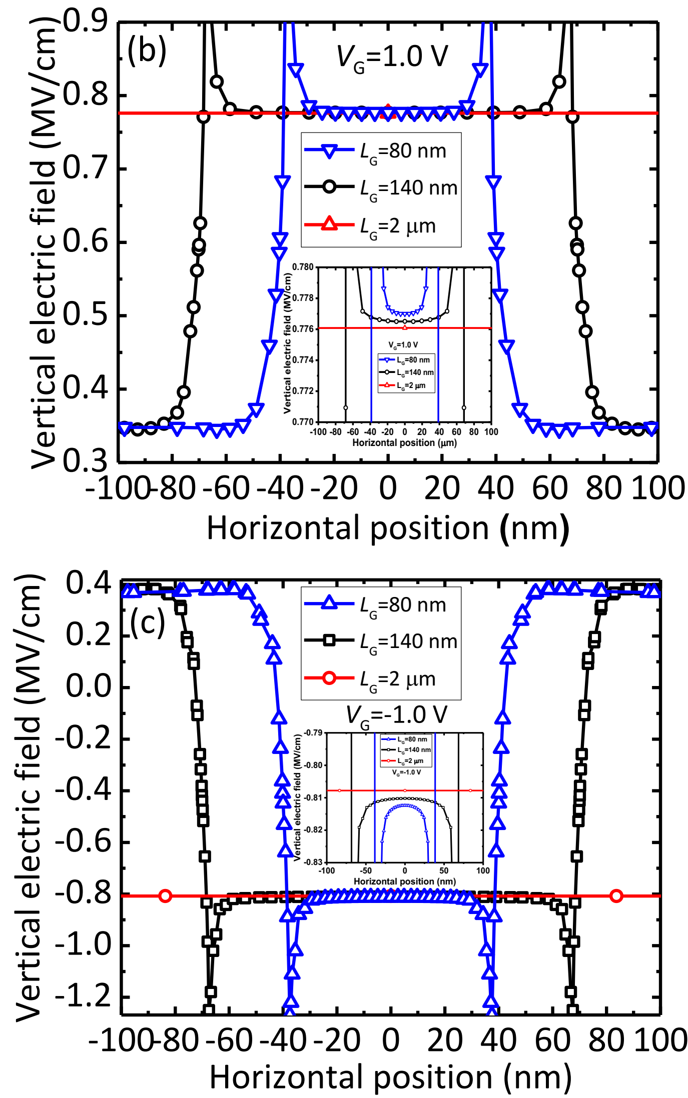

Fig. 5.10. (a) and (b) show the vertical electric field in the gate oxide along a horizontal cut line from source side to the drain side for different gate lengths biased at V_{GS} = +1.0 V and V_{GS}= -1.0 V, respectively.

Chapter 6. Conclusions and Future Work

This dissertation focuses on the understanding, characterization, and modeling of single-event-transients and total-ionizing-dose effects in emerging III-V MOSFETs for sub-10 nm node CMOS. Chapter Chapter 2, Chapter 3, Chapter 4 study the transients characterization and mechanisms in GaAs surface channel, InGaAs quantum-well, and InGaAs FinFET MOSFETs, respectively. Charge collection mechanisms are investigated and compared with those III-V FETs with non-insulating gates, such as JFET, MESFET, and HEMT devices, in terms of their similarities and differences. Combined electrical stress and X-ray irradiation are performed to characterize the TID response of InGaAs quantum-well channel MOSFETs. The main results obtained from these studies are summarized in Table 6.1.

Table 6.1. Charge collection characteristics of the III-V MOSFETs with different architectures

	Surface channel	**Quantum-well channel**	**FinFET**	**…**
Peak current gate bias dependence	Medium	High	High	…
Parasitic bipolar amplification (PBA)	Medium	High	High	…
Charge enhancement factor	~5	N/A	~14	…
PBA current flow	Bulk	Quantum-well channel	Quantum-well channel	…
PBA gate length dependence	High	High	High	…
Long transient tails at ON state	√	√	√	…
Comparison with Si MOSFET	More enhancement than 0.25 μm bulk MOSFET	SOI like confinement, but larger sensitive volume	PBA dominated, not drain junction dominated collection	…

Chapter 2 studies the charge collection in GaAs surface channel MOSFETs with thick high-κ gate dielectric. This device is very similar to Si MOSFETs except that the semiconductor material changes to GaAs. So direct comparison can be made between III-V MOSFETs and Si MOSFETs.

The key difference is that the significant contribution of channel current to the transient current in GaAs MOSFETs, instead of simply drain junction collection, as often observed in most Si MOSFETs. When the radiation strikes the drain side not far away from the gate, the generated holes diffuse towards the source. These holes modulate the source to channel barrier, which causes electrons injected from the source and collected by the drain, contributing to channel current. This effect is also observed in III-V non-insulating gate FETs. The charge collection process is weakly dependent on the gate bias because the current flow away from the surface channel.

Chapter 3 investigates the charge collection mechanism in InGaAs quantum-well channel MOSFETs. The device structure is different from the surface channel MOSFETs. It is more like a SOI device, since both the electrons and holes are confined in the quantum-well channel. This device has better scalability, compared with the surface channel, because gate can have control over the quantum-well channel. After the irradiation, this quantum-well efficiently collects the generated electrons and holes. The local electrostatic potential is strongly modified by the accumulated holes, such that there is almost no barrier between the source and channel. As a result, significant channel current flows. This is very similar to the Si SOI technology, where the bipolar amplification effect is active. Since the quantum-well channel is the place where most the charge collection takes place and it is controlled by the gate, the charge collection is highly gate bias dependent, different from the GaAs surface channel MOSFETs.

Chapter 4 presents a tunable wavelength laser system for studying charge collection in high mobility MOSFETs with multiple layers in the device. This laser is applied to study the InGaAs double gate FinFET device. For sub-10 nm node, multiple gates architecture is necessary to combat the short-channel effects. The bipolar amplification gain is semi-empirically measured with the new laser system. It is found that with technology scaling, the bipolar amplification is getting more and more serious. Therefore, single event transient investigation in III-V MOSFETs suggests they are highly sensitive to ionizing radiation, compared with Si counterparts.

Chapter 5 studies the TID effects in InGaAs quantum-well MOSFETs. Due to large amount of pre-existing traps in the oxide and the poor interface between oxide and InGaAs, the electrical stress alone can cause significant degradation when the device is biased during irradiation. Therefore, combined electrical stress and X-ray testing are performed to characterize the TID response of the device. It is found that electrical stress-induced electron trapping compensates radiation-induced hole trapping during positive gate-bias irradiation. Stress-induced hole trapping

adds to the effects of radiation-induced hole trapping under negative gate bias. Therefore, electrical stress plays an important role in determining the biased irradiation response of III-V MOSFETs. For the future commercial applications, the bias instability has to be addressed and reduced, it can be expected that the electrical stress induced degradation will be reduced, which necessitates combined electrical stress and X-ray testing.

In this dissertation, single event transients and total ionizing dose effects are investigated on a device level. The next step moving forward would be to study the radiation effects in a single device fabricated on a Si substrate and to consider effects in circuits, such as SRAM cells and flip-flops. However, heterogeneous integration of NMOS and PMOS devices on Si substrates has not been demonstrated and CMOS circuits based on these device technologies are still not implemented. However, NMOS based circuits could be tested for early study and insight. Meanwhile, TCAD simulations could be applied to study the CMOS based circuits without much difficulties.

A preliminary charge sharing study between devices has been performed. In that study, the device spacing is 30 μm and fabricated on semi-insulating InP substrate, the devices are well isolated from each other. In practical applications, devices will be much closer to each other. So the next step is to place devices much closer and study the charge sharing behavior. Another interesting topic would be to compare the effect of substrate on charge sharing behavior. Since Si substrate conductivity is much higher than the semi-insulating substrate, it should be expected that the charge sharing behavior would be different.

Another topic that is under consideration is compact modeling of TID effects in InGaAs quantum-well MOSFETs. This work is in collaboration with MIT. The idea is to include the TID effects in the MIT virtual source (MVS) model [161]. So far, the only bias condition that has been considered is all-terminals grounded and very small degradation was observed. For the next step, irradiation with negative gate bias is planned and more degradation is expected. From the results described above, InGaAs quantum-well MOSFETs exhibit little or no degradation due to negative gate bias electrical stress. Therefore, the TID response could be easily studied.

Appendix A. Tunable Wavelength Laser System

Introduction

The tunable wavelength laser system is based on the TPA laser system developed at Vanderbilt, with a wavelength of 1.26 μm, which is optimized for Si based devices. Fig. 4.3 is repeated here for illustration. Many of the optical components are the same as that shown in [139], but several new components are introduced to be able to adjust the wavelength. To be complete, the introduction to some components are copied from [139] .

System Components

Components	Description
Laser Source	A titanium-sapphire (Ti/S) pumped Optical Parametric Generator (OPG). The OPG is pumped at a 1 kHz repetition rate with 1 mJ, 150 fs pulses centered at 800 nm from a chirped-pulse amplifier. The amplifier is seeded with a passively mode-locked Ti/S oscillator. The OPG uses non-linear parametric frequency conversion in a Beta Barium Borate (BBO) crystal to generate and amplify signal and idler wavelengths that are continuously tunable from ~1200 nm to ~2400 nm. Using harmonic, sum, and difference frequency-generating crystals outside the OPG, wavelengths from ~200 nm to ~10 μm can be 60 generated with average pulse energies varying from 1μJ/pulse to 100μJ/pulse, depending on the wavelength
Prism	A prism is used to isolate the desired wavelength from the output of the laser system. Since the light output from the laser source has mixed and discrete wavelengths, it will be separated by a prism, due to dispersion effect. The distance between the prism and mirror M1 is large enough so that different wavelength is well separated.
Aperture	An aperture is used to select desired wavelength. Other undesired wavelengths are out of the aperture, so that they are not included in the optical system.
Spatial Filter	A rail-mounted section of the optical path consisting of various components (irises, lens, pinhole) used to direct, align, and shape the beam.

Polarizer	Adjusts the beam polarization following the Half-Wave plate. A means of controlling the incident pulse energy that is not intended to be adjusted during measurements
Photodiode	The primary means by which the pulse energy is measured during experiments. The photodiode peak current response has been calibrated to the incident laser pulse energy at the DUT location. For the experiment, InGaAs and PbS photodiodes are used for 1.26 μm and 2.2 μm wavelength, respectively. However, calibration is needed for 2.2 μm wavelength.
Black Box	A light-tight box responsible for directing the beam to the focusing objective, photodiode, and infrared camera. A focusing lens is included in front of the photodiode to ensure that the entire beam is incident on the detector.
Near IR Camera	A near-infrared camera whose purpose is to image the DUT and the laser spot of the focused laser beam.
BB Source	A broad spectrum light source provides background illumination through the focusing objective for imaging devices under test.
Computer	A Windows-based PC that runs software for controlling the X, Y, and Z stages. Also interfaces with various pieces of measurement equipment for capturing and analyzing experimental data.
XY-Stages	Modified probe station for mounting DUTs and probes (if needed). The probe station was manufactured by Creative Devices and modified in-house at Vanderbilt. The XYstages are mounted beneath probe station platen to move the entire probe station surface.
Z-Stage	Z-stage controls the Z-location of the focused laser spot.
Focusing Objective	Focuses the incoming laser light to a small spot size. Two objectives are common on this setup, the Mitutoyo Plan Apo NIR 50X and the Mitutoyo Plan Apo NIR 100X. Of the two, the 100X version is the most commonly used for SEE experimental work.

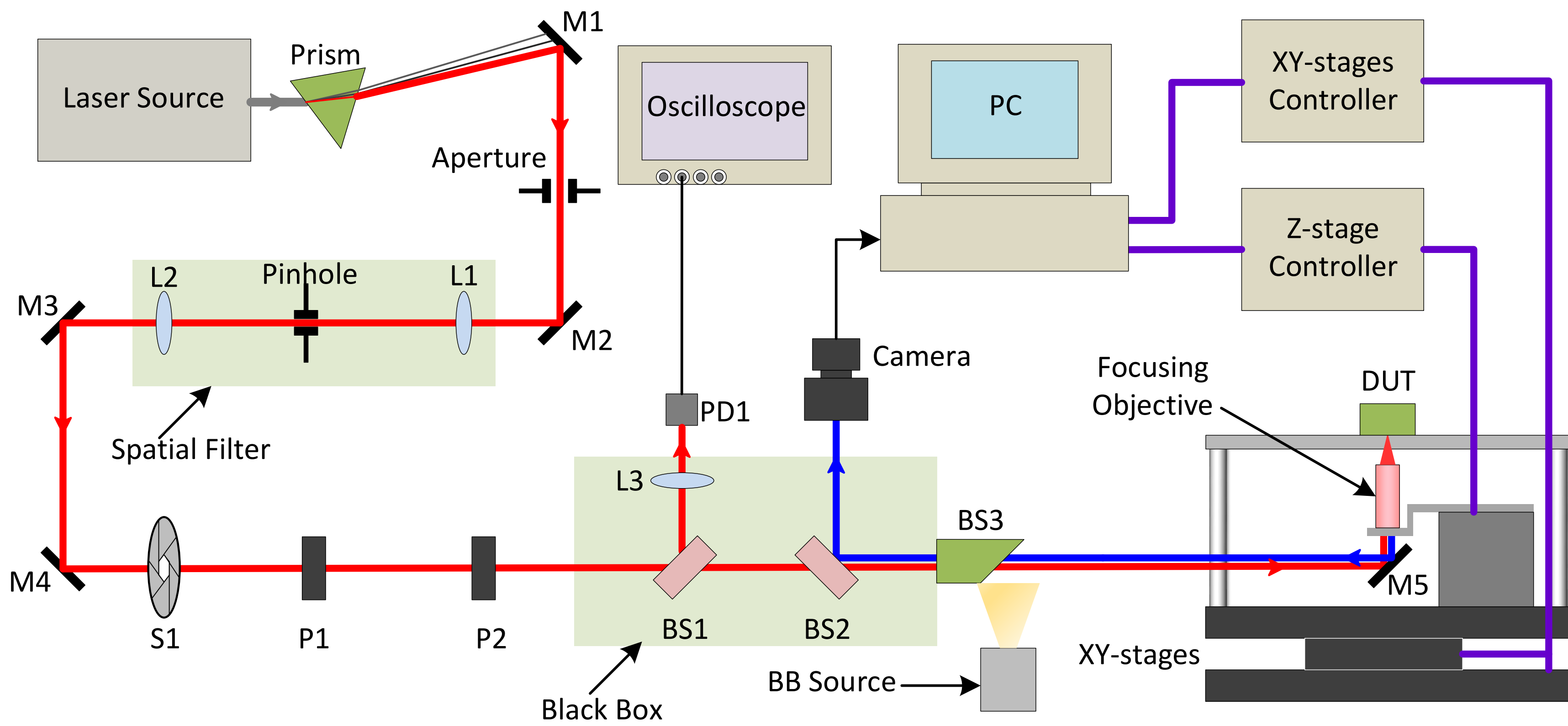

Fig. 4.3. A simplified block diagram of TPA test setup. The red line indicates the laser beam propagation path and the blue line indicates reflected light, which is imaged by the near-infrared camera.

Appendix B. TCAD Scripts

Introduction

In this appendix, some useful TCAD simulation scripts are attached, in case they will be helpful for students who are interested. Two sets of scripts are attached here; one is the 16 nm Si FinFET based SRAM mixed circuit simulation and the other one is the InGaAs FinFET device. The details of the SRAM circuits are presented in [162]. Some necessary comments are provided to help understanding. For the mixed SRAM simulation, only the irradiated NMOS is modeled in TCAD, and all the rest transistors are modeled by 16 nm predictive technology model (PTM) from ASU. Those models are copied from the PTM website to local directory and converted to models used in the TCAD tools by command “spice2sdevice”.

16 nm Si FinFET SRAM mixed-circuit simulation

```
******************************************************************************
finfet_dvs.cmd    ;file name for the structure generation file
******************************************************************************
(sde:clear)
;=============================================================================
;lateral length
(define Ltot      2) ;total length of the simulation domain
(define Lg        0.016) ;gate length
(define Lsd       0.014) ;source/drain contact length
(define Lsp       0.010) ;the spacer length
(define Lfin      (+ (+ Lg (* Lsd 2.0))) (* Lsp 2.0)) ;fin length

(define Hsub      10) ;substrate thickness
(define Hsti      0.01) ;STI oxide thickness
(define Hfin      0.026) ;fin height
(define Hoxi      0.00538) ;the oxide thickness, EOT=1nm
(define Wsub      2) ;Substrate width
(define Wfin      0.012) ;fin thickness/width

;doping definition
(define Dopingsub 1e15) ;body doping
(define Dopingsd  3e20) ;source/drain doping

(define Zstrike   0.018) ;the strike location
;=============================================================================
;derived quantities
;X is along fin width, Y is along the fin height, Z is along the channel length
(define Xmaxr     (/ Wsub 2.0)) ;the maximum X coordinate of substrate
(define Xmaxl     (* Xmaxr -1.0)) ;the minimum X coordinate of substrate
(define Xfinr     (/ Wfin     2.0)) ;the maximum X coordinate of fin
(define Xfinl     (* Xfinr -1.0)) ;the minimum X coordinate of fin
(define Xoxir     (+ Xfinr Hoxi)) ;the maximum X coordinate of the side oxide
(define Xoxil     (* Xoxir -1.0)) ;the minimum X coordinate of the side oxide

(define Ysti      (* Hsti 1.0)) ;the y coordinate of STI oxide
(define Ysub      (+ Ysti Hsub)) ;the y coordinate of substrate
```

```
(define Yfin      (* Hfin -1.0)) ;the y coordinate of Fin
(define Yoxi      (- Yfin Hoxi)) ;the y coorinate of the oxide

(define Zmaxr     (/ Ltot 2.0)) ;the maximum z coordinate of the substrate
(define Zmaxl     (* Zmaxr -1.0)) ;the minimum z coordinate of the substrate
(define Zgr       (/ Lg 2.0)) ;the maximum z coordinate of the gate
(define Zgl       (* Zgr -1.0)) ;the minimum z coordinate of the gate
(define Zspr      (+ Zgr Lsp)) ;the maximum z coordinate of the spacer
(define Zspl      (* Zspr -1.0));the minimum z coordinate of the spacer
(define Zsdr      (+ Zspr Lsd));the maximum z coordinate of the s/d contact
(define Zsdl      (* Zsdr -1.0));the minimum z coordinate of the s/d contact

(sdegeo:set-default-boolean "ABA")  ;the new replaces old
(define GATE (sdegeo:create-cuboid (position 0.0      0.0   0.0) (position (+
Xoxir 0.01) (- Yfin 0.01) (+ Zgr 0.00)) "Gold" "Gate"))
(sdegeo:create-cuboid (position 0.0 Ysti  0.0)  (position   Xmaxr Ysub Zmaxr)
      "Silicon"   "Substrate")
(sdegeo:create-cuboid (position 0.0 0.0   0.0)        (position   Xmaxr Ysti
      Zmaxr)      "Oxide"           "STI")
(sdegeo:create-cuboid (position 0.0 0.0   0.0)        (position   Xoxir Yoxi
      Zgr)  "HfO2"            "Gateoxide")
(sdegeo:create-cuboid (position 0.0 Ysti  0.0)  (position   Xfinr Yfin  Zsdr)
      "Silicon"   "Fin")
(sdegeo:mirror-selected (get-body-list) (transform:reflection (position 0 0 0)
(gvector 0 0 -1)) #t)
(sdegeo:fillet (find-edge-id (position Xfinr Yfin 0)) 0.002)      ;round   the
corners

(sdegeo:set-default-boolean "BAB")
(define DRAIN     (sdegeo:create-cuboid (position 0.0 (+ Yfin 0.01)     Zspr)
(position Xfinr (- Yfin 0.01) Zsdr) "Gold" "Drain"))
(define SOURCE    (sdegeo:create-cuboid (position 0.0 (+ Yfin 0.01)     Zspl)
(position Xfinr (- Yfin 0.01) Zsdl) "Gold" "Source"))

;=============================================================================
;defining contact
(sdegeo:define-contact-set "substrate" 4.0(color:rgb 0.0 1.0 0.0) "%%")
(sdegeo:define-contact-set "drain" 4.0    (color:rgb 0.0 1.0 0.0) "**")
(sdegeo:define-contact-set "gate" 4.0     (color:rgb 1.0 0.0 0.0) "++")
(sdegeo:define-contact-set "source" 4.0   (color:rgb 1.0 1.0 0.0) "@@")

(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-faces GATE)
(sdegeo:delete-region GATE)
(sdegeo:set-current-contact-set "drain")
(sdegeo:set-contact-boundary-faces DRAIN)
(sdegeo:delete-region DRAIN)
(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-boundary-faces SOURCE)
(sdegeo:delete-region SOURCE)
(sdegeo:define-3d-contact (find-face-id (position 0.005 Ysub 0)) "substrate")

;=============================================================================
;defining doping profile
(sdedr:define-constant-profile  "Const.Substrate"    "BoronActiveConcentration"
Dopingsub )
(sdedr:define-constant-profile-region      "Sub.Place"      "Const.Substrate"
"Substrate")
```

```
(sdedr:define-constant-profile-region "Fin.Place" "Const.Substrate" "Fin")

;drain doping
(sdedr:define-refinement-window "DrainWin" "Cuboid" (position 0.0 Yfin (+ (/ (+
Zspr Zgr) 2.0) 0.001) ) (position Xfinr -0.005 Zsdr))
(sdedr:define-constant-profile   "Const.Drain"   "ArsenicActiveConcentration"
Dopingsd)
(sdedr:define-constant-profile-placement     "Drain.place"     "Const.Drain"
"DrainWin" 0.002)

;source doping
(sdedr:define-refinement-window "SourceWin" "Cuboid" (position 0.0 Yfin (- (/
(+ Zspl Zgl) 2.0) 0.001) ) (position Xfinr -0.005 Zsdl))
(sdedr:define-constant-profile   "Const.Source"   "ArsenicActiveConcentration"
Dopingsd)
(sdedr:define-constant-profile-placement    "Source.place"    "Const.Source"
"SourceWin" 0.002)

;==========================================================================
;defining mesh
;substrate multibox
(sdedr:define-multibox-size "Multi.Substrate" (/ Wsub 10) (/ Hsub 10) (/ Ltot
10) (/ Wsub 30) (/ Hsub 30) (/ Ltot 30) 1 1.2 1 )
(sdedr:define-refeval-window "Ref.Substrate" "Cuboid" (position 0.0     Ysti
      Zmaxl) (position Xmaxr  Ysub  Zmaxr))
(sdedr:define-multibox-placement   "Multi.Substrate.Place"   "Multi.Substrate"
"Ref.Substrate")

;Fin structure
(sdedr:define-refeval-window "Ref.fin" "Cuboid" (position 0.0     (+      Ysti
0.005)      Zsdl) (position   Xfinr Yfin  Zsdr))
(sdedr:define-refinement-size "Size.fin" (/ Wfin 10.0) (/ Hfin 15.0) (/ Lfin
10.0) (/ Wfin 15.0) (/ Hfin 30.0) (/ Lfin 20.0))
(sdedr:define-refinement-function       "Size.fin"       "DopingConcentration"
"MaxTransDiff" 0.5)
(sdedr:define-refinement-placement "Size.fin.Place" "Size.fin" "Ref.fin")

;Fin under gate
(sdedr:define-refeval-window "Ref.fin.Gater" "Cuboid" (position 0.0     Ysti
      0) (position      Xfinr Yfin  (+ Zgr 0.00)))
(sdedr:define-multibox-size "Multi.fin.Gater" (/ Wfin 10.0) (/ Hfin 15.0) (/ Lg
10.0) (/ Wfin 15.0) (/ Hfin 30.0) (/ Lg 15.0) 1.0 1.1 -1.2)
(sdedr:define-refinement-function   "Multi.fin.Gater"   "MaxLenInt"   "Silicon"
"HfO2" 1e-4 1.05)
(sdedr:define-multibox-placement   "Multi.fin.Gater.Place"   "Multi.fin.Gater"
"Ref.fin.Gater")

(sdedr:define-refeval-window "Ref.fin.Gatel" "Cuboid" (position 0.0     Ysti
      0) (position      Xfinr Yfin  (- Zgl 0.00)))
(sdedr:define-multibox-size "Multi.fin.Gatel" (/ Wfin 10.0) (/ Hfin 15.0) (/ Lg
10.0) (/ Wfin 15.0) (/ Hfin 30.0) (/ Lg 15.0) 1.0 1.1 1.2)
(sdedr:define-refinement-function   "Multi.fin.Gatel"   "MaxLenInt"   "Silicon"
"HfO2" 1e-4 1.05)
(sdedr:define-multibox-placement   "Multi.fin.Gatel.Place"   "Multi.fin.Gatel"
"Ref.fin.Gatel")

;the top of the fin
```

```
;(sdedr:define-refeval-window "Ref.fin.Corner" "Cuboid" (position 0.0   (-
Yfin 0.0004)      Zgl) (position    Xfinr (+ Yfin 0.0004)   (+ Zgr 0.00)))
;(sdedr:define-refinement-size "Size.fin.Corner" 5e-4 1e-4 5e-4 1e-4 5e-5 1e-
4)
;(sdedr:define-refinement-placement  "Size.fin.Corner.Place"  "Size.fin.Corner"
"Ref.fin.Corner")

;Gate oxide
(sdedr:define-refinement-size "Size.oxide" (/ Hoxi 2) (/ Hoxi 2) (/ Lg 4) (/
Hoxi 4) (/ Hoxi 4) (/ Lg 8))
(sdedr:define-refinement-function "Size.oxide" "MaxLenInt" "Silicon" "HfO2" 5e-
4 1.2)
(sdedr:define-refinement-region "Size.oxide.Place" "Size.oxide" "Gateoxide")

;the ion strike path
(sdedr:define-refeval-window  "Ref.ion"  "Cuboid"  (position  0  Yfin  (-  Zstrike
0.005)) (position 0.005 Ysub (+ Zstrike 0.005)))
(sdedr:define-refinement-size "Size.ion" 0.0025 0.05 0.0025 1e-4 0.005 1e-4)
(sdedr:define-refinement-placement "Size.ion.Place" "Size.ion" "Ref.ion" )

(sde:build-mesh "snmesh" "" "finfet_half")
(system:command "tdx -mtt -x -M 0 -S 0 finfet_half_msh  finfet_msh")
*****************************************************************************
finfet_des.cmd ;file name for the transient simulation
*****************************************************************************
Device NMOS{
      File {
            Grid="finfet_msh.tdr"
      }
      Electrode {
            {Name="source" Voltage=0}
            {Name="drain" Voltage=0}
            {Name="gate" Voltage=0 Workfunction=4.6}
            {Name="substrate" Voltage=0}
      }
      Physics {
            EffectiveIntrinsicDensity(NoBandGapNarrowing)
            Mobility(
                  DopingDependence
                  Enormal(Lombardi)
                  eHighFieldsaturation)
            Fermi
            Recombination(
                  SRH
                  Auger
                  Radiative)
            HeavyIon(
                  PicoCoulomb
                  Direction=(0,1,0)
                  Location=(0,-0.025,0.018)
                  Time=1e-9
                  Length=5
                  Wt_hi=0.05
                  LET_f=0.1
                  Gaussian)
      }
*     Physics(Region="Fin") {
*           eQuantumPotential
```

```
*     }
      Plot{
            *carrier densities
                  eDensity hDensity EffectiveIntrinsicDensity IntrinsicDensity
            *currents and current components
                  eCurrentDensity hCurrentDensity
                  TotalCurrent/Vector  eCurrent/Vector  hCurrent/Vector
                  eMobility hMobility eVelocity hVelocity
                  DisplacementCurrent
                  DisplacementCurrent/Vector
            *fields, potentials and charge distribution
                  ElectricField/Vector
                  Potential
                  eQuasiFermi hQuasiFermi eQuantumPotential
                  SpaceCharge
            *Doping Profiles
                  Doping
            *Band Structure
                  BandGap
                  ElectronAffinity
                  ConductionBandEnergy ValanceBandEnergy
      }
}
Math{
      Number_Of_Threads=4
      Extrapolate
      Derivativites
      Iterations=20
      RelErrControl
      Digits=5
      NotDamped=20
      CNormPrint
      Spice_gmin=1e-15
}
File{
      Current="finfet_see"
      Plot="finfet_see"
      Output="finfet_see"
      SPICEPath="."
}
System{
      nfet mn1("source"=0 "gate"=nq "drain"=n2 "bulk"=0 "temp"=300)
      NMOS mn2( "source"=n2 "gate"=nq "drain"=nd "substrate"=0)
      pfet mp1 ("drain"=n1 "gate"=nq "source"=n3 "bulk"=n3 "temp"=300)
      pfet mp2 ("drain"=nd "gate"=nq "source"=n1 "bulk"=n3 "temp"=300)
      pfet mp3 ("drain"=nqb "gate"=nphi "source"=n2 "bulk"=n3 "temp"=300)
      nfet mn3 ("source"=n1 "gate"=nphib "drain"=nqb "bulk"=0 "temp"=300)
      pfet mp4 ("drain"=n4 "gate"=nd "source"=n3 "bulk"=n3 "temp"=300)
      pfet mp5 ("drain"=nq "gate"=nphi "source"=n4 "bulk"=n3 "temp"=300)
      nfet mn5 ("source"=n5 "gate"=nphib "drain"=nq "bulk"=0 "temp"=300)
      nfet mn4 ("source"=0 "gate"=nd "drain"=n5 "bulk"=0 "temp"=300)
      *pfet mp6 ("drain"=n3 "gate"=nqb "source"=n5 "bulk"=n3 "temp"=300)
      *nfet mn6 ("source"=n4 "gate"=nqb "drain"=0 "bulk"=0 "temp"=300)
      pfet2 mp7 ("drain"=nqb "gate"=nq "source"=n3 "bulk"=n3 "temp"=300)
      nfet2 mn7 ("source"=0 "gate"=nq "drain"=nqb "bulk"=0 "temp"=300)
      Vsource_pset vdd (n3 0) {dc=0.8 }
      Vsource_pset vphi (nphi 0) {dc=0}
      Vsource_pset vphib (nphib 0) {dc=0.8}
```

```
      Initialize (nq = 0)
      Initialize (nd = 0.8)
      Initialize (nqb = 0.8)
      Initialize (n2 = 0.8)
      Plot "DC_initial" (n1 n2 n3 n4 n5 nq nqb nd i(mp1,n1))
      Plot "SEE_tran" (time() n1 n2 n4 n5 nq nqb nd i(mp1 n1) i(mn1 n2) i(mn2
d) i(mp2 d) i(mp1 n1) i(mp5 nq) i(mn5 nq) i(mn4 n5) i(mp4 n4))
}
Solve{
      Coupled (Iterations=20) {Poisson }
      Coupled (Iterations=20) {Poisson Electron Hole}
      Coupled (Iterations=20) {Poisson Circuit Contact Electron Hole}
      Save(FilePrefix="Bias") *can be separated into different files and then
load the Bias

      Load(FilePrefix="Bias")
      Transient(
            InitialTime=0
            FinalTime=0.9e-9
            InitialStep=1e-12
            MaxStep=1e-10
            Increment=1.2)
            {
                  Coupled{mn2.poisson   mn2.electron   mn2.hole   mn2.contact
circuit}
                  Plot    (Time=(0.001e-9;    0.9e-9)    FilePrefix="SE_DataA"
NoOverwrite)}
      Transient(
            InitialTime=0.9e-9
            FinalTime=1.0e-9
            InitialStep=1e-12
            MaxStep=5e-12
            Increment=1.2)
            {
                  Coupled{mn2.poisson   mn2.electron   mn2.hole   mn2.contact
circuit}
                  Plot      (Time=(0.98e-9;1.0e-9)      FilePrefix="SE_DataB"
NoOverwrite)}
      Transient(
            InitialTime=1.0e-9
            FinalTime=2e-9
            InitialStep=1e-13
            MaxStep=5e-11
            Increment=1.2)
            {
                  Coupled{mn2.poisson   mn2.electron   mn2.hole   mn2.contact
circuit}
                  Plot   (Time=(1.001e-9;1.005e-9;1.1e-9;1.2e-9;1.5e-9;1.8e-9)
FilePrefix="SE_DataC" NoOverwrite)}
}
```

InGaAs FinFET

```
*****************************************************************************
InGaAs_finfet_dvs.cmd   ;file name for the structure generation file
*****************************************************************************
(sde:clear)
;============================================================================
```

```
;lateral length
(define Ltot      5) ;total length of the device
(define Lg        0.05) ;gate length
(define Lsd       0.014) ;source/drain length
(define Lsp       0.010) ;the space length
(define Lfin      2) ;the total length of the fin structure
(define Hsub      20) ;Substrate thickness
(define Hbuf      0.4) ;InAlAs buffer thickness
(define Hoxi      0.005) ;the oxide thickness
(define Hchannel  0.04) ;InGaAs channel thicknesss
(define Hcap      0.03) ;Cap thickness
(define Hfin      0.22) ;fin height, including channel and etched buffer
thickness
(define Hfinbuf   (- Hfin Hchannel)) ;the thickness of the etched buffer
(define Hbufrem   (- Hbuf Hfinbuf)) ;the thickness of the remained buffer
(define Hhard     0.04) ;thickness of the hardmask on the top
(define Wsub      5) ;Substrate width
(define Wfin      0.020) ;fin thickness/width
(define Delthick  0.002) ;Delta doping thickness
(define Deldist   0.005) ;Delta doping distance to the bottom of channel
layer

;doping definition
(define Deltadoping 2e19) ;delta doping
(define Capdoping 3e19) ;cap doping

(define Zstrike   0.63)
;=============================================================================
;derived quantities
;x direction is along the width direction
(define Xmaxr     (/ Wsub 2.0)) ;the maximum X coordinate of substrate
(define Xmaxl     (* Xmaxr -1.0)) ;the minimum X coordinate of substrate
(define Xfinr     (/ Wfin     2.0)) ;the maximum X coordinate of fin
(define Xfinl     (* Xfinr -1.0)) ;the minimum X coordinate of fin
(define Xoxir     (+ Xfinr Hoxi)) ;the maximum X coordinate of the side oxide
(define Xoxil     (* Xoxir -1.0)) ;the minimum X coordinate of the side oxide

;y direction is along the thickness direction, perpendicular to the plane
;y=0 is defined at the bottom of the fin
(define Ybuf      (* Hbufrem 1.0)) ;the y coordinate of buffer bottom
(define Ysub      (+ Ybuf Hsub)) ;the y coordinate of substrate
(define Yfinbuf   (* Hfinbuf -1.0)) ;the y coordinate of buffer in the fin
(define Yfincha   (- Yfinbuf Hchannel)) ;the y coordinate of the channel in
the fin
(define Yhard     (- Yfincha Hhard)) ;the y coorinate of the hard mask
(define Ycap      (- Yfincha Hcap)) ;the y coordinate of the cap layer
(define Ydel      (+ Deldist Yfinbuf)) ;the y coordinate of delta doping

(define Zmaxr     (/ Ltot 2.0)) ;the maximum z coordinate of the substrate
(define Zmaxl     (* Zmaxr -1.0)) ;the minimum z coordinate of the substrate
(define Zgr       (/ Lg 2.0)) ;the maximum z coordinate of the gate
(define Zgl       (* Zgr -1.0)) ;the minimum z coordinate of the gate
(define Zspr      (+ Zgr Lsp)) ;the maximum z coordinate of the spacer
(define Zspl      (* Zspr -1.0)) ;the minimum z coordinate of the spacer
(define Zfinr     (/ Lfin     2.0)) ;the maximum z coordinate of the fin
(define Zfinl     (* Zfinr -1.0)) ;the minimum z coordinate of the fin

;=============================================================================
```

```
 (sdegeo:set-default-boolean "ABA") ;the new replaces old
(define GATE (sdegeo:create-cuboid (position 0.0      -0.001      0.0)
(position (+ Xoxir 0.01) (- Yhard 0.01) (+ Zgr 0.00)) "Gold" "Gate"))
(define OXIDE (sdegeo:create-cuboid (position 0.0     0.0   0.0) (position (+
Xoxir 0.00) (- Yhard Hoxi) (+ Zgr 0.00)) "Al2O3" "Oxide"))
(sdegeo:create-cuboid (position 0.0 Ybuf  0.0) (position    Xmaxr Ysub
      Zmaxr)      "InP"       "Substrate")
(sdegeo:create-cuboid (position 0.0 0.0   0.0) (position    Xmaxr Ybuf
      Zmaxr)      "InAlAs"    "Buffer")
(sdegeo:create-cuboid (position 0.0 0.0   0.0) (position    Xfinr Yfinbuf
      Zgr)  "InAlAs"    "Finbuffer")
(sdegeo:create-cuboid (position 0.0 Yfinbuf     0.0) (position    Xfinr
      Yfincha     Zgr)  "InGaAs"    "Finchannel")
(sdegeo:create-cuboid (position 0.0 0.0   Zgr) (position    Xfinr Yfinbuf
      Zfinr)      "InAlAs"    "Finbufferd")
(sdegeo:create-cuboid (position 0.0 Yfinbuf     Zgr) (position    Xfinr
      Yfincha     Zfinr)      "InGaAs"    "Finchanneld")

(define A (sdegeo:create-cuboid (position 0.0   (+ Yfincha 0.000) 0.0)
(position   Xfinr Yhard Zgr)  "SiO2"            "Hardmask"))
(sdegeo:create-cuboid (position 0.0 (+ Yfincha 0.0)   Zgr) (position    Xfinr
      Ycap  Zfinr)      "InGaAs"    "Capd")
(sdegeo:mirror-selected (get-body-list) (transform:reflection (position 0 0
0) (gvector 0 0 -1)) #t)

;renaming of the duplicated regions
(sde:add-material (find-body-id (position (/ Xfinr 2.0) (/ (+ Yfinbuf
Yfincha) 2.0) (/ (+ Zgl Zfinl) 2.0))) "InGaAs" "Finchannels")
(sde:add-material (find-body-id (position (/ Xfinr 2.0) (/ (+ 0.0 Yfinbuf)
2.0)  (/ (+ Zgl Zfinl) 2.0))) "InAlAs" "Finbuffers")
(sde:add-material (find-body-id (position (/ Xfinr 2.0) (/ (+ Ycap Yfincha)
2.0)  (/ (+ Zgl Zfinl) 2.0))) "InGaAs" "Caps")

;===========================================================================
 (sdegeo:set-default-boolean "BAB")
(define DRAIN     (sdegeo:create-cuboid (position 0.0 (+ Ycap 0.00)     (+
Zgr 0.0001)) (position Xmaxr (- Ycap 0.01) Zmaxr) "Gold" "Drain"))
(define SOURCE    (sdegeo:create-cuboid (position 0.0 (+ Ycap 0.00)     (-
Zgl 0.0001)) (position Xmaxr (- Ycap 0.01) Zmaxl) "Gold" "Source"))

;defining contact
(sdegeo:define-contact-set "substrate"    4.0   (color:rgb 0.0 1.0 0.0) "%%")
(sdegeo:define-contact-set "drain"        4.0   (color:rgb 0.0 1.0 0.0) "**")
(sdegeo:define-contact-set "gate"         4.0   (color:rgb 1.0 0.0 0.0) "++")
(sdegeo:define-contact-set "source"       4.0   (color:rgb 1.0 1.0 0.0) "@@")

(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-faces GATE)
(sdegeo:delete-region GATE)
(sdegeo:set-current-contact-set "drain")
(sdegeo:set-contact-boundary-faces DRAIN)
(sdegeo:delete-region DRAIN)
(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-boundary-faces SOURCE)
(sdegeo:delete-region SOURCE)

;===========================================================================
;defining doping profile
```

```
;cap doping
(sdedr:define-constant-profile "Capdoping" "ArsenicActiveConcentration"
Capdoping)
(sdedr:define-constant-profile-region "Capdopingplacements" "Capdoping"
"Caps")
(sdedr:define-constant-profile-region "Capdopingplacementd" "Capdoping"
"Capd")
(sdedr:define-constant-profile-region "Capdopingplacementcons" "Capdoping"
"Concaps")
(sdedr:define-constant-profile-region "Capdopingplacementcond" "Capdoping"
"Concapd")

;buffer delta doping
;(sdedr:define-refinement-window "Deltadopingwin" "Cuboid" (position 0.0 Ydel
Zfinl) (position Xfinr (+ Ydel Delthick) Zfinr))
(sdedr:define-refinement-window "Deltadopingwin" "Cuboid" (position 0.0 Ydel
Zmaxl) (position Xmaxr (+ Ydel Delthick) Zmaxr))
(sdedr:define-constant-profile "Deltadoping" "ArsenicActiveConcentration"
Deltadoping)
(sdedr:define-constant-profile-placement "Deltadopingplacement" "Deltadoping"
"Deltadopingwin")

;=============================================================================
;defining mesh
;substrate multibox
(sdedr:define-multibox-size "Multi.Substrate" (/ Wsub 10.0) (/ Hsub 10.0) (/
Ltot 10.0) (/ Wsub 15.0) (/ Hsub 30.0) (/ Ltot 15.0) 1 1.5 1 )
(sdedr:define-refeval-window "Ref.Substrate" "Cuboid" (position 0.0     Ybuf
      Zmaxl) (position Xmaxr  Ysub  Zmaxr))
(sdedr:define-multibox-placement "Multi.Substrate.Place" "Multi.Substrate"
"Ref.Substrate")

;buffer multibox
(sdedr:define-refeval-window "Ref.Bufferl" "Cuboid" (position 0 Yfinbuf
Zmaxl) (position Xmaxr Ybuf 0) )
(sdedr:define-multibox-size "Multi.Bufl" (/ Wsub 10.0) (/ Hbuf 5.0) (/ Ltot
10.0) (/ Wsub 15.0) (/ Hbuf 10.0) (/ Lfin 50.0) 1 1 -1.5 )
(sdedr:define-multibox-placement "Multi.Bufl.Place" "Multi.Bufl"
"Ref.Bufferl")

(sdedr:define-refeval-window "Ref.Bufferr" "Cuboid" (position 0 Yfinbuf
Zmaxr) (position Xmaxr Ybuf 0) )
(sdedr:define-multibox-size "Multi.Bufr" (/ Wsub 10.0) (/ Hbuf 5.0) (/ Ltot
10.0) (/ Wsub 15.0) (/ Hbuf 10.0) (/ Lfin 50.0) 1 1 1.5 )
(sdedr:define-multibox-placement "Multi.Bufr.Place" "Multi.Bufr"
"Ref.Bufferr")

(sdedr:define-refeval-window "Ref.Buf.Win" "Cuboid" (position 0 Yfinbuf
Zmaxl) (position Xmaxr Ybuf Zmaxr) )
(sdedr:define-refinement-size "Ref.Buf" (/ Wsub 1) (/ Hsub 1) (/ Ltot 1.0) (/
Wsub 1) (/ Hsub 1) (/ Ltot 1.0))
(sdedr:define-refinement-function "Ref.Buf" "MaxLenInt" "InAlAs" "Al2O3" 1e-3
1.5)
(sdedr:define-refinement-placement "Ref.Buf.Place" "Ref.Buf" "Ref.Buf.Win")

;delta doping
(sdedr:define-refinement-size "Refdelta" (/ Wsub 1.0) (/ Delthick 2.0) (/
Ltot 1.0) (/ Wsub 1.0) (/ Delthick 4.0) (/ Ltot 1.0))
```

```
(sdedr:define-refinement-placement "Refdeltapla" "Refdelta" "Deltadopingwin")

;channel multibox
(sdedr:define-refeval-window "Ref.Channell" "Cuboid" (position 0 Yfinbuf
Zmaxl) (position Xmaxr Ycap 0) )
(sdedr:define-multibox-size "Multi.Channell" (/ Wsub 10.0) (/ Hchannel 5.0)
(/ Ltot 20.0) (/ Wsub 15.0) (/ Hchannel 10.0) (/ Lfin 80.0) 1 1 -1.5 )
(sdedr:define-multibox-placement "Multi.Channell.Place" "Multi.Channell"
"Ref.Channell")

(sdedr:define-refeval-window "Ref.Channelr" "Cuboid" (position 0 Yfinbuf
Zmaxr) (position Xmaxr Ycap 0) )
(sdedr:define-multibox-size "Multi.Channelr" (/ Wsub 10.0) (/ Hchannel 5.0)
(/ Ltot 20.0) (/ Wsub 15.0) (/ Hchannel 10.0) (/ Lfin 80.0) 1 1 1.5 )
(sdedr:define-multibox-placement "Multi.Channelr.Place" "Multi.Channelr"
"Ref.Channelr")

(sdedr:define-refeval-window "Ref.Channel.Win" "Cuboid" (position 0 Yfinbuf
Zmaxl) (position Xmaxr Ycap Zmaxr) )
(sdedr:define-refinement-size "Ref.FinChannel" (/ Wsub 1) (/ Hsub 1.0) (/
Ltot 1.0) (/ Wsub 1) (/ Hsub 1.0) (/ Ltot 1.0))
(sdedr:define-refinement-function "Ref.FinChannel" "MaxLenInt" "InGaAs"
"SiO2" 1e-3 1.5)
(sdedr:define-refinement-placement "Ref.FinChannel.Place" "Ref.FinChannel"
"Ref.Channel.Win")

;fin buffer
(sdedr:define-refeval-window "Ref.FinBufWin" "Cuboid" (position 0 0.005
Zfinl) (position Xfinr Ydel Zfinr))
(sdedr:define-refinement-size "Ref.FinBuf" (/ Wfin 5.0) (/ Hchannel 2.0) (/
Lfin 5.0) (/ Wfin 10.0) (/ Hchannel 10.0) (/ Lfin 5.0))
(sdedr:define-refinement-function "Ref.FinBuf" "MaxLenInt" "InAlAs" "Al2O3"
5e-4 1.5)
;(sdedr:define-refinement-function "Ref.FinBuf" "MaxLenInt" "InAlAs" "InGaAs"
1e-3 1.5)
(sdedr:define-refinement-placement "Ref.FinBuf.Place" "Ref.FinBuf"
"Ref.FinBufWin")

;fin channel
(sdedr:define-refeval-window "Ref.FinChaWin" "Cuboid" (position 0 Yfinbuf
Zfinl) (position Xfinr Yfincha Zfinr))
(sdedr:define-refinement-size "Ref.FinCha" (/ Wfin 5.0) (/ Hchannel 5.0) (/
Lfin 5.0) (/ Wfin 10.0) (/ Hchannel 20.0) (/ Lfin 5.0))
(sdedr:define-refinement-function "Ref.FinCha" "MaxLenInt" "InGaAs" "SiO2"
1e-3 1.5)
(sdedr:define-refinement-function "Ref.FinCha" "MaxLenInt" "InGaAs" "Al2O3"
5e-4 1.5)
;(sdedr:define-refinement-function "Ref.FinCha" "MaxLenInt" "InGaAs" "InAlAs"
1e-3 1.5)
(sdedr:define-refinement-placement "Ref.FinCha.Place" "Ref.FinCha"
"Ref.FinChaWin")

;along the channel direction, under the gate
(sdedr:define-refeval-window "Ref.FinGateWin" "Cuboid" (position 0 0 (- Zgl
0.001)) (position Xfinr Yfincha (+ Zgr 0.001)))
(sdedr:define-refinement-size "Ref.FinGate" (/ Wfin 5.0) (/ Hchannel 1.0) (/
Lg 10.0) (/ Wfin 5.0) (/ Hchannel 1.0) (/ Lg 15.0))
```

```
(sdedr:define-refinement-placement "Ref.FinGate.Place" "Ref.FinGate"
"Ref.FinGateWin")

;ion strike
(sdedr:define-refeval-window "Ref.Ion.Win" "Cuboid" (position -0.05 Ycap (-
Zstrike 0.05)) (position 0.05 Ysub (+ Zstrike 0.05)) )
(sdedr:define-refinement-size "Ref.Ion" 0.01 0.5 0.01 0.002 0.05 0.002)
(sdedr:define-refinement-placement "Ref.Ion.Place" "Ref.Ion" "Ref.Ion.Win")
(sdeaxisaligned:set-parameters "minEdgeLength" 1e-3 )
(sdedelaunizer:set-parameters "minEdgeLength" 1e-3 "edgeProximity" 0.3)

(sde:build-mesh "snmesh" "" "finfet_half")
(system:command "tdx -mtt -x -M 0 -S 0 finfet_half_msh  InGaAs_finfet_msh")
******************************************************************************
InGaAs_finfet_des.cmd   ;file name for the single event file
******************************************************************************
File {
      Grid="InGaAs_finfet_msh.tdr"
      Current="InGaAs_finfet_see"
      Plot="InGaAs_finfet_see"
      Parameter="materials.par"}
Electrode {
      {Name="source" Voltage=0}
      {Name="drain" Voltage=0}
      {Name="gate" Voltage=-0.6 Workfunction=4.65 }}
Physics (Region="Buffer") {
      MoleFraction(xFraction=0.48 Grading=0)}
Physics (Region="Finbuffer") {
      MoleFraction(xFraction=0.48 Grading=0)}
Physics (Region="Finbuffers") {
      MoleFraction(xFraction=0.48 Grading=0)}
Physics (Region="Finbufferd") {
      MoleFraction(xFraction=0.48 Grading=0)}
Physics (Region="Caps") {
      MoleFraction(xFraction=0.47 Grading=0)}
Physics (Region="Capd") {
      MoleFraction(xFraction=0.47 Grading=0)}
Physics (Region="Finchannel"){
      MoleFraction(xFraction=0.47 Grading=0)}
Physics (Region="Finchannels"){
      MoleFraction(xFraction=0.47 Grading=0)}
Physics (Region="Finchanneld"){
      MoleFraction(xFraction=0.47 Grading=0)}
Physics {
      EffectiveIntrinsicDensity(NoBandGapNarrowing)
      Mobility(
            ConstantMobility
            Enormal(Lombardi)
            eHighFieldSaturation)
      Fermi
      Recombination(
            SRH
            Auger
            Radiative)
      HeavyIon(
            PicoCoulomb
            Direction=(0,1,0)
            Location=(0,-0.25,0.63)
```

```
            Time=1e-9
            Length=8
            Wt_hi=0.05
            LET_f=0.076
            Gaussian)}
Plot{
      *carrier densities
            eDensity hDensity EffectiveIntrinsicDensity IntrinsicDensity
      *currents and current components
            eCurrentDensity hCurrentDensity
            eCurrentDensity/Vector hCurrentDensity/Vector
            eMobility hMobility eVelocity hVelocity
      *fields, potentials and charge distribution
            ElectricField/Vector
            Potential
            eQuasiFermi hQuasiFermi
            SpaceCharge
      *Temperatures
            LatticeTemperature
            eTemperature hTemperature
      *Doping Profiles
            Doping
      *Band Structure
            BandGap
            ElectronAffinity
            ConductionBandEnergy ValanceBandEnergy
      *Recombination
            SRH Auger
}
Math{
      Number_Of_Threads=4
      Extrapolate
      Derivativites
      Iterations=20
      RelErrControl
      Digits=5
      NotDamped=20
      CNormPrint
      ExitOnFailure
}
Solve{
      Coupled (Iterations=20) {Poisson }
      Coupled (Iterations=20) {Poisson Electron Hole}
      Quasistationary( InitialStep=0.01 Increment=1.5 MinStep=1e-4
MaxStep=0.1 Goal{Name="drain" Voltage=0.5} ){ Coupled{ Poisson Electron
Hole}}
      Save(FilePrefix="Bias")

      Load(FilePrefix="Bias")
      Transient(
            InitialTime=0
            FinalTime=0.95e-9
            InitialStep=1e-13
            MaxStep=1e-10
            Increment=1.2)
            {
                  Coupled{Poisson Electron Hole}
                  Plot (Time=(0.001e-9) FilePrefix="SE_DataA" NoOverwrite)
```

```
		}
	Transient(
		InitialTime=0.95e-9
		FinalTime=2.0e-9
		InitialStep=1e-13
		MaxStep=1e-10
		Increment=1.2)
		{
			Coupled{Poisson Electron Hole}
			Plot (Time=(0.999e-9;1.0e-9;1.05e-9;1.1e-9;1.15e-9;1.2e-
9;1.3e-9;1.4e-9;1.5e-9;1.6e-9;1.7e-9;1.8e-9) FilePrefix="SE_DataB"
NoOverwrite)
		}
	Transient(
		InitialTime=2.0e-9
		FinalTime=30e-9
		InitialStep=1e-12
		MaxStep=2e-10
		Increment=1.2)
		{
			Coupled{Poisson Electron Hole}
			Plot (Time=(2.1e-9;3.0e-9;4.0e-9;5.0e-9;6e-9;7e-9;8e-9;9e-
9;10e-9;12e-9;14e-9;16e-9;20e-9) FilePrefix="SE_DataC" NoOverwrite)
		}
}
```

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