SINGLE-EVENT TRANSIENTS IN INDIUM GALLIUM ARSENIDE MOSFETS FOR SUB-10 NM CMOS TECHNOLOGY

By

Huiqi Gong

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Approved:

Ronald D. Schrimpf, Ph.D.

Daniel M. Fleetwood, Ph.D.

Robert A. Reed, Ph.D.

Michael L. Alles, Ph.D.

Enxia Zhang, Ph.D.

Sokrates T. Pantelides, Ph.D.

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Chapter 1

Introduction

MOSFETs are the building blocks of modern electronics. A modern microprocessor contains billions of transistors. The microelectronics revolution can be characterized by the motto 'smaller is better', due to its cost reduction, enhanced performance and greater efficiency [1]. There are various energetic particles existing in the space, atmospheric and terrestrial radiation environments [2]. These energetic particles generate excess electron-hole pairs while passing through semiconductor devices. The excess carriers then move inside devices through either drift or diffusion process, resulting in a transient current at the device terminals [3]. This transient current, called a single-event transient (SET), may produce soft errors in microelectronic circuits in space applications. As technology scales, soft errors in terrestrial integrated circuits (IC) emerge as one of the most important reliability issues. Many technical conferences, such as the International Reliability Physics Symposium (IRPS), now include sessions on soft errors and single-event effects (SEE) [3].

III-V FinFETs are promising candidates for the sub-10 nm technology due to their effective gate control and superior transport properties [4]. However, obtaining high performance III-V MOSFETs is challenging because of the lattice mismatch between III-V materials and silicon. Most III-V MOSFETs are still integrated on semi-insulating III-V substrates to improve the electronic performance [5]-[14]. To be compatible with current CMOS technology, III-V MOSFETs must be integrated on silicon substrates. Recently, successful integration of III-V FinFETs on 300 mm silicon wafers has been demonstrated, representing significant progress towards application in next generation logic transistors [15]-[18].

The objective of this work is to explore the SET response and charge collection mechanisms of III-V FinFETs on semi-insulating and silicon substrates. Both pulsed laser and heavy-ion irradiation were used to examine the SET sensitivities in these devices. The heavy-ion experiments are of particular interest to the radiation-effects community, because of their analogy to space environments. There is growing interest in pulsed-laser experiments because they are less expensive than heavy-ion experiments, and are non-destructive to semiconductor devices. By changing the pulsed-laser focus position with respect to the devices under test, sensitive area information can be extracted from either peak current or total collected

charge.

Comparisons of SET sensitivity between FinFETs with various fin widths, FinFETs and planar devices, semi-insulating substrate and silicon substrate devices, and various charge injection locations provide systematic understanding of the charge collection mechanisms in III-V FinFETs. Shunt effects and parasitic bipolar amplification effects typically contribute to charge collection in III-V FinFETs. Device level technology computer aided design (TCAD) simulations were used to provide further insight into the charge collection mechanisms. For pulsed-laser irradiation, plasmonic effects resulting from the nanoscale metal-dielectric-metal geometry of the fin structures may play an important role in the most advanced FinFET technologies and future nanowire technologies. Optical simulations were carried out using the Lumerical optical design tool with finite-difference time-domain (FDTD) analysis. This thesis is organized as follows:

Chapter 2 provides brief background information on relevant topics including MOSFET scaling, III-V MOSFETs, radiation environments, and single-event effects. The basic charge collection mechanisms and shunt effects are discussed in this chapter. Previous SETs investigations on both silicon and III-V MOSFETs are reviewed. Parasitic bipolar amplification effects in III-V MOSFETs are discussed in detail. Plasmonic effects on charge generation are introduced. These background topics provide the foundation to understand the work in the following chapters.

Chapter 3 describes the single-event transient response of InGaAs FinFETs with different fin widths. Both pulsed-laser and heavy-ion irradiation were used to study the scaling effects of InGaAs FinFETs. Devices with wider fins collect more charge in both environments. Quantum-well structures confine charge collection in the channel, and determine the sensitive volume. Simulations show that the charge density produced by irradiation is similar for devices with different fin widths, but more charge is collected by wider fin devices due to the larger channel volume. Charge accumulated in the buffer and substrate layers modulates the body potential, altering the degree of backgate control, leading to additional effects associated with charge accumulation in wider fin devices. Optical simulations for a model system suggest that optical phenomena in the fins should be considered for laser testing. These include optical interference, plasmonic enhancement at the metal–dielectric interfaces, and enhanced

electron–hole pair recombination due to multiple reflections in nonplanar devices with nanoscale dimensions.

Chapter 4 describes the plasmonic effect in pulsed-laser induced single-event transients in InGaAs FinFETs. The transient currents in FinFETs and planar MOSFETs with similar stack materials are compared. Enhanced charge collection in the fin region is observed in FinFETs. Plasmonic effects may improve SET sensitivity in the fin region, even with low charge generation efficiency. 3-D TCAD simulations show the transient peaks are mainly due to charge deposition in the channel. The substrate charge collection contributes to the tail current. Optical simulation shows that the enhanced charge deposition in the fin channel is likely due to plasmonic effects. Plasmonic effects may play an important role for pulsed-laser SET characterization of modern CMOS technologies.

Chapter 5 describes the pulsed-laser single-event transient response of InGaAs FinFETs on bulk silicon substrates. Charge collection due to a source-drain shunt effect and drain-to-substrate junction charge collection contribute to the observed transients. The transient response of these silicon substrate devices is compared to that of InGaAs FinFETs on semi-insulating substrates. Faster transients with reduced peak currents and peak widths are observed on the silicon substrate devices. Simulations show hole collection by the silicon substrate. This reduces the amount of source-barrier lowering and bipolar-amplification relative to other III-V devices. Moreover, the reduced hole lifetime in the GaAs buffer layer also contributes to the relative reduction of the bipolar amplification in these devices.

Chapter 6 summarizes the conclusions of the dissertation.

Chapter 2

Background

2.1 MOSFET scaling

MOSFET scaling is best described by Moore's law that the transistor density and performance of integrated circuits doubles every year [1], which was revised to doubling every two years later [19].

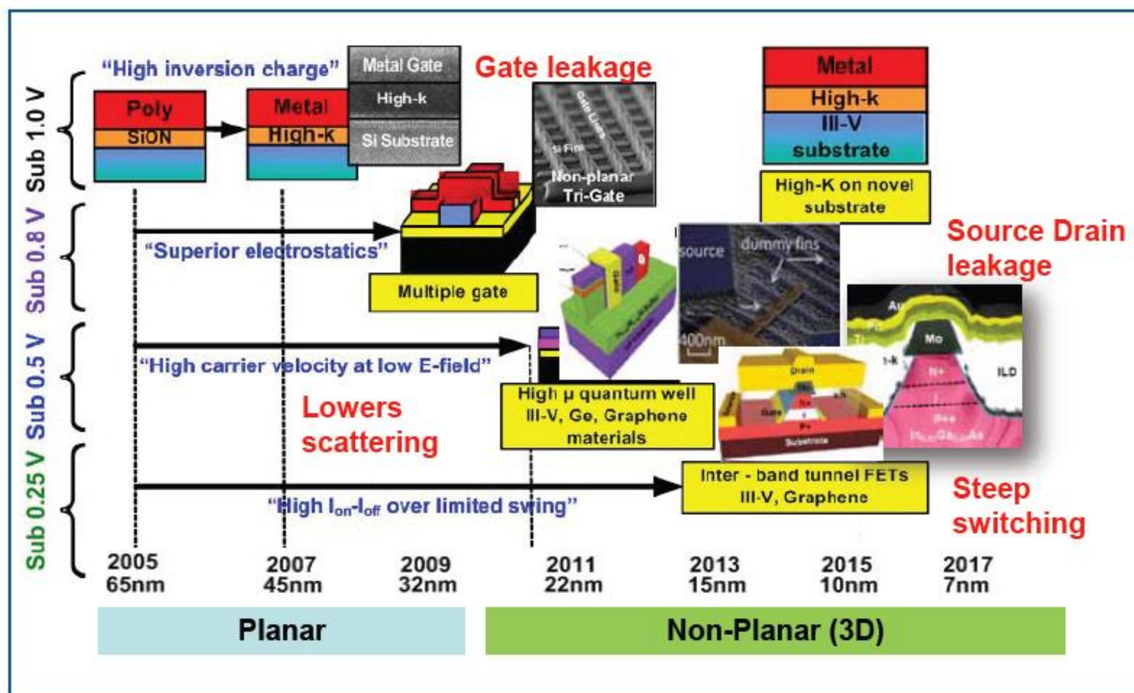


Fig. 2.1. Trend in state-of-the-art high performance (HP) CMOS transistor innovation. Transformative changes in materials (high-k dielectric, Ge, III-V channel) and the transistor architecture (3D, Tunnel FET) being implemented and explored to maintain historical rate of performance, density and power scaling [20].

However, it is becoming more and more challenging to follow the roadmap as the transistor feature size moves to the nanometer region. Several transformative changes in materials and transistor architecture have been implemented and explored to maintain MOSFET scaling, as shown in Fig. 2.1 [20]. Strain engineering was introduced in the 90 nm node to increase both electron and hole mobility [21],

[22]. Metal-gate/high-k gate stacks were introduced in the 45 nm node to reduce the gate leakage and eliminate poly-silicon depletion [23], [24]. The FinFET technology was introduced in the 22 nm node for combating short channel effects [25]-[27]. Vertically stacked gate-all-around (GAA) Si nanowire MOSFETs with excellent short channel characteristics have been developed for the 5 nm node [28]-[30]. GAA architectures offer optimal electrostatic control, thereby enabling ultimate CMOS device scaling [31]. Functional ring oscillators based on GAA MOSFETs have also been manufactured by imec [32]. Fig. 2.2 shows the cross-sectional TEM images of a GAA MOSFET [28]. The devices show excellent short-channel characteristics (SS = 65 mV/dec, DIBL = 42 mV/V) at performance levels comparable to finFET reference devices [28].

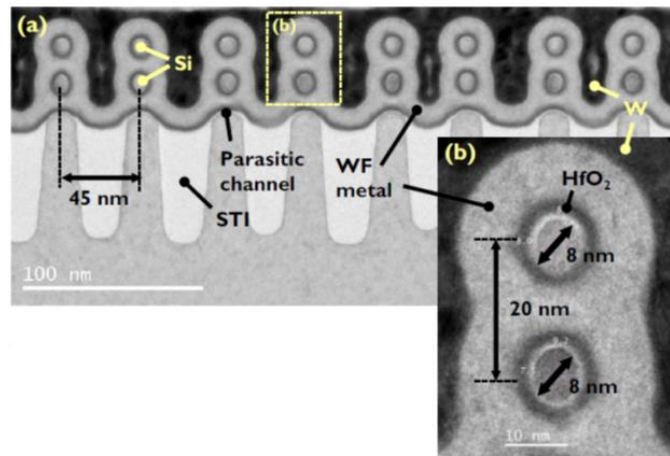


Fig. 2.2. TEM images of an NMOS GAA Si NWFET (L_G = 70 nm): (a) overview of the Si NW array, and (b) detailed view of two stacked Si NWs. The rounded NW shape, the narrow NW size distribution, and the conformally deposited HK/MG layers are clearly visible [28].

2.2 III-V MOSFETs

MOSFET scaling has progressed for decades, but is now limited by power constraints as the power density dissipated by logic chips hits around 100 W/cm^2 [33]. Power density cannot increase much further without incurring substantial packaging and cooling costs. Continued MOSFET scaling will require a reduction in the operating voltage, but this will compromise switching speed [4]. The III-V compound

semiconductors with superior transport properties provide a promising solution to the continued scaling.

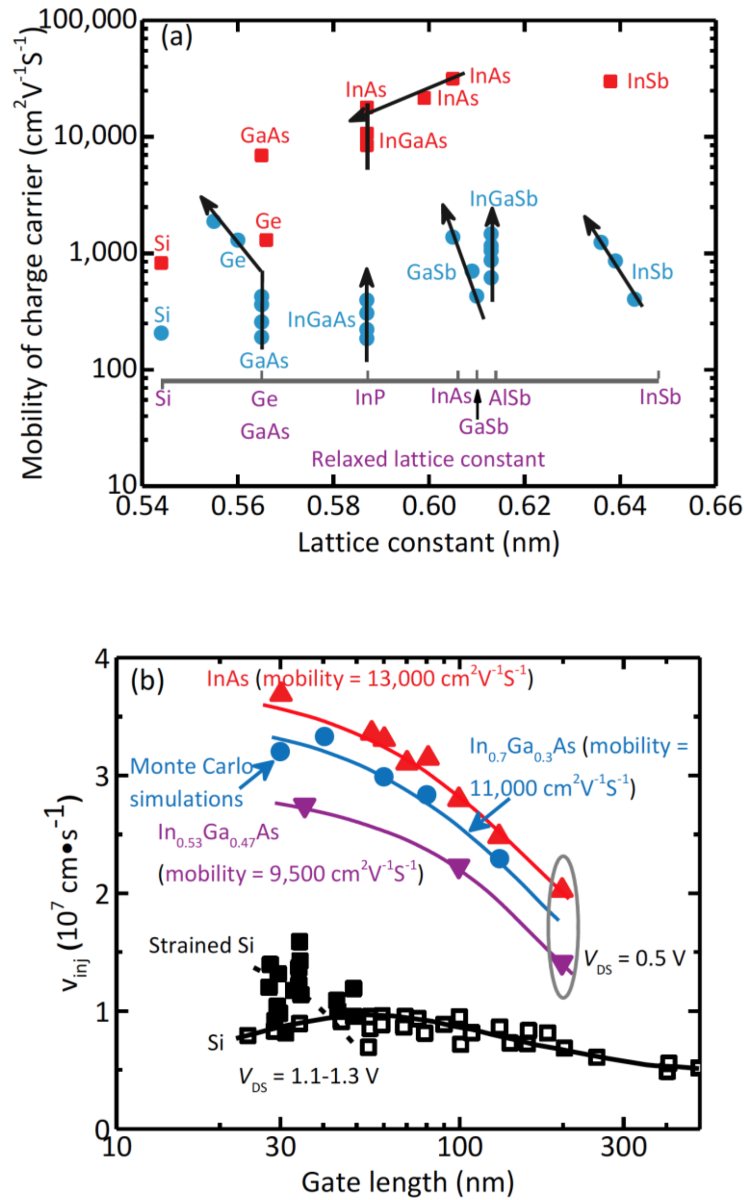


Fig. 2.3 (a) Electron and hole mobility of group III-V compound semiconductors. Electron mobility is marked red and hole mobility is in blue. The arrow indicates the increase of biaxial compressive strain. (b) Electron injection velocity in III-V compound semiconductors [4].

The low field carrier mobility and electron injection velocity of III-V compound semiconductors are shown in Fig. 2.3 [4]. In InGaAs or InAs, the electron mobility is more than 10 times higher than in

silicon at a comparable sheet charge density. For sub-10 nm technology, transistors are operating in the quasi-ballistic region, where carriers experience few scattering events [34]. The drive current, I_{on}, is affected by the injection velocity, v_{inj} [35]:

$$I_{on} \propto v_{inj} Q_i \approx v_{inj} C_i (V_{gs} - V_t) \tag{2.1}$$

Q_i gives the inversion layer charge, and V_{gs}-V_t is the gate overdrive. The injection velocity of III-V materials is more than twice that of comparable silicon MOSFETs at less than half the voltage. As a result, III-V compound semiconductors are promising materials for sub-10 nm technology.

Two main architectures of III-V FETs have been developed, High-Electron Mobility transistors (HEMTs) and MOSFETs. HEMTs made persistent progress since their invention, and have also been turned into a successful transistor technology [36]. Unlike the commercialized silicon MOSFETs and III-V HEMTs, there little progress was made on III-V MOSFETs before the mid-2000s. The initial attempt to fabricate III-V MOSFETs goes back to the 1960s [37]. Unlike the nearly perfect interface between SiO_2 and Si, there are no ideal native oxides for III-V compounds. Recent advances in atomic layer deposition (ALD) of high κ dielectric materials have provided the technology to address this challenge [5],[6]. In order to obtain high quality interfaces to reduce scattering, InGaAs or InAs channels sandwiched between barriers forming high performance quantum-well MOSFETs have been developed [7]. Similar to silicon technology, both InGaAs FinFETs [8]-[11] and InGaAs gate-all-around nanowire transistors [12]-[14] have been developed to reduce short channel effects. InGaAs MOSFETs have now matched transconductance and better ON-resistance compared with InGaAs HEMTs as shown in Fig. 2.4 [36].

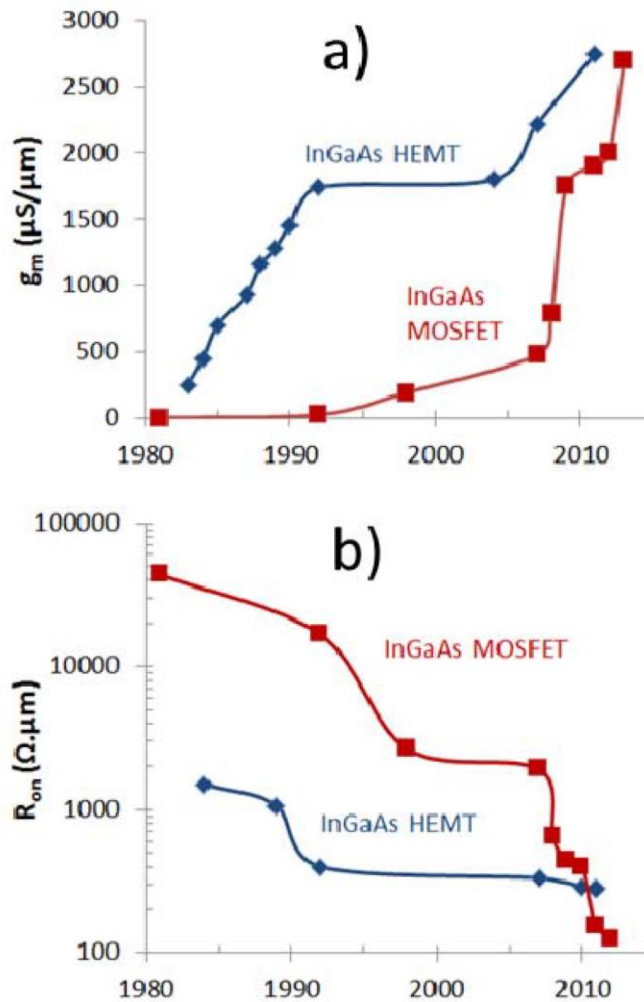


Fig. 2.4. Performance comparison of inversion-type InGaAs MOSFETs and HEMTs (with InAs composition between 0 and 1) vs. year: (a) transconductance, (b) ON resistance [36].

2.3 Radiation environments

Typical radiation environments can be divided into space environments, atmospheric environments, and nuclear reactor environments. Detailed discussions on radiation environments can be found in [2], [38]. All studies in this dissertation are within the scope of space and atmospheric radiation environments; nuclear reactor environments are not discussed in this dissertation.

One of the main source of energetic particles in space environments are particles trapped in the Earth's radiation belts, including electrons, protons, and heavy-ions and cosmic rays, including protons

and heavy-ions. For space applications, devices have to withstand radiation exposure. SEEs are one of the most important issues need to be considered for modern technologies. SEEs are caused when highly energetic particles (e.g., protons, neutrons, alpha particles, or other heavy ions) strike sensitive regions of a microelectronic circuit [3]. They may cause nondestructive effects such as single-event upset (SEU), single-event transients (SET) or potential destructive effects such as single-event latchup (SEL). The physical origin of SEE comes from the charge released by ionizing radiation.

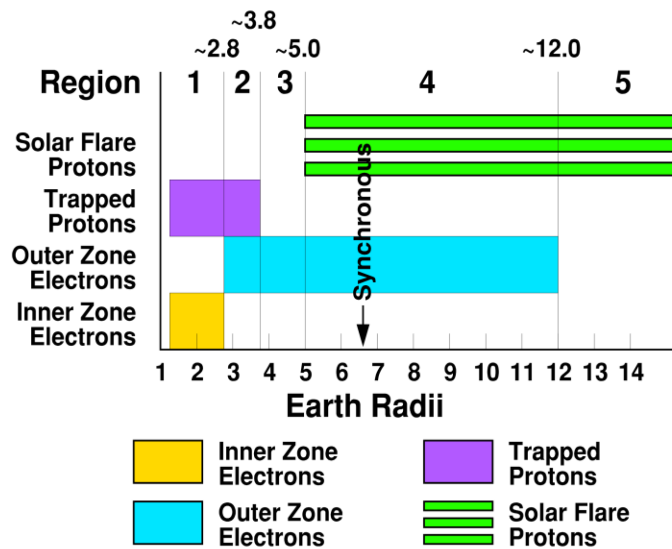


Fig. 2.5. The charged particles trapped by the Earth's magnetosphere [38].

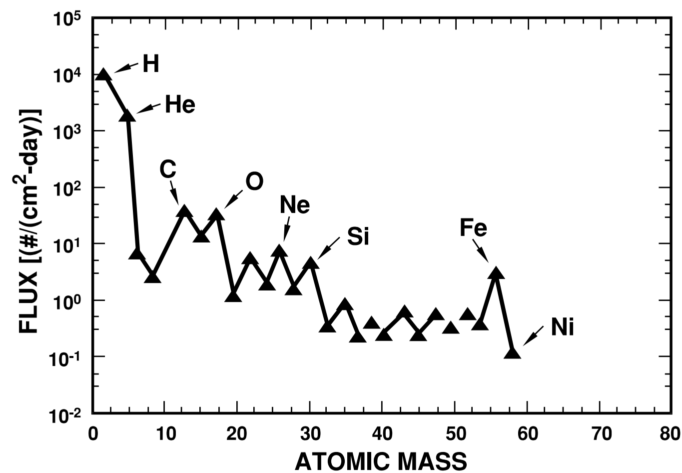


Fig. 2.6. Relative abundance of the elements from hydrogen to the iron group [39].

The particle distributions in the Earth's belts are shown in Fig. 2.5 [38]. Cosmic rays including the galactic cosmic rays and solar cosmic rays include protons and heavy ions. The galactic cosmic ray flux consists mostly of protons and alpha particles. Fig. 2.6 shows the abundance distribution of the elements of the galactic cosmic rays [39]. The solar cosmic rays show similar distributions [39].

As cosmic rays enter the top of Earth's atmosphere, they interact with nitrogen and oxygen atoms and produce a "shower" of secondary particles including protons, electrons, neutrons, heavy-ions, muons, and pions [2], among which neutrons are the most important product. Neutrons can affect avionics through SEEs due to nuclear interactions. The neutron induced SEE rate increases with altitude and latitude [40].

Even for terrestrial level applications, SEEs can play an important role in microelectronic circuits. The energetic particles can interact with back end of line (BEOL) materials, which leads to secondary particles through nuclear reactions [41], [42]. The secondary particles can produce single-event upset in a hardended SRAM [42]. This may produce serious reliability issues for modern technologies, even for terrestrial applications.

2.4 Single-Event Effects

2.4.1 Charge deposition

When an energetic particle passes through a semiconductor device, it will lose energy through Coulomb scattering. The energy loss per unit path for a particle is described by linear energy transfer (LET) [3]:

$$LET = \frac{1}{\rho}\frac{dE}{dx}, \quad MeV \cdot cm^2 / mg \tag{2.2}$$

where ρ is the material density. In silicon, an LET of $97\, MeV \cdot cm^2 / mg$ corresponds to a charge deposition of $1\ pC/\mu m$. The energy loss generates excess electron-hole pairs in semiconductor

materials.

Another efficient way to inject excess electron-hole pairs in a semiconductor is through single-photon absorption (SPA) if the photon energy is above the bandgap [43], or two-photon absorption (TPA) if the photon energy is subbandgap [44]. Semiconductor devices are usually irradiated from the backside to avoid the reflections from metal contacts on top. The sensitive area is typically located near the channel region at the surface. The substrates are usually hundreds of μm thick, which produces a serious absorption problem for SPA. Fig. 2.7 shows the room temperature absorption spectrum of silicon in the visible and near-infrared regions [44]. There is very low absorption in the subbandgap region. At sufficiently high intensities, the material can absorb two photons simultaneously to generate a single electron-hole pair.

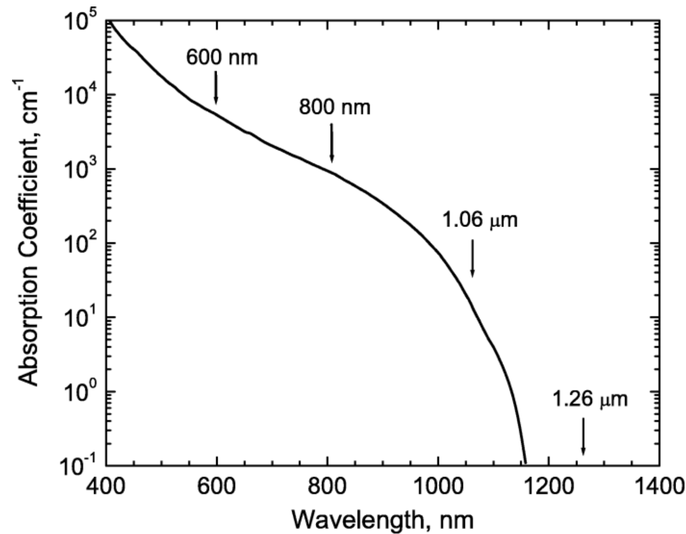


Fig. 2.7. Room temperature absorption spectrum of silicon in the visible and near-infrared region of the spectrum illustrating the common laser wavelengths used for above-bandgap single-event effects measurements and also that for the subbandgap experiment [44].

In TPA, the energy deposited in materials is quadratically dependent on the laser irradiance [45], [46]. Therefore, the carrier generation occurs only in the focused region with high irradiance. This enables 3-D mapping of the SEE sensitivity for a device or a circuit. The following equations show the pulse propagation and charge deposition in a semiconductor material [45], [46]:

$$\frac{dI(r,z)}{dz} = -\alpha I(r,z) - \beta_2 I^2(r,z) - \sigma_{ex} N I(r,z) \tag{2.3}$$

$$\frac{d\Phi(r,z)}{dz} = \beta_1 I(r,z) - \gamma_1 N(r,z) \tag{2.4}$$

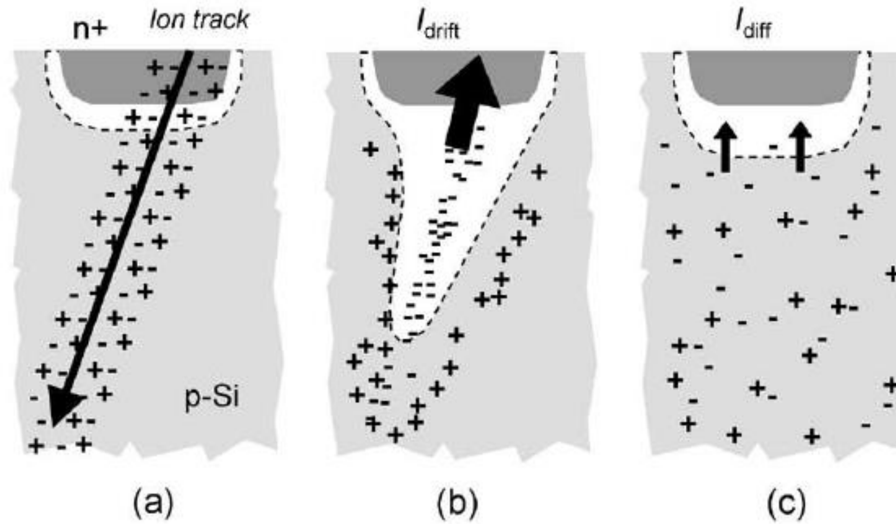
$$\frac{dN(r,z)}{dz} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \tag{2.5}$$

where I is the laser intensity, N is the density of free carriers, Φ is the phase, α is the single-photon absorption coefficient, β_2 is the two-photon absorption coefficient which is proportional to the imaginary part of $\chi^{(3)}$ (the third-order nonlinear-optical susceptibility), σ_{ex} is the absorptivity of generated free carriers, β_1 is proportional to the real part of $\chi^{(3)}$, γ_1 describes the refraction due to free carriers, and z is the depth in the material.

2.4.2 Charge collection mechanism

Once the free carriers are generated either by energetic particles or photons, they can be collected by the terminals at specified bias conditions. The most sensitive regions are reverse-biased p-n junctions due to the high electric field presented in the depletion region. Fig. 2.8 shows the single-event transient by high energy ions and the subsequent charge collection through drift and diffusion in a reverse biased p-n junction [47]. The figure also shows a typical time-dependent current at a struck p-n junction. The figure shows clearly a short-term charge collection process dominated by drift, which contributes to the peak, and a relatively slow process dominated by diffusion, which contributes to the tail.

It is worthwhile to mention that in Fig. 2.8 (b), the electrostatic field is disturbed by the free carriers generated along the ion path, which was termed a “field funnel” [48]. This funneling effect extends the sensitive region from the initial depletion region deep into the substrate, and more carriers will be collected.



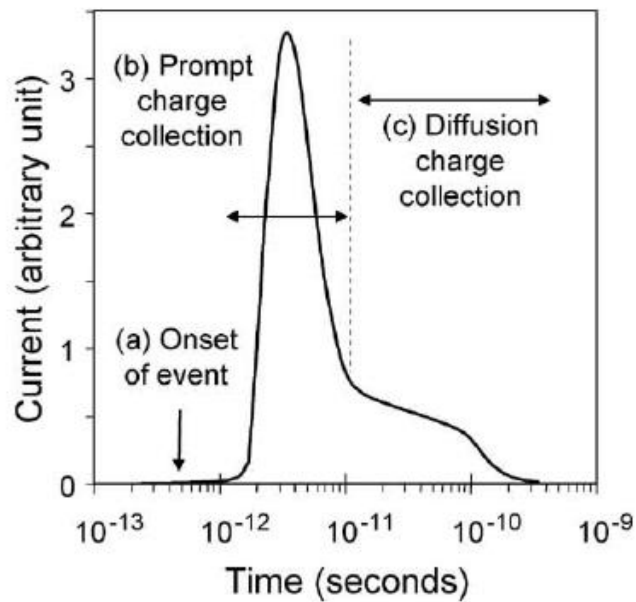


Fig. 2.8. Charge generation and collection phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion [47].

2.4.3 Shunt effect

As technology scales, transistor size reduces such that multiple junctions can be disturbed by energetic particles and photons. A transient conductive path may connect two adjacent junctions due to the high density of free carriers, which was termed a "shunt effect" [49]. Fig. 2.9 shows the schematic of

an ion track shunt effect in a multilayer structure. The high density ion track penetrates both junctions, forming a highly conductive ohmic-like region, and the junction charge collection cannot be considered independently. For most advanced technologies, the shunt effect will form a conductive path along the channel, forming a source-drain conduction current, which contributes to the transient current [50]-[57].

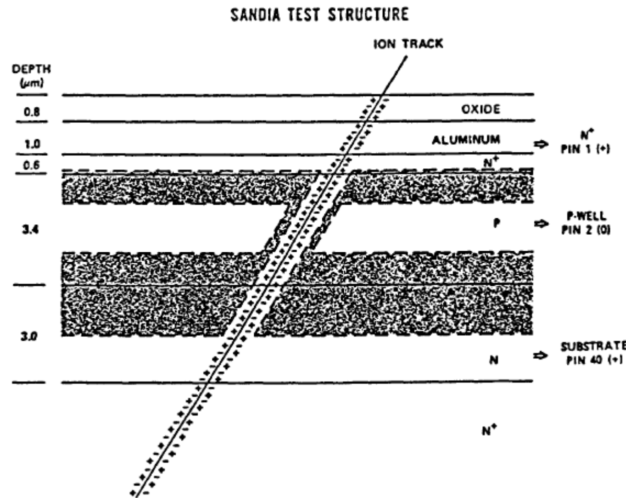


Fig. 2.9. Illustration of ion track shunt effect in two-junction experimental structure [49].

2.4.4 Single-event transient in silicon MOSFETs

As technology scales, modern IC's vulnerability to SEE increases as the sensitive volume decreases dramatically. Fig. 2.10 shows the transient drain currents induced by pulsed laser irradiation in 0.25 μm NMOS and 50 nm NMOS transistors [58]. With comparable pulsed laser irradiation, the smaller device shows smaller peak current with narrower peak width.

The transient response of silicon FinFETs has been explored with both laser and heavy ion experiments [50]-[53]. As the active channel volume decreases, the charge collection in the drain region masks the contributions of the fins [52], [53]. Fig. 2.11 shows the transient drain current with different contact type [53]. A device with larger contact area shows larger drain current. The drain (or source) to substrate junction charge collection contributes significantly in modern technologies. Improving the drain region design provides an effective radiation hardening technique for future technologies.

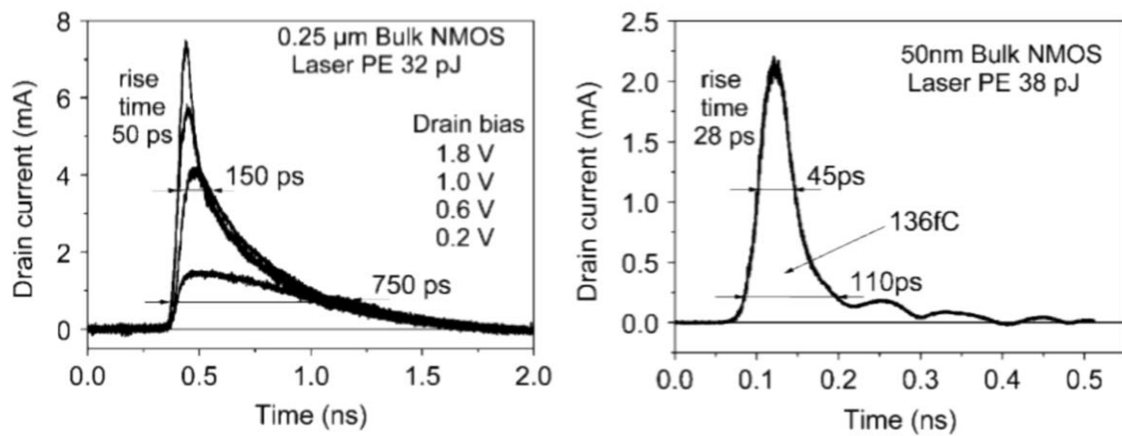


Fig. 2.10. Transient drain currents induced by pulsed laser irradiation in 0.25 μm NMOS and 50 nm NMOS transistors [58].

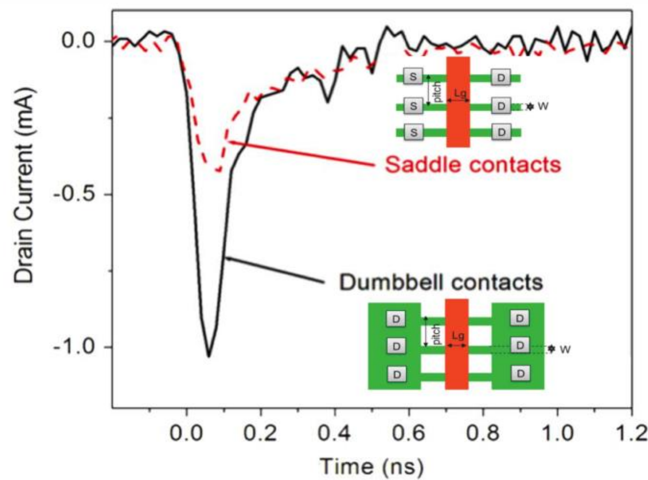


Fig. 2.11. Drain current induced by heavy ion irradiation in bulk FinFETs with different contact type. Solid (black) curve is the largest transient curve that was recorded in a FinFET (W_f/L = 20/70) with dumbbell contacts. The dashed (red) curve is the largest current transient recorded in a FinFET (W_f/L = 20/60) with saddle contacts [53].

2.4.5 Bipolar amplification effect

A significant amount of research focused on SEEs in III-V FETs has been reported [54], [55], [59]-[66]. III-V MOSFETs are found to be more sensitive to SEE compared with Si counterparts. One important reason is the charge enhancement in III-V FETs. Fig. 2.12 illustrates the charge enhancement

mechanism in a GaAs FET [63]. During an ion strike, a high density of e-h pairs is generated along the ion track. The electrons are quickly collected, while holes remain in the active region due to larger effective mass. Holes accumulated near the source reduce the conduction barrier from source to substrate, causing electron injection from source to substrate, and are collected by the drain, which is similar to a bipolar transistor biased at forward active condition. In addition, holes beneath the channel act as a back gate, creating a source-drain current path as long as the excess hole density is present. These charge enhancement effects, unknown as bipolar amplification effects, result in amplification, causing more charge to be collected than was generated.

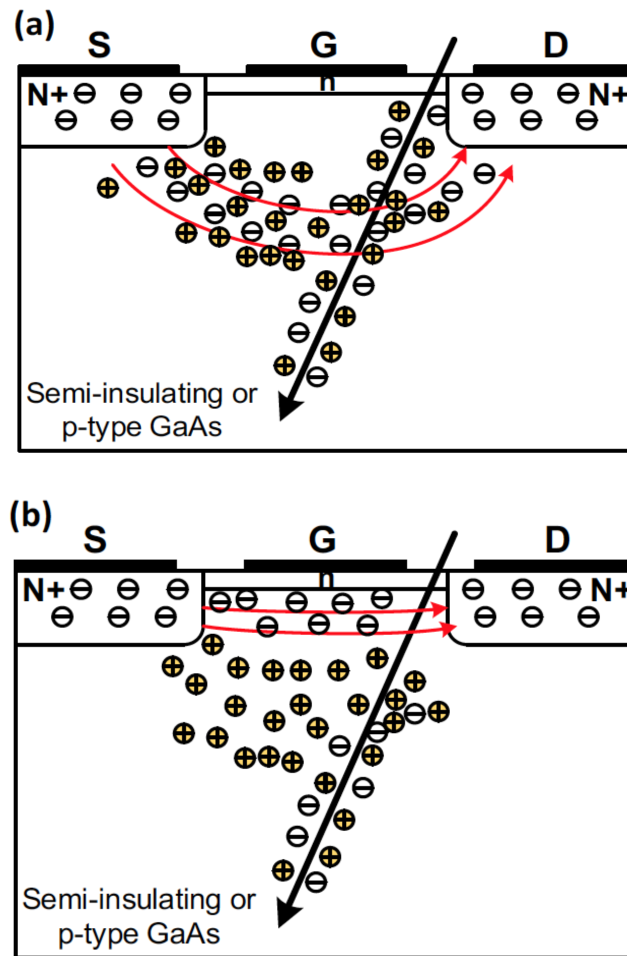


Fig. 2.12. Schematic diagram illustrating (a) the bipolar gain and (b) channel-modulation charge enhancement mechanisms that contribute to the charge collection processes of GaAs FETs [63].

Charge enhancement has been observed in all different kinds of III-V FETs, including III-V MESFETs and HEMTs [63], surface-channel GaAs MOSFETs [66], planar quantum-well InGaAs MOSFETs [65], and quantum-well InGaAs FinFETs [54], [55]. Fig. 2.13 shows the SEE sensitivity dependence on gate length scaling of InGaAs FinFETs [54]. The peak drain current is inversely proportional to the gate length due to the suppressed bipolar amplification effect in long channel devices.

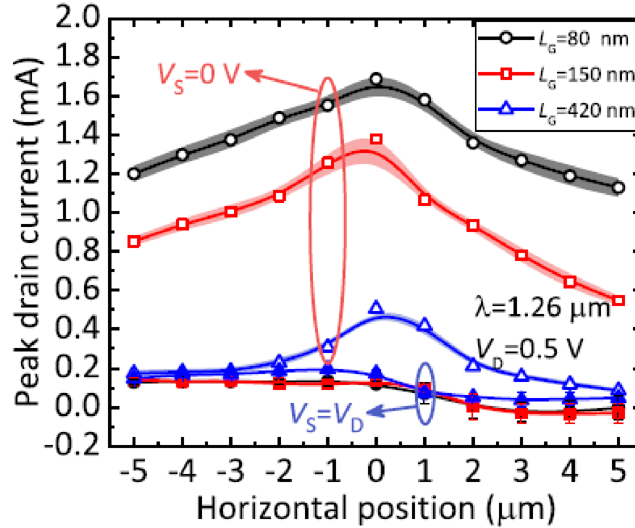


Fig. 2.13. Peak drain current along a line scan for different gate lengths. The laser wavelength λ = 1260 nm. The shadow represents the standard deviation among the 50 transients recorded at each position. $V_G - V_{TH}$ = 0 V. W_{FIN} = 30 nm. Laser pulse energy is 0.65 ±0.01 nJ [54].

2.4.6 Plasmonic effects

Plasmonic effects have been widely investigated in the nano-photonic community, while it has not attracted much attention from the radiation community. As MOSFETs move from planar to 3-D FinFET structures starting from the 22 nm technology node, the plasmonic effect in the narrow fin structures during pulsed-laser experiments may not be ignored. When a pulsed-laser irradiates a nanoscale metal-dielectric interface, the free electrons at the interface between the metal and dielectric medium will oscillate, typically known as "surface plasmons" [67]. Fig. 2.14 shows a surface plasmon at the interface between a metal and a dielectric material [67]. As shown in Fig. 2.14 (a), the electric field component is

normal to the surface. The electric field is maximum at the surface and decays exponentially into both the metal and dielectric material, as shown in Fig. 2.14 (b). The decay length of the field is of the order of half the wavelength of light involved.

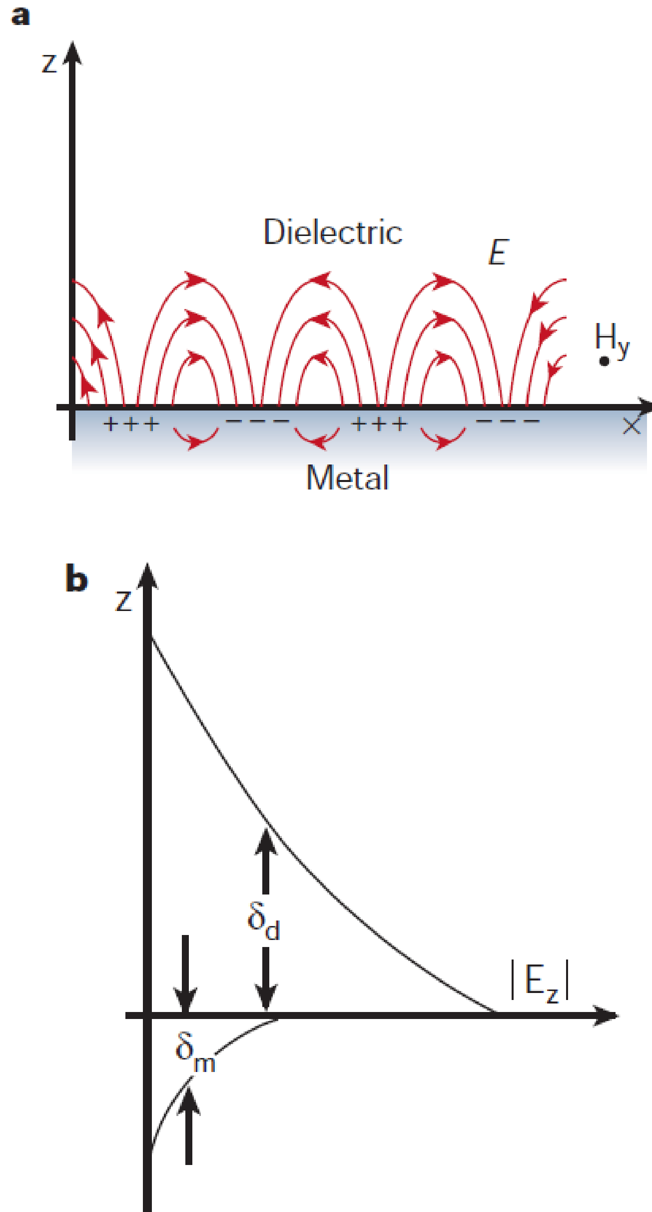


Fig. 2.14. (a) Schematic of surface plasmons at the interface between a metal and a dielectric material. (b) The field component perpendicular to the surface being enhanced near the surface and decaying exponentially with distance away from it [67].

In nanostructures, such as fins in a FinFET, the field is enhanced as the decay length is large compared with the nanostructures. Strong enhanced electric field will be observed in the nanostrucures. This plasmonic enhancement effect has been widely used in nanoscale photonic waveguides [68], [69], modulators [70], photovoltaics [71], [72], Raman spectroscopy [73], [74], and biosensing[75], [76]. Fig. 2.15 shows plasmonic solar-cell design [71]. The plasmonic scattering and coupling by the nanostructure helps improve the solar-cell efficiency. These nano-structures are very similar to fin structures in a FinFET.

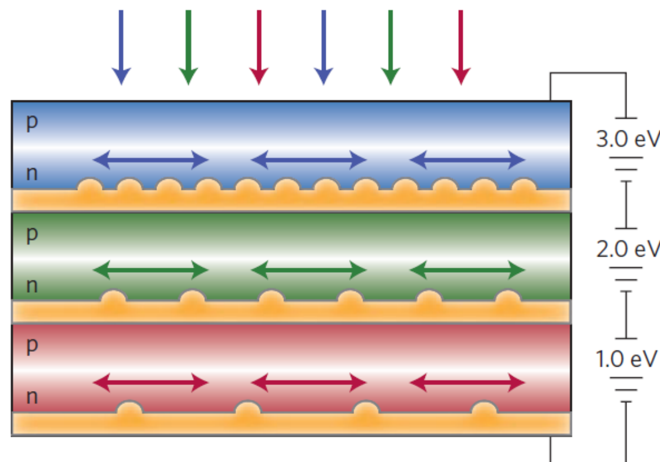


Fig. 2.15. Plasmonic tandem solar-cell geometry. Semiconductors with different bandgaps are stacked on top of each other, separated by a metal contact layer with a plasmonic nanostructure that couples different spectral bands of the solar spectrum into the corresponding semiconductor layer [71].

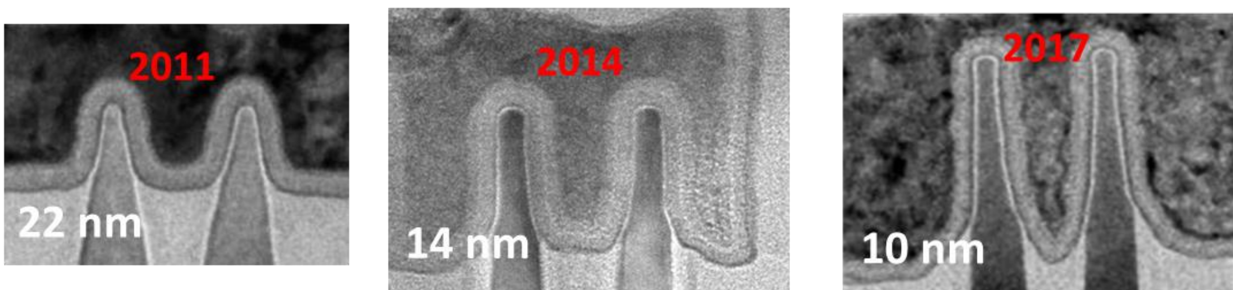


Fig. 2.16. FinFETs evolution in Intel from 22 nm node to 10 nm node [78].

The FinFET technology was first introduced in 2001 by Hu, et al. from the University of California, Berkeley [77]. It is now the mainstream technology. Fig. 2.16 shows the FinFET structure in Intel from 22 nm node to 10 nm node [78]. It is a metal/dielectric/metal stack along the fin width direction. Surface plasmons may be generated along the metal dielectric interface during pulsed-laser SET experiments. The fin width in Intel's 10 nm technology is 7 nm, which is much smaller compared with the electric field decay length. Strong electric field enhancement due to surface plasmons may enhance the charge deposition inside the narrow fin region.

There has been much effort to convert measurable pulsed-laser energy to equivalent LET in order to make comparisons with heavy-ion experiments [79]. One efficient way is to compare the transient shapes from pulsed-laser and heavy-ion irradiation experimentally. The correlation between these two types of experiments strongly depends on the facilities and the experiment conditions. The other path is to use theoretical calculations to predict the pulsed-laser induced carrier generation, and convert the charge deposition to equivalent LETs [80], [82]. Optical effects, such as plasmonic effects, may be incorporated into the calculations to improve the accuracy.

Chapter 3

Scaling effects on single-event transients in InGaAs FinFETs

3.1 Introduction

Incorporation of compound semiconductors is a promising candidate to address scaling challenges beyond the 7 nm node due to their outstanding electron transport properties [4]. Their high electron mobility and high frequency response make these devices an ideal option for many space applications [4], [59], [60]. A significant amount of research focuses on single-event effects in these devices [59]-[66]. Most of these works consider III-V planar MESFETs and HEMTs. Only limited work describing the SEE response of III-V FinFETs has been reported. InGaAs and Ge complementary FinFET technology is promising for next generation NMOS/PMOS FETs. Recent work suggests that SEE in circuits built in this technology are likely to be dominated by ion strikes on the InGaAs FinFET [54].

Fin geometry is optimized for device electrical performance and manufacturability of a given process. Dimensions can scale as process generations scale, and vary among manufacturers and even within a single process [4]. From the 22-nm technology node to the 10-nm technology node, fin height increases while fin width decreases [78]. The gate length dependence of the single-event transient response of InGaAs FinFETs has been evaluation by Ni et al. using a high-speed pulsed-laser system [54]. The peak drain current was found to increase as the gate length decreased, which suggests that parasitic bipolar action is fully suppressed in longer channel devices [54]. In this chapter, we evaluate the impact of fin width on the SET response of InGaAs FinFETs via pulsed-laser and heavy-ion irradiation. Over all, the trends observed in pulsed-laser irradiation are consistent with those of heavy-ion irradiation. However, there are a few differences. In both situations, devices with wider fins collect more charge, due to their greater sensitive volumes. Charge accumulated in the buffer and substrate modulates the body potential, leading to additional charge collection in wider fin devices. Finite-difference time-domain simulations for a model system carried out using Lumerical [83] show that optical intensity is modulated inside narrow fins during laser irradiation. As technology scales, this optical modulation is important to consider.

3.2 Device structure and experimental setup

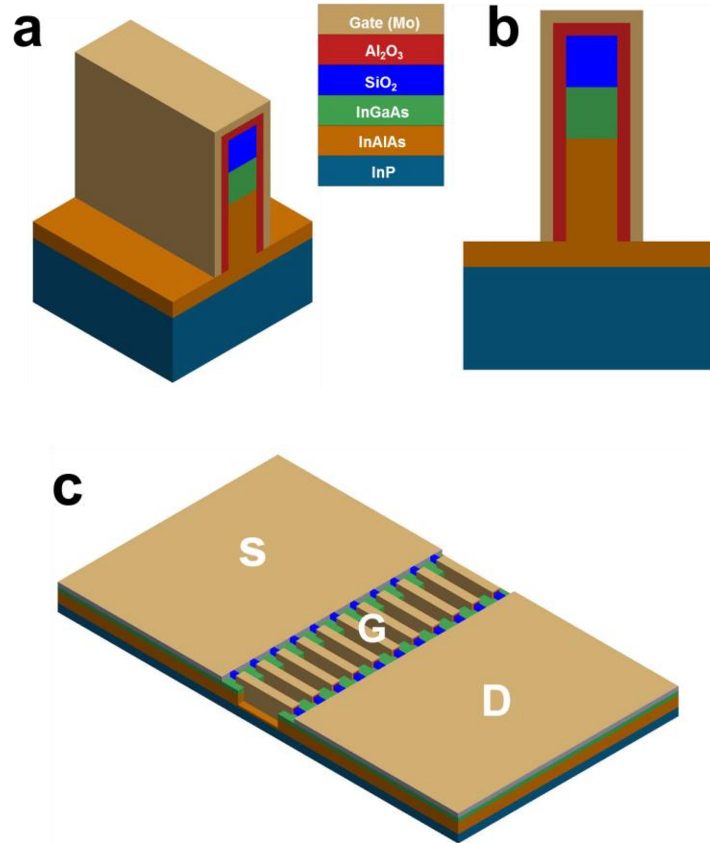


Fig. 3.1. (a) 3D qualitative representation of the fin structure of the InGaAs double-gate FinFETs, (b) cross-section along the fin width direction, and (c) 3D schematic diagram of 11 fin InGaAs double-gate FinFETs. Gate (G), drain (D), and source (S) are labeled on the diagram. (Not drawn to scale)

The device under test is a double-gate InGaAs FinFET [84]. A 3D qualitative view of the device is shown in Fig. 3.1c; layers are not drawn to scale. Details of the fin structure are shown in Fig. 3.1a. Fig. 3.1b shows a cross-sectional diagram along the fin width direction of a single fin structure. There are 11 fins in parallel for each device, with 0.8 μm pitch between fins. The height of each fin is 220 nm, with a 40 nm thick $In_{0.53}Ga_{0.47}As$ channel layer, and the gate length is 100 nm for all devices reported here. Under the channel, a 0.4-μm $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600-μm semi-insulating InP substrate. 40 nm of SiO_2 serves as a hard mask, which electrostatically decouples the top gate from the

channel. As a result, devices are only controlled by the two side gates. A 5-nm Al_2O_3 gate dielectric is deposited by atomic layer deposition. A silicon delta doping layer 5 nm below the channel is used to enhance channel electron density. The detailed fabrication process is described in [10]. Fig. 3.2a and b show the energy band diagrams in the fin width and fin height directions, respectively.

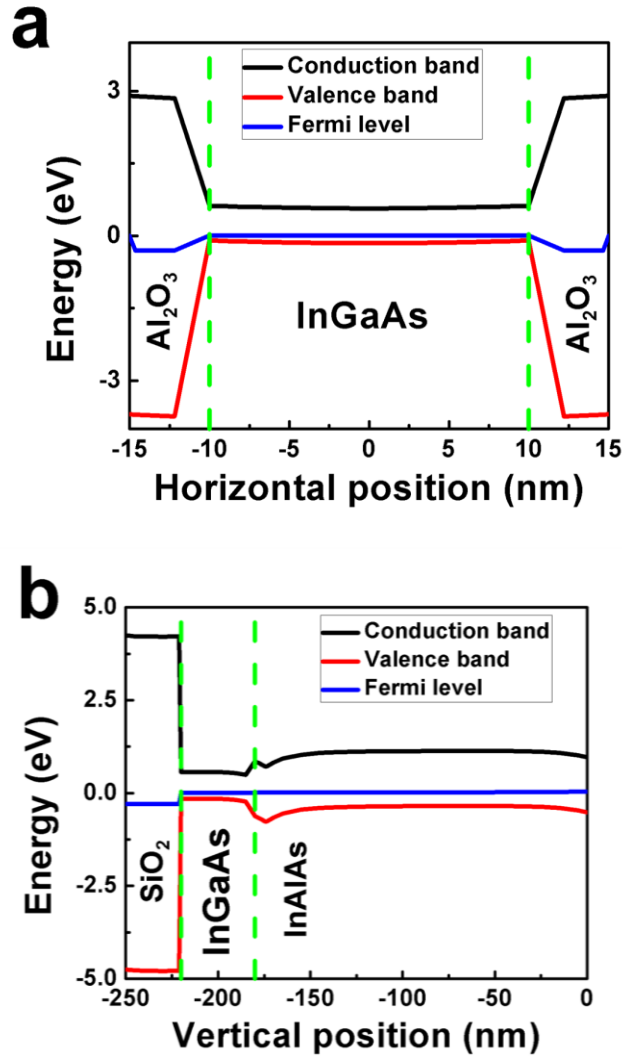


Fig. 3.2. Band diagrams cut through the fin structure along the (a) fin width direction and (d) fin height direction.

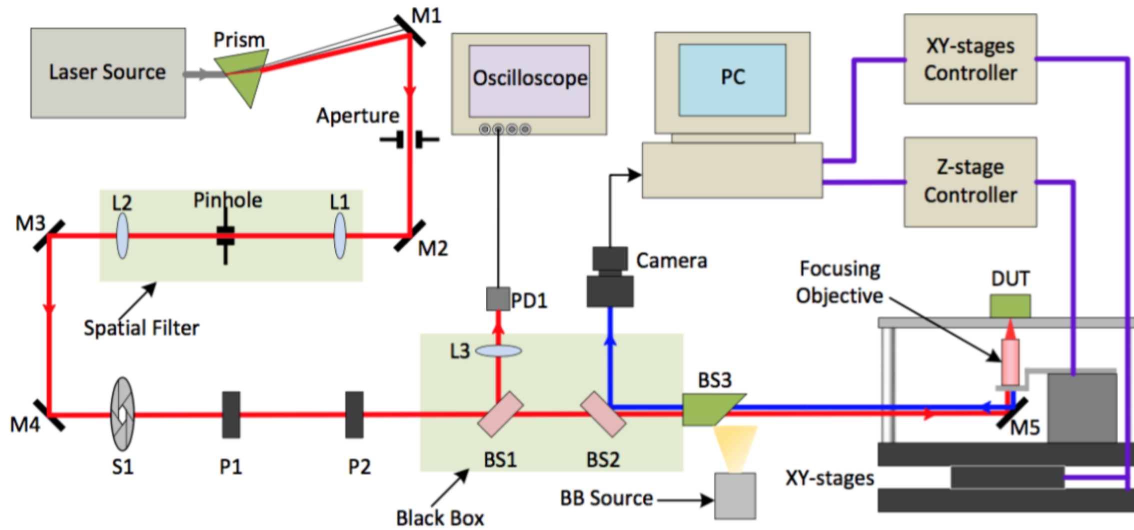


Fig. 3.3. A simplified block diagram of TPA test setup. In the figure, ‘L’ stands for lens, ‘M’ stands for mirror, ‘S’ stands for shutter, ‘P’ stands for polarizer, ‘BS’ stands for beam splitter, ‘PD’ stands for photodiode, and “BB” represents the broadband light source. The red line indicates the optical path traveled by the laser beam. The blue line indicates the reflected light that is imaged by the near infrared camera [54].

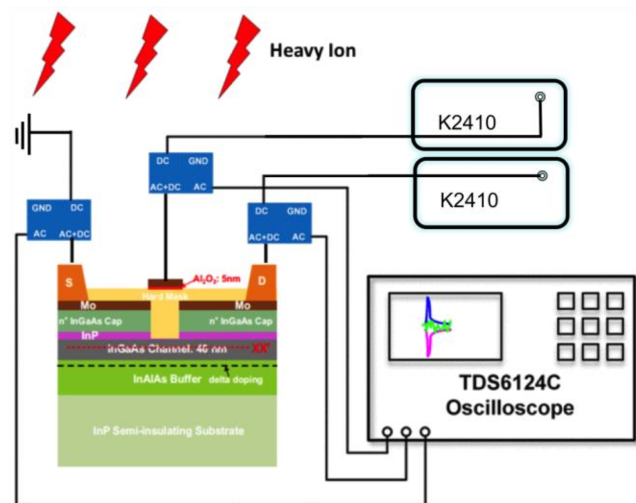


Fig. 3.4. Schematic diagram of the heavy-ion experiment setup. Two Keithley 2410 working as SMUs for gate and drain terminals. The source terminal is grounded by a 50 Ω terminator.

Devices with different fin widths were tested with both pulsed-laser and heavy-ion irradiations. A tunable wavelength laser system and high resolution transient capture system are used for laser testing.

The pulsed-laser testing experiments were performed at Vanderbilt University. The laser system setup is shown in Fig. 3.3. The laser system generates 150 fs pulses with 1 kHz repetition rate. The laser wavelength in this experiment is 1260 nm with spot size of approximately 1.2 μm [85]. As shown in Fig. 3.3, the devices under test (DUTs) are irradiated from the backside by focusing the pulsed-laser spot such that the channel region is contained within the charge generation region from the laser pulse. The heavy-ion experiments were performed with the 88 inch cyclotron at Lawrence Berkeley National Laboratory (LBNL). Fig. 3.4 shows the schematic diagram of the experiment setup.

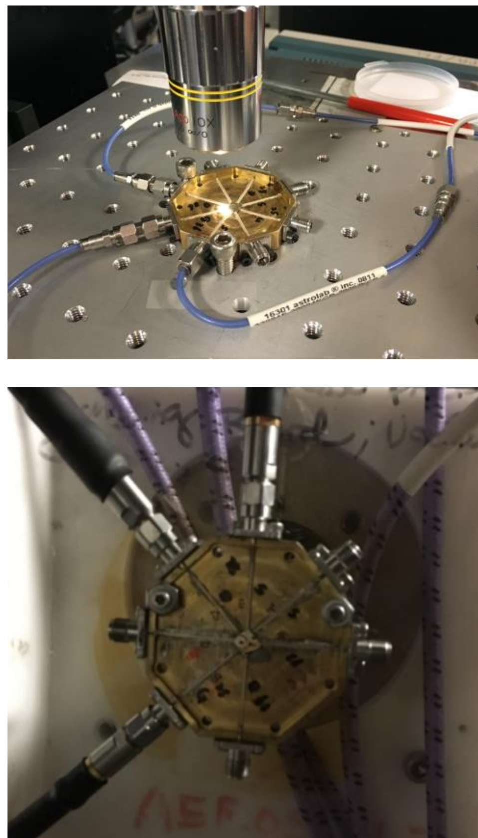


Fig. 3.5. Brass high-speed packages for pulsed-laser experiments (top) and heavy-ion experiments (bottom).

Transients are captured using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36-GHz front-end bandwidth and 80 GS/s sampling rate for pulsed-laser experiments and a Tektronix TDS6124C oscilloscope with 12 GHz front-end bandwidth and 20 GS/s-sampling rate for heavy-ion experiments. The DC bias is supplied with a semiconductor parameter analyzer, HP 4156A, for pulsed-laser experiments

and Keithley 2410 for heavy-ion experiments, through bias tees with 50-GHz bandwidth. The DUTs are mounted and bonded in a brass high-speed package with RF connectors [86]. Fig. 3.5 shows the InGaAs FinFETs mounted on high-speed packages used in the pulsed-laser experiments and heavy-ion experiments.

3.3 Experimental results and discussion

3.3.1 Pulsed-laser induced charge generation

The pulsed-laser wavelength used in the experiment is 1260 nm, corresponding to a photon energy of 0.98 eV, which is above the band gap of $In_{0.53}Ga_{0.47}As$. Table 3.1 lists the charge generation mechanisms in the materials used in the devices. Both two-photon absorption (TPA) and single-photon absorption (SPA) mechanisms contribute to charge generation in the InGaAs channel, while only TPA contributes to charge generation in the InAlAs and InP layers.

Table 3.1. Charge generation mechanism for 1260 nm laser

Material	**Band gap (eV)**	**Photon absorption mechanism**
$In_{0.53}Ga_{0.47}As$	0.75	SPA/TPA
$In_{0.52}Al_{0.48}As$	1.46	TPA
InP	1.35	TPA

Fig. 3.6 shows a typical laser-induced transient for a pulse delivered to the center of a device with fin width of 40 nm under a bias condition of $V_D = 0.5$ V, $V_S = 0$ V, and $V_G = V_{th}$, where V_{th} is the threshold voltage of the devices with initial value in the range of -0.1 ±0.1 V. The spot size of the incident Gaussian beam is approximately 1.2 μm, as determined via a typical knife-edge measurement at the beam waist [85]. The maximum peak current is achieved when the center (maximum intensity) of the laser spot is

located on the fin. The radius of the spot (0.6 μm) is smaller than the fin pitch (0.8 μm), which localizes the irradiation on a single fin. Transient signals are recorded mainly on the drain and source; the peak gate current is negligible. This occurs because, across the fin width direction, the InGaAs channel and Al_2O_3 gate dielectric form a deep type-I quantum-well. Along the fin height direction, the InGaAs channel, InAlAs buffer, and SiO_2 also form a type-I quantum-well, as shown in Fig. 3.2a and b. Thus, carriers generated by irradiation are confined in the channel layer once they have been collected. This makes the channel layer critical to the charge collection. The transients on drain and source are symmetric for various strike locations, which suggests the transient current comes mainly from channel collection. There is a tail (compared with the prompt peak current) on the transient signal, which is consistent with previous work on planar III-V MOSFETs [65] and FinFETs [54]. The tail current in Fig. 3.6 is mainly caused by charge collection from the substrate. Charge generated more deeply within the substrate leads to a longer time for carriers to transport into the channel. This response differs significantly from bulk Si FinFETs, where no tail current is observed within the transient signal [52]. This is because most deposited charge in the substrate of a Si bulk FinFET is collected by the substrate contact through the conductive substrate, instead of the source or drain. All peak drain currents in this chapter are reported as absolute values. For both laser and heavy ion tests, the total collected charge is based on integration of current vs. time beginning and ending at 10% of the peak value.

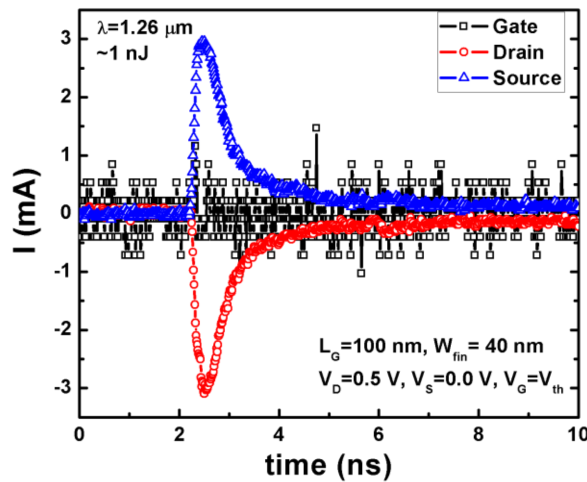


Fig. 3.6. SET captured during TPA testing for an InGaAs FinFET. L_G = 100 nm, W_f = 40 nm.

Figs. 3.7a and b show peak drain current and collected charge along a line scan from source to drain for devices with different fin widths. There is some spatial asymmetry; the peak drain current is higher when the laser is on the drain side, due to the higher electric field on the drain side. Both the peak drain currents and collected charge for narrower fin devices (W_{fin} = 20 nm) are much smaller compared with wider fin devices (W_{fin} = 30 nm and 40 nm).

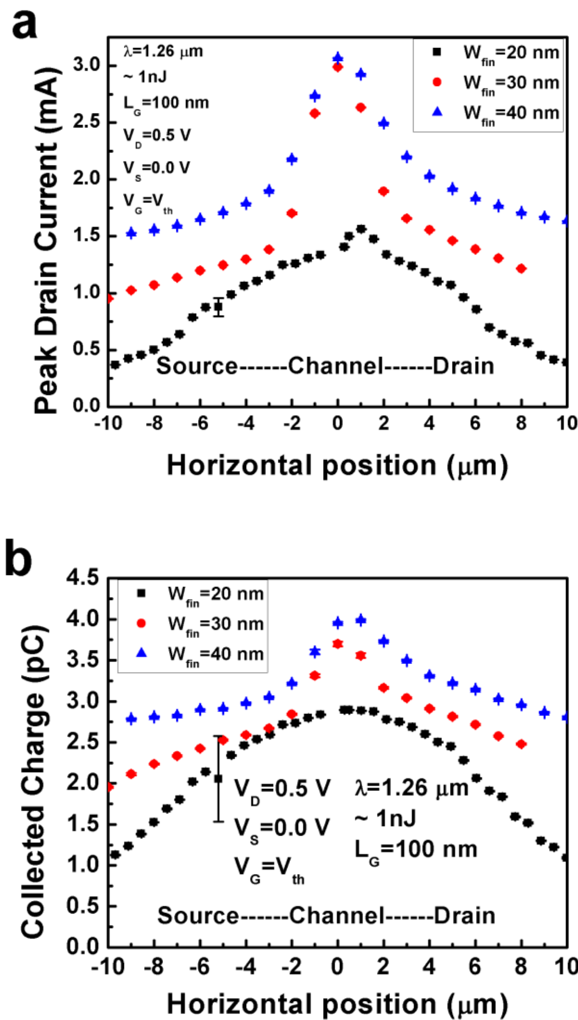


Fig. 3.7. Peak drain current (a) and drain collected charge (b) along a line scan for InGaAs FinFETs of different fin widths during TPA testing.

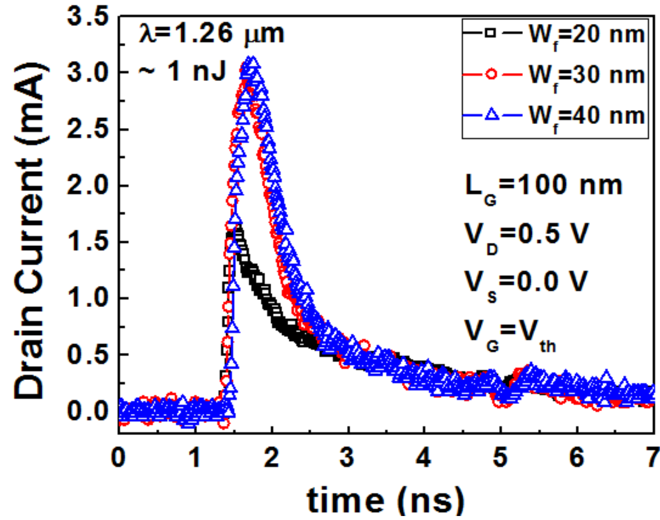


Fig. 3.8. Drain current transients for InGaAs FinFETs of different fin widths during TPA testing (peak drain current is taken as absolute value). The laser strike is at the center of the gate.

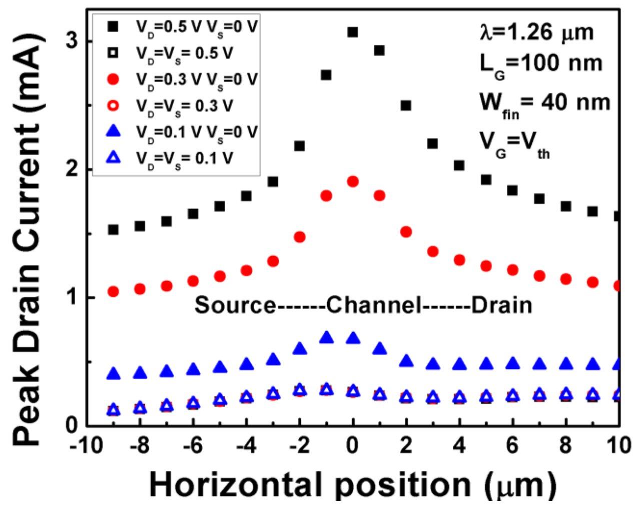


Fig. 3.9. Peak drain current along a line scan at different drain bias during TPA testing. W_f = 40 nm, L_G = 100 nm.

A comparison of drain current transients for devices with different fin widths is shown in Fig. 3.8. For the 20 nm fin width device, peak currents are much smaller than for 30 nm or 40 nm fin widths. The tails of the transients overlap for all three devices, because all devices have the same substrate material and geometry, leading to similar charge collection from the substrate in all cases. Charge collection of the

charge injected in the channel produces the prompt increase in current. Even though all transients have similar tails, the integrated collected charge is much smaller for the 20 nm devices due to the lower peak current.

The peak drain current along a line scan at different drain biases is shown in Fig. 3.9. Higher drain bias produces a stronger electric field, resulting in higher peak drain current. When the drain and source are biased at the same potential, the electric field along the channel is a minimum. The peak drain current is much lower when the source and drain are tied together. This is consistent with previous studies in InGaAs FinFETs [54], and differs significantly from Si and SiGe FinFETs, for which larger charge collection occurs typically at the S/D junctions [52], [53], [87]. Hence, the detailed nature of the gate materials and/or presence or absence of quantum well structures can fundamentally alter the charge collection in FinFETs based on compound semiconductor materials, causing parasitic bipolar effects [54].

3.3.2 Heavy-ion induced charge generation

The heavy ions used in this experiment are Xeon, Krypton, Argon, and Neon. Table 3.2 lists the linear energy transfer (LET) in $In_{0.53}Ga_{0.47}As$ and energy of these ions.

Table 3.2. Ions that comprise the LBNL 10 MeV/u cocktail

Ions	LET (MeV cm^2/mg)	Energy (MeV)
Ne	2.4	216
Ar	6.4	400
Kr	20	886
Xe	40	1233

Fig. 3.10 shows typical heavy-ion induced transients for a device with fin width of 40 nm biased at $V_D = 0.5$ V, $V_S = 0$ V, and $V_G = V_{th}$. The peak current produced by the 40 MeV cm^2/mg Xe ion is similar to that measured in previous studies [65] of heavy-ion induced charge collection in planar InGaAs

MOSFETs irradiated with 14.3 MeV oxygen ions, which has a lower LET of 3.9 MeV cm^2/mg in $In_{0.53}Ga_{0.47}As$. This suggests that planar InGaAs MOSFETs are more sensitive to SET than FinFETs due to the larger sensitive volumes for planar devices.

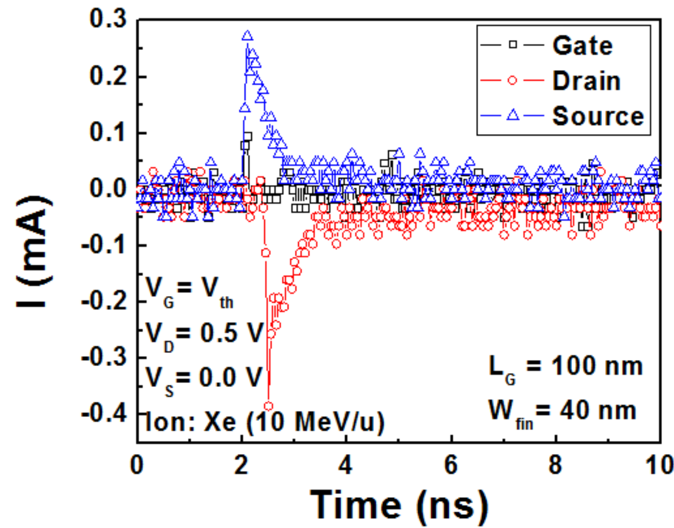


Fig. 3.10. SET captured during heavy ion testing for an InGaAs FinFET. L_G = 100 nm, W_f = 40 nm.

The heavy-ion induced transient currents in Fig. 3.10 are much smaller than the laser-induced transients in Figs. 3.6 and 3.8 because the laser pulse energy used generates a larger amount of charge in and near the sensitive volume than that generated by these particular ions. There is asymmetry on the drain and source transient signals, where the peak drain current shows a delay, compared with the peak source current. In contrast, there is no delay in the pulsed-laser induced SET. This is mainly due to the limited oscilloscope temporal resolution (50 ps) for the heavy ion tests rather than any device-level effects. In Fig. 3.10, a single data point is recorded on the rising edge, which may miss the real peak value. All laser tests are done with an oscilloscope with time resolution of 12.5 ps, which is capable of more precise peak current measurement than that of the oscilloscope available for the remote-site heavy ion testing. The time delay is also likely affected by the signal paths being slightly different, caused by variation in cable length and feedthroughs.

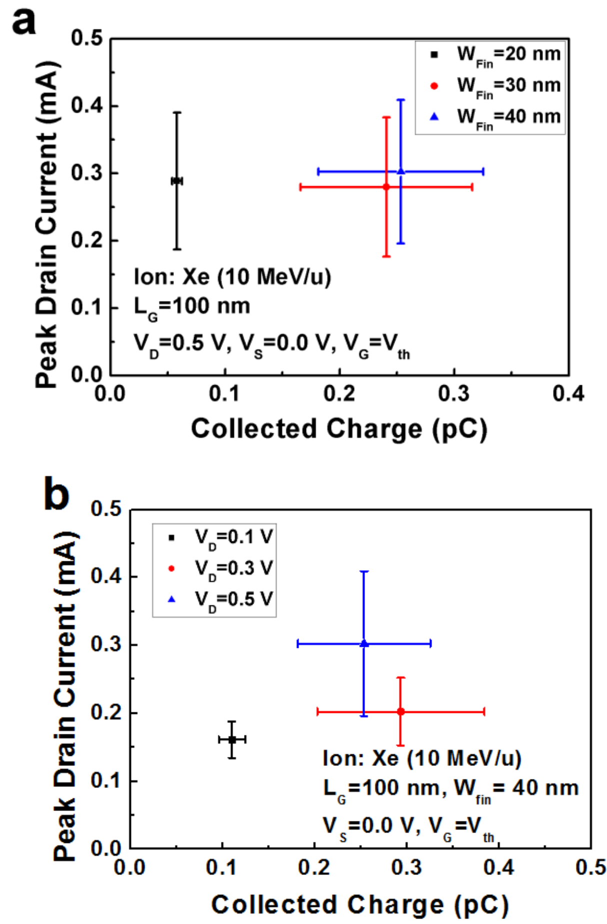


Fig. 3.11. Collected charge and peak drain current during Xe irradiation for devices with different fin width (a) and drain bias (b). Each data point is averaged from 50 transient events.

Fig. 3.11a shows collected charge vs. peak drain current for 10 MeV/u Xenon ion irradiation of devices with different fin widths. Each data point is averaged from 50 transient events. The 20 nm fin-width device shows much less charge collection than the 30 nm and 40 nm fin width devices, consistent with the pulsed-laser results. The peak current is independent of fin width, which is different from the pulsed-laser results. This result is most likely caused by differences between spatial and temporal charge distributions generated by pulsed-laser and heavy-ion irradiation. For example, in pulsed laser testing, a large amount of charge is generated at the focal point. In heavy-ion testing, much less charge is generated in surrounding regions of the device. Moreover, the optical phenomena discussed in

Section V for laser irradiation do not apply in ion testing. Fig. 3.11b shows collected charge and peak drain current for a 40 nm device at different drain biases. Higher drain bias leads to higher peak drain current. There is no transient observed if the drain and source are biased at the same potential.

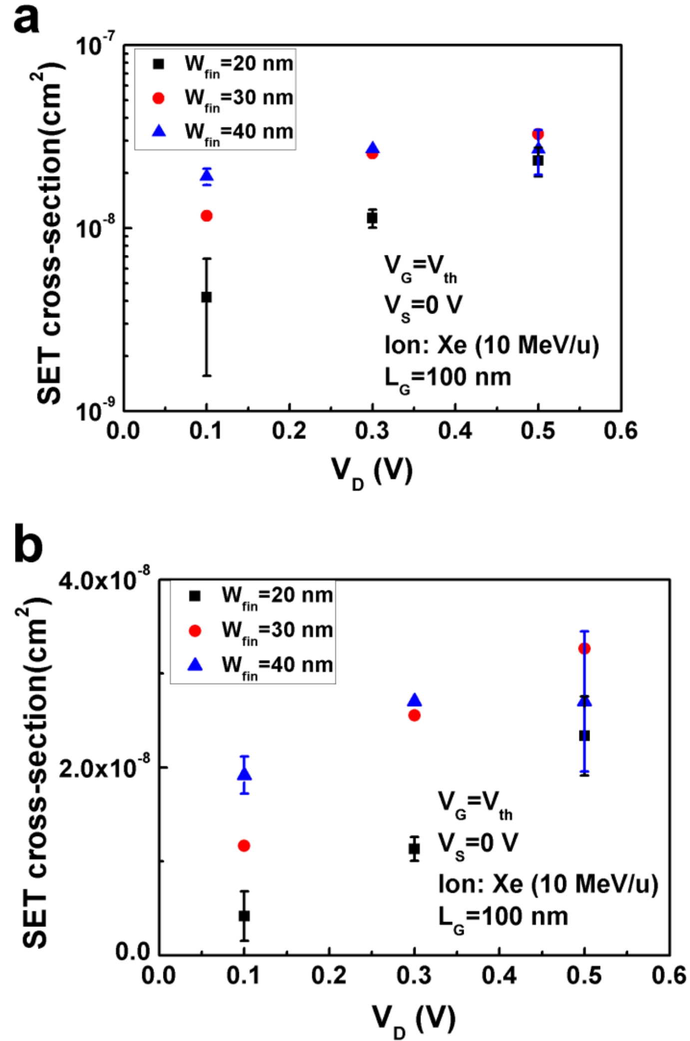


Fig. 3.12. SET cross-section vs. V_{DS} for InGaAs FinFETs with different fin widths (a) log scale and (b) linear scale. Each data point is averaged from 50 transient events.

The SET cross-section has been calculated in the usual way:

$$\sigma = \frac{N}{\phi \cdot t} \tag{3.1}$$

where σ is the SET cross-section, N is the number of transients observed, ϕ is the ion flux, and t is the observation time.

Fig. 3.12 shows the SET cross-section for devices under 10 MeV/u Xenon irradiation. The minimum detectable event was 40 μA peak current for all tests. Each cross-section result is averaged from two tests. The SET cross-section shows a strong dependence on fin width. Narrow fin devices show smaller cross-sections compared with wider fin devices.

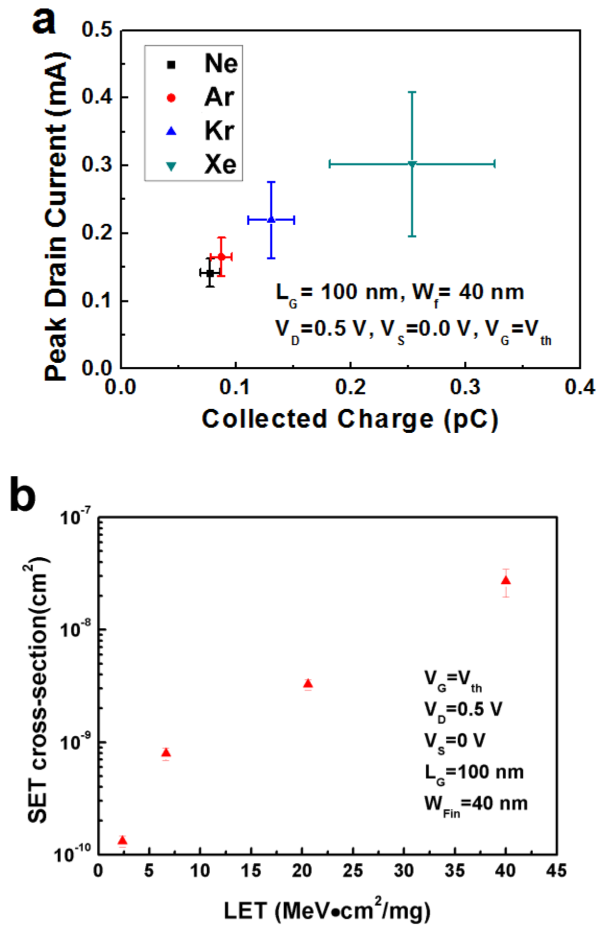


Fig. 3.13. (a) Collected charge, peak drain current and (b) SET cross-section for a 40 nm device with heavy-ion irradiation at different LET in $In_{0.53}Ga_{0.47}As$.

By irradiating devices with various ions, LET effects on charge collection are investigated. Fig. 3.13a shows the peak drain current and collected charge for a 40 nm fin width device irradiated with ions of

different LETs. As expected, more charge is collected for particles with higher LETs, and thus higher peak currents. Fig 3.13b shows the SET cross-section for a 40 nm fin width device irradiated with different ions. The SET cross-section increases as LET increases, and no saturation cross-section is observed. This response is not surprising because the area of the devices (1.8×10^{-7} cm^2) is larger than the observed cross-sections.

3.4 TCAD Simulations

3.4.1 Geometric effect

3-D TCAD simulations were performed with Sentaurus to investigate charge collection mechanisms for both pulsed-laser and heavy ion irradiation [88]. The simulated devices have gate lengths of 100 nm, with different fin widths. Only single fin structures were simulated, which is sufficient to understand the trends in charge collection. The deposited charge in the simulations was 75 fC/μm over a distance of 8 μm, which is qualitatively similar to that produced by pulsed-laser irradiation. The characteristic width of the Gaussian distribution is 50 nm (fin spacing is much larger than this value). Charge was injected from the top of the gate to the substrate, centered at the middle of the channel. The Gaussian temporal distribution was centered at 1 ns with a characteristic time of 2 ps. For simplicity, optical absorption (only present in the 40 nm $In_{0.53}Ga_{0.47}As$ layer) was neglected in these TCAD simulations.

Fig. 3.14a shows simulated drain transient currents for devices at a gate bias of -0.6 V. The wider fin devices show both higher peak current and larger charge collection. Fig. 3.14b shows how the potential along the channel, represented by the conduction band energy, evolves after the charge is deposited. At 1 ns, as the charge is deposited, the barrier from the source to drain has dropped significantly due to hole accumulation at the source side, corresponding to the rising edge at 1 ns in Fig. 3.14a. After about 5 ns, the barrier recovers to the initial value, which makes the transient current disappear, as shown in Fig. 3.14a. These results are consistent with the pulsed-laser results, where reduced peak current and charge are observed for the narrowest fin device. These results also are qualitatively consistent with trends

observed in SEE tests on Intel's 14-nm second-generation tri-gate technology, in which the soft error rate (SER) improvements for narrower fin technology were also primarily attributed to reduced charge collection due to smaller collection volumes [89].

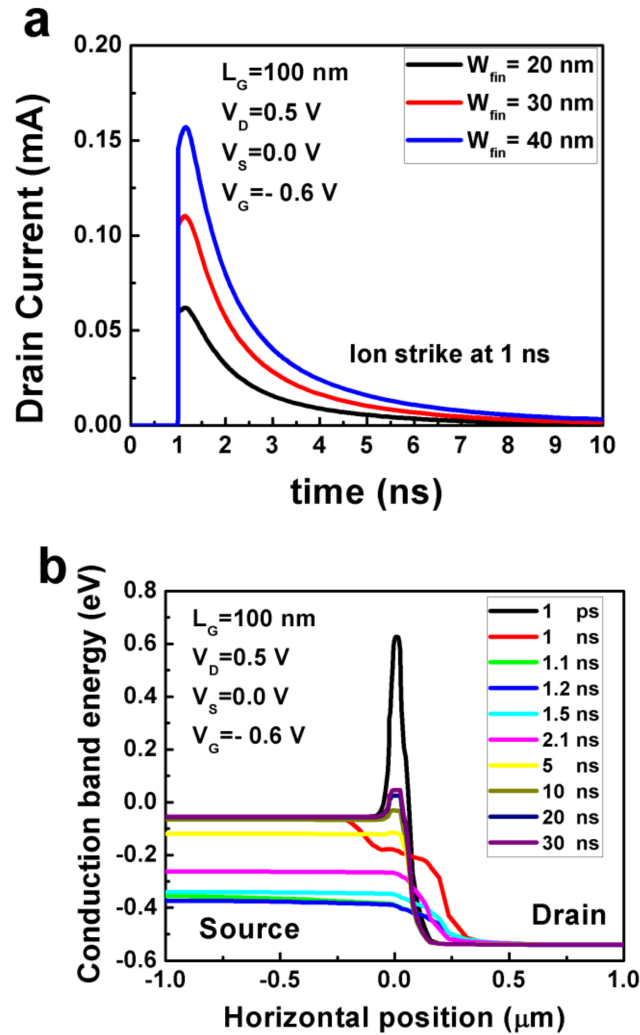


Fig. 3.14. (a) Drain current transients for InGaAs FinFETs of different fin widths from TCAD simulation, (b) conduction band energy evolution along the channel after charge deposition.

3.4.2 Channel modulation by the substrate

The generated charge may accumulate underneath the channel during the transient, acting as a back gate and modulating the channel. The electrostatics of the effect are similar to what has been examined

for TID effects in FinFETs, which show that the modulation of channel potential by charge beneath the fin is stronger for wider fin devices. Narrow fin devices have better control from the two side gates [90]-[92].

Fig. 3.15a shows a TCAD simulation on 20 nm fin-width devices with different amounts of charge in the silicon delta doping (red) region underneath the channel. As the charge density beneath the fin increases from $2\times10^{19}/cm^3$ to $2\times10^{21}/cm^3$, the electron density in the channel is strongly affected. For wider fin devices, the charge acts as a back gate, modulating the charge density in the channel. Narrower fin devices are less affected by the back gate modulation effect due to its shorter back gate length which is equivalent to the fin width, and the channels are more strongly modulated by the two side gates.

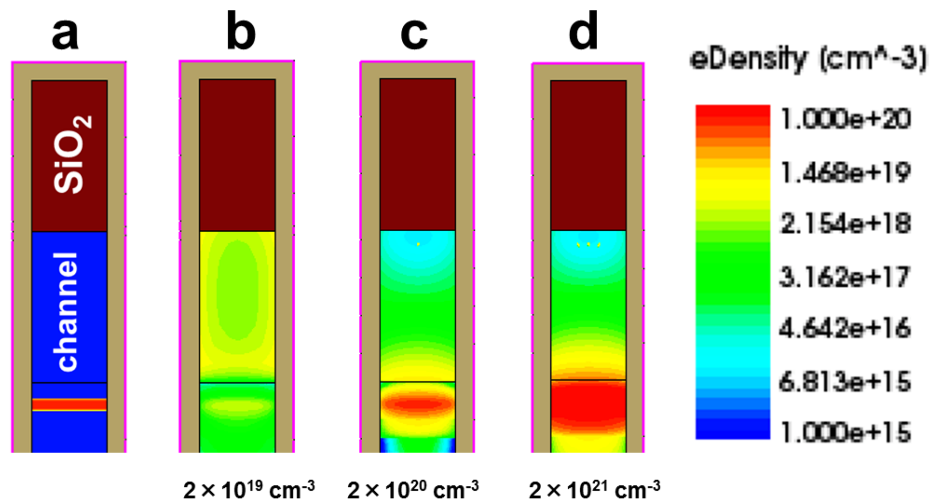


Fig. 3.15. Electron density distribution (b,c,d) for 20 nm fin-width devices with different doping in the red region (a). $V_G = 0.6$ V, $V_D = 0.5$ V, $V_S = 0$ V.

3.5 Optical Simulations

Both pulsed-laser and heavy-ion experiments show that the charge collection is not linearly related to fin width. The difference in peak current dependence between the laser testing and ion testing results suggests that other mechanisms affect charge collection that have not been previously considered. In particular, during pulsed-laser tests, the optical intensity distribution is modified by optical interference effects, and the peak optical intensity may be enhanced inside the fin due to plasmonic effects resulting from the nanoscale metal-dielectric-metal geometry of the fins.

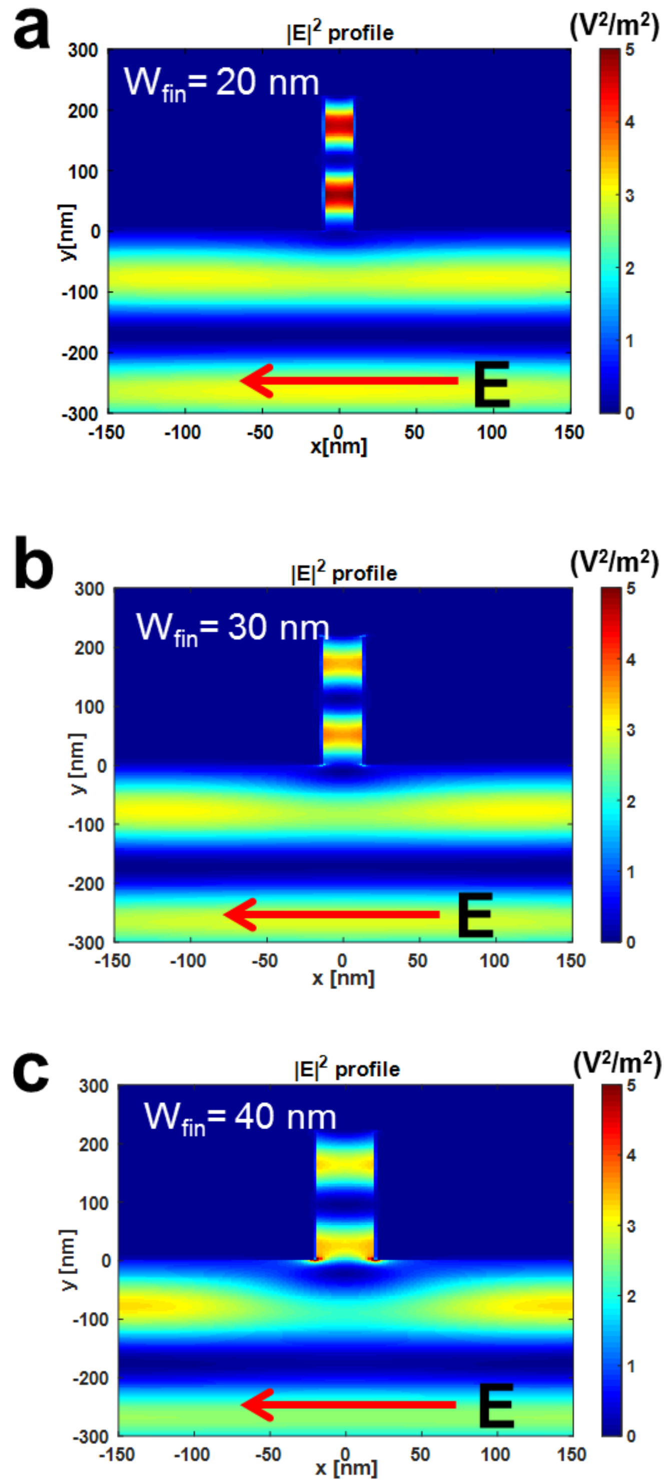


Fig. 3.16. Optical (E^2) field distribution calculated by 2D Lumerical simulations for simplified silicon FinFETs with different fin width.

To evaluate the potential effects of optical phenomena that occur in laser testing but not ion testing, optical simulations were carried out using the Lumerical optical design tool and a simplified model system. Fig. 3.16 shows initial optical simulation results on a simplified FinFET model system with different fin widths, conducted using two-dimensional FDTD analysis [83]. These simulations provide intuition on the relative importance of optical phenomena and geometric size-based effects in nanoelectronic devices. In the simulations, for simplicity, the fins are modeled to be Si and the metal contact on the top is selected to be Al. Laser excitation is modeled as a Gaussian source, polarized orthogonal to the vertical dimension of the fin and propagating from the bottom of the structure toward the fin. The wavelength of the source in the simulations is 1250 nm with a 1 μm radius focused at the bottom of the fins; the absorption coefficient of Si is ~ 0.0181 m^{-1} [83], [93]. This model system evaluates the optical response of a fin to sub-band-gap irradiation [44], [94], as is the case for the majority of the fin (180 nm out of 220 nm) in the device under test. In this first-order approximation, the integrated E^2 intensity in the fins is assumed to be proportional to the energy absorbed in the fins, which is in turn related to the charge generation in the fins.

Optical interference and plasmonic enhancement are revealed in Fig. 3.16 by the periodic oscillations of the E^2 intensity and by the peak E^2 intensity values, respectively. The change in the spacing of the E^2 intensity oscillations for the different fin widths can be explained by traditional optical interference effects between the incident and reflected light waves [95]. In a more realistic three-dimensional model that incorporates sidewall surface roughness, multiple reflections may build up inside the fin, modifying the interference pattern and potentially enhancing the electric field inside the fin. The higher peak E^2 intensity in the narrower fins revealed by examination of the color bar scale in Fig. 3.16 is consistent with plasmonic enhancement in nanoscale metal-dielectric-metal structures in which the enhancement scales inversely with the thickness of the dielectric layer [96], [97]. The strongest plasmonic enhancements in such structures typically occur for gaps of less than 10 nm between metal features; hence plasmonic effects are likely to be weak in the tested FinFETs. Therefore, while plasmonic enhancement likely increases the E^2 intensity and hence the expected charge generation by SPA per unit area in the 20 nm fin, the geometric effect is dominant and the increased area in the larger fins more than compensates for the

weak plasmonic effect. Hence, the integrated E^2 intensity in the 40 nm fin is larger than that in the 30 nm fin, which in turn is larger than that in the 20 nm fin in both the optical simulations and laser testing experiments. Moreover, multiple reflections are likely to lead to a significant increase in local e-h pair density in the smallest devices, leading to an enhanced recombination rate. This may also contribute to the reduced charge collection in the 20 nm fin devices. Based on these general considerations, we believe that optical phenomena will play a significant role in laser-based testing of FinFET technology at the 14 nm node and below. We conclude that these initial simulations in a simple model system are qualitatively consistent with charge collection trends in this work; a more detailed analysis will be the topic of future work.

3.6 Conclusion

This section describes the SET response of InGaAs FinFETs with different fin widths. For both pulsed-laser irradiation and heavy-ion irradiation, wider fin devices collect more charge. The SETs exhibit similar drain bias dependence for both types of irradiation. Larger drain bias increases the electric field on the drain side, which produces higher peak drain current and more collected charge. The SET cross section also scales with fin width, and stronger scaling effects are observed for lower drain biases. The transient tails overlap for all devices, which is due to similar charge collection in the substrate for all device widths. The SET dependence on ion LET is also reported. Ions with higher LET generate more electron-hole pairs in the channel, and thus higher peak drain current, more collected charge, and larger SET cross-section.

3D TCAD simulations show that the enhanced charge collection of the wider fin devices is mainly due to larger geometric volumes. Charge accumulated underneath the fin functions as a back gate, which produces stronger channel modulation effects for wider fin devices. Lumerical simulations on a simple model system are consistent with observed trends of laser-induced charge collection with fin width, and suggest that optical phenomena including plasmonic effects and enhanced e-h pair recombination due to multiple reflections within confined, multi-gate structures will play an increasingly important role for

pulsed-laser induced SET tests of advanced nanoelectronic technologies. These include emerging FinFETs and gate-all-around (GAA) devices, and thus is an important consideration in testing of nanoscale devices.

Chapter 4

Plasmonic-enhanced charge deposition in InGaAs FinFETs

4.1 Introduction

Pulsed-laser systems have been successfully applied to evaluate the SEE sensitivity of devices and circuits [94], [98]. One attractive feature of pulsed laser testing is that the spatial information is obtained without any radiation damage to devices. By focusing the laser spot to about micrometer size, and scanning the spot across the devices and circuit, information on the sensitivity of SEE at different locations can be obtained. As the main stream CMOS technology started to use FinFETs at the 22 nm node, optical phenomena such as plasmonic effects could affect the charge deposition in SET characterization [55]. Nanostructures, such as the narrow fin, can exhibit subwavelength optical confinement [99], [100]. It has been widely used in nanoscale photonic waveguides [68], [69], modulators [70], photovoltaics [71], [72], Raman spectroscopy [73], [74], and biosensing [75], [76]. Similar to the field enhancement effect in all these applications, the plasmonic effect enhances the electric field inside the narrow fin, which eventually enhances the free carriers generated in the channel [55]. Both single-photon absorption (SPA) and two-photon absorption (TPA) can inject charge in semiconductor materials. The charge density for SPA is a maximum at the surface and decreases with depth in the material, whereas the maximum charge density for TPA is at the focus point of the beam [98]. As a result, SPA is more used in SEE testing on surface channel devices. Metal lines on devices and circuits also add difficulties to SPA testing. TPA testing with back side illumination can avoid such difficulties.

As technology scales, the active region of devices is much smaller compared with the laser spot size. Obtaining spatial information on the sensitive area of devices becomes challenging. Tunable wavelength pulsed laser systems provide promising solutions to explore the sensitive area of the most advanced technologies with quantum well structures. In this chapter, the pulsed-laser induced single-event transients are explored on InGaAs MOSFETs with both FinFET and planar architectures. Enhanced charge collection is observed in the fin region of InGaAs FinFETs at different pulsed-laser wavelengths.

3-D TCAD simulation shows the transient peaks are mainly due to charge deposition from the channel. The substrate charge collection contributes to the tail current. Optical simulation shows enhanced charge deposition in the fin channel may be due to plasmonic effects. Area mapping illustrates the improved SET sensitivities by plasmonic effects in the fin region.

4.2 Device structure and experimental setup

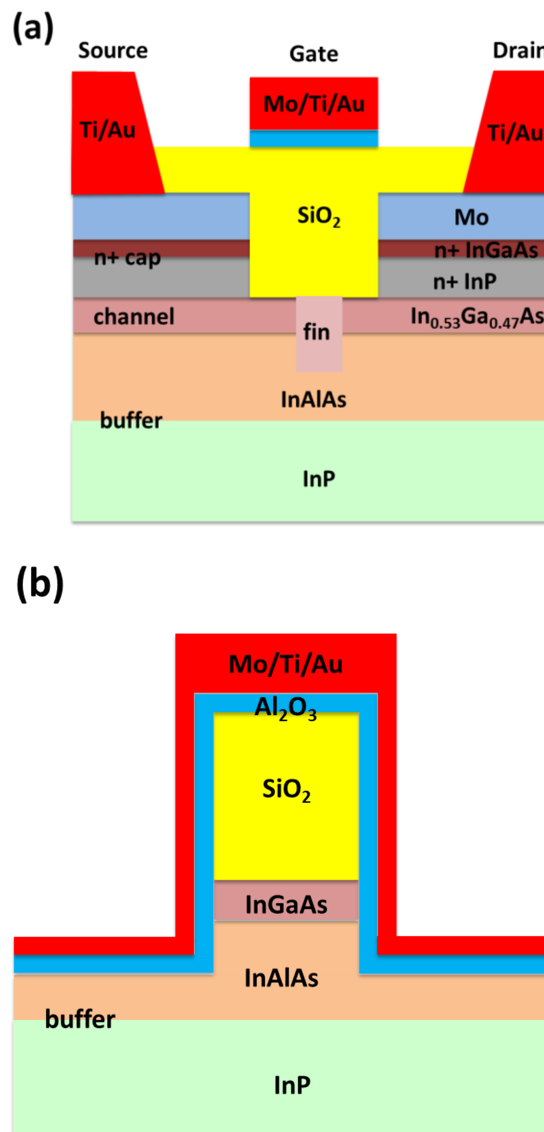


Fig. 4.1. (a) Schematic cross section and (b) side-view of an InGaAs double-gate FinFET (not drawn to scale).

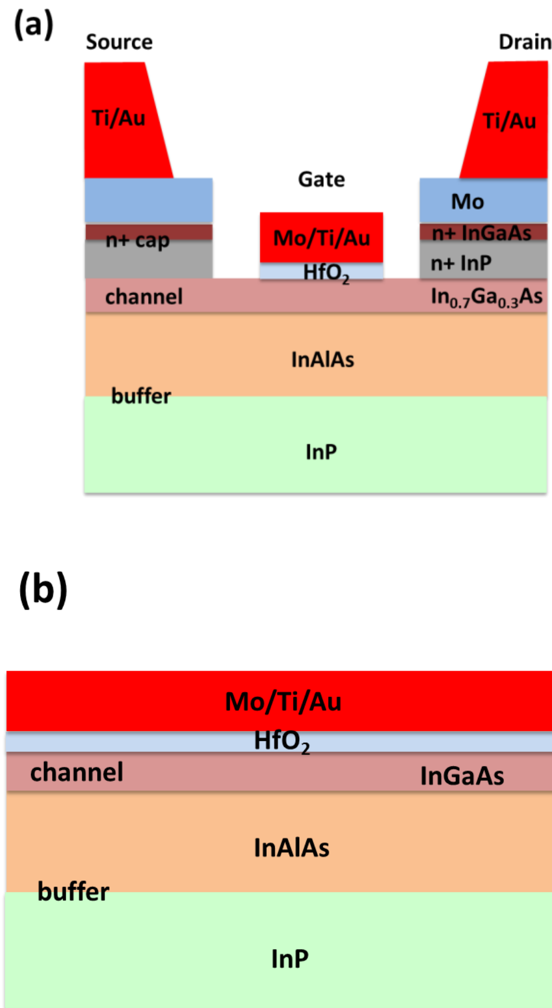


Fig. 4.2. (a) Schematic cross section and (b) side-view of an InGaAs planar MOSFET (not drawn to scale).

The InGaAs FinFETs and planar MOSFETs are both fabricated using a self-aligned process [84], [7]. This is a gate-last process with the contact formed first and the intrinsic region created by etching of the contact and cap layers. Fig. 4.1 and Fig. 4.2 show the cross-sectional and side-view schematic diagrams of an InGaAs FinFET and InGaAs planar MOSFET, repectively. The FinFETs have 42 fins in parallel, with 0.2 µm pitch between fins. The height of each fin is 220 nm, with a 40 nm thick $In_{0.53}Ga_{0.47}As$ channel layer. Under the channel, a 0.4-µm $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600-µm semi-insulating InP substrate. 40 nm of SiO_2 serves as a hard mask, which electrostatically decouples the top gate from the channel. As a result, the devices are only controlled by the two side gates. A 5-nm Al_2O_3

gate dielectric is deposited by atomic layer deposition. The detailed fabrication process is described in [10]. The InGaAs planar MOSFETs also have a 0.4-µm $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600-µm semi-insulating InP substrate. A 5 nm thick $In_{0.3}Ga_{0.7}As$ channel is grown on top of the buffer layer. A 2-nm HfO_2 gate dielectric is deposited by atomic layer deposition. The detailed fabrication process is described in [7]. As shown in Fig. 3.2 in the previous chapter, the heterostructure stack forms a quantum-well for both electrons and holes in both devices.

Pulsed-laser testing experiments were performed at Vanderbilt University. The pulsed-laser system is shown in Fig. 3.3. The laser system generates 150 fs pulses with 1 kHz repetition rate. The laser wavelengths in this experiment are 1260 nm with spot size of approximately 1.2 µm and 2200 nm with spot size of approximately 2.2 µm. The DUTs are irradiated from the backside by focusing the pulsed-laser spot near the channel region. Transients are captured using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36-GHz front-end bandwidth and 80 GS/s sampling rate. The DC bias is supplied with a semiconductor parameter analyzer, HP 4156A, through bias tees with 50-GHz bandwidth. The DUTs are mounted and bonded in a high-speed package with RF connectors [86]. The photon energy is 0.98 eV for the 1260 nm pulsed-laser and 0.56 eV for the 2200 nm pulsed laser. Table 4.1 summarizes the charge generation mechanisms in the materials used in both devices (single-photon absorption, or two-photon absorption).

Table 4.1. Charge generation mechanism in InGaAs FinFETs and planar MOSFETs

Material	**Band gap (eV)**	**1260nm**	**2200nm**
$In_{0.53}Ga_{0.47}As$ (FinFET)	0.75	SPA/TPA	TPA
$In_{0.3}Ga_{0.7}As$ (planar)	1.01	TPA	TPA
$In_{0.52}Al_{0.48}As$	1.46	TPA	NONE
InP	1.35	TPA	NONE

4.3 Experimental results and discussion

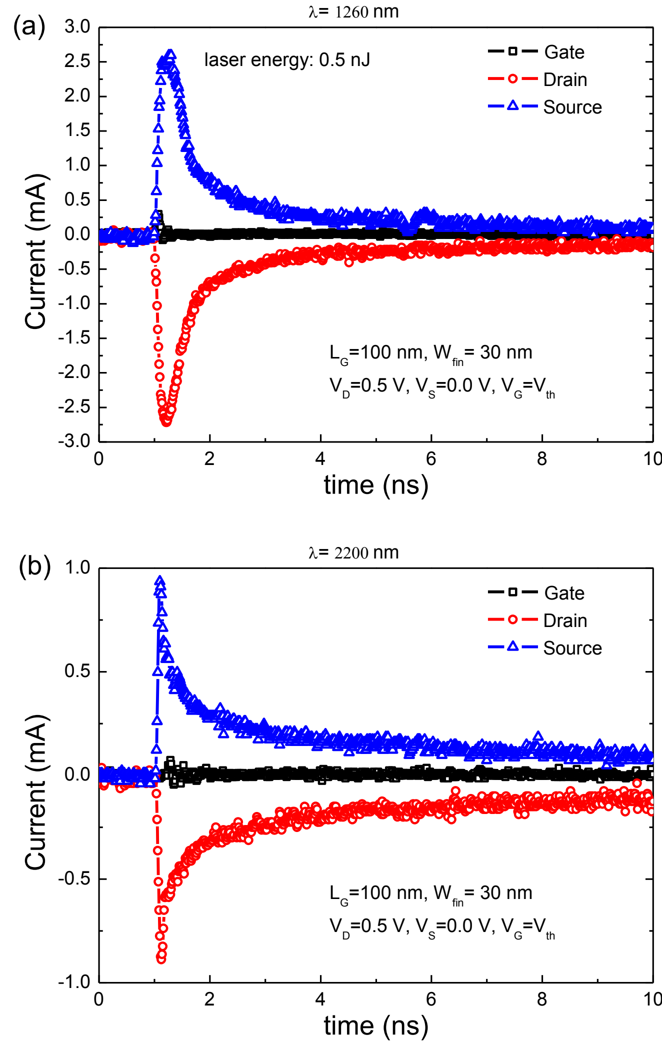


Fig. 4.3. SET captured during pulsed-laser testing for an InGaAs FinFET with wavelength at (a) 1260 nm and (b) 2200 nm. The strike point is at the center of the device. W_{fin} = 30 nm, L_G = 100 nm. $V_G - V_{th}$ = 0 V; V_{DS} = 0.5 V.

Fig. 4.3 illustrates typical transient currents on InGaAs FinFETs with two different wavelengths, 1260 nm and 2200 nm. Fig. 4.4 shows similar SET results on an InGaAs planar MOSFET. All transient signals are recoded mainly on the drain and source, and the gate transient currents are negligible. This occurs mainly due to the type-I quantum-well structure, as discussed in chapter 3. Charge collection in these devices is dominated by channel charge collection. The transients on drain and source terminals are

symmetric for various strike locations. There is a prompt peak charge collection which is mainly due to the shunt effect and parasitic bipolar amplification effect [54], [55]. The tail current is mainly the charge collection from substrate. As will be discussed in section 4.4, plasmonic effects may also contribute to the charge deposition in the InGaAs FinFETs.

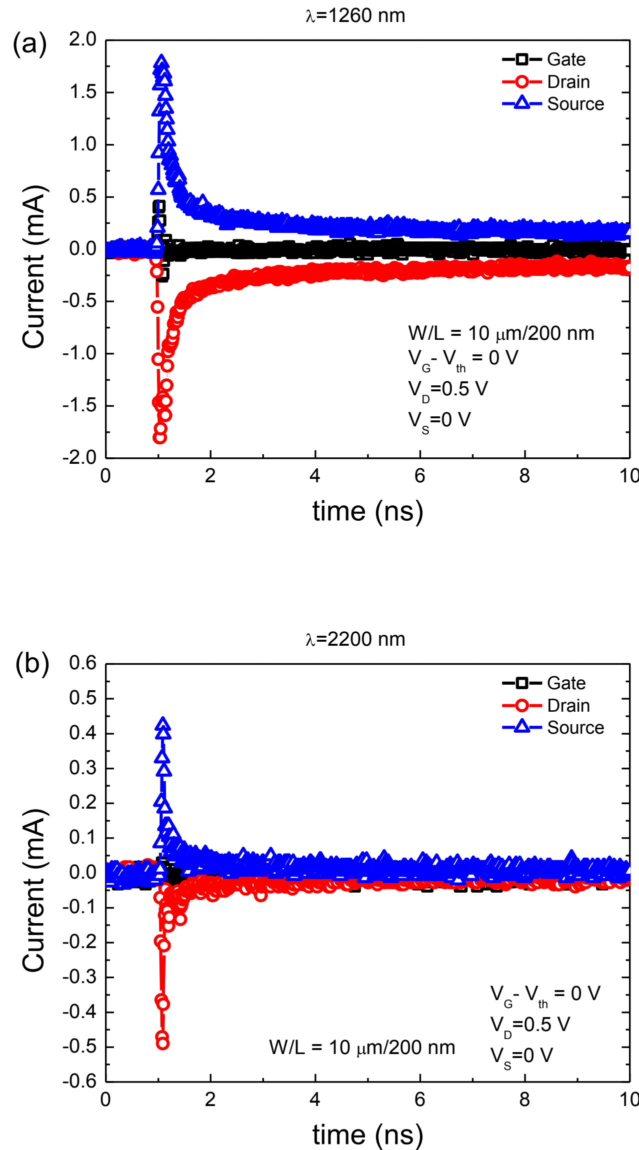


Fig. 4.4. SET captured during pulsed-laser testing for an InGaAs planar MOSFET with wavelength at (a) 1260 nm and (b) 2200 nm. The strike point is at the center of the device. W/L = 10 μm/200 nm. $V_G - V_{th} = 0$ V; $V_{DS} = 0.5$ V.

The drain current comparisons between InGaAs FinFET (solid lines) and planar MOSFET (dashed lines) with different wavelengths are shown in Fig. 4.5. The fall times are faster at a wavelength of 2200 nm than at 1260 nm for both devices. This is because the charges are generated only in the InGaAs channel at 2200 nm through TPA, as shown in Table 4.1. There is no charge deposition in the substrates. At 1260 nm, carriers are generated from the channel to substrate layers. The charges generated in the substrate slow the collection process.

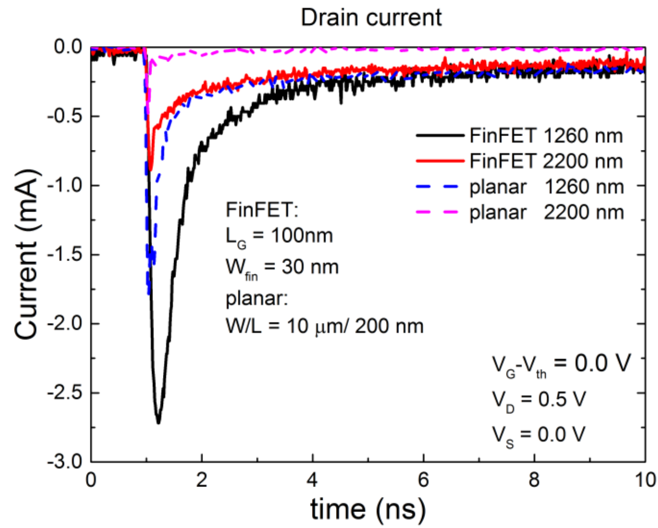


Fig. 4.5. Drain current comparison for an InGaAs FinFET (solid lines) and planar MOSFET (dashed lines). The strike point is at the center of the device. $V_G - V_{th} = 0$ V; $V_{DS} = 0.5$ V.

The peak drain current along a line scan for an InGaAs FinFET at different drain biases is shown in Fig. 4.6. All error bars in this work represent the standard deviation of the mean. Fig. 4.6 (a) shows the drain bias dependence at 1260 nm, and Fig. 4.6 (b) shows the drain bias dependence at 2200 nm. Fig. 4.6 (c) shows the cross-section view of an InGaAs FinFET with the scale showing the line scan positions with respect to the device geometry. At both wavelengths, the peak current increases as drain bias increases due to the increased electric field along the channel. The peak current is higher at the drain side than at the source side, which is consistent with the bias applied to the drain and source terminal, $V_{DS} = 0.5$ V. The electric field is larger on the drain side than on the source side.

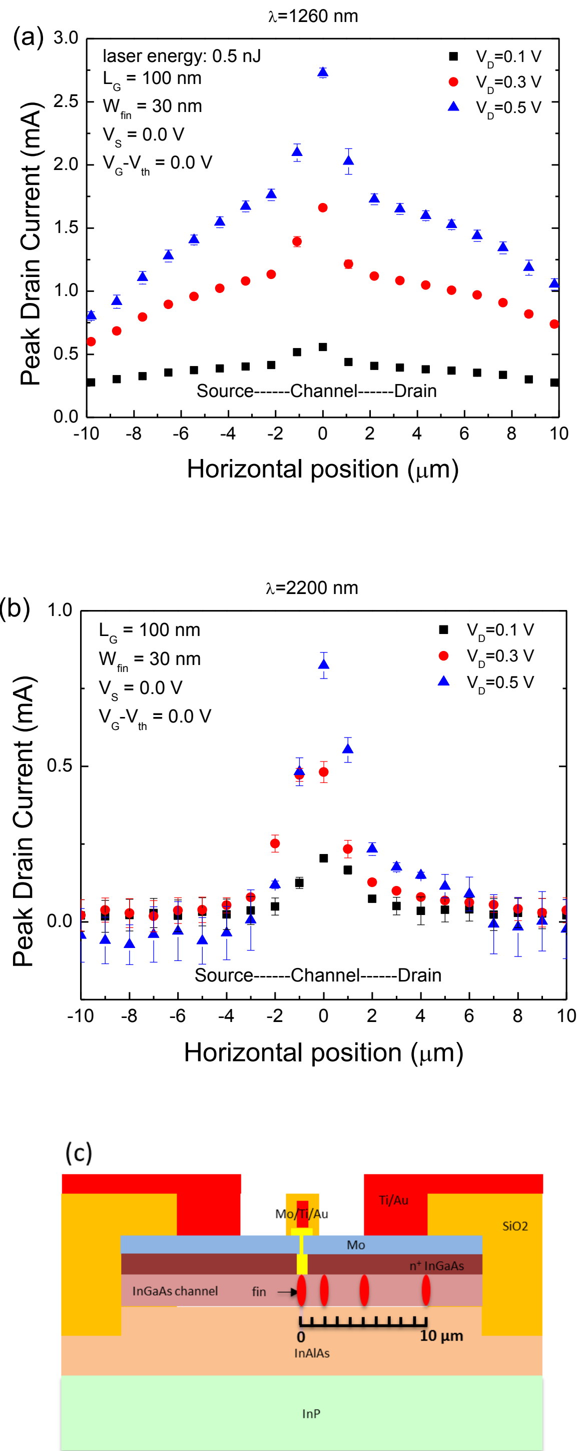


Fig. 4.6. Peak drain current along a line scan at different drain biases for an InGaAs FinFET with wavelength at (a) 1260 nm and (b) 2200 nm. The error bars represent the standard deviation of the mean. (c) The cross-section view of an InGaAs FinFET with scale shows the line scan positions w.r.t. the device geometry. Geometry on vertical direction is not scaled.

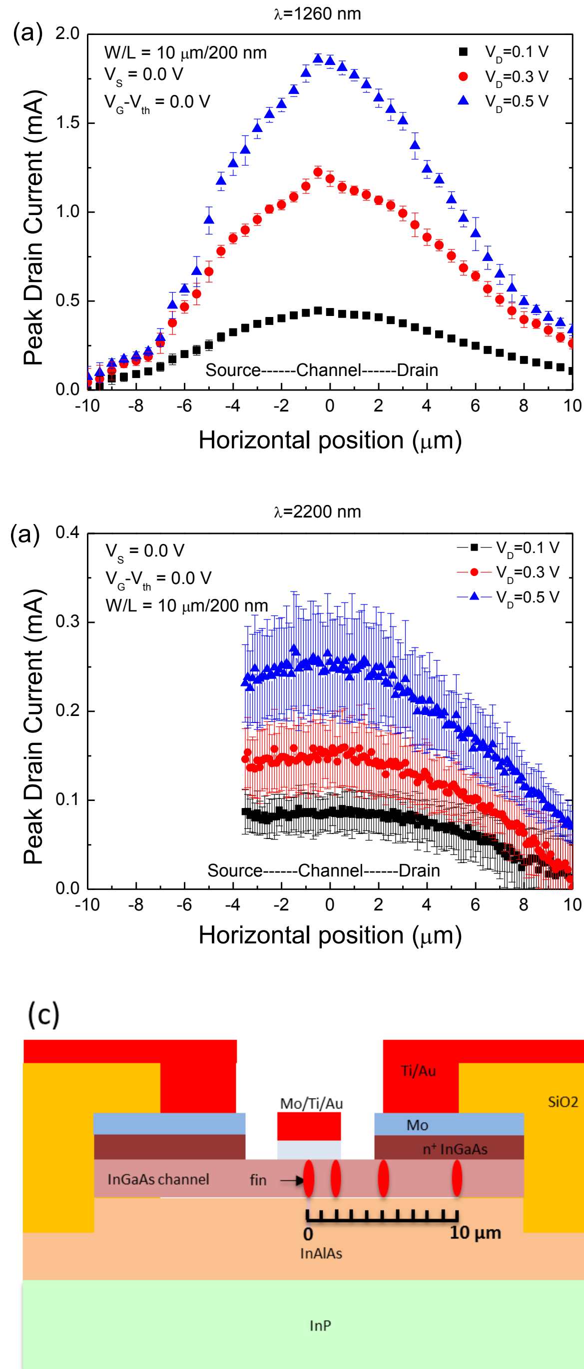


Fig. 4.7. Peak drain current along a line scan at different drain biases for an InGaAs planar MOSFET with wavelength at (a) 1260 nm and (b) 2200 nm. The error bars represent the standard deviation of the mean. (c) The cross-section view of an InGaAs planar MOSFET with scale shows the line scan positions w.r.t. the device geometry. Geometry on vertical direction is not scaled.

Similar drain bias dependence for an InGaAs planar MOSFET is shown in Fig. 4.7. The peak current also increases as drain bias increases due to the increased electric field along the channel. The key difference between the FinFET and planar MOSFET is that the peak current increases abruptly for the FinFET when the laser is focused in the region from -2 to 2 μm. This may be due to the plasmonic effect, as will be discussed in section 4.4.

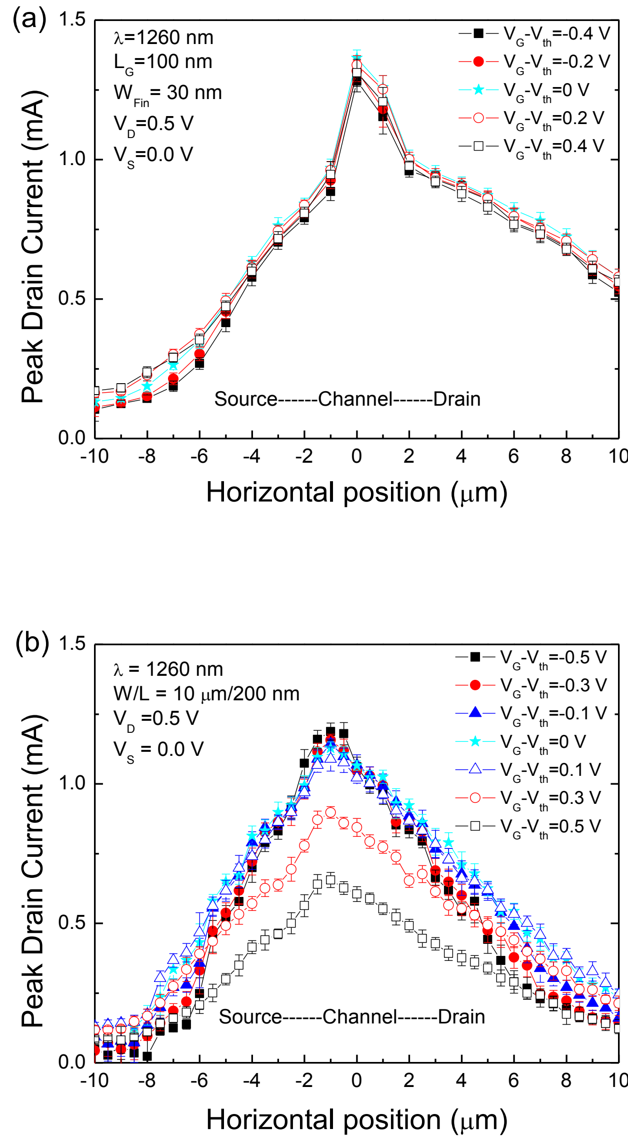


Fig. 4.8. Peak drain current along a line scan at different gate bias for InGaAs (a) FinFET and (b) planar MOSFET. The error bars represent the standard deviation of the mean.

Fig. 4.8 shows the peak drain current along a line scan at different gate bias for an InGaAs FinFET and an InGaAs planar MOSFET, respectively. There is no gate bias dependence for the InGaAs FinFETs, while the peak current reduces for the planar MOSFET biased above threshold. This is due to the reduced excess electron density in the channel when it is biased in inversion [65]. In InGaAs FinFETs, the channel is thin and fully depleted, thus no gate bias dependence will be observed in FinFETs [54], [56]. In addition, the plasmonic-enhanced charge deposition in the narrow fin may dominate the excess carrier density, which is an optical effect and does not depend on the gate biases.

The area mapping of the sensitive region is performed by fixing the focused laser spot at the surface, and moving the x-y stage. The results are shown in Fig. 4.9 (a) at 1260 nm and (b) at 2200 nm, respectively. The peak current is normalized to its maximum current in each figure. The black box in each figure marks the sensitive area in the xy plane at each wavelength. The corresponding cross-section view of the InGaAs FinFET is also shown in each figure. In Fig. 4.9 (a), the sensitive area matches the geometry of the mesa in the InGaAs FinFET. All carriers generated in the channel layer and substrate layer can be collected by the terminals. In Fig. 4.9 (b), the sensitive area is reduced to only the fin region. This is because charge is generated only in the channel through TPA. The free excess carriers decrease significantly; thus the transient signal decreases when the laser spot is away from the gate region. When the laser spot hits the gate region, the transient signal increases significantly mainly due to a shunt effect and a parasitic bipolar amplification effect. Plasmonic-enhanced charge deposition may also help increase the SET sensitivity in the fin region. As a result, strong transient current is observed in the fin region even though the carrier generation rate is low for irradiation at 2200 nm.

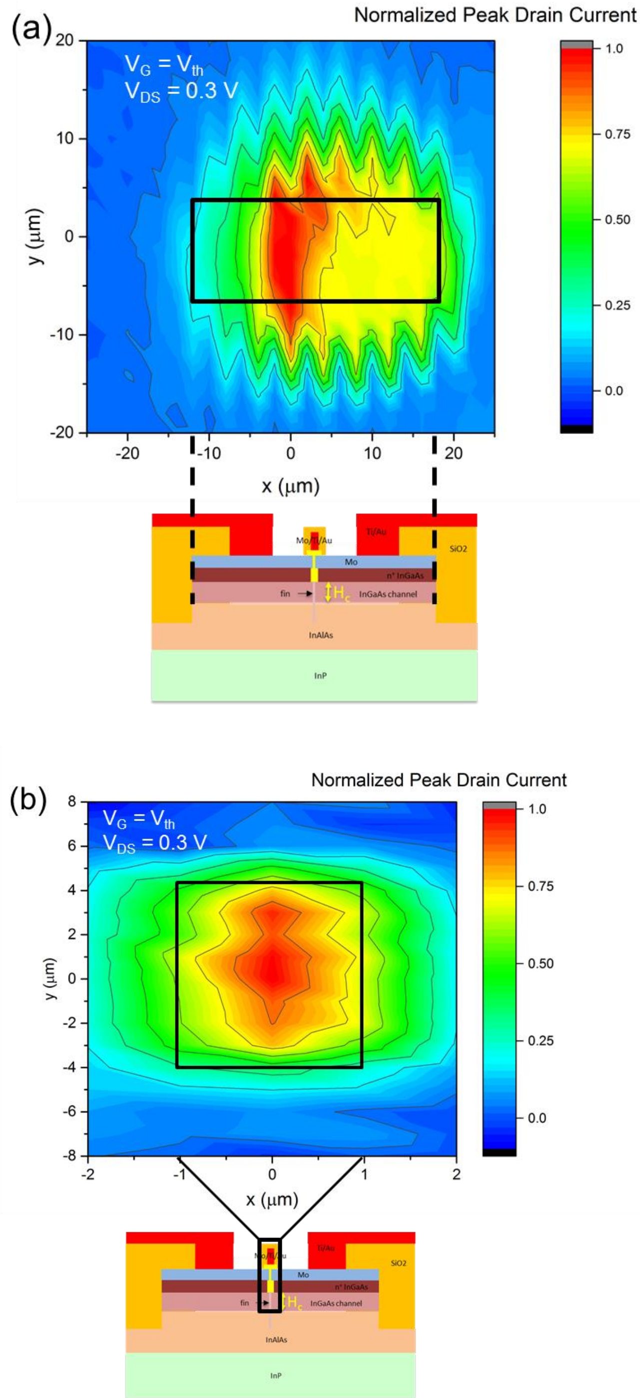


Fig. 4.9. Peak drain current area mapping for an InGaA FinFET with wavelength at (a) 1260 nm and (b) 2200 nm. The peak current is normalized to the maximum peak current in both figures. The black box in each figure marks the sensitive area at different wavelength. The corresponding cross-section view of the device is also shown in each figure.

4.4 Plasmonic effect in InGaAs FinFETs

To evaluate the optical effects that occur in the laser testing, 2-D optical simulations with FDTD analysis were carried out using the Lumerial optical design tool. Laser excitation is modeled as a Gaussian source, polarized orthogonal to the vertical dimension of the fin and propagating from the bottom of the structure toward the fin. The wavelength of the source in the simulations is 1250 nm with a 1 μm radius focused at the bottom of the fins; the absorption coefficient of Si is ~ 0.0181 m^{-1} [83], [93]. Fig. 4.10 shows the optical field propagation in the FinFET structure. The electric field inside the fin is higher than that in the substrate. This is due to the plasmonic effect in a metal/dielectric/metal structure of the fin, which enhances the electric field in the narrow fin.

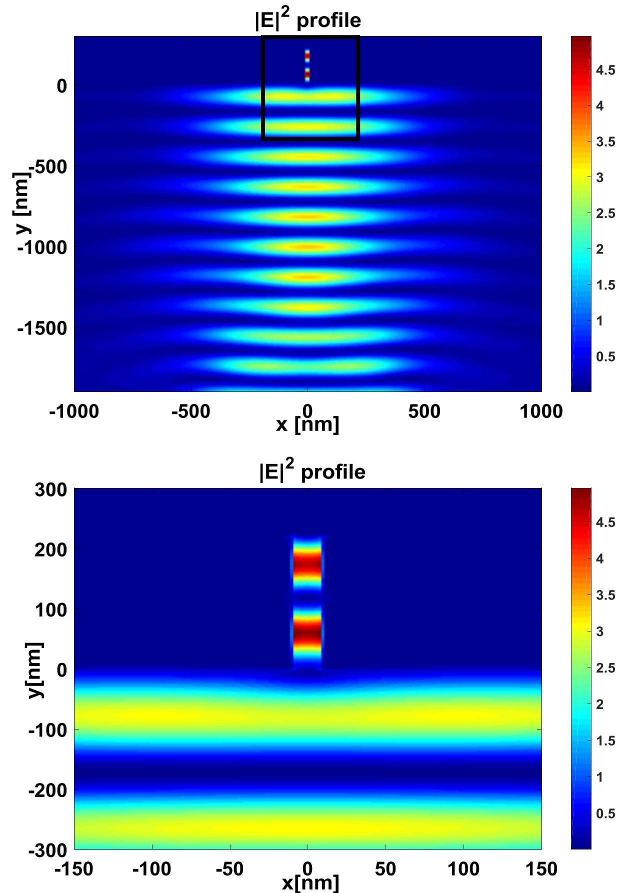


Fig. 4.10. Optical (E^2) field propagation calculated by 2-D Lumerical simulations for simplified FinFET structure.

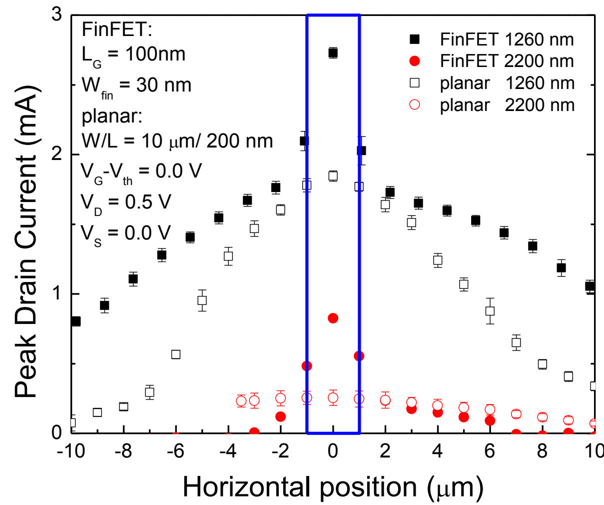


Fig. 4.11. Peak drain current comparison along a line scan between an InGaAs FinFET (solid symbols) and an InGaAs planar MOSFET (open symbols) with wavelength at 1260 nm (black) and 2200 nm (red). The blue box marks the fin dimension for the InGaAs FinFET. The error bars represent the standard deviation of the mean. $V_G - V_{th} = 0$ V; $V_{DS} = 0.5$ V.

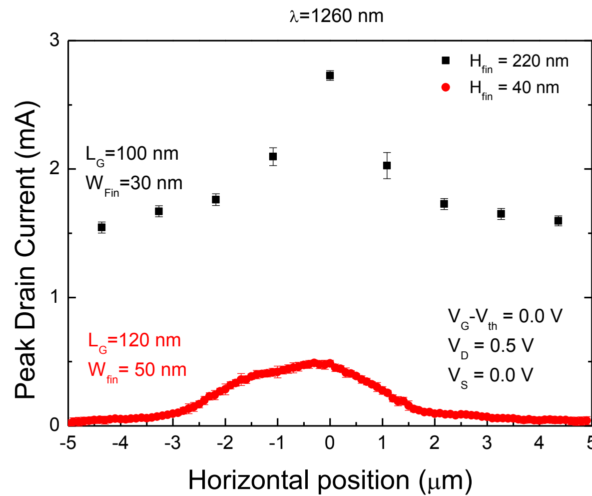


Fig. 4.12. Peak drain current comparison along a line scan between an InGaAs FinFET with fin height of 220 nm (black box) and 40 nm (red circle) [56] at wavelength of 1260 nm. The error bars represent the standard deviation of the mean. $V_G - V_{th} = 0$ V; $V_{DS} = 0.5$ V.

The integrated E^2 is proportional to the energy deposited in the material. The enhanced electric field

causes increased free carrier generation in the fin. Fig. 4.11 shows the peak drain current comparison along a line scan between an InGaAs FinFET and an InGaAs planar MOSFET at different wavelength. The blue box marks the fin dimension in the InGaAs FinFET. When the laser spot strikes the fin from -1 μm to 1 μm, the peak current increases abruptly in the FinFET at both wavelengths. In the planar MOSFET, the peak current increases gradually at both wavelengths. This suggests plasmonic effects may contribute to the charge deposition in the InGaAs FinFET while not in the InGaAs planar MOSFET.

Fig. 4.12 shows the peak drain current comparison along a line scan between an InGaAs FinFET with fin height of 220 nm and a silicon substrate InGaAs FinFET with fin height of 40 nm in previous work [56]. Similar to the InGaAs planar MOSFET, no abrupt increase is observed in the 40 nm fin height device. The substrate does not provide effective optical confinement if the fin height is low. From the 22-nm technology node to the 10-nm technology node, fin height increases while fin width decreases [78], which may result in increasing plasmonic effects in newer technologies.

4.5 TCAD simulation

3-D TCAD simulations were performed with Sentaurus to investigate the charge collection mechanisms in InGaAs FinFETs. The simulated devices have a gate length of 100 nm and fin width of 30 nm. Single fin structures were simulated, which is sufficient to investigate the charge collection mechanisms. The deposited charge in the simulation is 75 fC/μm. The injected charge has a Gaussian distribution in both space and time. The characteristic width of the Gaussian distribution is 50 nm. The Gaussian temporal distribution was centered at 1 ns with a characteristic time of 2 ps.

Fig. 4.13 (a) shows the charge generation length during the simulation. The charge generation in the channel simulation is similar to 2200 nm pulsed-laser irradiation. The charge injection in the channel and substrate simulation is similar to 1260 nm pulsed-laser irradiation. The corresponding drain transient currents are shown in Fig. 4.13 (b). Similar to the experimental results in Fig. 4.5, the fall time is faster for charge generation only in the channel than for charge generation in both the channel and substrate. This is because it takes about 0.3 ns for the charge generated in the substrate to be collected [54]. The peak

currents for these two charge generation methods are the same, which suggests the transient peak is mainly due to channel charge generation. This is consistent with the plasmonic effects discussion in chapter 4.4. The sudden peak current increase in the fin region may be due to the plasmonic effects in the fin channel.

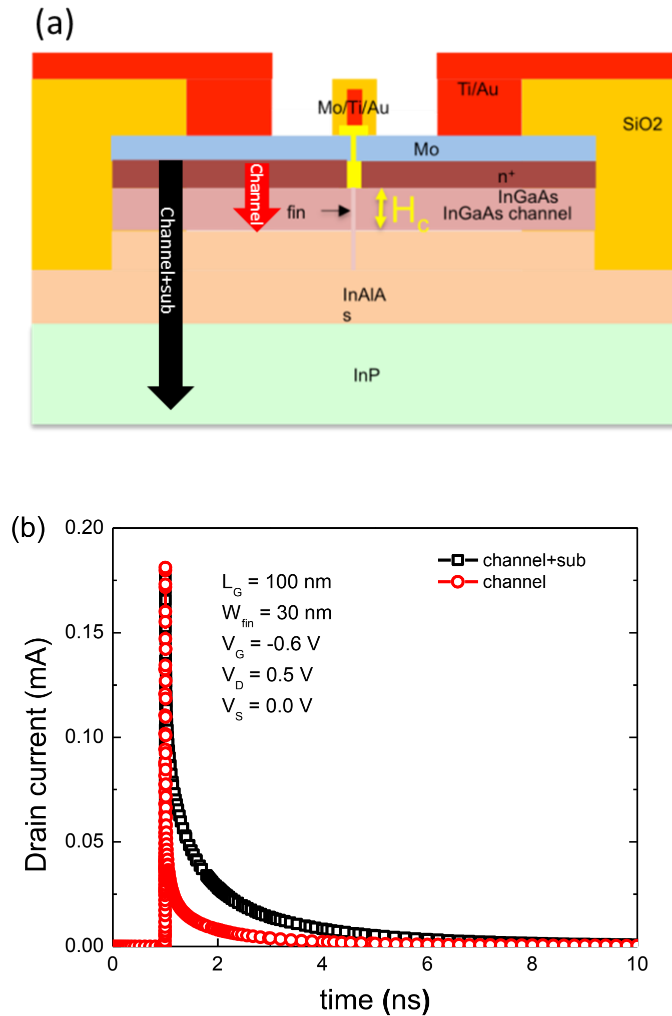


Fig. 4.13. (a) Charge injection schematic in SET simulations. (b) Drain current transients for charge injection only in channel (red) and both channel and substrate (black).

The electron current density distribution 50 ps and 500 ps after the strike is shown in Fig. 4.14. For charge generation in both the channel and substrate, electron current flow from the substrate is observed, while there is no electron current flow when charge is generated only in the channel. The additional

current flow from the substrate contributes to the transient tail, and reduces the fall times of the transients.

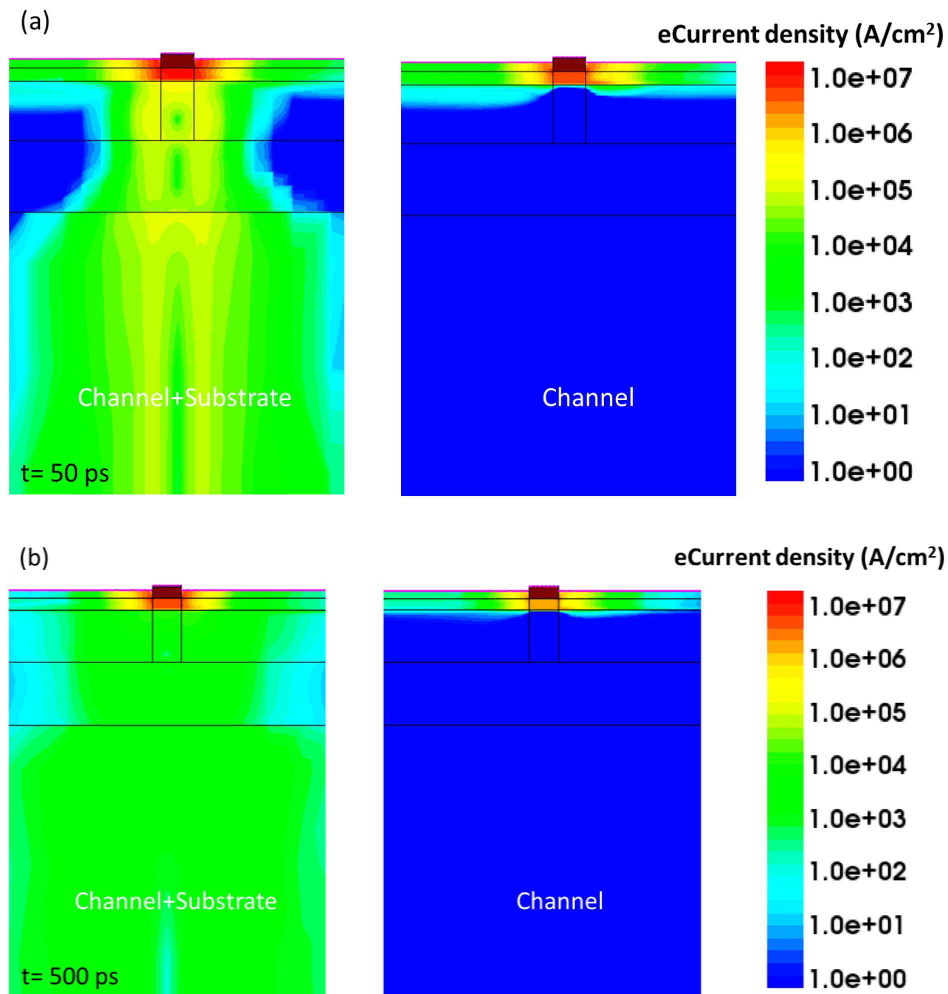


Fig. 4.14. Electron current density for charge deposition in both channel and substrate (left) and channel only (right) (a) 50 ps after charge deposition, and (b) 500 ps after charge deposition.

4.6 Conclusion

This chapter explores the pulsed-laser induced single-event transients on InGaAs MOSFETs with both FinFET and planar architectures at different wavelengths. 2200 nm pulsed-laser irradiation generates free carriers only in the channel, which reduces the transient fall times. Sudden increased peak currents are observed in the InGaAs FinFETs, which is due to the enhanced charge collection in the fin region. 3-D

TCAD simulation shows the transient peaks are mainly due to charge generation in the channel. The substrate charge collection contributes to the tail current. Optical simulation shows enhanced charge generation in the fin channel may be due to plasmonic effects. Plasmonic effects may play an important role for pulsed-laser SET characterization of modern CMOS technologies.

Chapter 5

Pulsed-laser induced single-event transients in InGaAs FinFETs on bulk silicon substrates

5.1 Introduction

III-V materials are promising for future alternative-channel nMOSFETs due to their superior transport properties [4]. Obtaining high performance devices is challenging because of the lattice mismatch between III-V materials and silicon. Most recent III-V MOSFETs have been fabricated on III-V sub-strates to reduce lattice mismatch [5], [7], [10], [11]. To be compatible with current CMOS technology, III-V MOSFETs must be integrated on silicon substrates. Recently, successful integration of III-V FinFETs on 300 mm silicon wafers has been demonstrated, representing significant progress towards application in next generation logic transistors [15]. Much work suggests that III-V MOSFETs are more sensitive to SET than silicon MOSFETs due to parasitic bipolar amplification effects [54], [55], [63]-[65], [101], [103], but the SET response of III-V MOSFETs on bulk silicon is largely unknown.

In this chapter, pulsed-laser irradiation is used to investigate the SET response of InGaAs FinFETs on bulk silicon substrates. Charge collection due to a source-drain shunt effect [49] and drain-to-substrate junction charge collection contribute to the observed transients. The laser-induced transient response of these silicon substrate devices is compared to that of InGaAs FinFETs on semi-insulating InP substrates. Faster transients with reduced peak currents and peak widths are observed on the silicon substrate devices compared to the InP substrate devices. 3-D TCAD simulations show that the energy barrier for holes in silicon substrate devices is relatively lower than the barrier for electrons. Consequently, the substrate collects holes efficiently, which reduces the amount of source-barrier lowering and bi-polar-amplification relative to other III-V devices. Moreover, defects within the semi-insulating GaAs buffer layer that underlies the InGaAs channel further reduce the hole life-time, and also contribute to the relative reduction of the bipolar amplification in these devices.

5.2 Experimental details

The devices considered here are InGaAs FinFETs on bulk silicon. A 3-D diagram is shown in Fig. 5.1. The detailed fabrication process is described in [15]. Devices are fabricated on 775 μm thick boron-doped p-type silicon (100) with doping concentration of ~ 5×10^{14} cm^{-3}. There are 4 fins in parallel for each device. A 40 nm thick n-doped (~ 1×10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$ channel layer is grown on a semi-insulating GaAs buffer layer (thickness ranges from 200 nm to 250 nm). A V-"Groove" underneath the buffer layer forms Si {111} planes to avoid misfit dislocations. A more detailed depiction of a typical layer stack is shown in Fig. 5.2. The insert in Fig. 5.1 shows the TEM of the gate stack (2 nm Al_2O_3/3 nm HfO_2/3 nm TiN). Highly doped (~ 2×10^{19} cm^{-3}) InAs forms the drain and source regions. Contact is made via a W-plug process. The energy band diagram of the Si-based InGaAs FinFET for a cut line (red dashed line in Fig. 5.1) through the gate to substrate is shown in Fig. 5.3. The heterostructure stack forms a quantum-well for both electrons and holes. The energy barrier for holes (0.27 eV) is relatively lower than the barrier for electrons (0.45 eV).

Pulsed-laser testing experiments were performed at Vanderbilt University. The laser system setup is shown in Fig. 3.3 from the previous chapter. The laser system generates 150 fs pulses with 1 kHz repetition rate. The laser wavelength in this experiment is 1260 nm with spot size of approximately 1.2 μm [85]. The DUTs are irradiated from the backside by focusing the pulsed-laser spot such that the channel region is contained within the charge generation region from the laser pulse. The photon energy is 0.98 eV, which is above the band gap of $In_{0.53}Ga_{0.47}As$. Transients are captured using a Teledyne Lecroy LabMaster 10-36Zi-A oscilloscope with 36-GHz front-end bandwidth and 80 GS/s sampling rate [54]. The DC bias is supplied with a semiconductor parameter analyzer, HP 4156A, through bias tees with 50-GHz bandwidth. The DUTs are mounted and bonded in a high-speed package with RF connectors [86]. Table 5.1 summarizes charge generation mechanisms in the materials used in the devices (single-photon absorption, or two-photon absorption).

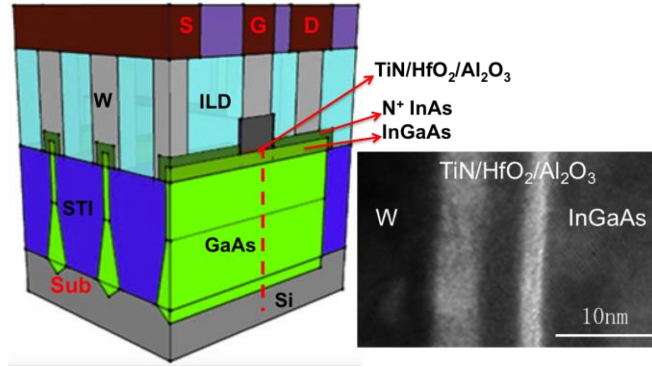


Fig. 5.1. 3-D diagram of InGaAs FinFET on bulk silicon. Gate (G), drain (D), source (S), and substrate (Sub) are labeled in red. The inset shows a TEM image of the gate stack [49].

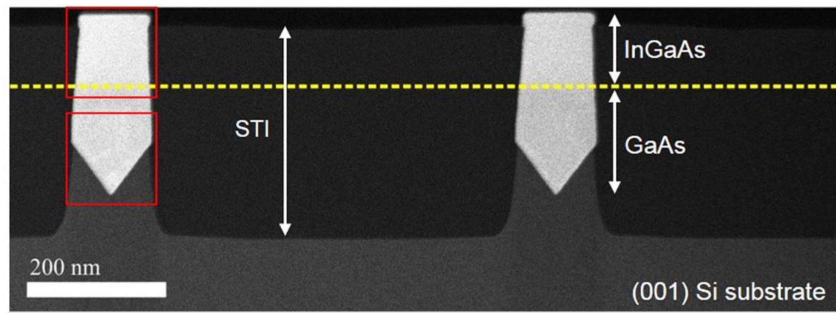


Fig. 5.2. HAADF-STEM images of an InGaAs/GaAs hetero-structure. The yellow dashed line visualizes the interface between InGaAs and GaAs [108].

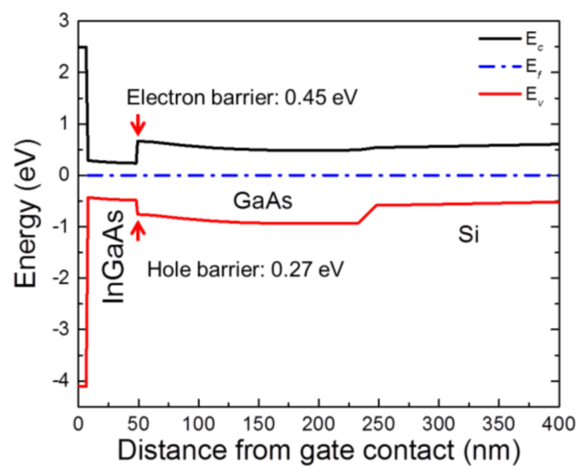


Fig. 5.3. Energy band diagram for a Si-based InGaAs FinFET for a cut line (red dashed line in Fig. 5.1) through the gate to substrate.

5.3 Experimental results and discussion

Fig. 5.4 illustrates a set of typical pulsed laser-induced transients for an InGaAs FinFET on bulk silicon. There is a fast charge collection process with full width at half maximum (FWHM) of 50 ps on the drain and source. This fast process is mainly due to a shunt effect [49], [52], which occurs because the laser spot size (~1.2 µm) is larger than the gate length (120 nm). A slower charge collection process (with FWHM of 250 ps) is observed on the substrate and drain due to charge collection from the substrate.

Table 5.1. Charge generation mechanism for 1260 nm laser

Material	**Band gap (eV)**	**Photon absorption mechanism**
$In_{0.53}Ga_{0.47}As$	0.75	SPA/TPA
GaAs	1.42	TPA
Si	1.12	TPA

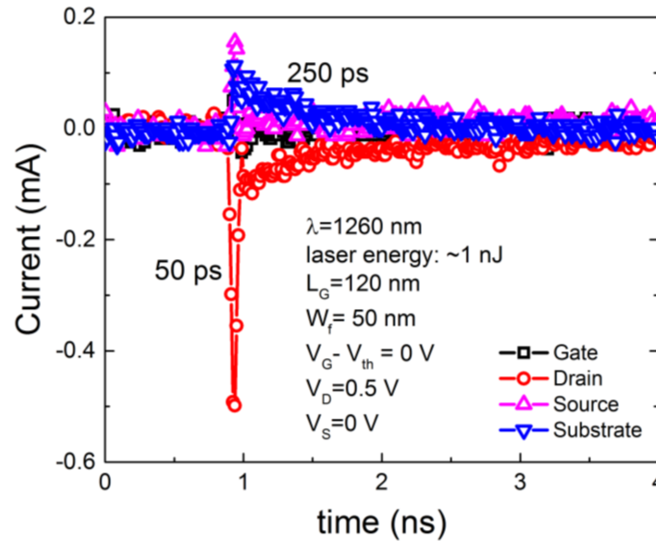


Fig. 5.4. SET captured during pulsed-laser testing for an InGaAs FinFET on bulk silicon. W_{fin} = 50 nm, L_G = 120 nm. $V_G - V_{th}$ = 0 V; V_{DS} = 0.5 V. The strike point is at the center of the device.

Normalized (to fin number) peak drain currents measured in InGaAs FinFETs on silicon (4 fins in parallel) and InGaAs FinFETs on InP [55] are compared in Fig. 5.5. The geometries of each fin in the two devices are comparable. Laser spot locations are optimized for maximum peak current in both experiments, and similar pulsed-laser energies are employed to make the comparison as fair and relevant as possible. The transient on the Si-based InGaAs FinFET in Fig. 5.5 shows significantly smaller peak current and peak width (50 ps) than the FinFET on the InP substrate (650 ps). This suggests that Si-based InGaAs FinFETs are less sensitive to SETs than InP-based InGaAs FinFETs. Previous work demonstrates that recombination in the semi-insulating GaAs buffer layer efficiently reduces charge collection [63], [103]. In addition, both electrons and holes are confined to the channel region for InP-substrate devices due to the quantum well structure [54], [55]. The confined holes reduce the barrier between source and channel, leading to significant charge injection into the channel that is collected by the drain. However, the generated holes in the silicon-substrate devices are efficiently collected by the substrate contact, which contributes to the substrate charge collection. The reduced density of holes near the channel eliminates source barrier lowering and bipolar amplification, further reducing SET sensitivity. 3-D TCAD simulations in section 5.4 explain these mechanisms in more detail.

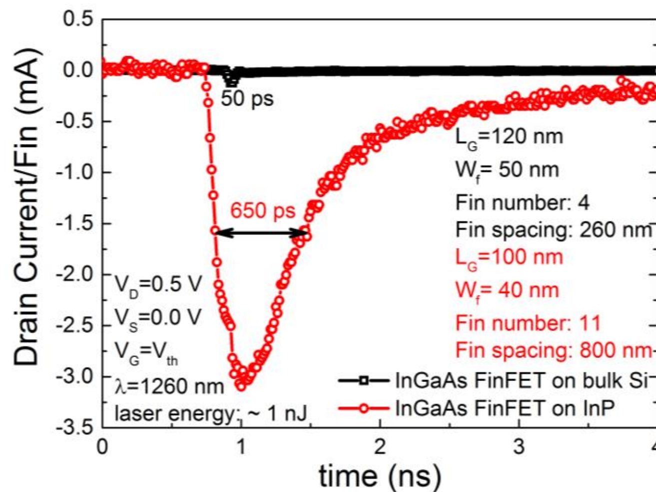


Fig. 5.5. Normalized (to fin number) drain currents between an InGaAs FinFET on silicon (black) and previous results for an InGaAs FinFET on InP (red) [55]. Devices are irradiated at the same pulsed-laser energy.

Fig. 5.6 shows transient peak currents at different gate biases. The transient peaks do not vary with gate bias, consistent with previous results on InP-substrate InGaAs FinFETs [54], but different than InP-substrate InGaAs planar MOSFETs [65]. This is because the body potential of the FinFET device is controlled by the tri-gates, which have little effect on the substrate below the fin.

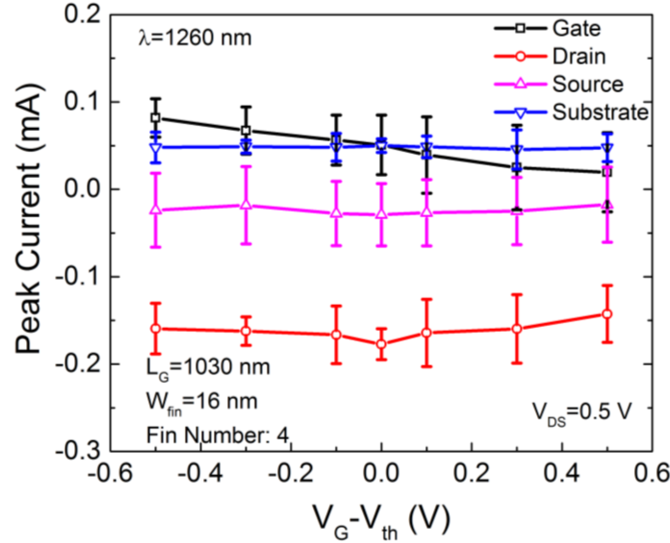


Fig. 5.6. Transient peak currents at different gate bias for an InGaAs FinFET on silicon. The error bars represent the standard deviation of the mean. W_{fin} = 16nm, L_G = 1030 nm. V_{DS} = 0.5 V.

Fig. 5.7(a) shows the peak drain current along a line scan at different drain and source biases. Two groups of curves are shown. The solid symbols correspond to V_S = 0 V and V_D > 0 V. For these bias conditions, channel current contributes most to the charge collection. The peak current increases as the drain bias increases from 0.3 V to 0.5 V. The open symbols correspond to $V_S = V_D$. For these bias conditions, drain (or source) and substrate junction charge collection is dominant since there is no source-drain electric field. The peak current monotonically increases with drain bias. This suggests that junction charge collection contributes significantly for these bias conditions, similar to what is observed for silicon and SiGe FinFETs [52], [53], [87], and different from other InGaAs FinFETs on semi-insulating substrates [54], [55]. Similar data collected on InP-substrate InGaAs FinFETs are shown in Fig. 5.7(b) [55]. The peak currents are the same for $V_S = V_D$ at different bias conditions. This suggests

that almost no junction collection contributes to the transients in these devices. The reasons for these differences are discussed in the next section.

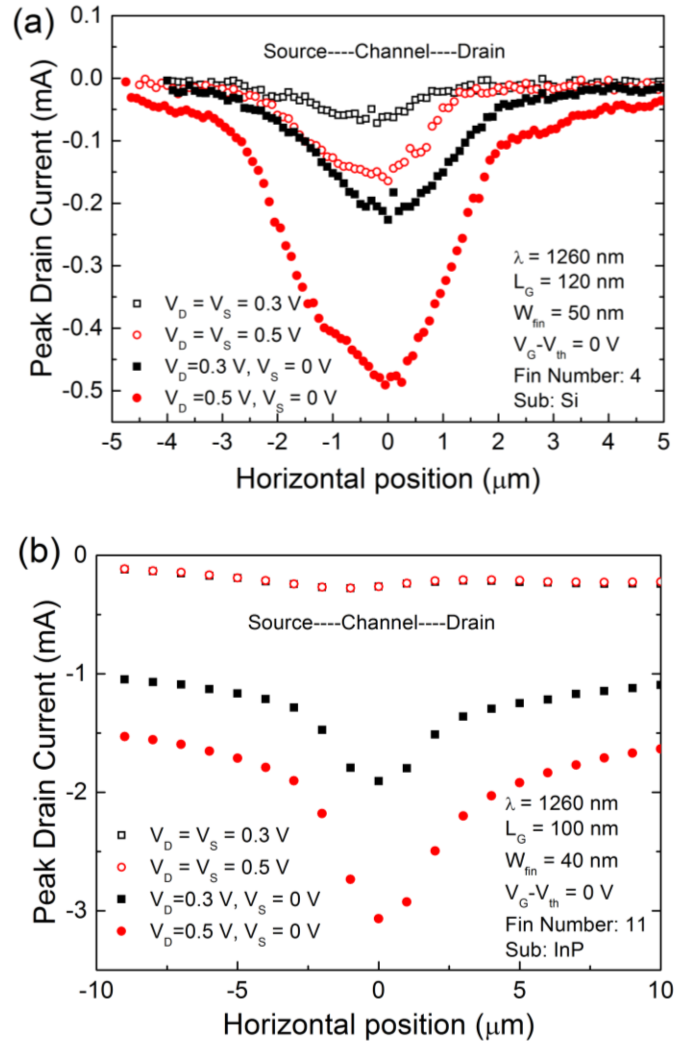


Fig. 5.7. Peak drain current along a line scan at different drain biases for an InGaAs FinFET on silicon (a) and an InGaAs FinFET on InP (b) [55]. Solid symbols correspond to $V_S = 0$ V; open symbols correspond to $V_S = V_D$.

5.4 TCAD simulations

3-D TCAD simulations were performed with Sentaurus to investigate charge collection mechanisms in these devices [88]. Fig. 5.8 shows the TCAD model of the device on silicon. The insert shows details of the gate region. The simulated devices have a gate length of 100 nm and fin width of 50 nm. The substrate

layer is truncated to 100 μm for ease of simulation. Only single fin structures were simulated, which is sufficient to understand trends in charge collection. The deposited charge in the simulations is 75 fC/μm over a distance of 8 μm, which is qualitatively similar to that produced by pulsed-laser irradiation. The charge was injected from the top of the gate to the substrate, centered at the middle of the channel. The injected charge has a Gaussian distribution in both space and time. The characteristic width of the Gaussian distribution is 50 nm. The Gaussian temporal distribution was centered at 1 ns with a characteristic time of 2 ps.

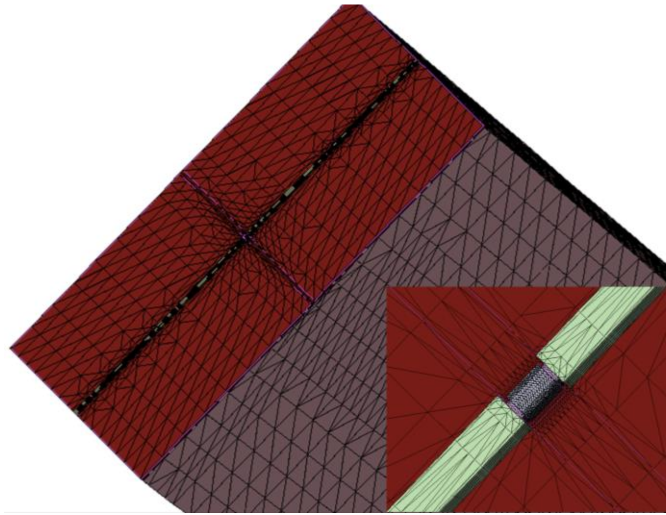


Fig. 5.8. 3-D TCAD model of an InGaAs FinFET on silicon substrate. The inset shows the details of the gate region. L_G =100 nm, W_{fin} =50 nm.

5.4.1 Parasitic bipolar amplification

III-V MOSFETs are found to be more sensitive to SET compared with silicon counterparts. One important reason is the charge enhancement in III-V FETs. The pulsed-laser generates high densities of e-h pairs. The electrons are quickly collected, while holes remain in the active region temporarily due to their relatively larger effective masses, as compared with electrons [104]. The holes accumulated in the channel or underneath the channel will produce parasitic bipolar amplification effects.

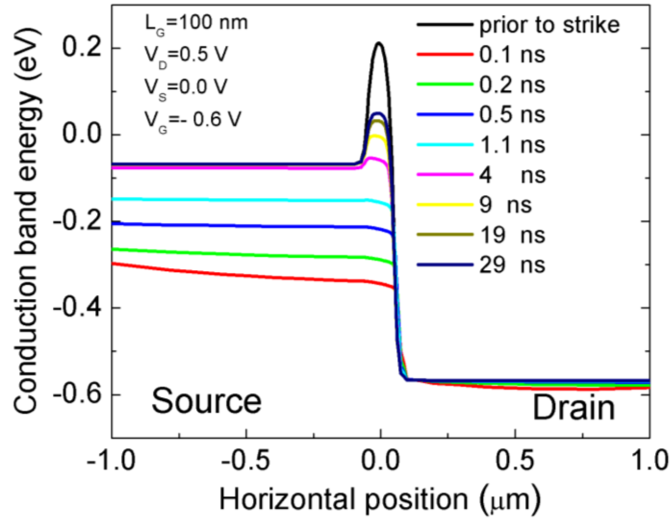


Fig. 5.9. Conduction band energy evolution along the channel after charge deposition for InGaAs FinFETs on silicon substrate. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

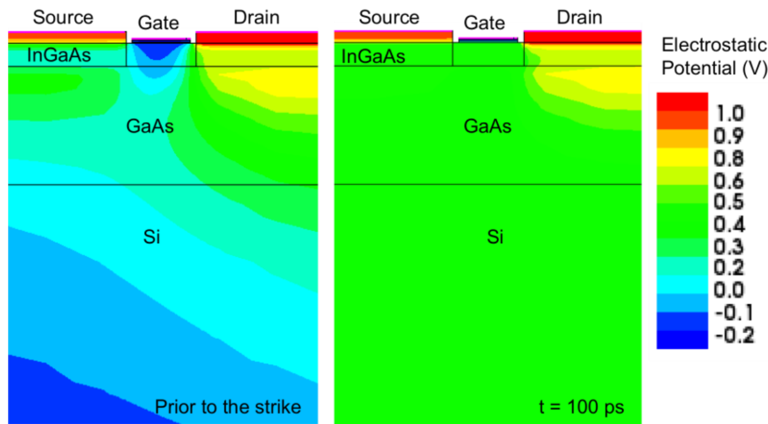


Fig. 5.10. Constant electrostatic potential contours for an InGaAs FinFET prior to the laser strike (left) and 100 ps after the strike. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

Fig. 5.9 shows how the conduction band energy along the channel evolves after charge is deposited. Prior to the charge deposition, there is a 0.3 eV barrier for electrons flowing from source to drain. After the charge deposition, the barrier disappears, and many more electrons are able to flow. This electron current contributes significantly to transient signals in typical III-V FETs. The temporal evolution of the electrostatic potential in Fig. 5.10 provides further insight into the nature of the charge enhancement in

these devices. Prior to the strike, the potential in the channel is negative underneath the gate. This negative potential prevents electrons from flowing from the source to the drain. 100 ps after the strike, the potential in the channel is positive everywhere. The electrons flow out from the source, and are collected by the drain.

5.4.2 Hole collection by the substrate

As shown in Fig. 5.3, the barrier for holes is 0.18 eV lower than that for electrons. This suggests that the substrate tends to collect holes instead of electrons. Figs. 5.11 and 5.12 show the temporal evolution of electron current density and hole current density in the substrate after the strike, respectively. There is almost no electron current observed in the substrate after the charge has been deposited, while there is a small amount of hole current flow to the substrate. The hole collection forms a positive transient current on the substrate contact. The sustained electron current on the drain matches that on the substrate, as shown in Fig. 5.4. Substrate charge collection results in less hole accumulation underneath the channel, and reduces the parasitic bipolar amplification. This leads to the low peak current and narrow FWHM transient illustrated in Fig. 5.5.

The heterostructure stack is quite different in InP-based InGaAs FinFETs [55] than in Si-based devices. Fig. 5.13 compares the band diagrams of an InP-based FinFET (solid lines) and a Si-based InGaAs FinFET (dot dashed lines). The barrier height differences for both electrons and holes are shown in the figure. The InP-based FinFET exhibits a 0.24 eV higher barrier for electrons and 0.37 eV higher barrier for holes, compared with Si-based InGaAs FinFETs. Both electrons and holes are effectively confined in the channel, which leads to strong parasitic bipolar amplification. This bipolar amplification significantly enhances the charge collection, and transients with high peak current and wide FWHM are observed in Fig. 5.5.

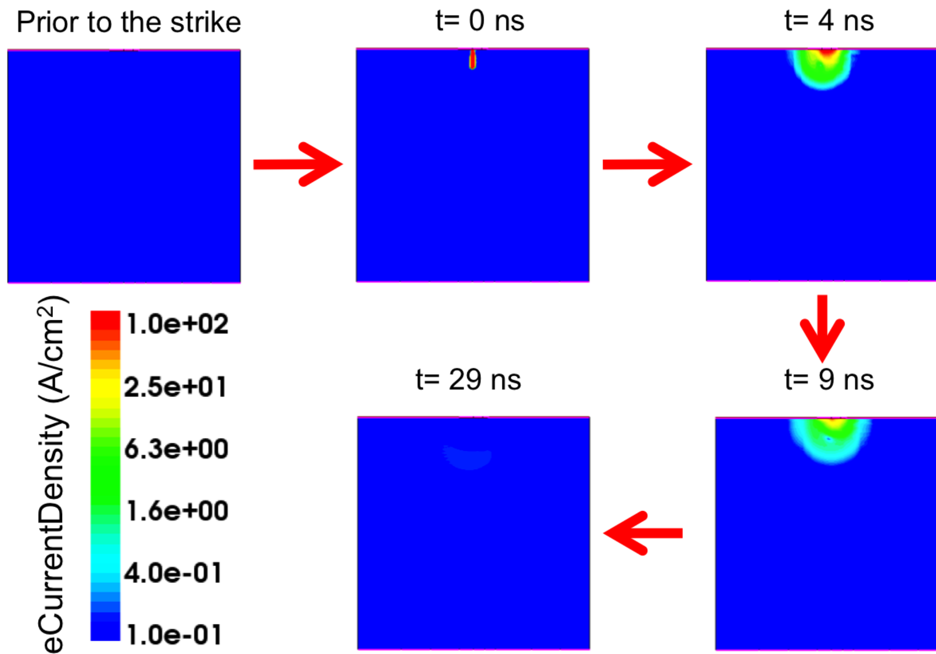


Fig. 5.11. Temporal evolution of electron current density in the substrate after the charge deposition. Substrate contact is at bottom. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

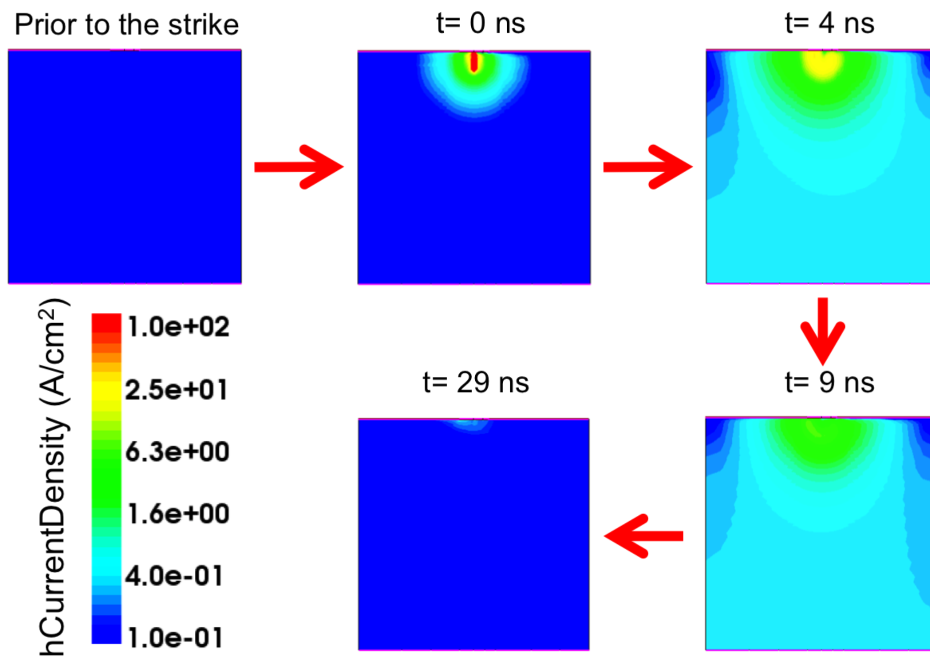


Fig. 5.12. Temporal evolution of hole current density in the substrate after charge deposition. The substrate contact is at the bottom. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

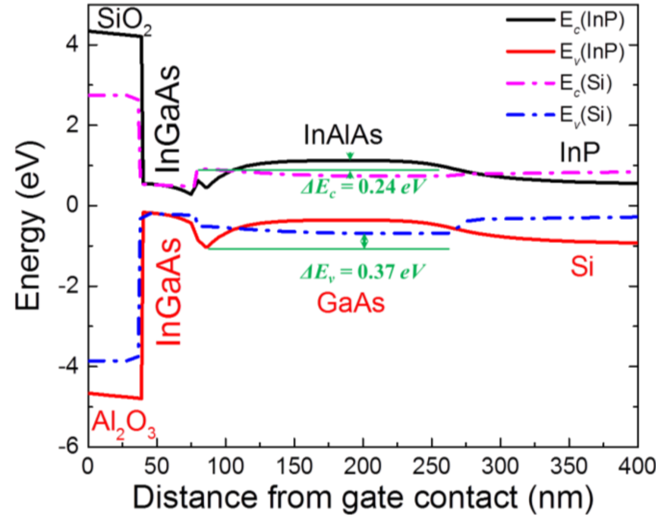


Fig. 5.13. Energy band diagrams for an InP-based InGaAs FinFET (solid lines, corresponding stack material is shown in black text, SiO_2/InGaAs/InAlAs/InP) and a Si-based InGaAs FinFET (dot dashed lines, corresponding stack material is shown in red text, Al_2O_3/InGaAs/GaAs/Si). The cut line is through the gate to substrate. The barrier difference between these two devices is also shown in the figure. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V.

5.4.3 Reduced carrier lifetime in GaAs

An efficient way to eliminate parasitic bipolar amplification effects is to use low-temperature grown GaAs (LT GaAs) buffer layers [63], [102], [103]. The measured carrier lifetime in LT GaAs can be less than 1 ps [105]-[107]. LT GaAs is grown in an As-rich environment [103]. It contains a high density of defects, which act as recombination centers for carriers. The generated e-h pairs quickly recombine, so the parasitic bipolar amplification is largely eliminated. The GaAs buffer layer (Fig 5.1 and 5.2) in this work starts with nucleation layer deposition at low temperature in the V-Groove structure. The mismatched GaAs is deposited in narrow oxide trenches, and forms defects in the buffer layer efficiently [16], [18], [108], [109]. These defects act as trapping centers for carriers, reducing the carrier lifetime in the buffer layer.

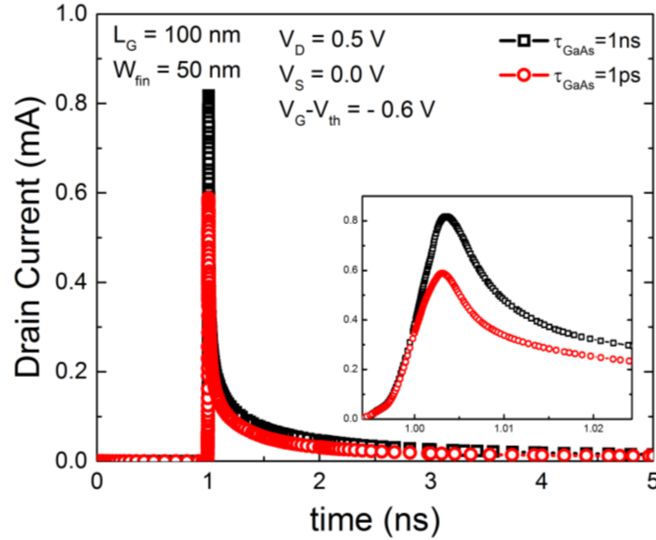


Fig. 5.14. Drain current transients for Si-based InGaAs FinFETs. The carrier lifetime is varied in the GaAs buffer layer. Black squares show transients with carrier lifetime of 1 ns, and the red circles show transients with carrier lifetime of 1 ps. The inset shows the detail of the transient peaks. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

Fig. 5.14 shows simulated drain transient currents for devices with different carrier lifetime in the GaAs buffer layer. The inset is an enlarged view of the peak region. The red curve has a lower and narrower transient peak compared with the black curve, due to the reduced carrier lifetime in the GaAs layer. This is consistent with the experimental results shown in Fig. 5.5. Fig. 5.15 shows the hole density distribution 50 ps after the strike. The figure on the left shows the hole density distribution for a GaAs layer with carrier lifetime of 1 ns. The figure on the right shows the hole density underneath the channel decreases due to the reduced carrier lifetime (1 ps). The corresponding conduction band energy along the channel is shown in Fig. 5.16. The reduction of hole density underneath the gate results in higher barriers for electrons. The increases in barrier height counteract the parasitic bipolar amplification effects, and make these devices less sensitive to SET compared with InP-substrate InGaAs FETs.

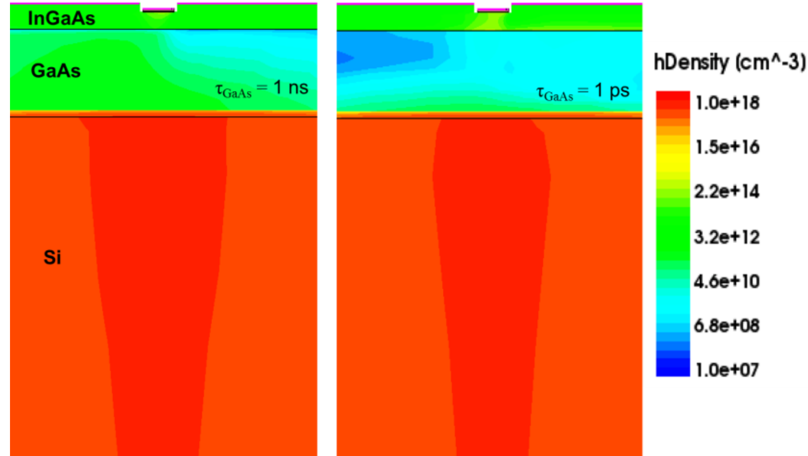


Fig. 5.15. Hole density distribution 50 ps after the strike for InGaAs FinFETs on silicon substrate. The carrier lifetime is varied in the GaAs buffer layer. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

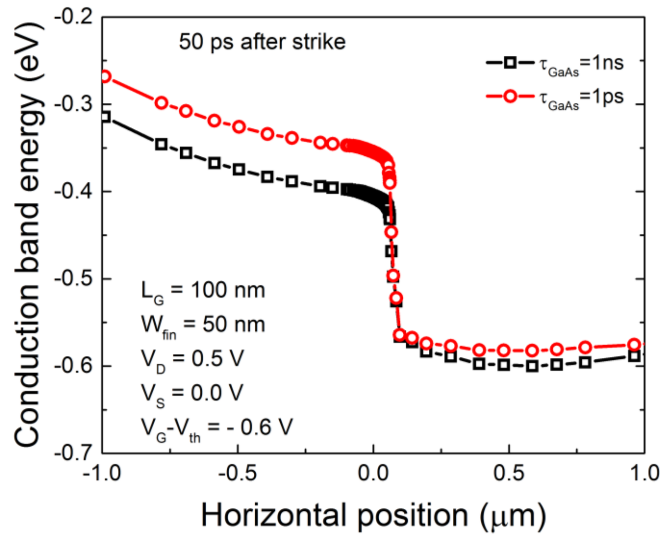


Fig. 5.16. Conduction band energy along the channel 50 ps after the strike for InGaAs FinFETs on silicon substrate. The carrier lifetime is varied in the GaAs buffer layer. $V_G - V_{th}$ = -0.6 V; V_{DS} = 0.5 V. L_G =100 nm, W_{fin} =50 nm.

5.5 Conclusions

This section describes the pulsed-laser induced SET response of InGaAs FinFETs on silicon substrates. Both channel charge collection and junction charge collection contribute to the transient

current. The channel current results from a transient source-drain shunt and parasitic bipolar amplification. The transient response is not controlled by the gate due to the 3-D FinFET structure. The SET response of Si-based InGaAs FinFETs is also compared with that of InP-based InGaAs FinFETs. The Si-based devices show lower peak current and narrower FWHM compared with their InP-substrate counterparts. TCAD simulations show that holes are efficiently collected by the substrate due to lack of confinement in the channel. Furthermore, the semi-insulating GaAs buffer layer reduces the hole lifetime, thereby reducing the hole density underneath the channel. The reduced hole accumulation in the channel eliminates source barrier lowering and bipolar amplification effects typically seen in other III-V devices, further reducing SET sensitivity. This makes Si-based InGaAs FinFET an ideal candidate for future high-mobility nMOSFET technologies.

Chapter 6

Conclusions

This dissertation focuses on understanding single-event transients in emerging III-V MOSFETs for the sub-10 nm technology node. Both pulsed-laser and heavy-ion induced SETs have been investigated. In general, heavy-ion experiments provide energetic particles analogous to space particles. This technique attracts people who care about radiation effects in space applications. Pulsed-laser experiments provide a nondestructive and low-cost method to study SEE in devices and circuits. Although the charge generation mechanisms and charge deposition profiles are different between heavy-ion and pulsed-laser testing, pulsed-laser experiments are still attractive techniques for charge collection mechanism studies. TCAD simulation tools are powerful to investigate the charge collection mechanisms. Device geometry, bias conditions, charge deposition profile, carrier lifetime, etc. can be varied to investigate the different phenomena in the charge collection process. Optical phenomena in pulsed-laser experiments are explored with Lumerical simulations, using FDTD analysis. Charge collection processes in InP-based InGaAs FinFETs, Si-based InGaAs FinFETs, and InGaAs planar MOSFETs have been explored. Multiple effects are discussed, including parasitic bipolar amplification effects, scaling effects, back-gating effects, and plasmonic effects. The key results from this dissertation are summarized in Table 6.1.

All DUTs in this dissertation are n-channel InGaAs MOSFETs with III-V materials as buffer layers to reduce the lattice mismatch. Two different materials are chosen as substrates; semi-insulating InP substrate MOSFETs are analogous to SOI MOSFETs, and the silicon substrate FinFETs are analogous to silicon bulk FinFETs. The SET responses are different from those of equivalent silicon technologies for InP-based InGaAs FinFETs and planar MOSFETs. A long tail current, which is mainly due to charge collection from the substrate, is observed in these devices. Instead, the silicon SOI MOSFETs show very quick transients due to the lack of charge collection from the substrate [51], [53]. Silicon substrate FinFETs show similar SET responces to silicon bulk FinFETs and other silicon substrate technologies, such as SiGe FinFETs [87]. In these silicon substrate technologies, the drain (or source) to substrate junction plays an important role due to the reduced channel charge collection as technology scales.

Table 6.1. Summary of single-event transients on sub-10 nm node III-V MOSFETs is this dissertation

Device		FinFET		Planar MOSFET
Channel		$In_{0.53}Ga_{0.47}As$	$In_{0.53}Ga_{0.47}As$	$In_{0.3}Ga_{0.7}As$
Buffer		$In_{0.52}Al_{0.48}As$	GaAs	$In_{0.52}Al_{0.48}As$
Substrate		InP	Si	InP
Equivalent silicon technology		SOI FinFET	Bulk FinFET	Planar SOI MOSFET
Pulsed-laser	1260 nm	√	√	√
	2200 nm	√	N/A	√
Heavy-ion		√	×	√ [65]
Peak current		shunt/bipolar/plasmonic	shunt	shunt/bipolar
Tail current		√	×	√
Substrate junction collection		×	√	×
Bipolar amplification effects		√	Reduced bipolar amplification effect	√
Plasmonic effects		Maybe	×	×
Bias dependence	Gate	×	×	√
	Drain	√	√	√
SET comparison with silicon technology		Different, tail current due to substrate charge collection	Similar, substrate junction charge collection	Different, tail current due to substrate charge collection

Since the channel length scales for modern technologies, a shunt effect contributes to the peak current as the charge generation area covers the whole channel. Bipolar amplification effects exist in both InGaAs FinFETs and planar MOSFETs on semi-insulating substrate due to the temporary hole accumulation in the channel or underneath the channel. In a silicon substrate InGaAs FinFET, the bipolar amplification effect decreases due to charge collection by the substrate contact and the reduced carrier lifetime in the GaAs buffer layer. Small transients with low peak current and narrow FWHM are captured during the pulsed-laser tests. No transients are captured during heavy-ion experiments due to the reduced bipolar amplification effect.

Plasmonic effects may only affect charge deposition in InP-based InGaAs FinFETs. The metal/dielectric/metal nano scale stack confines the optical field inside the narrow fin, causing a plasmonic effect, which enhances the electric field inside the fins. The enhancement effect is stronger for narrower fin devices than for the wider fin devices. The free carrier density increases due to the increased electric field, causing an abrupt peak current increase when the pulsed laser is focused in the fin region. This plasmonic effect is not observed in planar MOSFETs due to lack of nano-scale optical confinement. The plasmonic effect also does not affect the SET responses on silicon substrate InGaAs FinFETs. This is because the fin height in these devices is small, which does not provide effective optical confinement in the fins. The plasmonic effect may play an important role for pulsed-laser SET characterization as transistor feature sizes enter the nanometer region, such as the next generation nanowire MOSFETs.

The transients increase for all devices at high drain bias due to the increased electric field along the channel. SETs for both InP-based InGaAs FinFETs and Si-based InGaAs FinFETs do not depend on the gate bias. The peak current decreases for InGaAs planar MOSFETs when the gate is biased in inversion. This is due to the reduced excess electron density in the channel. In InGaAs FinFETs, the channel is thin and fully depleted, so the free carrier density does not change significantly. In addition, the plasmonic-enhanced charge deposition in FinFETs is an optical effect, which reduces the gate bias dependence.

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Appendix

A. TCAD Scripts for Si-based InGaAs FinFET

InGaAs_finfet_dvs ;file name for the structure generation file

```
(sde:clear)
; ===========================================================================================
;lateral length
(define Ltot        12.5) ;total length of the device
(define Lg          0.1)   ;gate length
(define Lsd         0.05) ;source/drain length
(define Lsp         0.010)        ;the space length
(define Lfin        12.5) ;the total length of the fin structure
(define Hsub              100)          ;Substrate thickness
(define Hbuf              0.2)   ;GaAs buffer thickness
(define Hox1              0.002)    ;Al2O3 thickness
(define Hox2              0.003)    ;HfO2 thicnkness
(define Hox3              0.003)    ;TiN thickness
(define Hoxi              (+ (+ Hox1 Hox2) Hox3))     ;the oxide thickness
(define Hchannel          0.04)      ;InGaAs channel thicknesss
(define Hj               0.02)      ;InAs D/S thickness

(define Wsub              5)      ;Substrate width
(define Wfin              0.050)        ;fin thickness/width

;doping definition
(define Channeldoping         1e17)         ;channel doping
(define Jdoping   2e19)                ;D/S junction doping
(define Subdoping 5e14)                  ;Substrate doping

(define Zstrike    0.0)
;==========================================================================================
;derived quantities
;x direction is along the width direction
(define Xmaxr             (/ Wsub 2.0))             ;the maximum X coordinate of substrate
(define Xmaxl             (* Xmaxr -1.0))           ;the minimum X coordinate of substrate
```

```
(define Xfinr      (/ Wfin   2.0))      ;the maximum X coordinate of fin
(define Xfinl      (* Xfinr -1.0))      ;the minimum X coordinate of fin
(define Xoxir      (+ Xfinr Hoxi))      ;the maximum X coordinate of the side oxide
(define Xoxil      (* Xoxir -1.0))      ;the minimum X coordinate of the side oxide
(define Xjr        (+ Xfinr Hj))        ;the maximum X coordinate of D/S
(define Xjl        (* Xjr -1.0))    ;the minimum X coordinate of D/S

;y direction is along the thickness direction, perpendicular to the plane
;y=0 is defined at the bottom of the fin
(define Ybuf       (* Hbuf 1.0))    ;the y coordinate of buffer bottom
(define Ysub       (+ Ybuf Hsub))       ;the y coordinate of substrate
(define Yfincha    (* Hchannel -1.0))   ;the y coordinate of the channel in the fin
(define Yox        (- Yfincha Hoxi))   ;the y coordinate of the gate oxide
(define Yj         (- Yfincha Hj))     ;the y coordinate of D/S

(define Zmaxr      (/ Ltot 2.0))        ;the maximum z coordinate of the substrate
(define Zmaxl      (* Zmaxr -1.0))      ;the minimum z coordinate of the substrate
(define Zgr        (/ Lg 2.0))         ;the maximum z coordinate of the gate
(define Zgl        (* Zgr -1.0))        ;the minimum z coordinate of the gate
(define Zspr       (+ Zgr Lsp))         ;the maximum z coordinate of the spacer
(define Zspl       (* Zspr -1.0))       ;the minimum z coordinate of the spacer
(define Zfinr      (/ Lfin   2.0))      ;the maximum z coordinate of the fin
(define Zfinl      (* Zfinr -1.0))      ;the minimum z coordinate of the fin

;=========================================================================================
(sdegeo:set-default-boolean "ABA")   ;the new replaces old
(define GATE (sdegeo:create-cuboid (position 0.0  0.0  0.0) (position (+ Xoxir 0.01) (- Yox 0.01) (+ Zgr 0.00)) "Tungsten" "Gate"))
(define GATE1 (sdegeo:create-cuboid (position 0.0 0.0  0.0) (position (+ Xoxir 0.00) (+ Yox 0.00) (+ Zgr 0.00)) "Tungsten" "Gate1"))
(define OXIDE1 (sdegeo:create-cuboid (position 0.0   0.0  0.0) (position (- Xoxir Hox3) (+ Yox Hox3) (+ Zgr 0.00)) "HfO2" "Oxide1"))
(define OXIDE2 (sdegeo:create-cuboid (position 0.0   0.0  0.0) (position (- (- Xoxir Hox3) Hox2) (+ (+ Yox Hox3) Hox2) (+ Zgr 0.00)) "Al2O3" "Oxide2"))
(sdegeo:create-cuboid (position 0.0   0.0  0.0) (position   Xmaxr   Ysub Zmaxr)   "Silicon"     "Substrate")
(sdegeo:create-cuboid (position 0.0   0.0  0.0) (position   Xmaxr   Ybuf Zmaxr)   "SiO2"   "STI")
(sdegeo:create-cuboid (position 0.0   0.0  0.0) (position   Xfinr Ybuf Zmaxr)   "GaAs"   "Buffer")
(sdegeo:create-cuboid (position 0.0   0.0  0.0) (position   Xfinr Yfincha   Zspr) "InGaAs"  "Finchannel")
(sdegeo:create-cuboid (position 0.0   0.0  Zspr) (position  Xjr  Yj   Zfinr)   "InAs"   "Junctiond")
(sdegeo:create-cuboid (position 0.0   0.0  Zspr) (position  Xfinr Yfincha   Zfinr)   "InGaAs"  "Finchanneld")
```

```
(sdegeo:mirror-selected (get-body-list) (transform:reflection (position 0 0 0) (gvector 0 0 -1)) #t)

;renaming of the duplicated regions
(sde:add-material (find-body-id (position (/ Xfinr 2.0) (/ Yfincha 2.0) (/ (+ Zspl Zfinl) 2.0))) "InGaAs" "Finchannels")
(sde:add-material (find-body-id (position (/ Xjr 2.0) (/ (+ Yfincha Yj) 2.0) (/ (+ Zspl Zfinl) 2.0))) "InAs" "Junctions")

;==========================================================================================
(sdegeo:set-default-boolean "BAB")    ; the old replaces new
(define DRAIN (sdegeo:create-cuboid (position 0.0 0.0    (+  Zspr  0.0001))  (position  Xmaxr  (-  Yj  0.01)  Zmaxr)  "Tungsten"
"Drain"))
(define SOURCE (sdegeo:create-cuboid (position 0.0 0.0 (-  Zspl  0.0001))  (position  Xmaxr  (-  Yj  0.01)  Zmaxl)  "Tungsten"
"Source"))

;defining contact
(sdegeo:define-contact-set "substrate" 4.0       (color:rgb 0.0 1.0 0.0) "%%")
(sdegeo:define-contact-set "drain" 4.0    (color:rgb 0.0 1.0 0.0) "**")
(sdegeo:define-contact-set "gate" 4.0    (color:rgb 1.0 0.0 0.0) "++")
(sdegeo:define-contact-set "source" 4.0 (color:rgb 1.0 1.0 0.0) "@@")

(sdegeo:set-current-contact-set "gate")
(sdegeo:set-contact-boundary-faces GATE)
(sdegeo:delete-region GATE)

(sdegeo:set-current-contact-set "drain")
(sdegeo:set-contact-boundary-faces DRAIN)
(sdegeo:delete-region DRAIN)

(sdegeo:set-current-contact-set "source")
(sdegeo:set-contact-boundary-faces SOURCE)
(sdegeo:delete-region SOURCE)

(sdegeo:define-3d-contact (find-face-id (position 0.005 Ysub 0)) "substrate")
;==========================================================================================
;defining doping profile

;Substrate doping
(sdedr:define-constant-profile "Subdoping" "BoronActiveConcentration" Subdoping)
(sdedr:define-constant-profile-region "Subdopingplacements" "Subdoping" "Substrate")
```

```
;channel doping
(sdedr:define-constant-profile "Channeldoping" "ArsenicActiveConcentration" Channeldoping)
(sdedr:define-constant-profile-region "Channeldopingplacement" "Channeldoping" "Finchannel")
(sdedr:define-constant-profile-region "Channeldopingplacements" "Channeldoping" "Finchannels")
(sdedr:define-constant-profile-region "Channeldopingplacementd" "Channeldoping" "Finchanneld")

;D/S junction doping
(sdedr:define-constant-profile "Jdoping" "ArsenicActiveConcentration" Jdoping)
(sdedr:define-constant-profile-region "Jdopingplacements" "Jdoping" "Junctions")
(sdedr:define-constant-profile-region "Jdopingplacementd" "Jdoping" "Junctiond")

;==========================================================================================
;defining mesh

(define XRM    20) ;maximum
(define YRM    20) ;maximum
(define ZRM    20) ;maximum

(define XRm    10) ;minimum
(define YRm    10) ;minimum
(define ZRm    10) ;minimum

(define XFRM    20) ;maximum
(define YFRM    20) ;maximum
(define ZFRM    20) ;maximum

(define XFRm    10) ;minimum
(define YFRm    10) ;minimum
(define ZFRm    10) ;minimum

;substrate multibox
(sdedr:define-multibox-size "Multi.Substrate" (/ Wsub 10.0) (/ Hsub 10.0) (/ Ltot 10.0) (/ Wsub 15.0) (/ Hsub 30.0) (/ Ltot 15.0) 1
1.5 1 )
(sdedr:define-refeval-window "Ref.Substrate" "Cuboid" (position 0.0 Ybuf Zmaxl) (position Xmaxr        Ysub Zmaxr))
(sdedr:define-multibox-placement "Multi.Substrate.Place" "Multi.Substrate" "Ref.Substrate")

;buffer multibox
(sdedr:define-refeval-window "Ref.Bufferl" "Cuboid" (position 0 0 Zmaxl) (position Xfinr Ybuf 0) )
(sdedr:define-multibox-size "Multi.Bufl" (/ Wfin 10.0) (/ Hbuf 5.0) (/ Ltot 10.0) (/ Wfin 15.0) (/ Hbuf 10.0) (/ Lfin 50.0) 1 1 -1.5
)
```

```
(sdedr:define-multibox-placement "Multi.Bufl.Place" "Multi.Bufl" "Ref.Bufferl")

(sdedr:define-refeval-window "Ref.Bufferr" "Cuboid" (position 0 0 Zmaxr) (position Xfinr Ybuf 0) )
(sdedr:define-multibox-size "Multi.Bufr" (/ Wfin 10.0) (/ Hbuf 5.0) (/ Ltot 10.0) (/ Wfin 15.0) (/ Hbuf 10.0) (/ Lfin 50.0) 1 1 1.5 )
(sdedr:define-multibox-placement "Multi.Bufr.Place" "Multi.Bufr" "Ref.Bufferr")

;fin channel
(sdedr:define-refeval-window "Ref.FinChaWin" "Cuboid" (position 0 0 Zfinl) (position Xfinr Yfincha Zfinr))
(sdedr:define-refinement-size "Ref.FinCha" (/ Wfin 5.0) (/ Hchannel 5.0) (/ Lfin 5.0) (/ Wfin 10.0) (/ Hchannel 20.0) (/ Lfin 5.0))
(sdedr:define-refinement-placement "Ref.FinCha.Place" "Ref.FinCha" "Ref.FinChaWin")

;along the channel direction, under the gate
(sdedr:define-refeval-window "Ref.FinGateWin" "Cuboid" (position 0 0 (- Zgl 0.001)) (position Xfinr Yfincha (+ Zgr 0.001)))
(sdedr:define-refinement-size "Ref.FinGate" (/ Wfin 5.0) (/ Hchannel 1.0) (/ Lg 10.0) (/ Wfin 5.0) (/ Hchannel 1.0) (/ Lg 15.0))
(sdedr:define-refinement-placement "Ref.FinGate.Place" "Ref.FinGate" "Ref.FinGateWin")

;ion strike
(sdedr:define-refeval-window "Ref.Ion.Win" "Cuboid" (position -0.05 Yfincha (- Zstrike 0.05)) (position 0.05 Ysub (+ Zstrike
0.05)) )
(sdedr:define-refinement-size "Ref.Ion" 0.01 0.5 0.01 0.002 0.05 0.002)
(sdedr:define-refinement-placement "Ref.Ion.Place" "Ref.Ion" "Ref.Ion.Win")
(sdeaxisaligned:set-parameters "minEdgeLength" 1e-3 )
(sdedelaunizer:set-parameters "minEdgeLength" 1e-3 "edgeProximity" 0.3)

(sde:build-mesh "snmesh" "" "finfet_half")
(system:command "tdx -mtt -x -M 0 -S 0 finfet_half_msh    InGaAs_finfet_msh")
```

InGaAs_finfet_des ;file name for device simulation

```
File {
	Grid="InGaAs_finfet_msh.tdr"
	Current="InGaAs_finfet"
	Plot="InGaAs_finfet"
	Parameter="materials.par"
}

Electrode {
	{Name="source" Voltage=0}
	{Name="drain" Voltage=0}
	{Name="gate" Voltage=-0.6 Workfunction=4.65 }
	{Name="substrate" Voltage=0}
}


Physics (Region="Buffer") {
}

Physics (Region="Substrate") {
}

Physics (Region="Finchannel"){
	MoleFraction(xFraction=0.47 Grading=0)
	*eQuantumPotential
	*hQuantumPotential
}
Physics (Region="Finchannels"){
	MoleFraction(xFraction=0.47 Grading=0)
}
Physics (Region="Finchanneld"){
	MoleFraction(xFraction=0.47 Grading=0)
}
Physics {
	EffectiveIntrinsicDensity(NoBandGapNarrowing)
	Mobility(
		ConstantMobility
			Enormal(Lombardi)
		eHighFieldSaturation
```

```
        )
        Fermi
        Recombination(
            SRH
            Auger
            Radiative
        )
    }

    Plot{
        *carrier densities
            eDensity hDensity EffectiveIntrinsicDensity IntrinsicDensity
        *currents and current components
            eCurrentDensity hCurrentDensity
            eCurrentDensity/Vector hCurrentDensity/Vector
            eMobility hMobility eVelocity hVelocity
        *fields, potentials and charge distribution
            ElectricField/Vector
            Potential
            eQuasiFermi hQuasiFermi
            SpaceCharge

        *Temperatures
            LatticeTemperature
            eTemperature hTemperature
        *Doping Profiles
            Doping
        *Band Structure
            BandGap
            ElectronAffinity
            ConductionBandEnergy ValanceBandEnergy
        *Recombination
            SRH Auger


    }

Math{
    Number_Of_Threads=4
    Extrapolate
```

```
        Derivativites
        Iterations=20
        RelErrControl
        Digits=5
        NotDamped=20
        CNormPrint
        ExitOnFailure
}


Solve{
        Coupled (Iterations=20) {Poisson }
        *Coupled (Iterations=30) {Poisson eQuantumPotential}
        Coupled (Iterations=20) {Poisson Electron Hole}
        *Coupled (Iterations=20) {Poisson Electron Hole eQuantumPotential}
        Quasistationary(  InitialStep=0.01  Increment=1.5  MinStep=1e-4  MaxStep=0.1  Goal{Name="drain"  Voltage=0.5}  ){
Coupled{ Poisson Electron Hole}}
        Save(FilePrefix="Bias")
        *Load(FilePrefix="Vd1")
        *NewCurrentPrefix="Vd1_"
        *Quasistationary( InitialStep=0.01 Increment=1.5 MinStep=1e-4 MaxStep=0.05 Goal{Name="gate" Voltage=-0.8} ){
*               Coupled{ Poisson Electron Hole eQuantumPotential}
*               Plot ( Time = (0.2; 0.4; 0.6; 0.8; 0.9) NoOverwrite)}
}
```

InGaAs_finfet_see_des ;file name for the transient simulation

```
File {
	Grid="InGaAs_finfet_msh.tdr"
	Current="InGaAs_finfet_see"
	Plot="InGaAs_finfet_see"
	Parameter="materials.par"
}

Electrode {
	{Name="source" Voltage=0}
	{Name="drain" Voltage=0}
	{Name="gate" Voltage=-0.6 Workfunction=4.65 }
	{Name="substrate" Voltage=0}
}


Physics (Region="Buffer") {
}

Physics (Region="Substrate") {
}

Physics (Region="Finchannel"){
	MoleFraction(xFraction=0.47 Grading=0)
	*eQuantumPotential
	*hQuantumPotential
}
Physics (Region="Finchannels"){
	MoleFraction(xFraction=0.47 Grading=0)
}
Physics (Region="Finchanneld"){
	MoleFraction(xFraction=0.47 Grading=0)
}
Physics {
	EffectiveIntrinsicDensity(NoBandGapNarrowing)
	Mobility(
		ConstantMobility
			Enormal(Lombardi)
		eHighFieldSaturation
```

```
        )
        Fermi
        Recombination(
                SRH
                Auger
                Radiative
        )
        HeavyIon(
                PicoCoulomb
                Direction=(0,1,0)
                Location=(0,-0.04,0)
                Time=1e-9
                Length=8
                Wt_hi=0.05
                LET_f=0.076
                Gaussian
        )
}

Plot{
        *carrier densities
                eDensity hDensity EffectiveIntrinsicDensity IntrinsicDensity
        *currents and current components
                eCurrentDensity hCurrentDensity
                eCurrentDensity/Vector hCurrentDensity/Vector
                eMobility hMobility eVelocity hVelocity
        *fields, potentials and charge distribution
                ElectricField/Vector
                Potential
                eQuasiFermi hQuasiFermi
                SpaceCharge

        *Temperatures
                LatticeTemperature
                eTemperature hTemperature
        *Doping Profiles
                Doping
        *Band Structure
                BandGap
                ElectronAffinity
```

```
            ConductionBandEnergy ValanceBandEnergy
        *Recombination
            SRH Auger



    }

Math{
    Number_Of_Threads=4
    Extrapolate
    Derivativites
    Iterations=20
    RelErrControl
    Digits=5
    NotDamped=20
    CNormPrint
    ExitOnFailure
}


Solve{
    Load(FilePrefix="Bias")

    Transient(
        InitialTime=0
        FinalTime=0.95e-9
        InitialStep=1e-13
        MaxStep=1e-10
        Increment=1.2)
        {
            Coupled{Poisson Electron Hole}
            Plot (Time=(0.001e-9) FilePrefix="SE_DataA" NoOverwrite)
        }

    Transient(
        InitialTime=0.95e-9
        FinalTime=2.0e-9
        InitialStep=1e-13
        MaxStep=1e-10
        Increment=1.2)
```

```
		{
			Coupled{Poisson Electron Hole}
			Plot		(Time=(0.999e-9;1.0e-9;1.05e-9;1.1e-9;1.15e-9;1.2e-9;1.3e-9;1.4e-9;1.5e-9;1.6e-9;1.7e-9;1.8e-9)
FilePrefix="SE_DataB" NoOverwrite)
		}

	Transient(
		InitialTime=2.0e-9
		FinalTime=30e-9
		InitialStep=1e-12
		MaxStep=2e-10
		Increment=1.2)
		{
			Coupled{Poisson Electron Hole}
			Plot			(Time=(2.1e-9;3.0e-9;4.0e-9;5.0e-9;6e-9;7e-9;8e-9;9e-9;10e-9;12e-9;14e-9;16e-9;20e-9)
FilePrefix="SE_DataC" NoOverwrite)
		}
}
```