CHAPTER I

INTRODUCTION

Indium Arsenide (InAs) channel high electron mobility transistors (HEMTs) with Aluminium Antimonide (AlSb) barriers are an exciting option for low power RF applications due to excellent quantum well confinement (ΔE_c = 1.3 eV) and very high low-field electron mobility (~ 25000 cm^2/V-s). While some studies of high temperature life testing have been performed on this device, the fundamental degradation trends and mechanisms for the device are yet to be adequately understood. In this thesis, a detailed analysis of DC and RF degradation under hot carrier stress is presented.

Based on electrical stress performed on devices with varied starting characteristics, we show that some devices are severely degradation prone in operating conditions where the electric field in the Indium Arsenide channel and the impact ionization rate are simultaneously high. Annealing results, coupled with device simulations and Density Functional Theory (DFT) calculations, show trends consistent with an oxygen-induced metastable defect in AlSb dominating the device degradation. Some physically abundant impurities like Carbon and Tellurium are shown to be unlikely candidates for producing the observed degradation.

When stressed with hot carriers or under high impact ionization conditions, the majority of the devices show negligible change in DC characteristics, but appreciable degradation in peak transition frequency (f_T). Short access region lengths exacerbate the degradation, which can be traced to a reduction in peak RF transconductance (g_m), resulting either

from reduced hole mobility or a stress-induced increase in thermodynamic relaxation time of electrons in the channel. Increase in parasitic capacitances after stress is shown to have a secondary contribution to the degradation in devices with long access regions. For devices with short access regions – a post-stress increase in gate to source parasitic capacitance (C_{gs}) significantly adds to degradation caused by reduction in peak RF g_{m}.

In Chapter II of this thesis, the special features of InAs as a high electron mobility material and the efficacy of the HEMT technology for low power RF applications are described. Then, the common performance and fabrication related difficulties are discussed. In the next chapter, the common types of electrical and physical degradation of the InAs - AlSb HEMT described in published literature so far are discussed in detail. In Chapter IV, we describe the general electrical characteristics of the devices used in this work. The DC stress experiments and most prominent degradation trends are described in Chapter V. In the next section, we relate our experimental data to a number of possible defects (based on their physical abundance in the InAs - AlSb material system) and discuss the methods of determining the feasibility of a defect being responsible for the observed types of degradation. This aspect of the analysis uses the results of first principles quantum mechanical calculations of the energetics of defects. In Chapter VII, we discuss the effects of DC stress on devices that show no perceptible signs of DC degradation but significant small signal performance degradation when stressed. This section focuses more on relating the degradation to components of the small signal equivalent circuit of the HEMT rather than specific defects at specific locations of the device.

CHAPTER II

INTRODUCTION TO INDIUM ARSENIDE ELECTRONICS

2.1. Material Properties and Device Performance

Indium Arsenide has generated interest as a candidate for very high speed, low power electronic devices. The electronic band structure of InAs allows for fast electron transport on account of its very low effective mass ($0.023m_o$) in the Γ-valley relative to almost all other common III-V semiconductors, except InSb, and a large Γ-L valley separation (relative to band gap and electron energies at nominal operating conditions) of 0.72 eV. The decrease in effective mass directly impacts the low-field mobility of each semiconductor material, as evidenced by a very high 300 K electron mobility of 25,000 cm^2/V-s in nominally undoped InAs. The InAs - AlSb HEMT derives its high-speed performance from the inherently fast electron transport properties of the channel semiconductor. In addition to this, a huge conduction band offset of 1.35 eV with the nearly lattice matched AlSb (a = 6.2 Å) allows for high electron confinement in the quantum well, large subband spacing and large 2 DEG densities ~ 2×10^{12} cm^{-2} [1]. For these reasons, the InAs - AlSb HEMT has the capability of being an ideal device for high speed, low power RF circuits [2-11].

Devices having very high DC and RF g_m (~1500 mS/mm at 500 mV drain bias) and peak f_T (~300 GHz) [5] have been reported consistently. However, the InAs - AlSb HEMT has traditionally suffered from a relatively high f_T /f_{max} ratio ~2. Bergman *et al.* achieved a simultaneously high peak RF g_m (~1500 mS/mm at 500 mV drain bias), peak f_T and peak

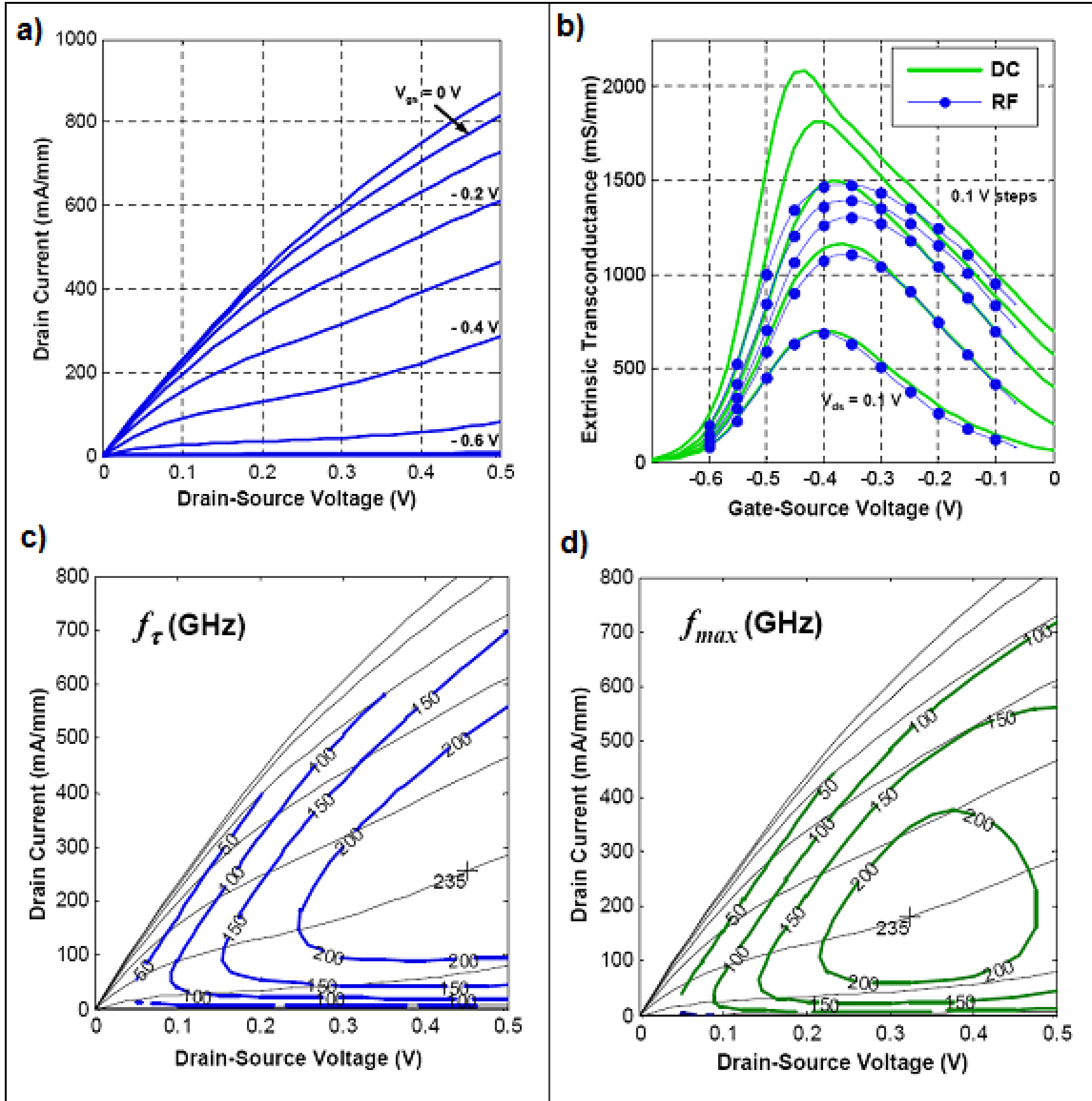

Fig. 1.a) The DC output characteristics of a vertically scaled 100 nm gate length InAs - AlSb HEMT. Drain currents above 800 mA/mm are observed with excellent pinch-off. The gate diode leakage current (not shown) is 2 nA/µm at -200 mV gate bias. b) The RF g_m exhibits a high peak value of 1500 mS/mm at V_{ds} = 500 mV, indicative of high electron velocities in the channel. The DC transconductance peaks at over 2000 mS/mm at a drain bias of 500mV – artificially enhanced by feedback of impact-generated holes. c) f_T contours show a peak of 235 GHz at a drain bias of 450 mV, and indicate that the InAs - AlSb HEMT maintains a high f_T, at very low drain voltages. d) f_{max} contours show a peak of 235 GHz at a drain bias of 300 mV. f_T remains above 100 GHz at drain biases as low as 100 mV [6].

f_{max} ~235 GHz at a drain bias of 300 mV, and f_T, f_{max} values exceeding 100 GHz at drain bias of only 100 mV. This was achieved by aggressively scaling the top barrier over the

InAs channel from the usual 18 - 25 nm to 14 nm. A composite barrier was used: a 9 nm top AlSb layer capped by a 5 nm $In_{0.5}Al_{0.5}As$ layer (Fig. 2) [6]. The capability of InAs - AlSb HEMTs in high speed, low power electronics has been demonstrated through the fabrication of an ultra wideband ultra-low-DC power high gain millimeter wave IC (MMIC) low noise amplifier (LNA) with differential RF input using 0.1-µm gate length devices. A 3 - 12 GHz wideband on-chip MMIC balun was used at the differential input. Even with the loss of the balun included, the differential amplifier demonstrated 4 dB typical noise figure with associated gain of 22 dB from 3 - 12 GHz at a low DC dissipation of 23 mW. Additionally, a single-ended LNA, on which the differential LNA was based, was also fabricated for evaluation. The single-ended LNA demonstrated 1.5 dB typical noise figure with associated gain of 25 dB from 1 - 16 GHz at a low DC dissipation of 16 mW [7].

2.2 Basics of HEMT Operation

InAs - AlSb HEMTs are typically depletion-mode devices. An extremely high conduction band discontinuity of 1.3 eV with the lattice matching AlSb ensures that even electrons from very deep donors in the AlSb layer end up in the InAs layer. The HEMT employs a Te delta doping (a very thin layer of dopant atoms to ensure maximum 2DEG density) placed roughly midway through the top AlSb layer (Fig. 2). The large spatial separation of channel electrons from their donors minimizes scattering from DX centers (a complex involving a donor atom and another constituent) [12-13]. It is possible to achieve channel carrier densities of ~ 2×10^{19} cm^{-3} without significantly degrading the low field mobility

[8]. The channel is depleted by putting a negative bias on a Au/TiW or Cr/Au Schottky gate. Thus, a high carrier density is achieved with little or no vertical electric field induced mobility reduction. A high transconductance device requires the top layer (marked InAlAs in Fig. 2) to be as thin and have as narrow band gap as possible. Additional material must be included above the top AlSb layer because it oxidizes easily, which increases the volume by almost a factor of two and cracks the entire epitaxial layer. Earlier devices used protective caps of InAs. While this was supposed to be useful for easy charge control due to the narrow band gap of InAs, it suffered from high gate leakage. Scaling the top AlSb layer, and using a relatively high band gap $In_{0.5}Al_{0.5}As$ (E_g = 1.3 eV) circumvented the problem.

The very deep quantum well plays two important roles. First it ensures that even very deep donors contribute to the 2DEG, at least close to the interface. The Fermi level is prevented from rising at a logarithmic rate with addition of ionized donors in the AlSb layer adjacent to the channel. For example, a typical device will have a high channel carrier density derived from the Te Δ-doping, but the Fermi level in the AlSb is close to or below midgap. This means that even donor-like defects close to midgap can play a significant role in influencing device characteristics, if present in large enough numbers. This also implies a stronger immunity to the carrier freeze-out effect that occurs in doped semiconductors at low temperatures. In a HEMT channel, this effect is avoided since the electrons are in a region of energy below the donor levels in the high band gap material. Thus a high carrier density can be maintained at very low temperature, exploiting the low temperature improvement in transport. Extremely low noise, high gain microwave devices are possible exploiting this low temperature feature for special applications such

as deep space signal reception. The second role is the fairly large separation of the states in the quantum well (E_0 and E_1 are separated by almost 0.4 eV in a typical structure) (Fig. 2), which reduces scattering and keeps the mobility at a high value in the region of operation of the HEMT.

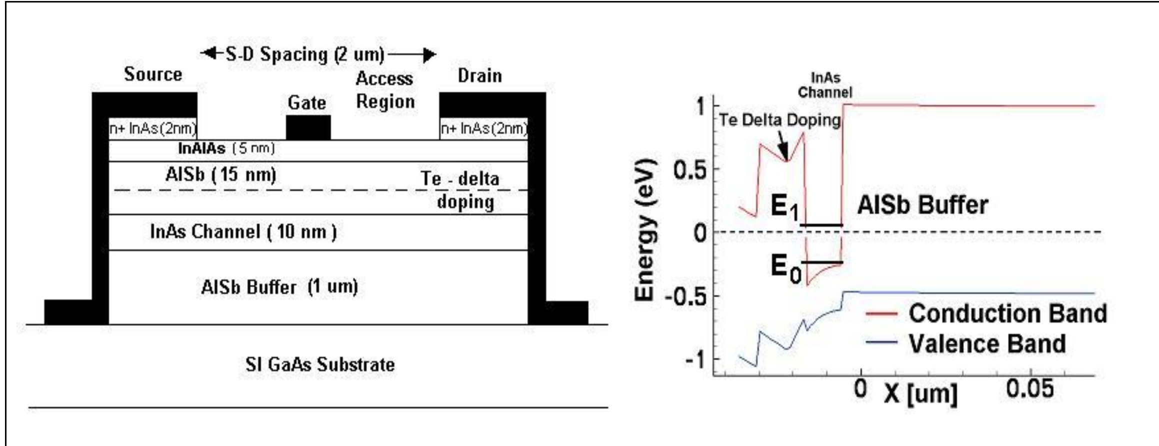

Fig. 2. Cross Section and simulated vertical band profile of the InAs - AlSb HEMT. For the simulated case, E_1 - E_0 ~ 0.4 eV.

The AlSb buffer thickness at the back of the channel plays an important role in reducing threading dislocations with the semi-insulating GaAs substrate, whose lattice constant (a = 5.65 Å) is significantly different from either InAs or AlSb.

2.3 Electron Transport in the InAs - AlSb 2DEG (Comparison to Popular High-Speed RF Devices)

The InAs - AlSb HEMT, like its counterparts in the GaAs and InP material systems, derives its high-speed performance from the inherently fast electron transport properties

of the channel semiconductor, as opposed to the field effect transistors in homogeneous materials (like Silicon) for which advanced device engineering dictates the transistor performance. As discussed in Section 2.1, the low effective mass of InAs ($m_e = 0.023m_o$) permits the realization of InAs quantum wells with very high electron mobilities. Of greater importance in a HEMT is the improvement in the peak and saturation electron velocities in InAs over those of GaAs and $In_{0.53}Ga_{0.47}As$ (two popular materials for high-speed RF circuits), which increases the maximum possible transistor speed by lowering electron transit times through the channel. The electron velocity in the channel is related to the intrinsic transconductance by:

$$g_{mi} = C_{gs}.v_e \tag{1}$$

where g_{mi} is the intrinsic transconductance per unit gate width, C_{gs} is the specific gate to source capacitance (capacitance per unit area), and v_e represents the average electron velocity [10]. This result yields the dependence of the cutoff frequency f_T on the electron velocity:

$$f_T = 1/2\pi.(v_e/ L_g) \tag{2}$$

where L_g is the gate length. This is a simplified formula because it neglects additional parasitic capacitances and resistances present in a practical HEMT equivalent circuit. Because InAs has the highest electron velocity of any III-V semiconductor, an InAs channel HEMT should be able to obtain the highest possible device speed at a given gate

length. Use of AlSb barriers (because the nearly lattice-matched AlSb has a conduction band offset of 1.35 eV relative to InAs [14], the largest conduction band offset of any pair of (nearly) lattice-matched III-V semiconductors) gives additional advantage. The InAs - AlSb combination makes possible a very deep quantum well that can hold a much higher electron density than that achievable in GaAs/AlGaAs and InGaAs/InAlAs HEMTs. Development of GaAs PHEMTs (pseudomorphic HEMTs where the quantum well is formed between 2 layers of significant lattice mismatch – achieved by making the top layer extremely thin so that it simply stretches over the bottom layer without increasing defect density at the interface) and InP-based HEMT technologies has shown that a high electron sheet density is the most critical parameter in the realization of fast transistors. In fact, nearly all of the high frequency performance improvement of InGaAs/AlGaAs PHEMTs over GaAs HEMTs can be attributed to the higher modulation efficiency attributable to the deeper quantum well [15], since there is no significant change in the electron mobility or drift velocity. Comparisons of otherwise identical $In_{0.53}Ga0_{.47}As/In_{0.52}Al_{0.48}As$ HEMTs indicate that raising the channel sheet charge through delta doping in the HEMT increases the transistor’s cutoff frequency and linearity [16]. The essential properties of the InAs - AlSb HEMT 2DEG are listed in Table 1, with those of the GaAs HEMT, GaAs PHEMT, and InP-based HEMT included for comparison [10]. The Hall sheet charge and mobility represent the high end of published values for sheet charge density and mobility for each technology. The channel sheet conductivity for the heavily doped InAs - AlSb HEMT ($n_s = 8.0 \times 10^{12}$ cm^{-2}, $\mu =$ 19,000 cm^2/V-s) [1] is four times that of an InP-based HEMT, demonstrating the potential for high-speed operation at low drain voltages.

The inherent improvement in electron transport properties in InAs - AlSb HEMTs are compared to those of GaAs or InP-based HEMTs in Table I. The typical InAs - AlSb HEMT targets a sheet charge density of 3-4 $\times 10^{12}$ cm^{-2}, and exhibits a room temperature mobility of about 18,000 cm^2/V-s, compared with 6,000 and 10,000 cm^2/V-s for quality GaAs and InP-based HEMTs, respectively.

	GaAs HEMT	GaAs PHEMT	InP HEMT	InAs HEMT
Channel Composition	GaAs	$In_{0.25}Ga_{0.75}As$	$In_{0.53}Ga_{0.47}As$	InAs
Barrier Composition	$Al_{0.3}Ga_{0.7}As$	$Al_{0.3}Ga_{0.7}As$	$In_{0.52}Al_{0.48}As$	AlSb
Channel Band Gap (eV)	1.42	1.21	0.73	0.36
Conduction Band Barrier Height (eV)	0.26	0.37	0.52	1.35
Peak Electron Velocity (cm/s)	2.0×10^7	$\approx 2.0 \times 10^7$	2.7×10^7	4.0×10^7
2DEG Sheet Charge (cm^{-2})	1.2×10^{12}	2.5×10^{12}	3.5×10^{12}	8.0×10^{12}
2DEG Hall Mobility (cm^2/Vs)	6,000	6,600	9,500	19,000

TABLE 1. Fundamental Properties of 2DEGs of four different high-speed technologies[10].

2.4 Common Performance and Reliability Issues in InAs - AlSb HEMT Operation

A. Kink Effect

The InAs channel is prone to effects related to avalanche-generated holes. The small band gap results in appreciable impact ionization rates even at normal operating voltages. The type II band alignment (valence band of AlSb is lower in energy than that of InAs) results in immediate discharge of holes into the AlSb layers. While the holes discharged towards

the gate are readily swept out, the ones directed towards the back channel move slowly through AlSb. The electrostatic effect of this lowers the source-channel barrier and increases the channel inversion level, increasing the output conductance of the device (Fig. 3). This hole-induced floating body effect is popularly known as the kink effect [9]. The kink can sometimes be masked by the fact that the operating drain biases are not large enough to cause channel pinch off or velocity saturation for the commonly high source-drain spacing. Along with the DC output conductance, the kink effect impacts dispersion at low microwave frequencies. A number of techniques can be employed to mitigate the kink effect – such as use of heavily p+ doped contacted GaSb back gates. However, most of these methods come at the cost of considerable structural complexity and sometimes significant loss of device performance (such as reduction of channel sheet charge density due to the use of heavily doped p+ GaSb layers).

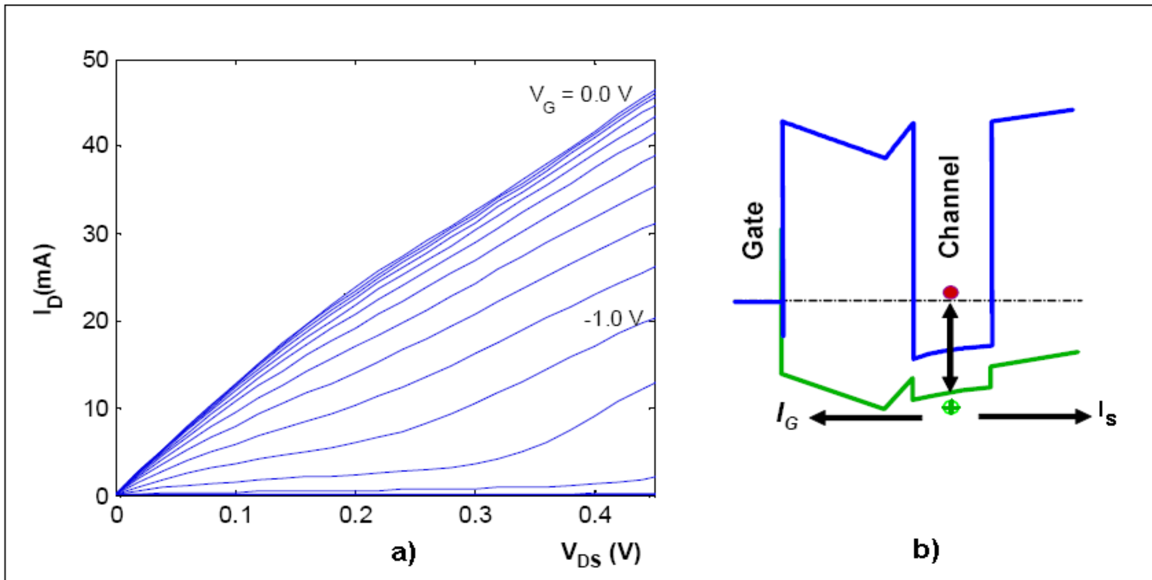

Fig. 3. a) High output conductance on a 2 × 20 × 0.1 μm HEMT, b) Schematic band diagram showing discharge of holes to AlSb due type II alignment [10].

B. Antimonide Processing Difficulties

One of the major obstacles in the development of InAs - AlSb HEMTs is the lack of experience in antimonide processing relative to the decades of processing experience in more common III-V semiconductors like GaAs. The most prominent problem in the initial stages was the extreme reactivity of the AlSb in air. When the AlSb metamorphic

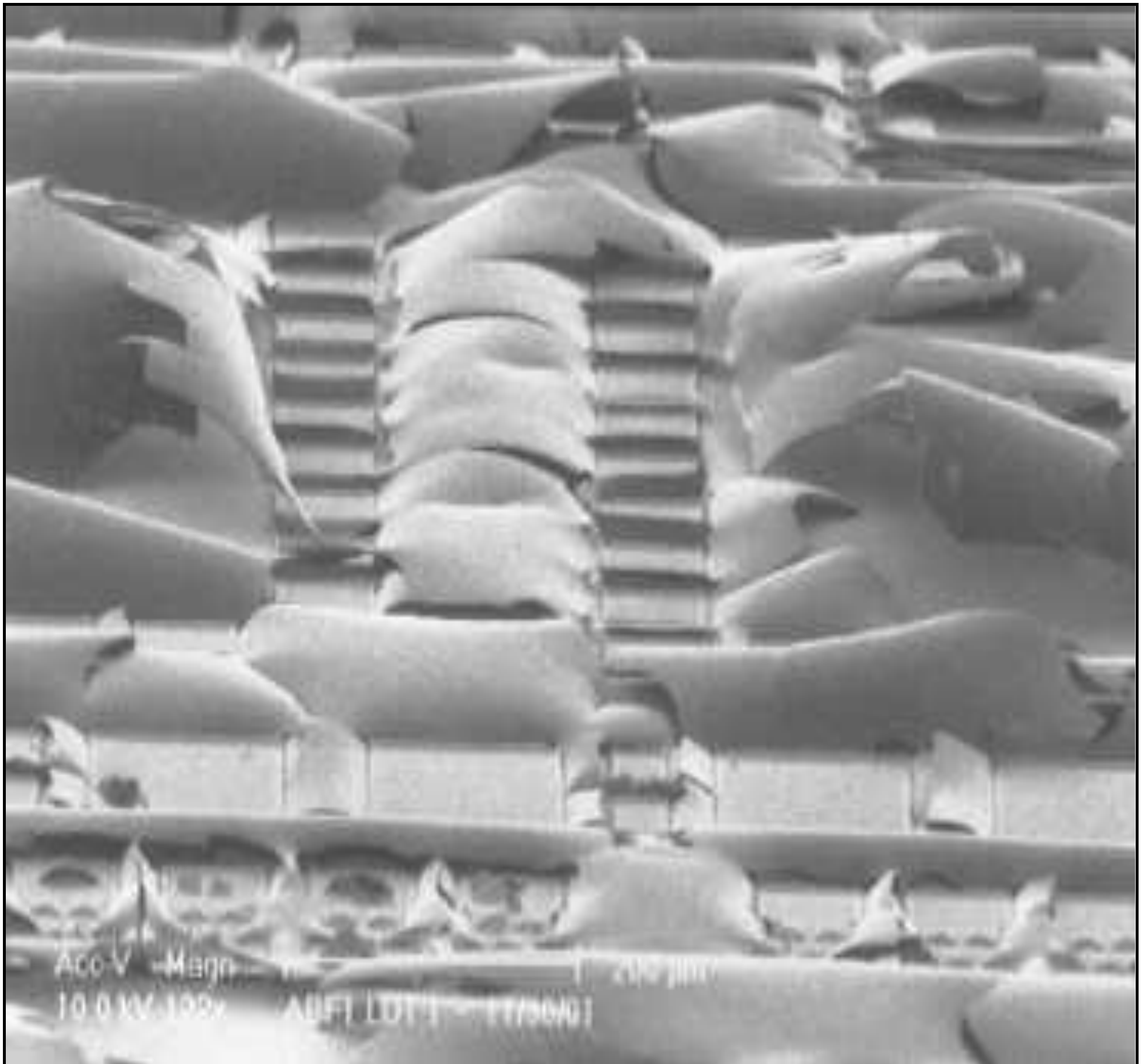

Fig. 4. SEM micrograph of an InAs - AlSb HEMT wafer after the AlSb buffer oxidized and cracked [10].

buffer layer wass exposed, it immediately oxidized, and within one day would be oxidized all the way to the GaAs substrate. Since the AlSb roughly doubles in volume as it oxidizes, the entire epitaxial layer would then crack and flake as shown in Fig. 4, destroying the wafer completely. Expanding the thickness of the buffer layer from 300 Å to 2000 Å solved this problem. However, it is difficult to achieve large transconductance values with such a thick buffer layer.

In addition to the oxidation problems associated with the AlSb buffers, the early HEMTs employed a 50 Å GaSb cap layer instead of the $In_{0.5}Al_{0.5}As$ layer [17], which created multiple difficulties in the HEMT processing. However, it was not possible to achieve acceptable Ohmic contact resistances with GaSb-capped HEMTs. Alloyed Pd and AuGe-based Ohmic contacts were unable to produce contacts with resistances below 0.3 Ω-mm, and the contacts exhibited poor linearity and reproducibility [10]. An Ohmic contact process by which the InAs channel was directly contacted after etching the overlying cap and barriers was tried without success. The first such experiments used NH_4OH: H_2O and CH_3COOH: H_2O_2: H_2O as selective wet chemical etches between Al(Ga)Sb and InAs [11], and yielded very poor contacts, with unacceptable contact linearity and contact resistances over 0.5 Ω-mm. The poor contacts could be explained by either the presence of a residual Sb oxide layer between the Ohmic metal and InAs or by the exposed InAs channel in the laterally undercut region. One experiment that addressed these problems used a BCl_3 Reactive Ion Etch to etch the contact holes to the InAs channel in order to minimize the lateral undercut and exposed InAs surface at the edge of the Ohmic metal. While the contact resistance improved to 0.2 Ω-mm, this was still not acceptable for a high-speed, low-voltage HEMT technology. When the transition was made to $In_{0.5}Al_{0.5}As$

caps, low-resistance, highly reproducible diffused Pd ohmic contacts were readily obtained. Finally, HEMTs with a GaSb cap showed high gate leakage, likely due to surface conduction between the gate and source/drain Ohmic contacts, in addition to hysteretic effects indicative of charge trapping. Again, these effects were eliminated after the transition was made to $In_{0.5}Al_{0.5}As$ caps.

The current Ohmic contact process employs diffused palladium contacts [18], which have consistently produced contacts with resistances less than 0.07 Ω-mm. The Ohmic metal is patterned with conventional photolithographic techniques and the Ohmic metal stack is deposited via electron-beam evaporation. After lift-off of the Ohmic metal, the Pd is diffused into the semiconductor with a low temperature anneal at 180 °C for 15 minutes. After mesa isolation, the measurement of contact resistances across each wafer using the transfer length method (TLM) shows low contact resistances ranging from 0.04 to 0.07 Ω-mm, with cross-wafer variances of less than 0.02 Ω [10].

C. Anisotropic Effects and Microcracks

Since the HEMTs used in our studies use an $In_{0.5}Al_{0.5}As$ cap, it is worth discussing one more performance and reliability issue related to these structures. Hall data on as-grown InAs - AlSb wafers with $In_{0.5}Al_{0.5}As$ caps has shown that the voltages in van der Pauw measurements varied substantially depending on the direction of the forced current. The magnitude of the anisotropy is variable, but it is more pronounced at 77 K than at room temperature. Insight into the cause of this anisotropic degradation of the channel conductivity is provided by atomic force microscopy of the as-grown InAs - AlSb wafers. Tiny micro-cracks of at least 200 Å in depth are observed on the surface of the wafers with $In_{0.5}Al_{0.5}As$ caps, and these cracks are primarily oriented parallel to the [011] axis. It

is suspected that these micro-cracks degrade the mobility of electrons in the direction perpendicular to the cracks. This hypothesis is supported by the dramatic increase in the anisotropy at 77 K relative to that measured at room temperature, implying that the mobility cannot increase with decreasing temperature as the mean free path of the electrons becomes larger than the separation between cracks. Since the anisotropy was first observed in the HEMTs with $In_{0.5}Al_{0.5}As$ caps, it was suspected that the strained cap layers were responsible for the phenomenon. Indeed, an increased V to III flux ratio alleviated this problem to a large extent; the micro-crack densities (defined as the area density multiplied by the average crack length) as determined by AFM were reduced by approximately a factor of five [10].

CHAPTER III

PREVIOUS DEGRADATION STUDIES – HIGH TEMPERATURE LIFE-TESTING

Before we discuss the effects of electrical stress and use them to characterize the InAs - AlSb system, it is useful to look at some earlier studies on the effects of thermal and electrical stress in this system. Chou *et al.* reported the results of high temperature (~170 °C) life-testing on 100 nm gate length devices [19-20]. The degraded devices showed increase of drain current, decrease of transconductance (g_m) and gate-current increase (Fig. 5). Three-temperature life-testing at $T_{ambient}$ of 150, 160, and 170 °C, with 11 samples for each temperature, was performed in N_2 atmosphere. To avoid potential lateral Ohmic metal diffusion-induced destructive failure, the testing temperature was kept below 190 °C. The devices were stressed at V_{ds} = 0.2 V and I_{ds} = 150 mA/mm with total power dissipation of 2.4 mW. Comprehensive DC characterization, including gate-source/gate-drain diode characteristics, characteristics of I_{ds} and g_m versus gate voltage (V_{gs}), and DC current-voltage (*I*-*V*) characteristics, was performed at room temperature on the samples after each interval of life-testing. After almost 180 hours of high temperature life-testing, devices showed no indication of gate sagging (mechanical collapse of the T-shaped gate). The three temperature life-testing shows that the activation energy (E_a) is approximately 1.5 eV and demonstrates a median time to failure (MTF) of 2×10^6 hours at $T_{junction}$ of 85 °C. The rate of increase in gate current and shift in characteristics were fairly steady over time (Fig. 6).

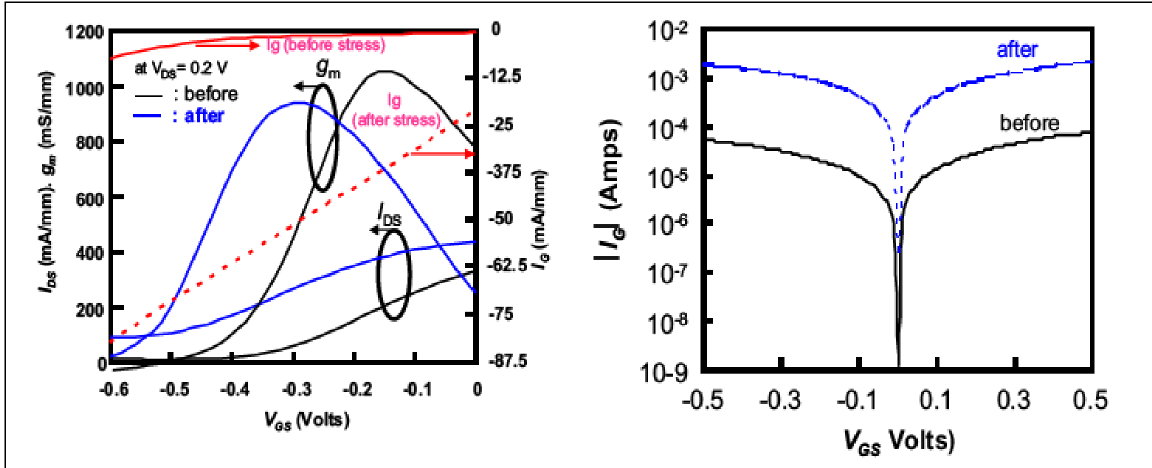

Fig. 5. Shift in transconductance, gate current and drain current for a 2 × 20 × 0.1 μm device after 200 hours of stressing at *Vds* = 200 mV and 150 mA/mm bias current. Gate diode characteristics before and after stress are shown separately for both forward and reverse bias [19].

Scanning-transmission electron microscopy (STEM) was used to examine the physical evidence of a degraded InAs - AlSb HEMT. A high resolution energy-dispersive analysis with X-ray (EDAX) was performed at 2 locations, location 1 under the gate, and location 2 in the recess region. The recess region showed a much higher oxygen signal than location 1. Both the oxygen and carbon signals were roughly of the same order of magnitude as those of aluminium or antimony – indicating very high concentrations for both contaminants. Strong evidence of oxidation was also seen at the $Al_{0.7}Ga_{0.3}Sb$ mesa floor, which changed color in the STEM image (Fig. 7). After the stressing, the EDAX images also showed some evidence of lateral diffusion of the metal from the source/drain Ohmic contacts into the access regions (Fig. 7). However, the extent of diffusion of Ohmic metal into the access regions was only ~ 200 - 300 nm. While this can be responsible for some reduction in access resistance, it does not explain a clear shift in threshold voltage, as evidenced by Fig. 8.

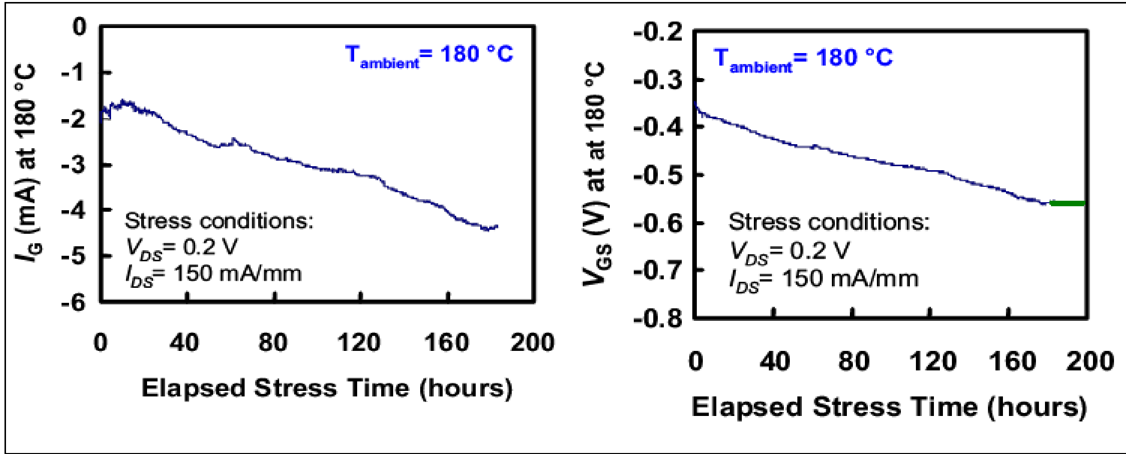

Fig. 6. I_g and V_{gs} evolution of a 0.1 μm InAs - AlSb HEMT subjected to 180 °C life-testing [19].

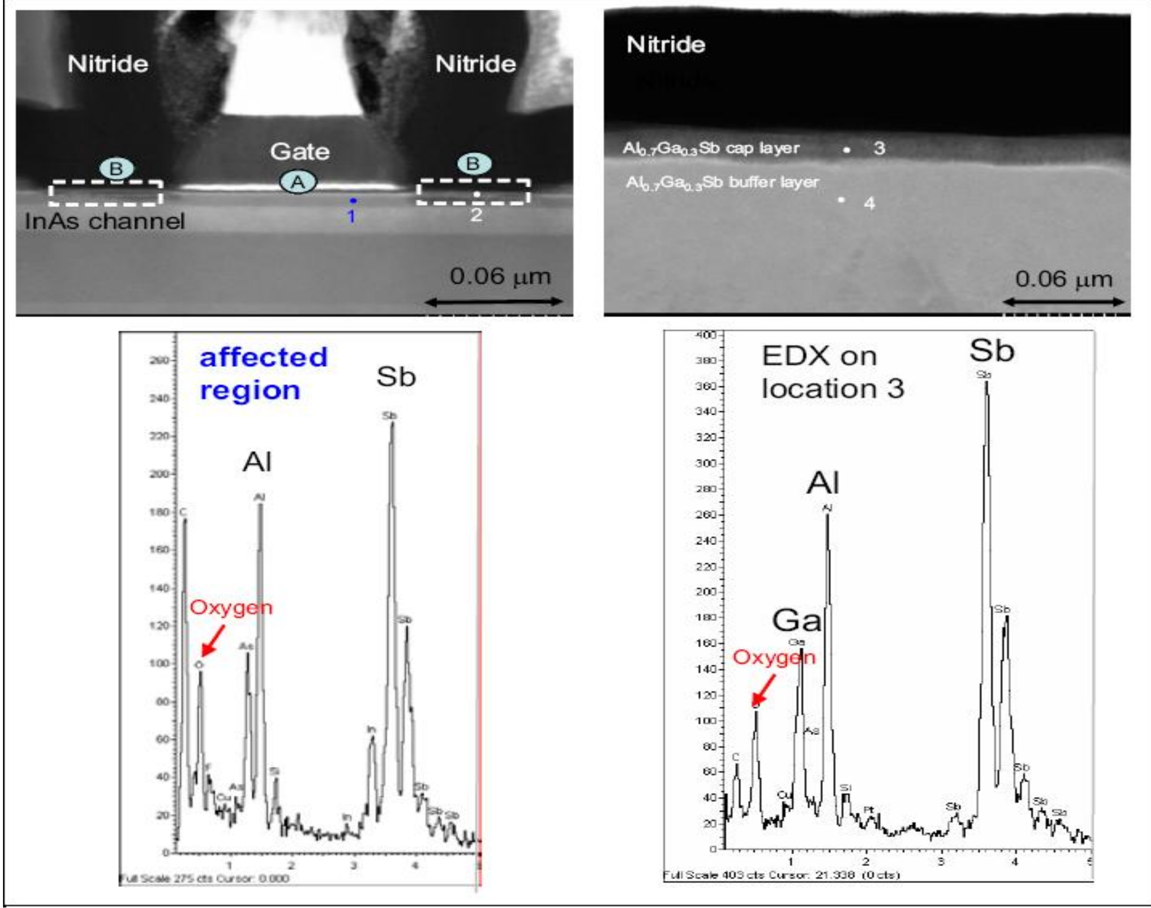

Fig. 7. (Right) The gate and gate-recess STEM micrograph of a degraded 0.1 μm InAs - AlSb HEMT, showing the gate-recess surfaces affected by oxidation. The EDAX spectrum on location 2 shows presence of oxygen on top AlSb layer. (Left) STEM image of the degraded HEMT on the Al0.7Ga0.3Sb-mesa-floor surface. The EDAX spectrum on location 3 shows oxygen presence in upper portion of the Al0.7Ga0.3Sb layer [19].

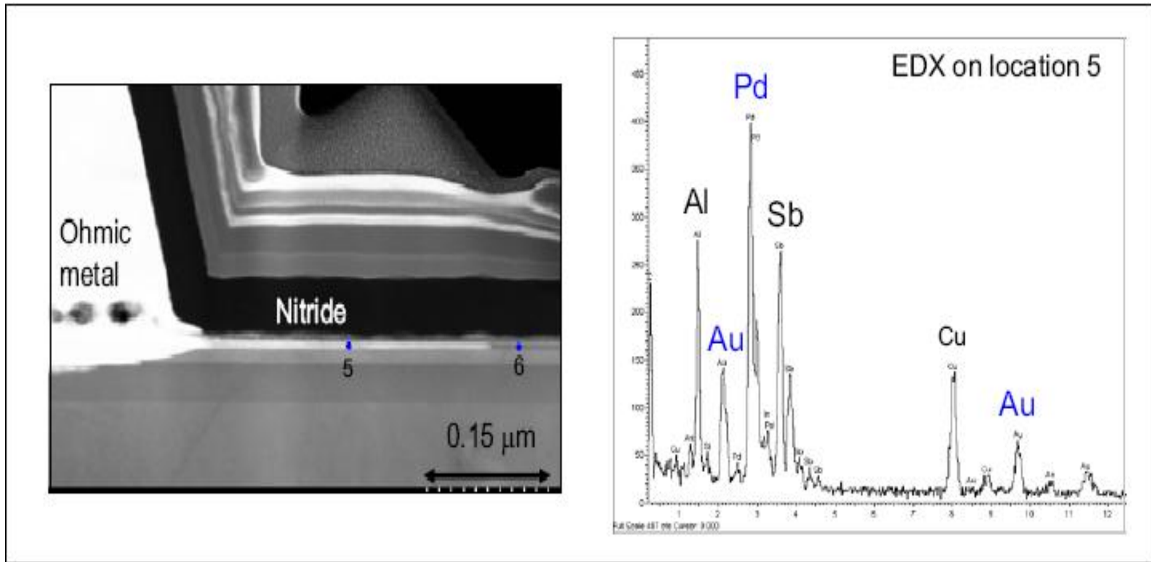

Figure 8. STEM micrograph of a degraded InAs - AlSb HEMT, showing physical evidence of Ohmic-metal lateral diffusion. The EDAX spectrum from location 5 exhibits evidence of Pd and Au Ohmic-lateral diffusion along the upper AlSb material [19].

While these results provide information about the degradation trends and some indications of the physical nature of degradation, no electrical characterization of the physically degraded entities was performed. Hence, no explicit connection was made between the physical degradation signatures and the electrical effects. Also, the combined natures of the electrical and thermal stresses made it difficult to understand the contribution of each of these to the degradation. In fact, it is not obvious from the results that the physical degradation signatures were directly or indirectly related to the shifts in device characteristics.

CHAPTER IV

DEVICE CHARACTERISTICS AND TYPES

4.1. Effect of Source-Drain Spacing and Gate Length Scaling on DC and RF Transconductance

The results presented in this thesis were obtained from stress experiments performed on devices fabricated by Teledyne Scientific. The devices employ a composite top barrier using AlSb and $In_{0.5}Al_{0.5}As$ with a total thickness of 14 nm, as described earlier. Earlier studies analyzed the DC and RF performance of devices with different source-drain spacings [21]. However, the effects of the source–drain spacing were not decoupled from the effects of gate scaling, and the S-D spacing to gate length ratio increased with scaling [21-22]. In this study, based on a combination of simulation results and device measurements, we demonstrate that large source-gate access region spacing leads to reduced peak transconductance in some InAs HEMTs.

4.2. Band Structure and Hole Removal

The kink effect in InAs-channel HEMTs has been demonstrated to be a consequence of slow hole removal from the AlSb buffer layer [9]. Avalanche-generated holes are readily transported to the adjoining AlSb layers, which have a slightly higher valence band energy. Such holes are partially removed through the gate. A large fraction of the holes

move slowly through the low mobility AlSb buffer [23]. The positive space charge due to the holes accumulated close to the channel leads to an increase in the electron density in the channel.

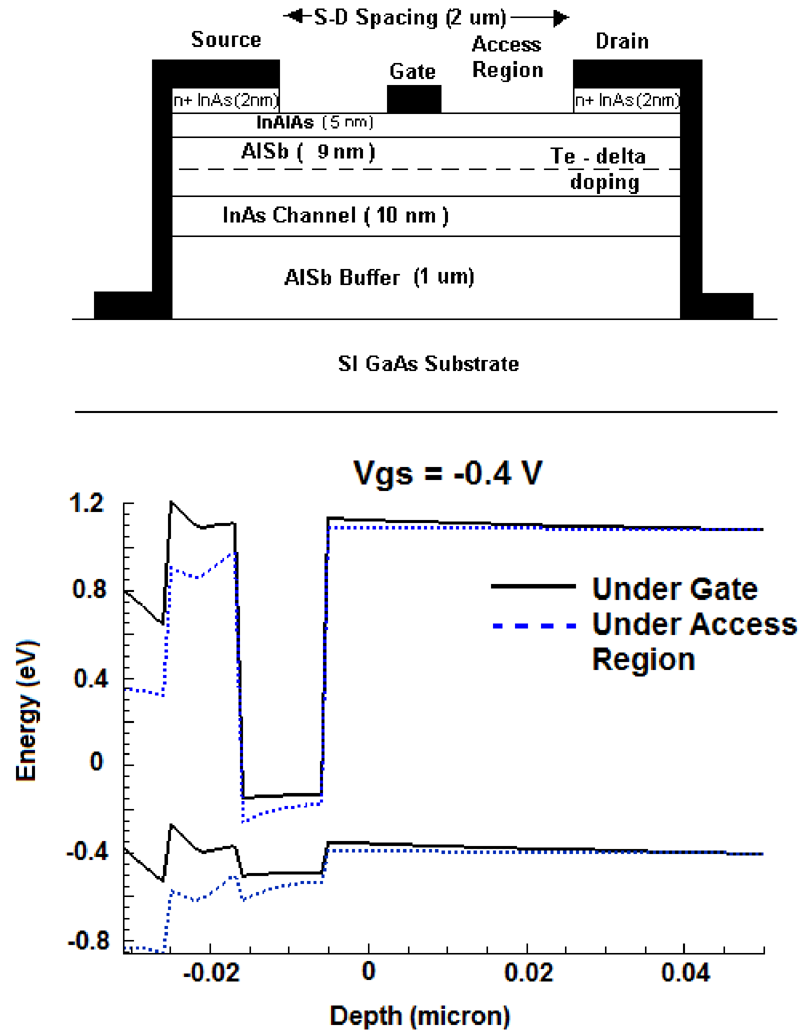

Figure 9. Vertical cross-section of InAs - AlSb HEMTs. b) Vertical band diagram underneath gate (solid line) and in the access regions (dashed line). The absence of the Schottky gate eliminates the band upslope of the top AlSb layer in the access regions.

The vertical band profile in Fig. 9 is plotted from a simulation of the HEMT structure using the Dessis tool suite [24]. For the standard Au/TiW or Cr/Au gate metallization, the band bending in the top AlSb layer is fairly large, which creates a favorable situation for

removal of holes. This is absent in the region between the source and gate edges (sometimes referred to as the access region), which makes it more favorable for holes to accumulate in the AlSb buffer below the channel, and increases the electron density in the channel. At high negative gate voltages, the difference between hole removal efficiencies under the gate and access regions increases. Thus, a device with long access regions and short gates can be expected to exhibit larger back channel hole transport. Carefully selecting the gate metal workfunction might eliminate the band upslope in the AlSb, but that has the disadvantage of placing the Fermi level in the InAlAs cap too high in the conduction band, so that all the donors from the Te delta doping end up in the cap, creating very high gate leakage and reducing the 2DEG density.

4.3. DC Transconductance and V_{th} Comparison for Different Source-Drain Spacing

To verify the effects of source-drain spacing on hole transport, we examine the DC transconductance and output conductance of devices with four different gate lengths and the same source-drain spacing as well as devices with the same gate lengths and two different source-drain spacings.

The g_m characteristics (Fig. 10) clearly demonstrate a more negative threshold voltage and lower peak transconductance in the devices with shorter gate lengths. The depletion of the channel due to gate bias is compensated by increasing avalanche rates, coupled with a slower rate of hole removal compared to devices with longer gate lengths. The importance of the gate length to access region ratio is demonstrated through a comparison

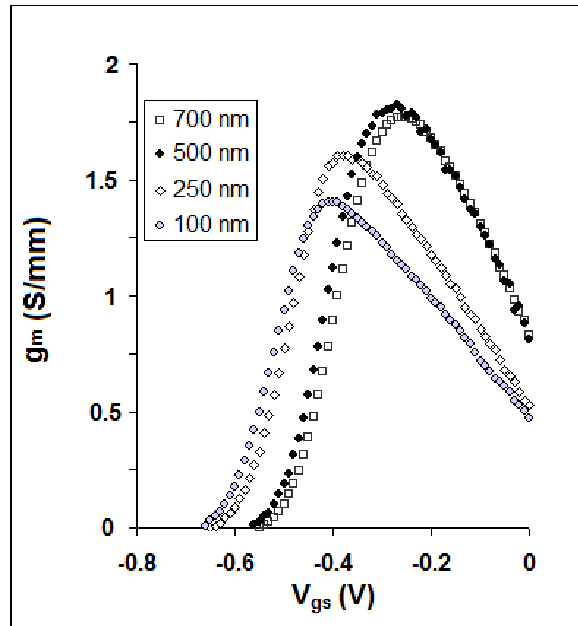

Figure 10. DC transconductance for 4 HEMTs with gate lengths of 100 nm, 250 nm, 500 nm and 700 nm and S/D spacing = 2 μm. The short gate length devices show significantly reduced peak g_m and more negative V_{th}.

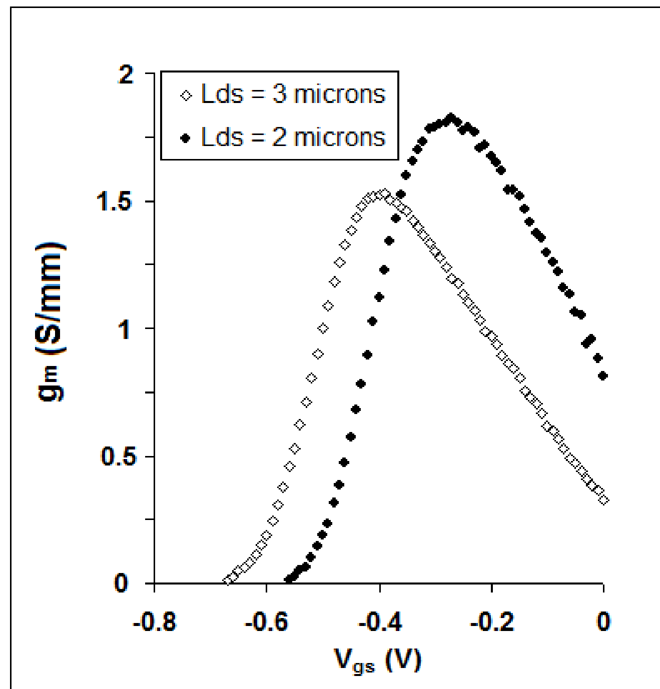

Figure 11. DC transconductance vs. gate voltage for HEMTs with two different access lengths (gate length = 250 nm). There is a significantly reduced peak g_m and higher negative V_{th} for the device with higher L_{ds} =3 μm.

between devices with the same gate length (250 nm) and different access spacings (L_{ds}) in Fig. 11. A similar reduction in peak g_m and higher negative V_{th} is seen in the device with higher access spacing.

Poor hole removal results in an increase in output conductance at high V_{ds}, especially at gate voltages that are moderately negative but above V_{th}. For V_{gs} = -0.4 V, the effect is seen strongly at drain voltages greater than V_g - V_{th} in shorter gate length devices (Fig. 12). With an increase of gate length, g_o decreases even for low V_{ds} (since the access region is always more conductive than the channel at V_{gs} = -0.4 V). The increase in g_o for $V_{ds} > V_g - V_{th}$ also reduces with increasing gate length.

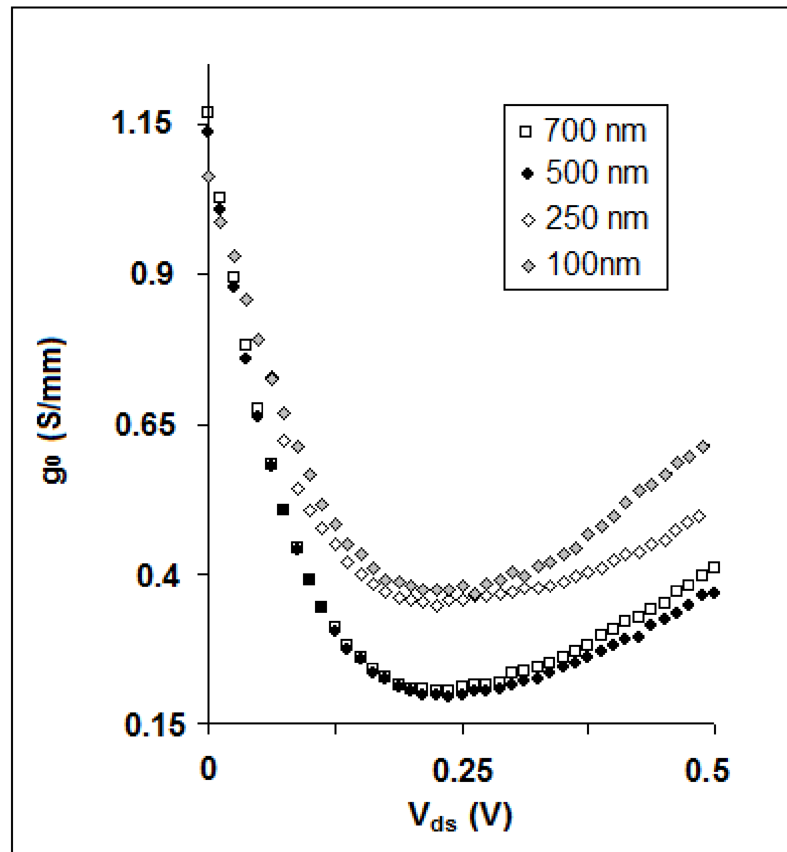

Figure 12. DC output conductance for 4 HEMTs with gate lengths 100 nm, 250 nm, 500 nm and 700 nm and S/D spacing = 2 µm. The short gate length devices show significantly increased g_o for drain voltages greater than V_g - V_{th}.

Since increasing the gate length amounts to reducing the gate to drain spacing for a constant L_{ds}, the avalanche rate becomes high enough after a certain gate length to compensate for the efficient hole removal, and the 700 nm gate length device exhibits a slightly higher increase in g_o for $V_{ds} > V_g - V_{th}$ than the 500 nm gate length device.

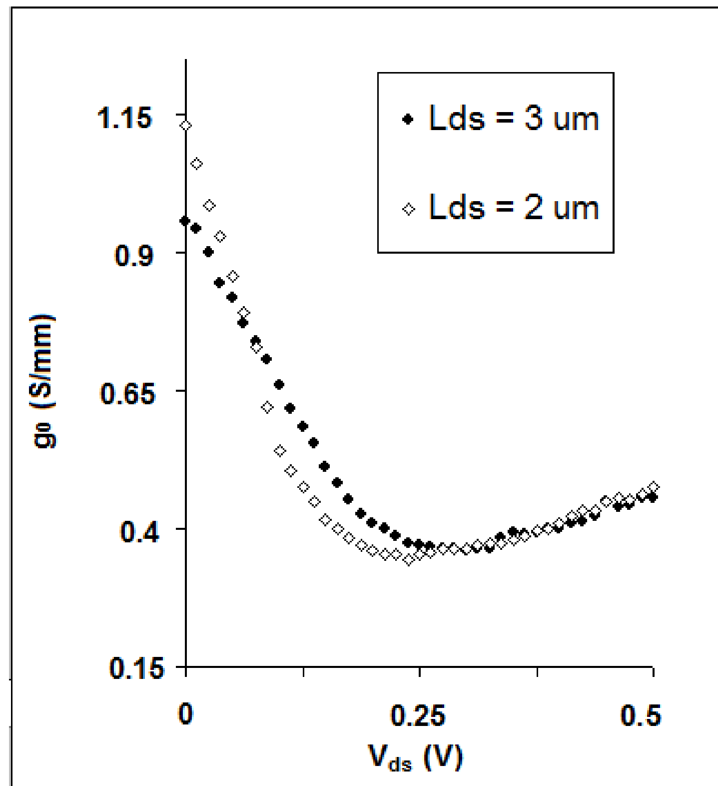

Figure 13. DC output conductance for HEMTs with gate length of 250 nm and L_{ds} = 2 μm and 3 μm.

For devices with access regions of 3 μm, the access resistance leads to a lower starting g_o than in the 2 μm devices (Fig. 13). The initial rate of fall in g_o is slower due to a greater source to drain edge spacing. The slow rate of hole removal compensates for lower avalanche rates at drain voltages greater than $V_g - V_{th}$.

Fig. 14 shows g_o at three different drain voltages for 16 devices of different gate lengths. In spite of variations in characteristics from device to device, the trend of increasing g_o at high V_{ds} is consistent in short gate length devices.

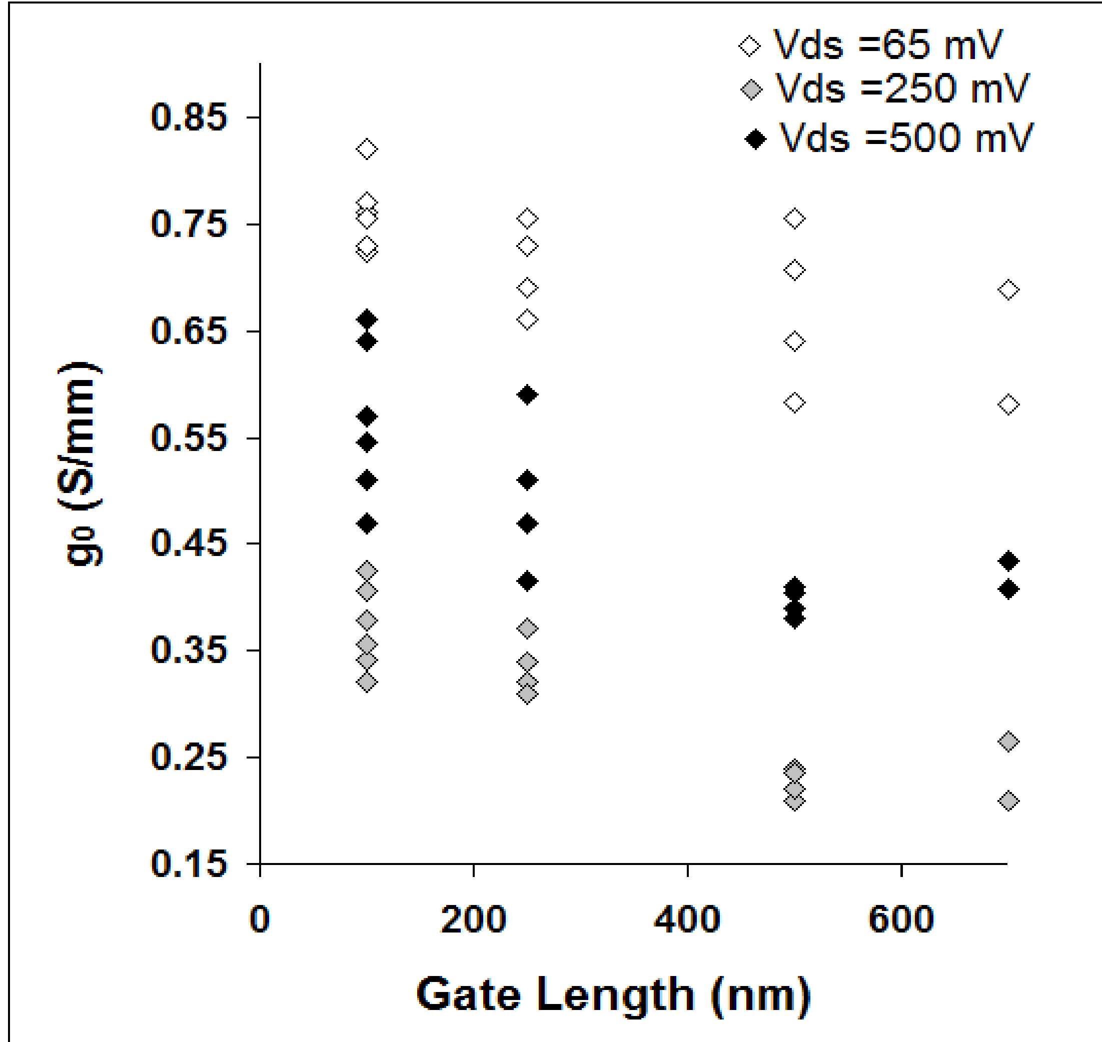

Figure 14. a) g_o at three different drain voltages for 16 devices of different gate lengths. The g_o increase at high V_{ds} is seen quite consistently at low gate lengths. At low V_{ds} , small gate length devices have much smaller variations in g_o.

A. Region of Maximum Transconductance Compression

The maximum reduction in g_m occurs under operating conditions when the 2DEG density and channel carrier temperature are simultaneously high. Fig. 15 shows the computed

electron density, carrier temperature and avalanche generation rate along the channel for an InAs - AlSb HEMT (turn off voltage ~ -0.7 V), obtained from a hydrodynamic simulation. The exponential contribution of carrier temperature to avalanche rate at moderately negative gate voltages (but not enough to deplete the channel) outweighs the reduction in channel electron density.

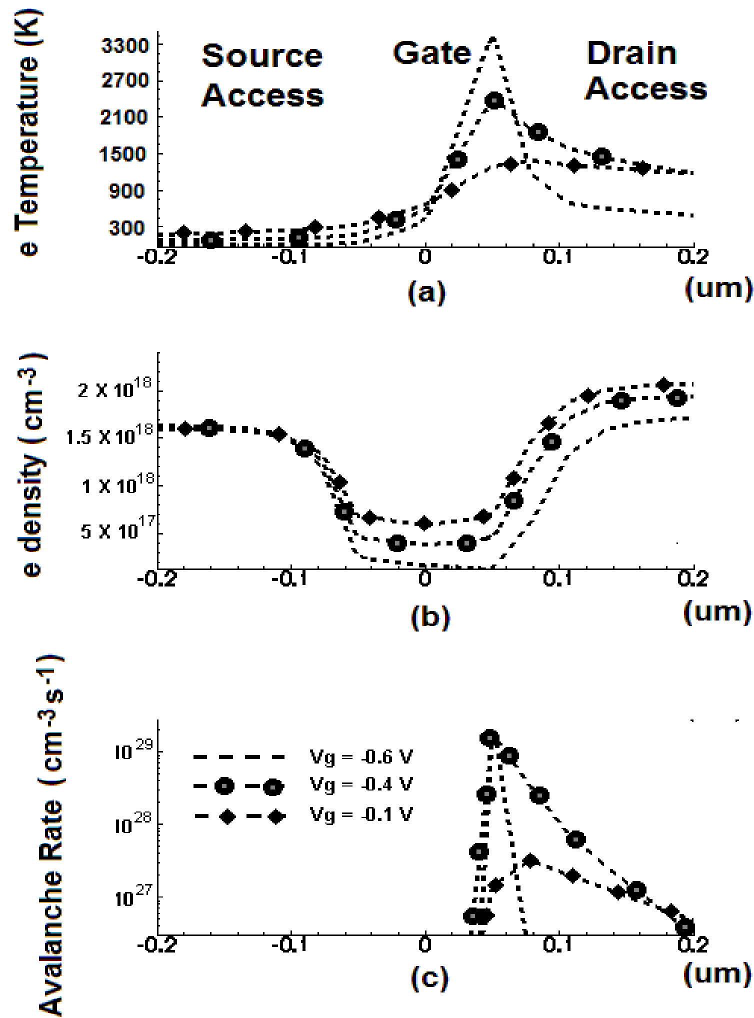

Figure 15. Simulated electron temperature, b) electron density and c) avalanche rates along the channel for V_{gs} = -0.1 V, -0.4 V and -0.6 V. The highest avalanche rate is observed for -0.4 V (simultaneously high e-density and temperature). The gate is between -0.05 and 0.05 micron.

It should be noted here that the effects of source-drain spacing are not the same for all substrate configurations. For example, a p-GaSb nucleation layer [2] increases the tendency of carriers to take the back-channel route by increasing the upslope of the valence band, making the hole-induced feedback a very significant fraction of the total drain current.

4.4. Avalanche History in RF Transconductance

High source-drain spacing increases R_{ds} and the kink effect. It also leads to a smaller reduction of high frequency g_m from the DC value, due to lower C_{gd} and C_{gs}. Hydrodynamic simulations of two HEMTs, having gate lengths of 100 nm and S-D spacings of 2 and 4 μm, show these trends. However, an additional feature is seen in the RF g_m for operation ~ 10 GHz with moderately low to high amplitude signals.

Fig. 16a gives the DC g_m for the two devices. The longer device, with more back channel hole transport, leads to reduced values of g_m in the moderate to high avalanche regime. When a 25 GHz AC signal with a peak to peak amplitude greater than 1 mV is applied, g_m (defined as $I_{d,ac} / V_{g,ac}$) is higher than the DC value. When a device switches from -190 to -210 mV, it transitions from a low avalanche to a high avalanche rate condition. There is a time delay associated with the energy relaxation of the channel carriers [25] and the transport of generated holes to the AlSb layer at the back channel. Thus, when the gate is pulsed by a certain voltage (say, 25 mV) within a few picoseconds, the channel and the adjoining areas are still in the avalanche environment of a gate bias that existed a few ps earlier (or, a smaller negative voltage – corresponding to a smaller avalanche rate).

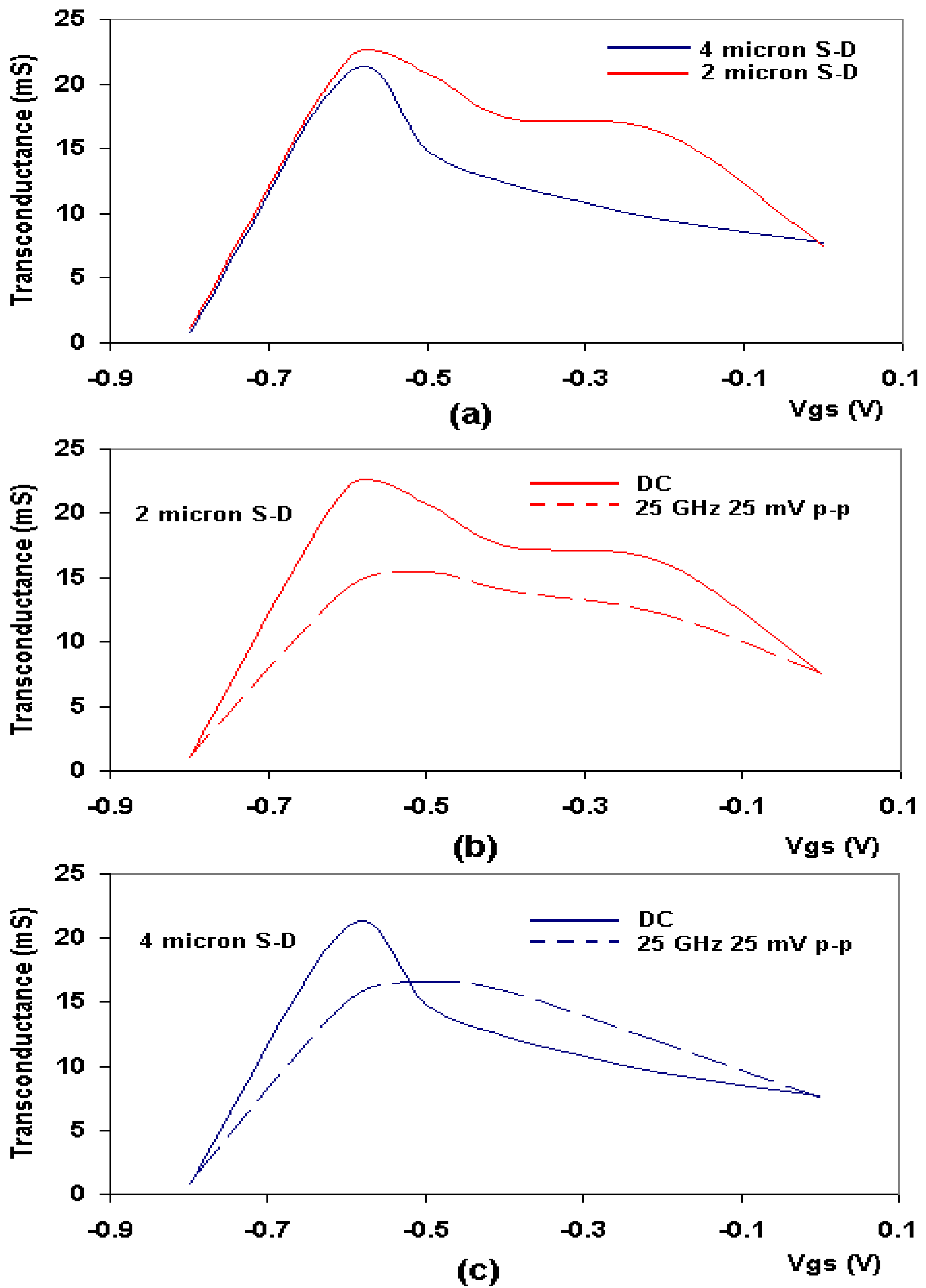

Figure 16. Simulated a) DC transconductance for devices with 100 nm gate length and S/D spacings 2 and 4 μm, with ac $g_m = I_{d,ac} / V_{g,ac}$, for a 25 GHz, 25 mV p-p signal, for the b) 2 μm and c) 4 μm S-D device.

Consequently, it is easier for the device to turn off than in steady state, which implies a higher g_m. Similarly, as the device emerges from the high to low avalanche regime (around ~ 0.4 V, as shown in sec. 4.3*A*), turning off the device is more difficult than in steady state, leading to a reduction in g_m. The flattening of the RF g_m curves for both devices around the peak is partly a consequence of this, in addition the effects of C_{gd} and C_{gs}. A consequence of the shift of the V_{gs}, corresponding to the highest avalanche condition during high frequency switching, is a slight shift of the g_m peak for both devices.

The increase in g_m above the DC value for moderately high amplitude, high frequency signals is expected to happen only in devices with sufficiently small parasitic capacitances and simultaneously high back channel hole transport. In the 2 μm device, with sufficiently high C_{gd} and C_{gs}, this effect is not observed.

4.5. Characteristics of Devices Used in Stress Experiments

Many of the device characteristics, especially the behavior of the gate current over the entire range of allowed biases, do not seem to follow naturally from the device structure and the bulk electrical characteristics of its constituent layers. There was also a high degree of variation in the devices tested for electrical stress. Most devices had threshold voltages equal to or less negative than -0.7 V. For devices which pinched off at more negative gate voltages than that, or in some extreme cases did not pinch off at all with the specified usable range of gate voltages (-0.8 V), the gate leakage current was the smallest

of all devices (Fig. 17). Most devices pinched off easily around -0.6 V, but also had a high gate leakage current.

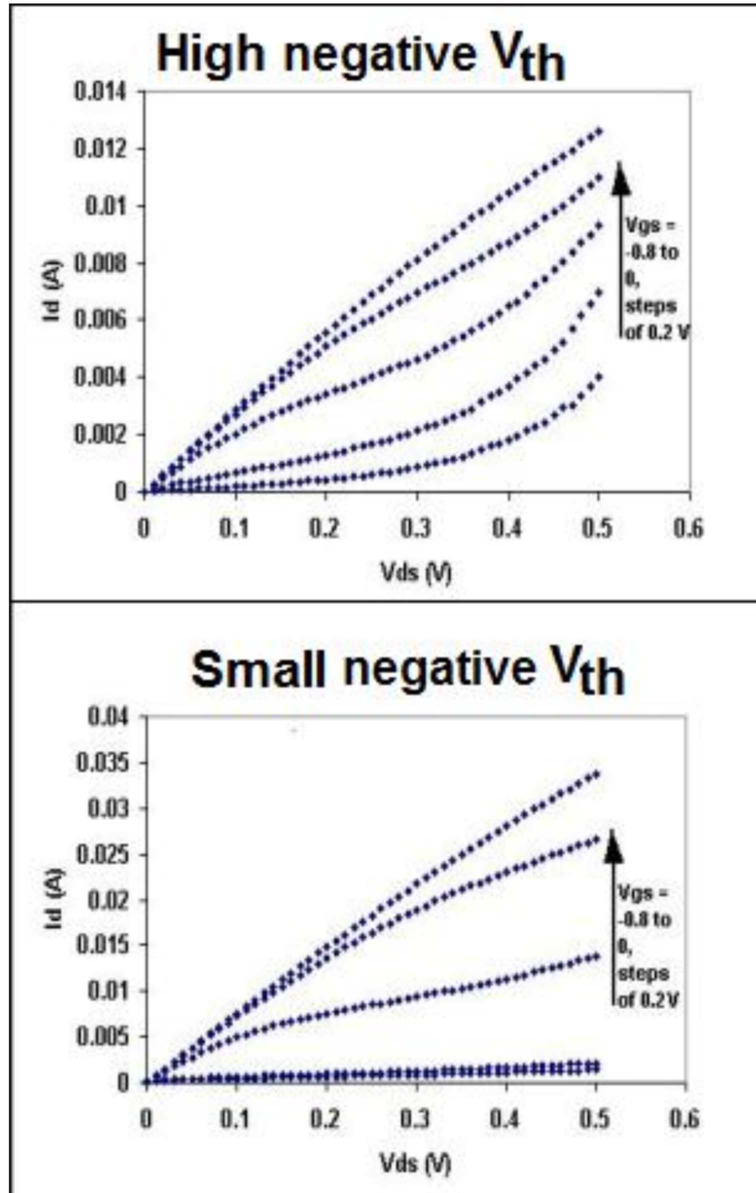

Fig. 17. High and low negative threshold voltage devices – both with 100 nm gate length.

This is slightly unusual, as the vertical flow of carriers (presumably holes) to the gate does not seem to sufficiently hinder a strong enough vertical field from penetrating into

the channel region. The devices with simultaneously low threshold voltage and gate current had a starting threshold voltage of about -0.6 V and a gate current at the highest negative gate voltage (V_{gs} = -0.8 V) and V_{ds} = 0 that was less than 0.1% of the drain current at V_{gs} = 0 and V_{ds} = 0.5 V. The range of leakage currents for the tested devices was high, with the I_d (V_{gs} = -0.8 V, V_{ds} = 0) / I_d (V_{gs} = 0, V_{ds} = 0.5 V) ratio being as low as 0.00005 in some devices to as high as 0.1 in some devices. As most of the good devices pinched off at ~ -0.7 V, we took the DC threshold voltage as an indication of the strength of the vertical field in the channel at the chosen bias condition.

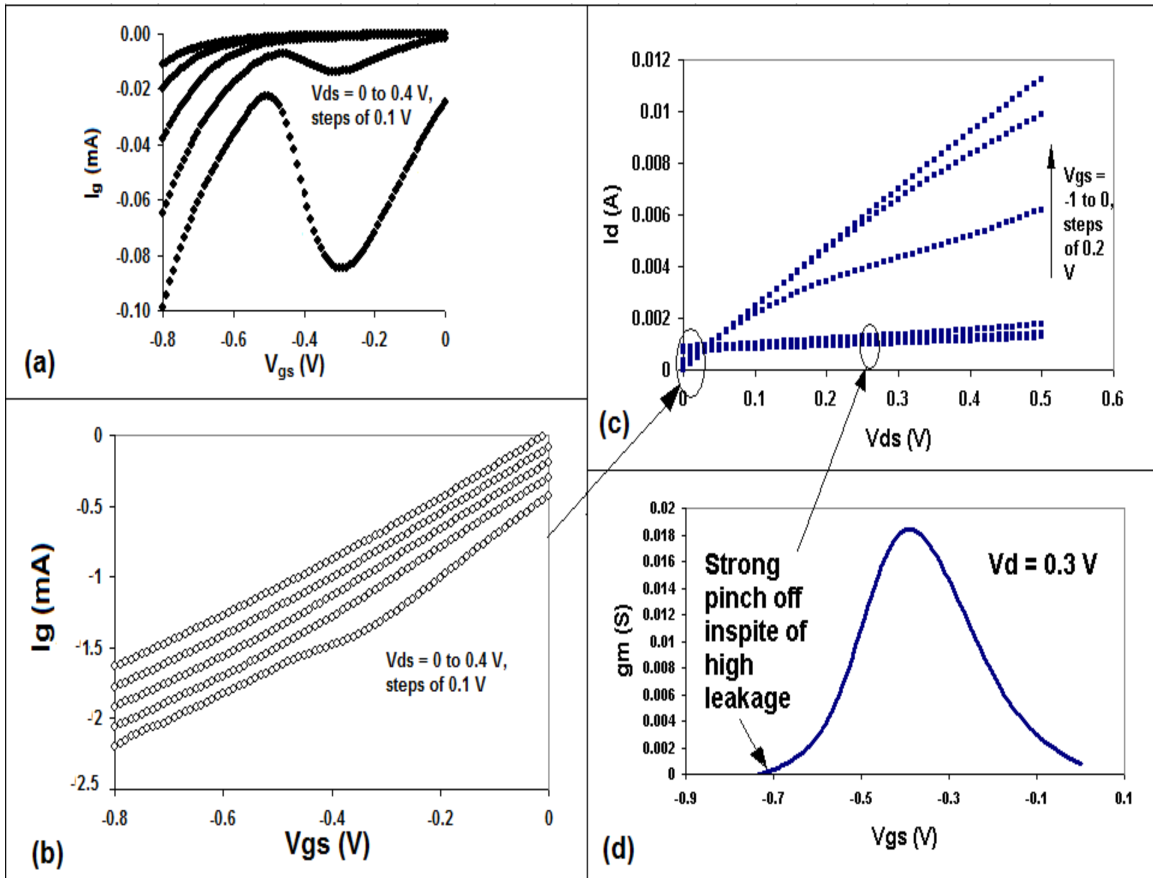

Figure 18. I_g-V_{gs} plots for 2 devices with 100 nm gate with a) low and b) high gate leakage. c) I_d-V_{ds} and d) g_m plots of the device with high gate leakage. Even very high gate leakage does not prevent good pinch off around -0.6 V.

Most devices had threshold voltages more negative than -0.7 V. The gate leakage current was lower in devices that had more negative threshold voltages. Many devices pinched off around -0.6 V, but also had high gate leakage current (Fig. 18). The devices with high gate leakage were clearly distinguishable from the incomplete pinch-off devices commonly observed in HEMTs with low levels of unintentional doping in the buffer and wide channels [26].

While incomplete pinch off devices exhibit source-to-drain current at high V_{ds} near or below the threshold voltage, the drain current in the devices with high gate leakage flows from gate to drain at similar gate biases, instead of the source. Thus, when the gate is biased at threshold and the drain bias is zero, incomplete pinch-off devices have negligible drain current, while devices with high gate leakage have appreciable drain current. The tested devices had threshold voltages ranging from (-0.6 V to -1.1 V) and peak gate leakage currents ranging from 1.5 to 50 mA/mm. None of the devices showed incomplete pinch-off. This is reasonable, since the highly scaled channel significantly reduces chances of incomplete pinch-off.

CHAPTER V

ELECTRICAL STRESS AND DEGRADATION

5.1. Bias Corresponding to Maximum Hot Carrier Condition

Fifty devices were tested on wafer at room temperature. The devices showed no signs of degradation when biased at the maximum current condition (V_{gs} = 0, V_{ds} = 0.5 V) or pinch-off (V_{gs} = -0.8 V, V_{ds} = 0.5 V). At negative gate voltages slightly more positive than the threshold voltage and positive drain voltage (V_g ~ -0.5 V, V_{ds} = 0.5 V), there were significant changes in the *I-V* characteristics.

In InAs - AlSb HEMTs, most hot carriers are derived from impact ionization in the channel. The narrow band gap of InAs (0.36 eV) results in a very low threshold for impact ionization in the channel. This is clearly shown in Fig. 18 by the gate current profile at high V_{ds}. As the gate bias moves from 0 to -0.5 V, (marked as Region 1 in Fig. 19) impact ionization increases, due to higher longitudinal fields in the channel. The holes discharged into the AlSb layer (whose valence band is 110 meV higher than that of InAs) form the largest component of the gate current. At more negative gate voltages (Region 2 in Fig. 19) there are very few electrons in the channel. As a result, the impact ionization rate and the gate current quickly drop, in spite of the increase in the field. At much more negative gate voltages (Region 3 in Fig. 19), $|I_g|$ increases again due to fields extending deeper into the buffer or the carrier rich access regions. However, even at these high biases, the hole energies are relatively small compared to the energies of impact

ionization-generated holes in the channel. This is because of the low hole mobilities of InAs, AlSb or $In_{0.5}Al_{0.5}As$, compared to electron mobility in InAs. (A hole generated by impact ionization in the InAs channel has energy that is a significant fraction of the energy of the electron in the InAs channel – before it gains further energy from the electric fields or band discontinuities).

Since the devices are most degradation prone near the impact ionization peak (as opposed to high drain or gate bias), this is a strong indication that the observed degradation is driven by hot carriers.

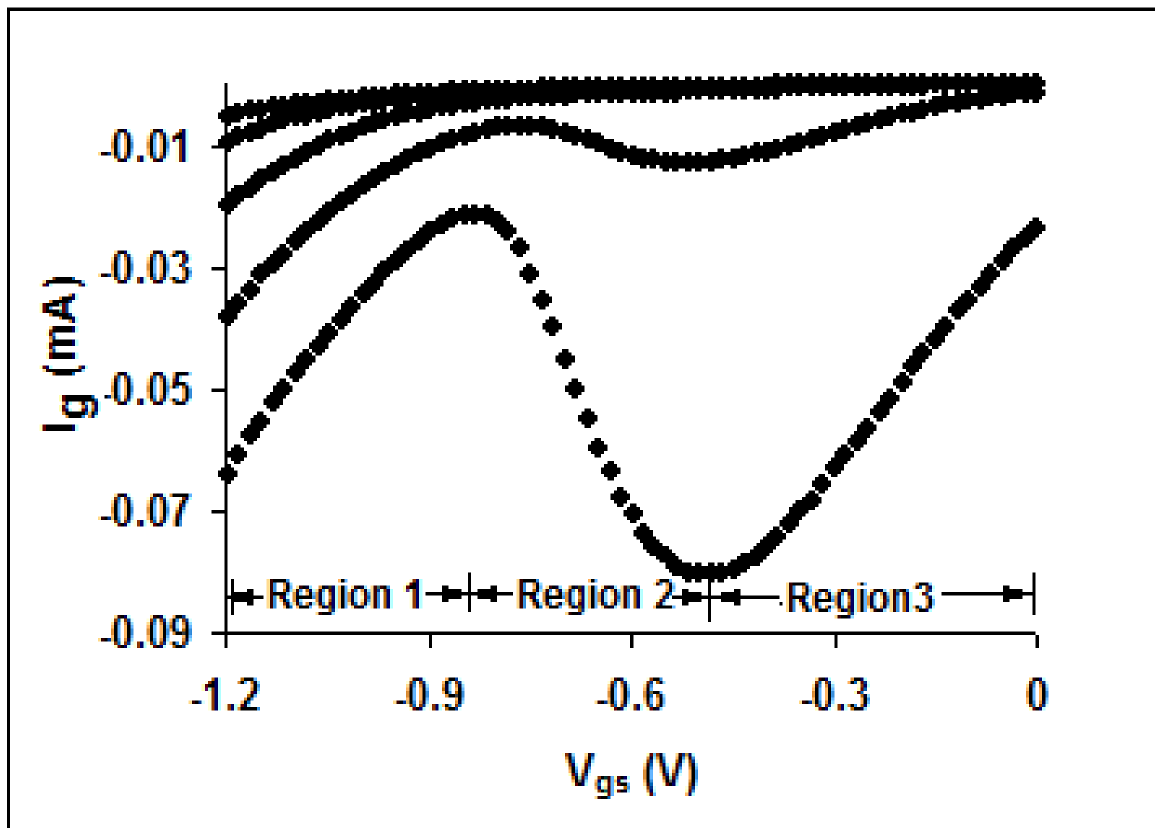

Figure 19. I_g-V_g characteristics of a 2 × 20 μm HEMT, for V_{ds} = 0 to 0.4 V, in steps of 0.1 V. Holes from avalanche in the channel dominate the gate current at V_{ds} = 0.4 V. the gate current peaks at V_{gs} = -0.5 V and then drops. The feature is absent at lower V_{ds} like 0.2 V.

5.2. Degradation – Threshold Voltage and Transconductance Peak Shift

More than 60% (34 devices) of these devices showed no visible signs of degradation under the stress conditions considered here. The other devices (16 devices) showed shifts of the threshold voltage and transconductance peak towards more negative gate voltage (Figs. 20 and 21). This trend has been observed earlier for InAs - AlSb HEMTs under thermal stress [19]. When the stressed devices were left at room temperature with no bias, they slowly recovered almost completely back to their initial characteristics. The evolution of gate current was less consistent, increasing in some cases and decreasing in others.

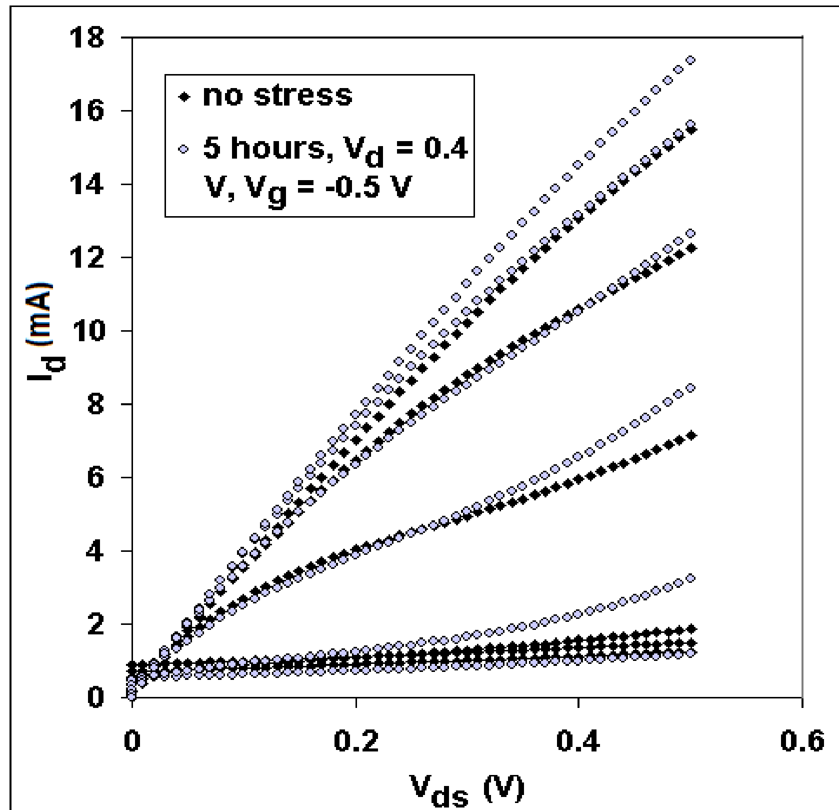

Figure 20. Degradation in I_d and shifts in threshold voltage under 5 hours of electrical stress at V_{gs} = -0.5 V, V_{ds} = 0.4 V. The I_d-V_{ds} plots are for a 2 × 20 mm HEMT with 100 nm gate, with swept values of V_{gs} = 0 to -1 V in steps of -0.2 V.

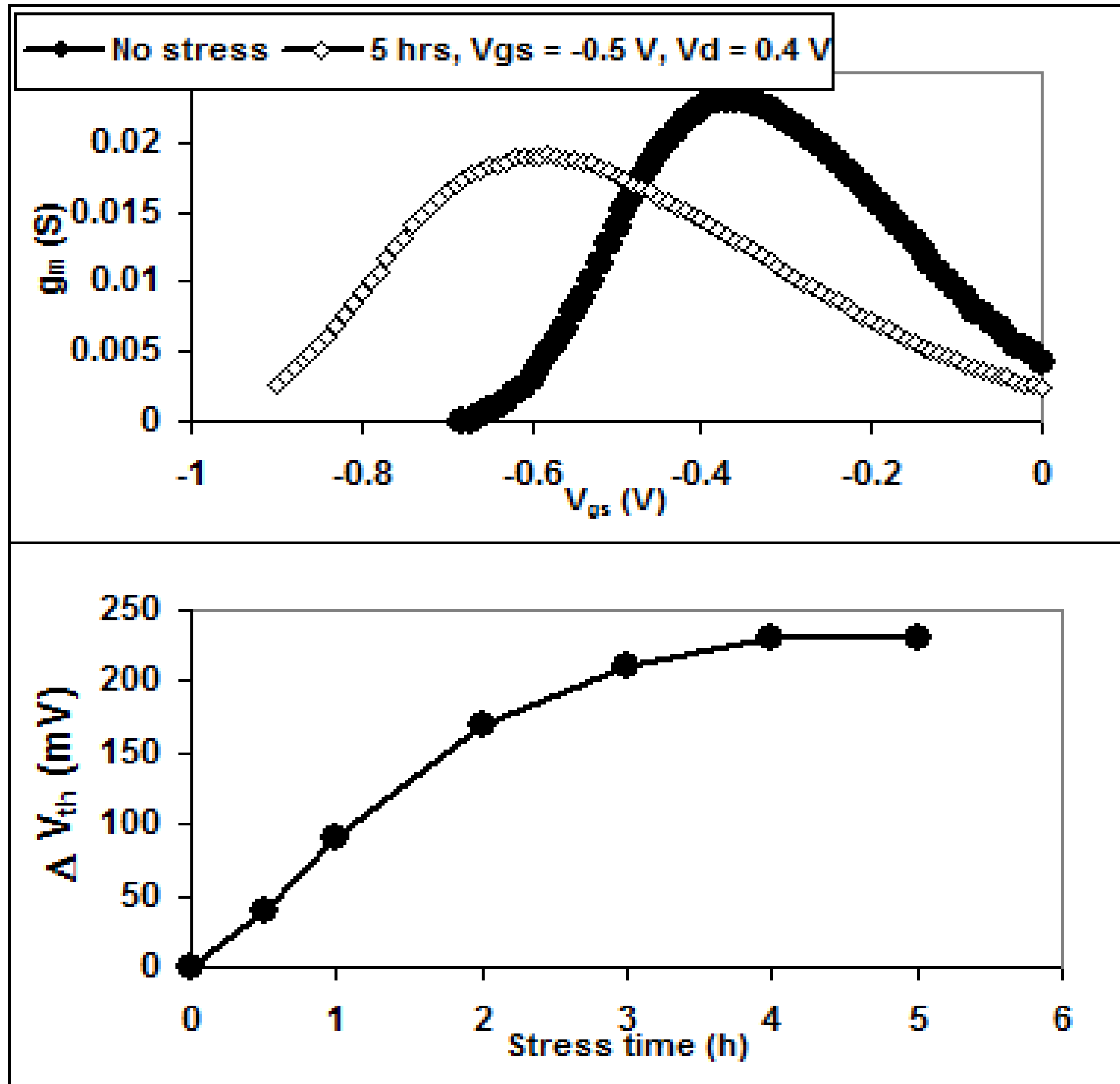

Figure 21. (Top) Degradation in peak g_m and shift in threshold voltage (V_{ds} = 0.4 V) under 5 hours of stress at V_{gs} = -0.5 V, V_{ds} = 0.4 V, and g_m plots of a 2 × 20 μm wide HEMT with 100 nm gate. (Bottom) Shift in V_{th} as a function of stress time in the same device.

Since the gate current is relatively high in these devices (~ -10 mA/mm) at high negative gate voltages, it contributes to a significant increase in the drain current by lowering the source-to-gate potential barrier. This resulted in the post stress drive currents having no distinct trend relative to the pre-stress drive currents. The change of threshold voltage in time followed an approximately exponential trend.

The tested devices had gate lengths of 100, 250, 500 and 700 nm. The 100 and 700 nm devices had source to drain spacing of 2 μm. 250 and 500 nm devices had source to drain spacing of 2, 2.5 and 3.5 μm. Devices with gate lengths greater than 250 nm and source drain spacing greater than 2 μm showed no degradation.

Because of the large variation in threshold voltage between devices, it was not possible to determine the relationship of the field in the channel and the shift in the threshold voltage or g_m peak without accounting for the threshold voltage variation, by simply changing the gate voltage. One way to do this is to study the degradation as a function of V_g - V_{th}. Since the stress introduces new defects (including ones that may not be electrically active at the given moment – but act as precursors for future degradation), stressing one device using a sequence of different gate voltages was also not an option to understand the dependence of the field in the channel to the shift in the threshold voltage or g_m peak.

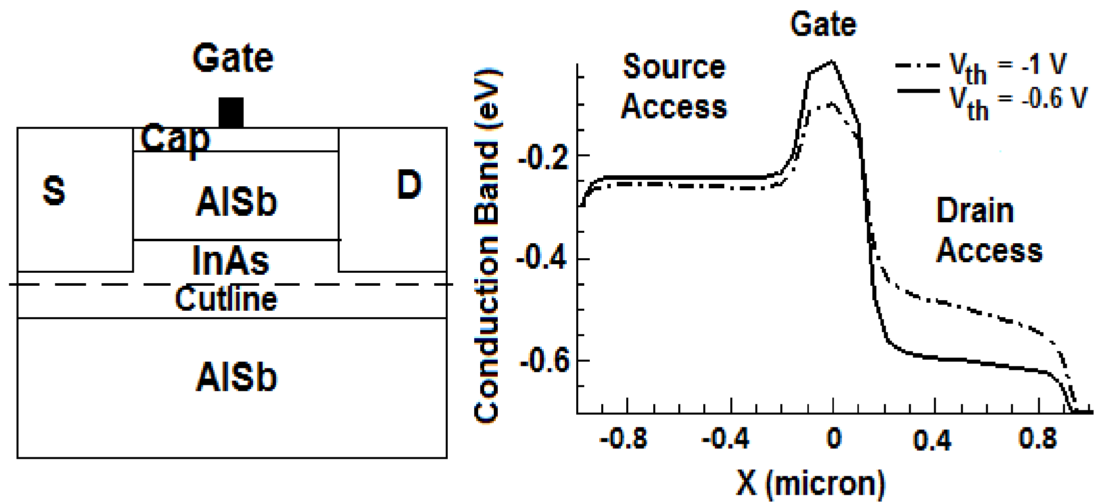

Figure 22. Simulated electrostatic potential along a cutline in the InAs channel for 2 devices with V_{th} = -0.6 V and -1 V for V_{gs} = -0.5 V and V_{ds} = 0.4 V.

Fig 22 demonstrates the relationship between the field in the channel in the direction of I_{ds} and (V_g - V_{th}). It shows the simulated electrostatic potential profile along the InAs channel under the gate, from source edge to drain edge, for two devices with V_{th} = -0.6 V and -1 V. As expected, for the same bias conditions (V_g = -0.5 V and V_{ds} = 0.4 V in this case), the device with a more negative V_{th} (-1 V) has a lower potential barrier at the gate-drain access region edge. Thus, for the same bias conditions, the device with greater V_g - V_{th} has a lower electric field in the channel. Making use of this correlation between V_{th} and field in the channel at a given gate bias, the stressing gate voltage was kept the same, and V_{th} was taken as a measure of the electric field in the channel. Figure 23 shows that the g_m-peak shift is related to the V_{gs} - V_{th} (pre-stress).

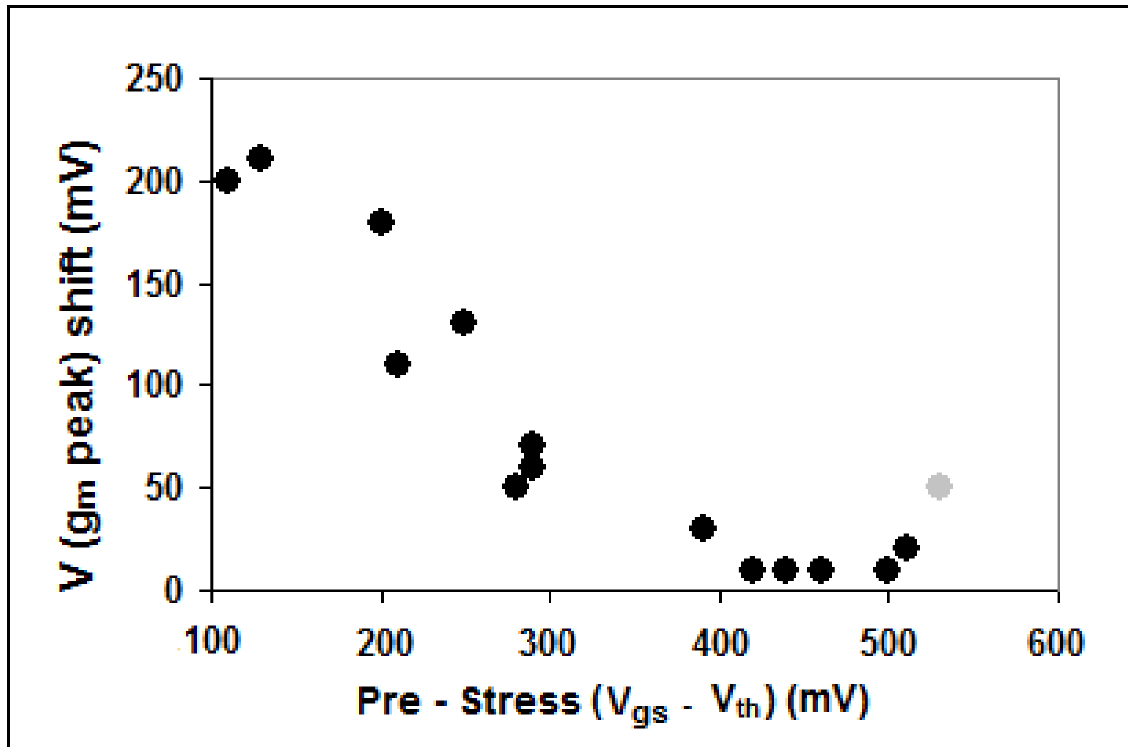

Figure 23. g_m (V_{ds} = 0.4 V) peak shift in sixteen 2 × 20 μm HEMTs as a function of pre-stress V_{th}. There is increased degradation at high vertical fields in the channel. The data point in grey is for a device with high kink effect – shown in Fig. 24.

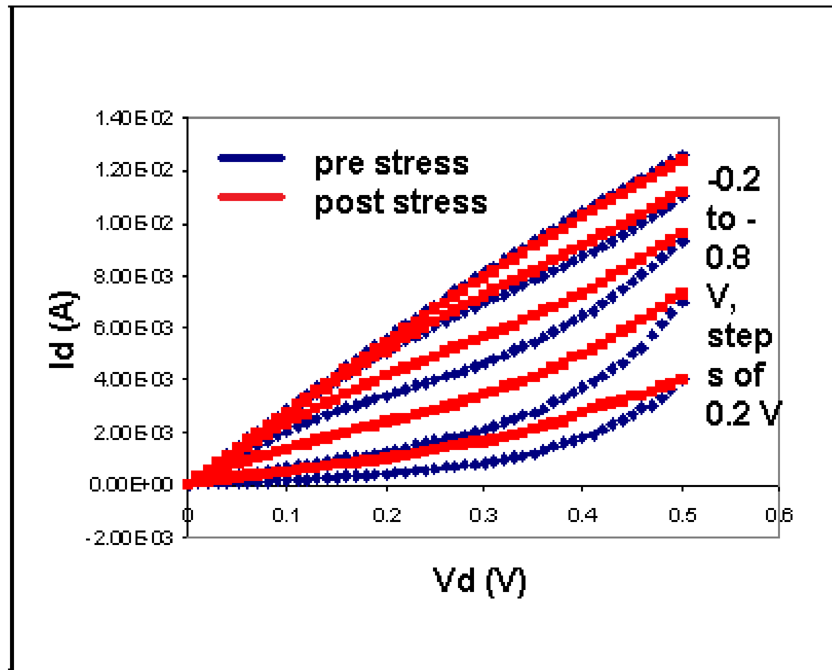

Figure 24. Pre and post-stress I_d-V_{ds} plots for device corresponding to the grey data point in Fig. 23. The pre stress device suffers from high output conductance or kink effect at high V_{ds}.

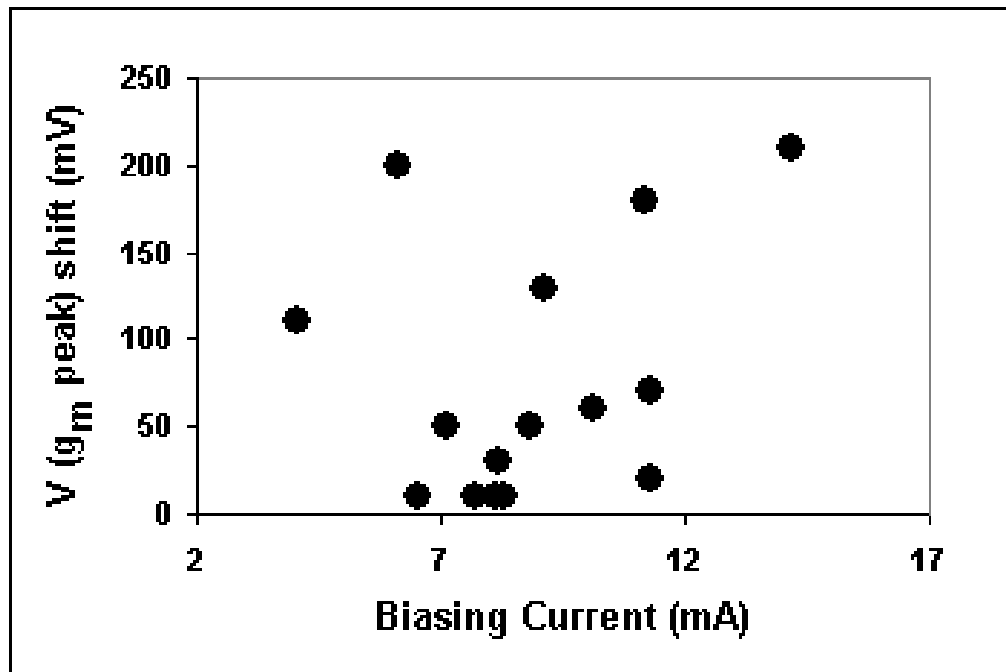

Figure 25. g_m peak shift as a function of biasing current (V_{gs} = -0.5 V, V_{ds} = 0.4 V). There is no clear trend of peak shift vs. biasing current.

In addition to the 16 devices shown in Fig. 23, other devices were tested under different bias conditions (such as V_{gs} = -0.8 V and V_{gs} = 0, both at V_{ds} = 0.4 V). All devices with V_{th} < -0.8 V were extremely resistant to g_m-peak shifts. Those that degraded significantly in spite of having high negative V_{th} had high kink-effect signatures (Fig. 24).

A. Biasing Current

There was no simple relationship between the biasing current (V_{gs} = -0.5 V, V_{ds} = 0.4 V) and degradation (Fig. 25) over the short time range for which these devices were biased (5 hours).

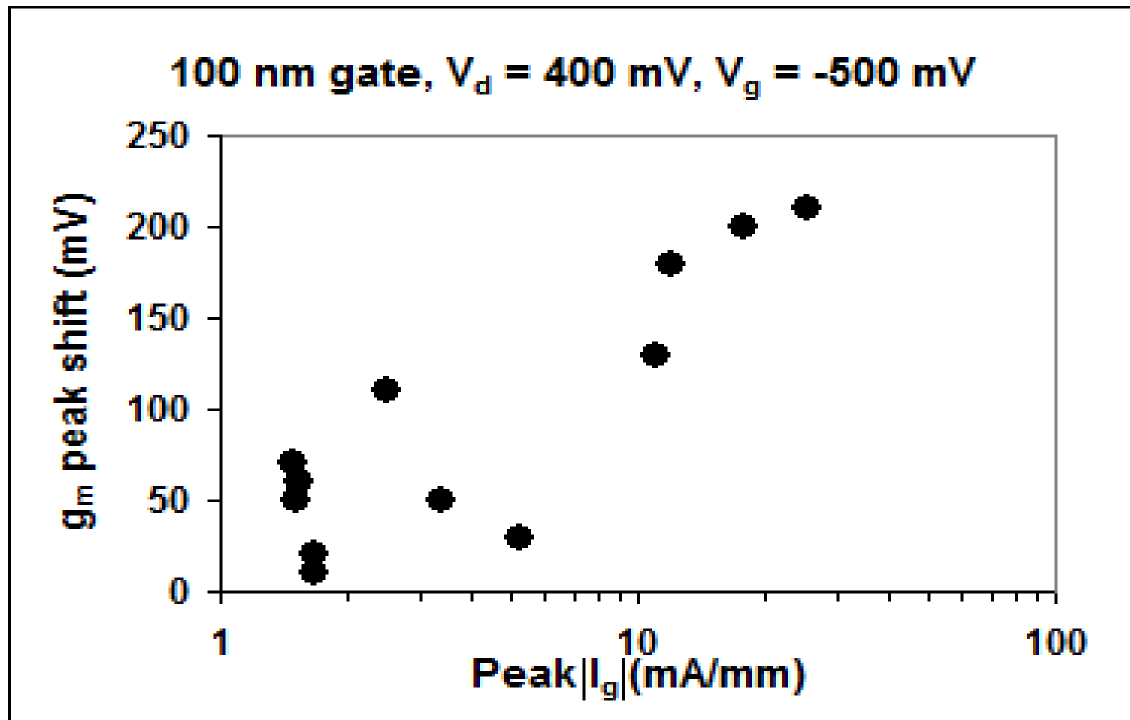

Figure 26. g_m peak shift (V_{ds} = 0.4 V) as a function of starting gate leakage. Very high gate leakage devices show more degradation. At the low gate leakage region, there is no definite trend of degradation as a function of starting gate leakage.

B. Pre-Stress Gate Current

The devices with very high $|I_g|$ were more prone to g_m shifts (Fig. 26). Since the gate current is quite high in these devices, there is a significant amount of injection-induced source-gate barrier lowering, which tends to promote recovery of any reduction in the magnitude of peak g_m or maximum drive current (current at zero gate voltage). However, the variation of the gate current from device to device is relatively large and no consistent trends are evident.

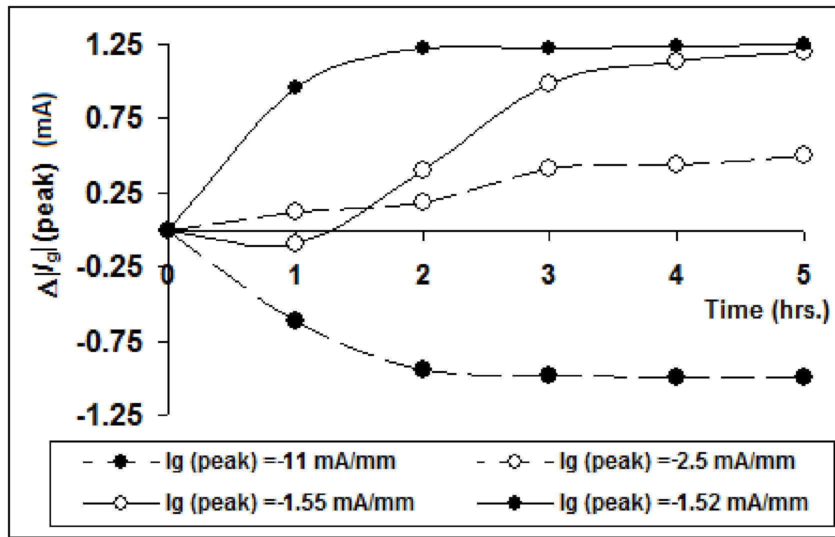

Figure 27. Peak gate current as a function of stressing time, for four different devices with starting gate leakage magnitudes of -11, -2.5, -1.55 and -1.52 mA/mm and final V_{th} shifts 130, 110, 20 and 70 mV, respectively.

Figure 27 shows the evolution of the gate current as a function of stressing time for four devices with different starting gate current magnitudes. As the gate current evolves while defects are activated or deactivated, the fields are modified by the changes in the charge states of the defects. Since the threshold voltage shifts negatively, an effective increase in the amount of positive charge in the gate stack takes place with stress. As shown in Fig. 28, the applied gate bias is distributed in the cap (Δ V_0), AlSb top buffer (Δ V_1), channel

(ΔV_2) and back AlSb buffer (ΔV_3). An increase in effective number of donors (ΔV_1) makes it easier for generated holes to gain energy to reach the gate contact. However, the reduction in the field in the channel, as evidenced by the reduction in peak g_m (Fig. 21), resulting from more of the applied bias being dropped across the top AlSb layer, results in a significant reduction in the hole generation rate through impact ionization. The relative change of fields in these two regions leads to the gate current increasing in some cases and decreasing in others.

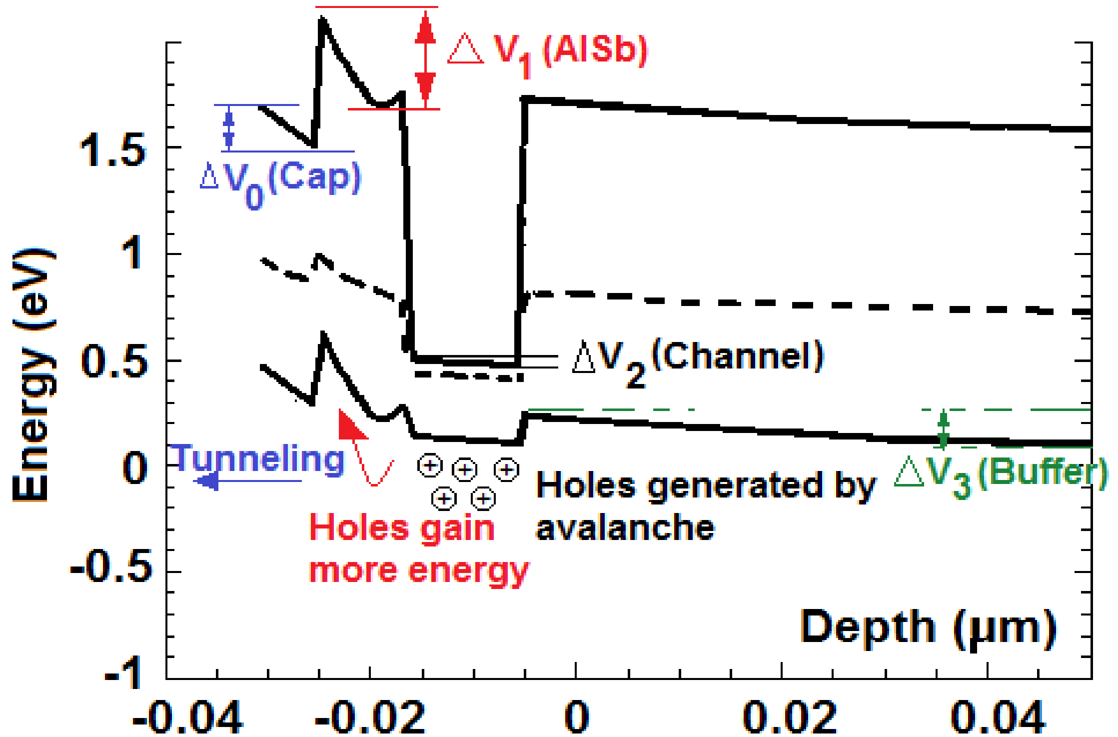

Figure 28. Band diagram along a vertical cutline at the center of the gate stack, showing different components of the applied gate bias V_{gs} = -0.8 V; here we showΔV_0 in the cap, ΔV_1 in the AlSb barrier, ΔV_2 in the InAs channel and ΔV_3 in the AlSb bottom buffer. The magnitude of ΔV_1 is controlled by the effective number of ionized donors, and ΔV_2 influences the rate of impact ionization.

A change in ΔV_0 in the cap can also change the tunneling efficiency of holes, introducing another component of uncertainty.

The degradation results shown in Fig. 23 and Fig. 26 have been summarized in Table II, where devices are arranged first in the order of increasing V_{th} and then decreasing $|I_g|$. It is evident that the degradation is related to pre-stress V_{th} and that high gate current devices are more degradation prone.

TABLE II
DEGRADATION AS A FUNCTION OF PRE-STRESS V_{TH} AND PEAK I_G

Dev. #	Pre-Stress V_{th} (mV)	$\Delta V_{gm, peak}$ (mV)	Dev. #	Pre-Stress Peak $\lvert I_g \rvert$ (mA)	$\Delta V_{gm, peak}$ (mV)
1	-610	200	2	25.4	210
2	-630	210	1	18	200
3	-700	180	3	12	180
4	-710	110	5	11	130
5	-750	130	9	5.2	30
6	-780	50	6	3.4	50
7	-790	70	4	2.5	110
8	-790**	60	15	1.69**	20
9	-890	30	10	1.68	10
10	-920	10	13	1.68	10
11	-940	10	11	1.67	10
12	-940	10	12	1.67	10
13	-960	10	14	1.67	10
14	-1000	10	8	1.55**	60
15	-1010**	20	16	1.52	50
16	-1030	50	7	1.5	70

Summary of the degradation ($\Delta V_{gm, peak}$) results as a function of pre-stress V_{th} and $|I_g|$.
**Devices 8 and 15 have L_g = 250 nm. All other devices have L_g = 100nm.

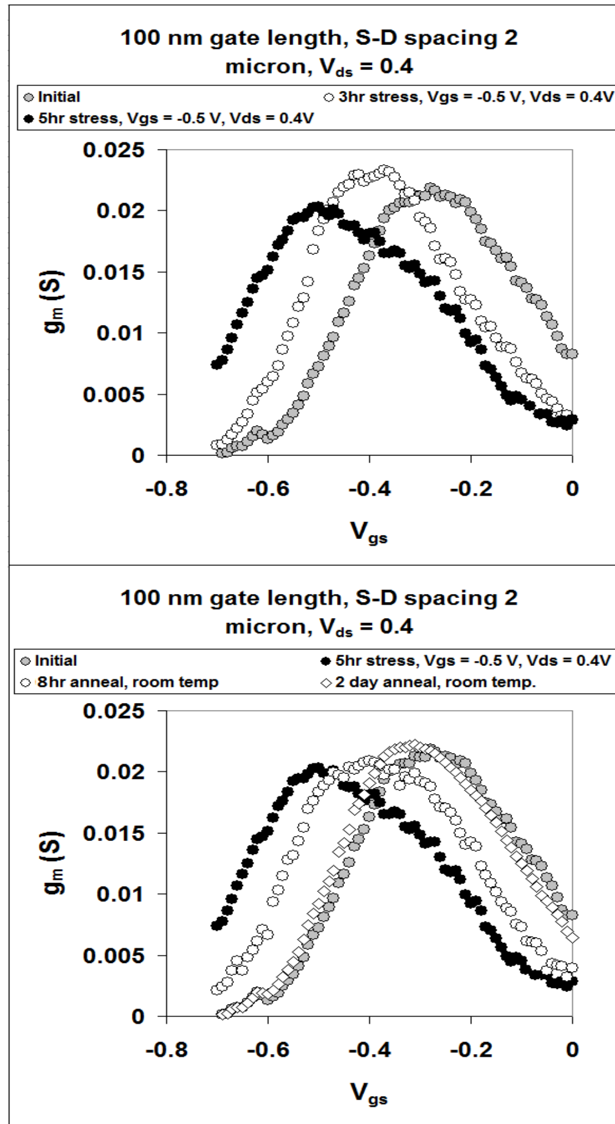

Figure 29. Degradation (threshold and peak gm shift) of a 2 × 20 mm HEMT with 100 nm gate length and 2 mm source-drain spacing. Devices were stressed at V_{gs} = -0.5 V and V_{ds} = 0.4 V for 5 hours. Annealing results at room temperature are shown. The device recovers almost completely in 2 days.

5.3 Room Temperature Annealing of Stressed Devices

Fig. 29 shows the degradation and recovery trends of a 2 × 20 μm HEMT with 100 nm gate length and 2 μm source-drain spacing. Devices were stressed at V_{gs} = -0.5 V and V_{ds}

= 0.4 V for 5 hours. The stressed devices almost completely recover to the pre-stress conditions in ~2 days. The devices were kept at room temperature with no applied gate or drain bias.

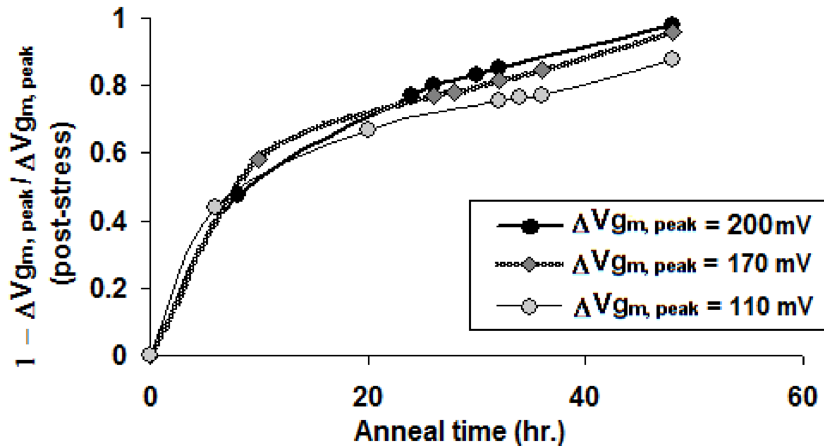

Figure 30. Fractional recovery of $V_{gm,\ peak}$ of three devices with varying degrees of initial degradation. For all the devices, 50 % recovery is achieved in 6-8 hours and more than 90 % recovery in 2 days.

Figure 30 shows the fractional recovery rates of three devices with varying degrees of post-stress degradation. The recovery rates are fairly similar with 50% recovery achieved in 6-8 hours and more than 90% recovery achieved in 2 days. At the initial stages of recovery, the recovery follows an almost exponential rate. When the devices get closer to complete recovery, there is departure from the expected exponential behavior. This might indicate that more than one type of defect is responsible for the device degradation. While a simple extrapolation of the trends near complete recovery suggests that longer annealing would lead to super recovering the device (introducing a threshold voltage shift towards a less negative value than the pre-stress threshold voltage), measurements after two weeks of annealing showed no signs of super recovery.

CHAPTER VI

PHYSICAL MECHANISMS OF DEGRADATION – METASTABLE DEFECTS IN AlSb

6.1 Location and Metastable Nature of Defect

Since the stress-induced degradation results in a negative shift of the threshold voltage, there is net positive charge trapping in the gate stack, corresponding to activation of donor traps or deactivation of existing acceptor traps. These traps are likely to be in the InAs channel or the AlSb buffer. Hole trapping and slow emission in the gate stack is unlikely due to the high gate current (about 1 - 5% of the drain current at the bias condition). Surface states in the device passivation are not responsible for the degradation, since these affect only the access regions, and are unable to produce large threshold voltage shifts. In addition, defects in the channel would degrade the mobility, which is not observed even for a significant negative shift of the g_m peak. For these reasons, traps in the top or bottom AlSb barriers appear to be responsible for the degradation. In addition, the gradual recovery of the devices to their initial states in a few days demonstrates the metastable nature of the degradation. Deep traps with long emission times (with no change in configuration or transition level following trapping or emission) are not responsible for this behavior, since the high gate currents prevent traps from remaining stable in their new charge states for long times.

The greater degradation at high fields in the channel indicates the role of hot carriers in the degradation process. While hot electrons are unlikely to retain sufficient energy in the AlSb away from the interface (given the high $\Delta E_c = 1.3$ eV), a sufficiently large number of energetic holes (derived from avalanching in the channel) exist at the stressing biases (Fig. 31).

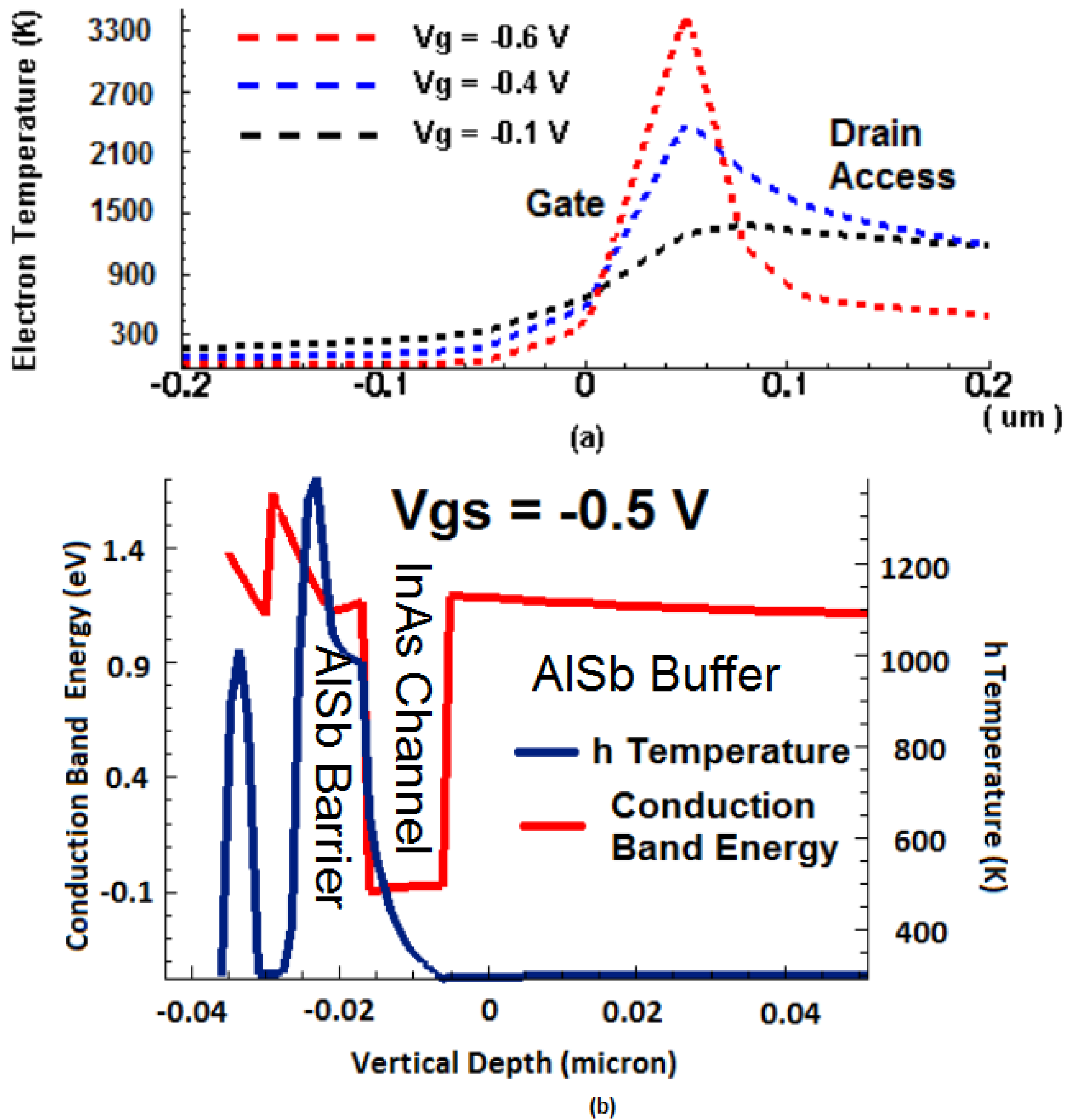

Figure 31. (a) Electron temperatures at bias condition at the gate-drain edge in the InAs channel, as shown in Fig. 21. (b) Impact ionization generated holes gain more energy as they move along the AlSb buffer away from the channel.

6.2 Native Defects

Recent density functional theory (DFT) calculations [27-28] show that the formation energy of the antimony antisites (Sb_{Al}) is the lowest among all native defects at the growth conditions of AlSb. This defect can change its configuration to a metastable state with a more positive charge state than its lower energy configuration. However, the results in Figure 32 show the formation energies of the ground state and metastable configurations of the Sb_{Al} antisite. The slope of the formation energy plot (marked in Fig. 32) for a given defect represents the charge state of the defect at a particular Fermi level or chemical potential. The (0/+1) transition energy (which is the energy at which the defect changes its charge state from 0 to +1 – or a donor level for the antisite) is much shallower for the ground state T_d structure than for the metastable C_{3v} structure.

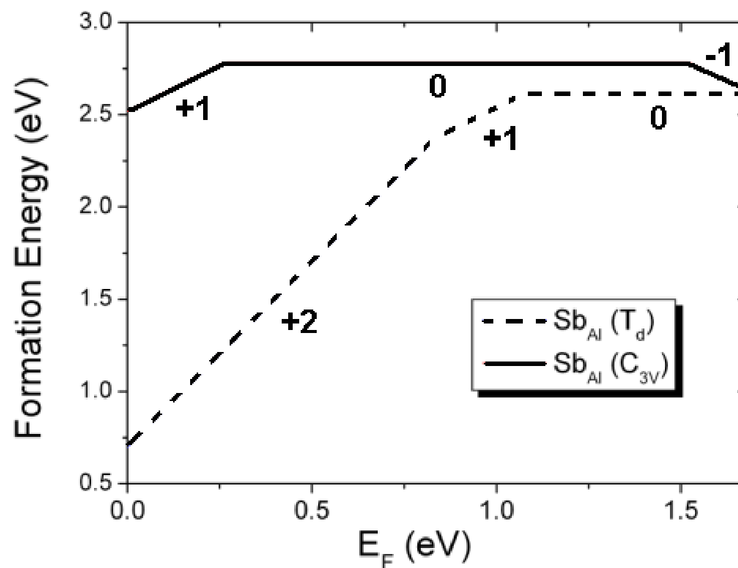

Figure 32. Thermodynamic transition levels for the ground-state (T_d) and the metastable (C_{3v}) Sb_{Al} defect in Al-rich conditions. The donor like transition level (0/+1) is shallower for T_d than for the metastable C_{3v} structure. This precludes the possibility of negative V_{th} shifts due to transition of some antisites from T_d to C_{3v} under applied stress.

This rules out the antimony antisite as the defect responsible for the observed degradation. Another defect with similar formation energies is the aluminum interstitial, Al_i. However, the diffusion barrier of the Al_i interstitial (1.28 eV) [28] is small and is likely to anneal during the fabrication process.

6.3. Oxygen Based Defects

The criteria for the negative shift in threshold voltage under electrical stress are satisfied by two oxygen-based defects that exhibit metastability. We now discuss the nature of these defects. Fig. 33 shows the position of the average of the electron and hole quasi Fermi levels along the AlSb top buffer at the center of the gate as obtained from a hydrodynamic simulation [29-35] using Synopsys Sentaurus. This average determines the charge state of defects in a region of non-equilibrium. The average of the quasi Fermi levels varies between 0.37 eV and 0.6 eV from the valence band edge as V_{gs} varies from 0 to -0.8 V (Fig. 33-bottom).

There is strong experimental evidence that oxygen is a key contaminant in AlSb [19]. Fig. 34 (bottom) gives a schematic picture of the formation energies of different configurations of substitutional oxygen O_{Sb}. The substitutional oxygen is a negative-U center (effective correlation energy U between two electrons in the same state is negative, so that ground state of the defect is diamagnetic [36-37]), with (+/−) transition level at 0.3 eV above the valence band edge, which explains the previously reported oxygen related deep donor in AlSb [38]. Transition from α/β-CCBDX configuration (CCBDX denotes DX center with cation-cation bond) [39] to the C_{3v} configuration at E_f ~ 0.47 eV or lower

changes the defect charge state from -1 to +1, causing a negative shift in threshold voltage.

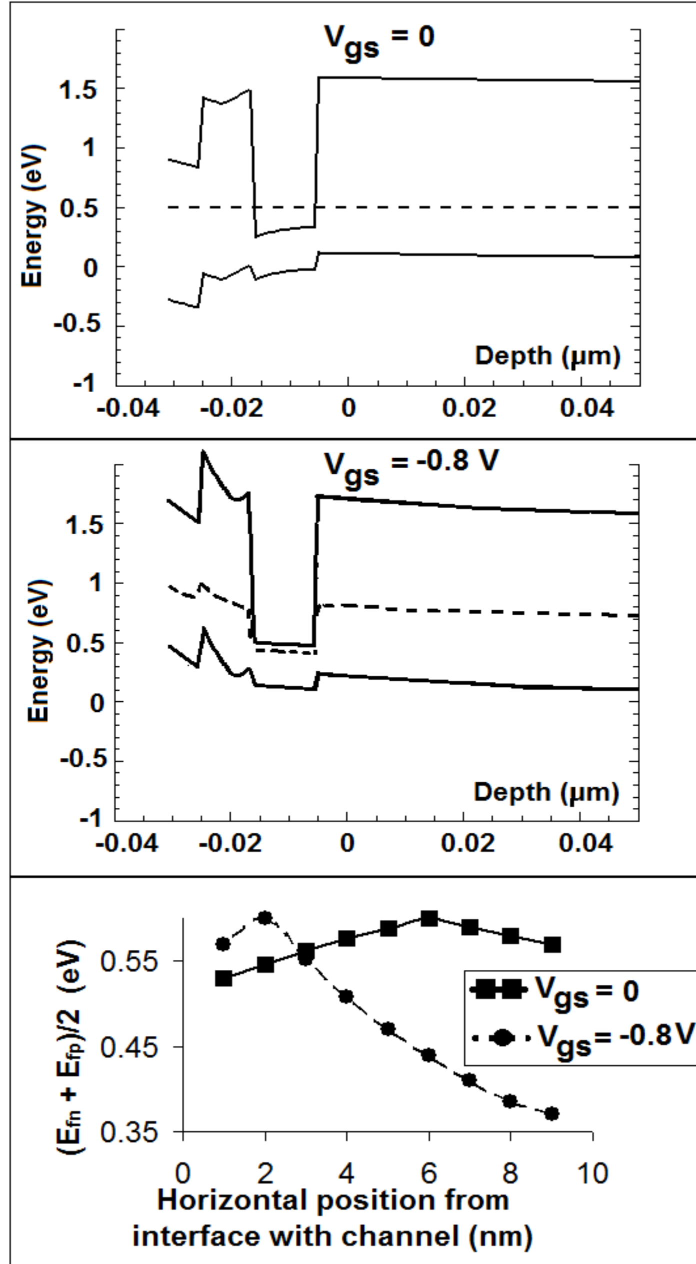

Figure 33. Position of the average of electron and hole quasi-Fermi levels (dashed lines) obtained from simulations of a HEMT with V_{th} ~ 0.6 V at V_{ds} = 0.4 V and V_{gs} = 0 (top) and -0.8 V (middle). The position of the average of the quasi-Fermi levels with respect to the valence band edge is plotted as a function of position in the AlSb buffer in the bottom panel.

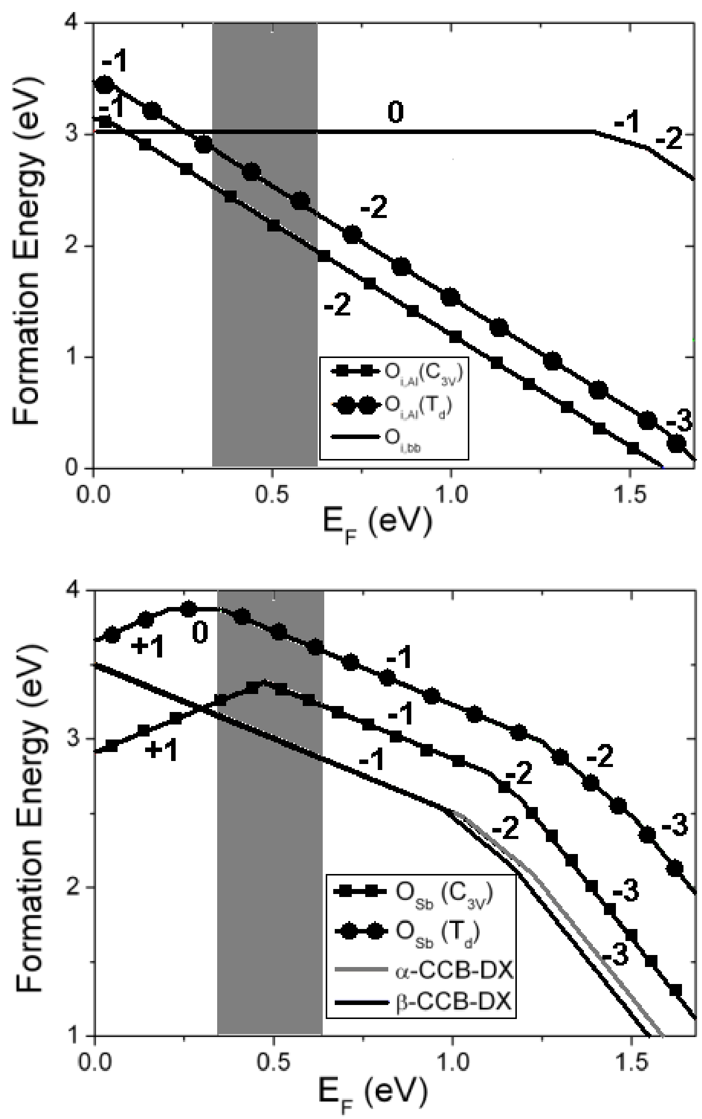

Figure 34. Transition levels for (bottom) substitutional and (top) interstitial oxygen shown. α/β-CCBDX are the lowest energy configurations for O_{Sb}, followed by C_{3v} and T_d configurations. Transition from α/β-CCBDX to either of the 2 defects at $E_f \sim 0.4$ eV will change the defect charge state from -1 to +1 or 0, causing a left shift in threshold voltage. A transition from $O_{i,\ Al}$ (C_{3v}) to $O_{i,bb}$ for the interstitial oxygen will give the same effect. The grey band shows the range of the average of the 2 quasi Fermi levels for the entire operating range of the device.

Also, the difference between the formation energies is sufficiently small (0 to 0.35 eV) in the region where they have different charge states so that enough holes have the requisite

energy ~(0 to 0.35 eV) to overcome the formation energy barrier. The gray band shows the range over which the average of the quasi-Fermi levels can vary within the operating range of the device, as calculated from Fig. 33.

The $O_{i,Al}$ (C_{3v}) and $O_{i,bb}$ configurations of interstitial oxygen are also consistent with the degradation trends (Fig. 34 (top)). For the range of E_f in AlSb, the higher energy configuration $O_{i,bb}$ (bb implies bridge-bond structure of interstitial similar to the interstitial oxygen in silicon [40]) is neutral, and hence is more positive than the -2 state of the most stable $O_{i,Al}$(C_{3v}). Near zero gate voltage, the states are separated by a large energy (~1.1 eV). However for high negative gate voltages, the energy difference can become as low as ~ 0.4 eV, making possible a transition to the more positive neutral state, which produces a negative shift in the threshold voltage.

6.4 High Negative V_{th} Devices and Oxygen Based Defects

Apart from satisfying the basic criteria for a negative shift of the threshold voltage, the transition energies of oxygen based substitutional and interstitial defects are consistent with the lack of degradation exhibited by the high negative threshold voltage devices. In Fig. 35, the transition levels for substitutional and interstitial oxygen are plotted vs. the Fermi level limits (V_g = -0.8 V to 0 V) for devices with V_{th} = -0.6 V (dotted line) and V_{th} = -1 V (solid line). For the device with V_{th} = -1 V, the Fermi level never enters the region where O_{Sb} (α/β-CCBDX) and O_{Sb} (C_{3v}) have different charge states. For the top AlSb layer of this device, the energy difference between $O_{i,Al}$ (C_{3v}) and $O_{i,bb}$ is always greater than 0.7 eV, making it very difficult for hot holes to modify the defect configuration.

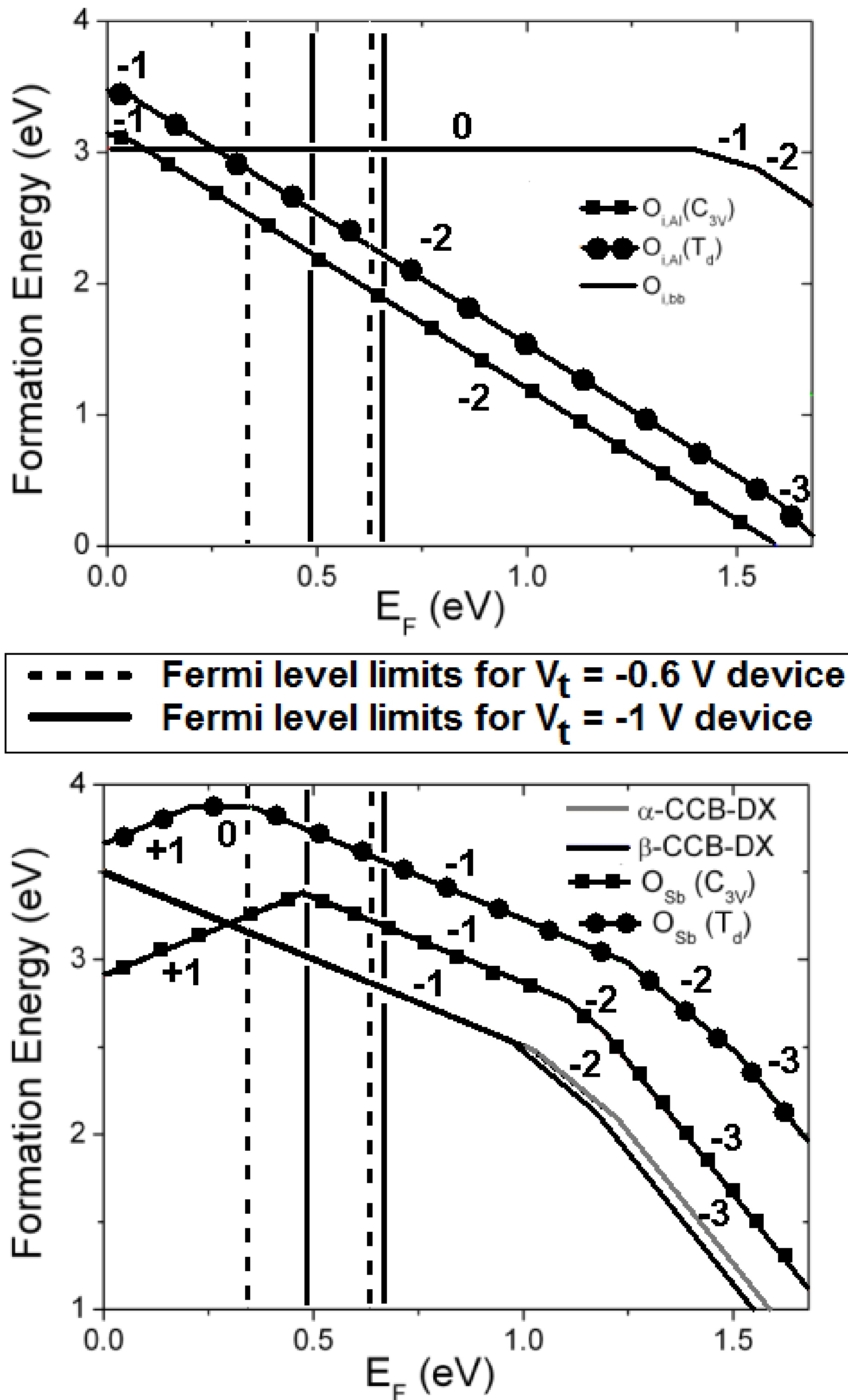

Figure 35. Transition levels for (bottom) substitutional and (top) interstitial oxygen plotted against the Fermi level limits (V_{gs} = -0.8 V to 0 V) for 2 devices with V_{th} = -0.6 V (dotted line) and V_{th} = -1 V (solid line).

6.5 Other Impurity Based Defects

Carbon is another common contaminant in AlSb [41-43]. A carbon peak is also observed in the EDAX measurement in [19]. According to Aberg [44] and Du [39], C exists in the form of C_{Sb}. The formation energies of possible stable configurations of C_{Sb} are shown in Figure 36(left). The ground state of C_{Sb} has T_d symmetry and is a shallow acceptor. The only metastable configuration we find is the BB-DX structure, which is stable in the -2 and -3 charge states. Since C_{Sb}(BB-DX) levels are more negative than the ground state, the carbon impurities cannot account for the observed degradation [45, 46].

Tellurium is used to Δ-dope the top AlSb layer of the InAs - AlSb HEMTs. Te atoms substitute for Sb and act as shallow donors, providing electrons to the InAs channel.

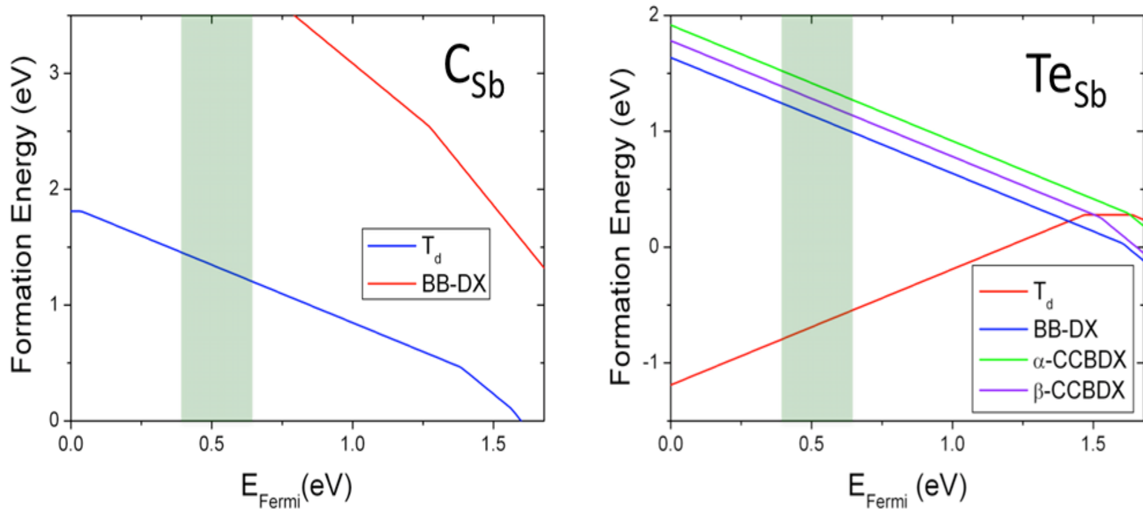

Figure 36. (Left) Formation energies of stable configurations of C_{Sb}. (Right) Formation energies of stable configurations of Te_{Sb} [46].

Under electrical stress, it is possible for the injected holes to reach the Δ-doped area and convert a Te_{Sb} from its ground state into a metastable configuration. The formation

energies of stable configurations of Te_{Sb} are shown in Figure 36 (right). For a wide range of the Fermi level, the ground state of Te_{Sb} is Te_{Sb}(Td)+. Close to the conduction band, the negatively charged BB-DX structure becomes the thermodynamical ground state. The other two DX-like structures, α-CCB-DX and β-CCB-DX, are also stable. The existence of these DX-like structures is consistent with experimental data [47]. It is clear that Te cannot account for the degradation observed, since the metastable DX structures are more negatively charged than the ground state, Te_{Sb} (Td)+. Based on the above analysis, among the common intrinsic and extrinsic point defects in these kinds of devices, oxygen impurities, both substitutional and interstitial, have long lived metastable states that are more positive than the ground states. Hence, these defects appear to be the most logical candidates for the degradation and recovery observed in the InAs - AlSb HEMTs. This result strongly suggests that minimizing O contamination during device fabrication should significantly enhance the reliability of InAs - AlSb HEMTs.

6.6. Origin of Long Lifetime

Since the excited metastable state is not the thermodynamical ground state of the defect, it will capture an electron and relax back to the ground state when the injection of holes is stopped. However, the excited state may have a very long lifetime because the electron capture can be very slow in this kind of structure. There are three possible processes for the defect in the excited state to capture an electron. The first process is capturing an electron from the conduction band. Since the Fermi level is far below the conduction band, the free electron concentration is very low. Thus, a defect can stay in the excited

configuration for a long time before it captures a conduction band electron. In the second process, the empty defect level gets occupied by an electron thermally excited from the valence band (thermal hole emission). This process can also be slow because the empty defect level is now far above the valence band. In the third process, the empty state gets occupied by an electron tunneling across the interface. Since the empty electronic level is far above the Fermi level, the tunneling process can also be slow, especially for defects that are far from the interface. Thus, a slow rate for overall electron capture can be achieved. Although the large shift of electronic level is usually found in a DX center, which also exhibits a sizable energy barrier for electron capture, a barrier is not needed to ensure a slow rate of electron capture. As long as the electron concentration in the conduction band is sufficiently low, the first process can be slow even if the barrier is small.

In principle, this kind of metastability can exist in bulk semiconductors, but it may be realized more easily in a heterostructure like an InAs - AlSb HEMT, where the Fermi level is controlled by other layers, and a flux of carriers can be injected across the interface to generate a non-equilibrium concentration of metastable states [46].

The relationship between the long defect recovery time and the low electron concentration in the top AlSb layer is supported by recovery trends under negative gate bias and no drain bias. Figure 37 shows the recovery of two devices with similar stress-induced degradation (transconductance peak changes of 110 and 130 mV). The device biased at $V_{gs} = -1$ V (Fig. 37a) shows significantly less recovery than the one biased at $V_{gs} = -0.7$ V (Fig. 37b). Fig 37c shows the fractional recovery in devices with ~ 110 mV post-stress degradation as a function of gate bias. Since more negative gate bias implies

Fermi levels closer to the valence band and hence fewer electrons, the slower recovery under negative gate bias suggests that the defect recovery time depends on the electron density in the top AlSb layer.

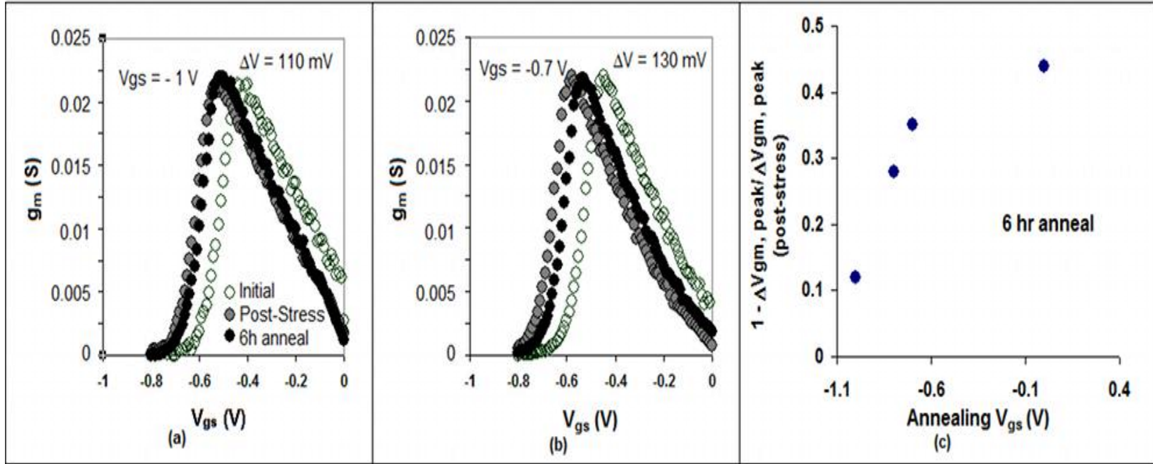

Figure 37. Transconductance vs. V_{gs} plots for devices before and after stress, and after 6 h of annealing at zero drain bias, for (a) $V_{gs} = -1$ V and (b) $V_{gs} = -0.7$ V. (c) Fractional recovery under four different gate biases, with zero drain bias in all cases [46].

6.7. Relative Formation Energies at Growth Conditions

The Fermi level at the time of growth can give important indications of the relative abundance of the defects that can produce the observed degradation. When the AlSb buffer is grown on the InAs channel, the Fermi level is very close to the valence band edge of AlSb. As the layer is grown, the Fermi level steadily rises (Fig. 38 a-d). The Fermi level during growth is plotted vs. the distance from the interface with the InAs channel in Fig. 38d. The formation energy of interstitial oxygen is lower than that of the substitutional oxygen by about 0.9 eV in the top half of the AlSb barrier (Fig. 38e). The formation energy of both substitutional and interstitial oxygen is highest when the Fermi

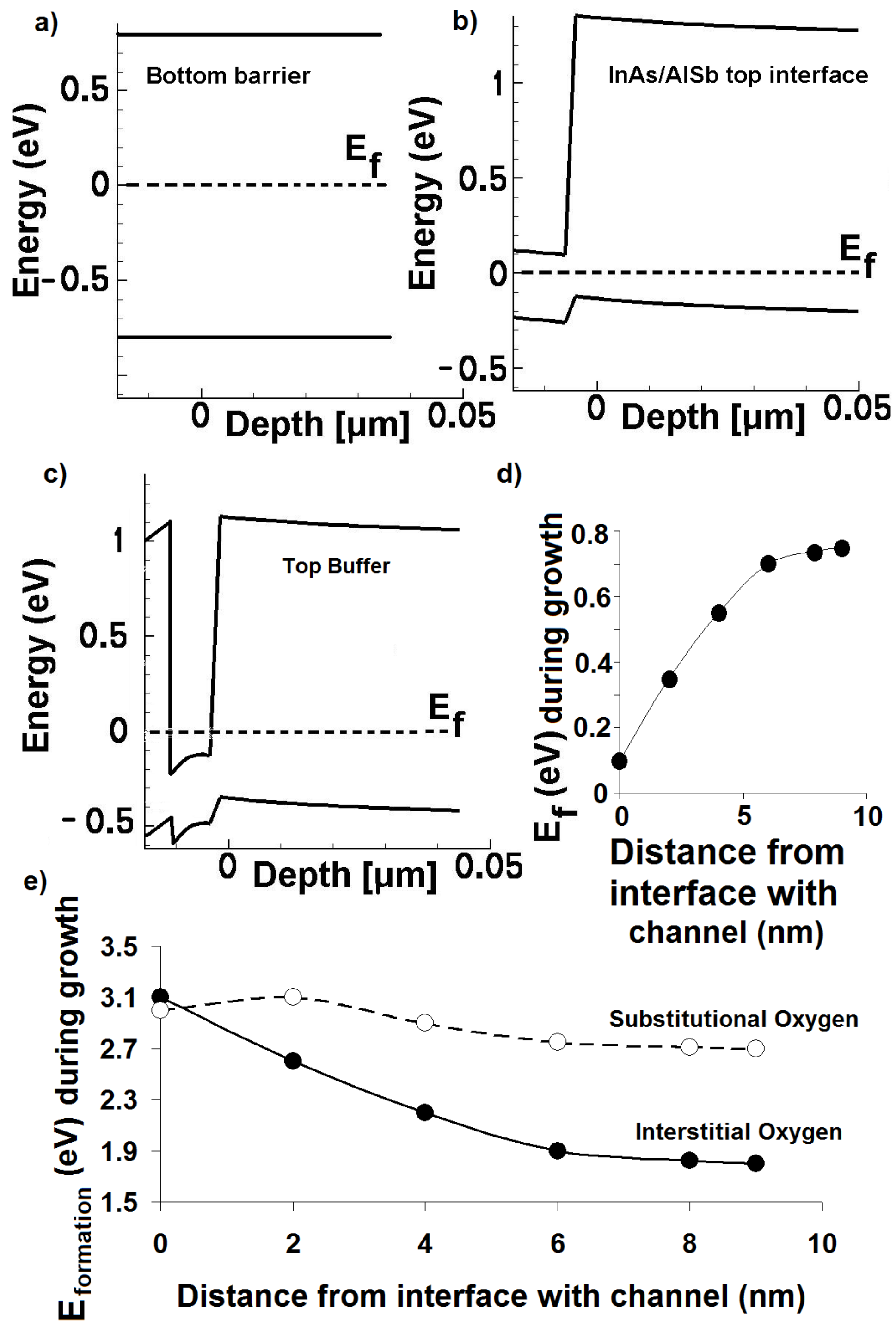

Figure 38. Surface Fermi levels during growth for a) bottom AlSb buffer, b) InAs - AlSb top interface and c) top /AlSb barrier. Growth Fermi level in the top AlSb layer is plotted as a function of distance from the channel interface. Using formation energy values of the lowest energy states of substitutional and interstitial oxygen from Fig. 34, the formation energies of both defects during the growth of the top AlSb layer are plotted.

level is near the valence band edge and progressively decreases towards the conduction band. Thus, both defects will be present in much lower concentrations near the channel – top barrier interface than in the upper portions of the top AlSb barrier. This is consistent with the high channel mobility of devices both before and after stress, irrespective of the magnitude of the threshold shift.

6.8 Synopsis of Degradation, Annealing and Comparison with Theoretical Defect Properties

A significant fraction of InAs - AlSb HEMTs exhibit degradation under hot carrier stress. Degradation is manifested as a shift in the transconductance peak toward more negative gate voltages, with no mobility degradation, indicating the activation of new donor defects or deactivation of existing acceptors in the AlSb layers flanking the channels. Devices with large-magnitude threshold voltages and those with long gate lengths exhibit very little degradation, indicating the role of hot carriers. The defects anneal out within a few days. The I_d-V_{ds} trends and gate current magnitudes point to the existence of a metastable deep acceptor state that is modified by hot carriers. Density Functional Theory calculations of the energetics of substitutional and interstitial oxygen show metastable states consistent with the degradation trends. The defects satisfy the basic trend of threshold voltage shift towards more negative voltages under stress. The calculated defect energies are also consistent with the strong dependence of degradation on the threshold voltage of the unstressed device. The origin of the long lifetime of the metastable state can be justified by considering the low density and hence slow rate of electron capture in

AlSb. This is further supported by the dependence of annealing times on applied bias and the slowness of recovery under negative gate bias conditions. Other physically abundant impurities like carbon and tellurium forming defects with metastable configurations as well as known native defects with metastable states are considered. The energies of these defects show that they are unlikely candidates for the observed degradation. The analysis can be considered as part of a general method to estimate the importance of a given defect in the reliability of a device under stress.

CHAPTER VII

DEGRADATION IN SMALL SIGNAL PARAMETERS UNDER HOT CARRIER STRESS

7.1. Degradation in Small Signal Performance for Devices with Negligible DC Degradation

In the previous two chapters, we presented degradation results and defect analysis for the InAs - AlSb HEMTs which showed perceptible, and in some cases severe, DC degradation within 3 - 5 hours of bias time. As we mentioned earlier, more than half of the devices showed no perceptible signs of DC degradation. However, the small signal performance for all devices degraded considerably after stress. The devices showed significant changes in peak f_T. Short access region lengths exacerbated the degradation, which could be traced to a reduction in peak RF g_m in all devices, resulting from reduced hole mobility in AlSb. Post-stress increase in scattering of holes is identified as a potential cause. Increase in parasitic capacitances after stress had a significant contribution to the degradation in devices with short access regions.

7.2. Devices and Small Signal Measurements

Devices with 4 different gate lengths (100, 250, 500 and 700 nm) with 2 μm spacing between source and drain edges (L_{ds}) as well as 250 and 500 nm gate length devices with

L_{ds} = 2.5 and 3.5 μm were tested. S-parameters were measured on-wafer from 0.5 - 26.5 GHz employing TRL (thru-reflect-line) calibration structures. From the measured s-parameters, the short circuit current gain, and Mason's unilateral power gain were obtained. The maximum frequency of oscillation, f_{max}, was obtained by extrapolating to unity gain. In the measurements, $|h_{21}|$ rolls off more slowly than -20 dB/decade. This is due to two effects – first C_{gd} is significant and leads to an additional high-frequency zero in the transfer function. But more importantly, the gate leakage current limits $|h_{21}|$ at low frequencies. Nevertheless, the frequency dependence of $|h_{21}|$ and U is very close to linear in the high frequency range of the measurement. Fig 39 shows the short circuit current gain and unilateral gain for a device with L_g = 100 nm and L_{ds} = 2 μm.

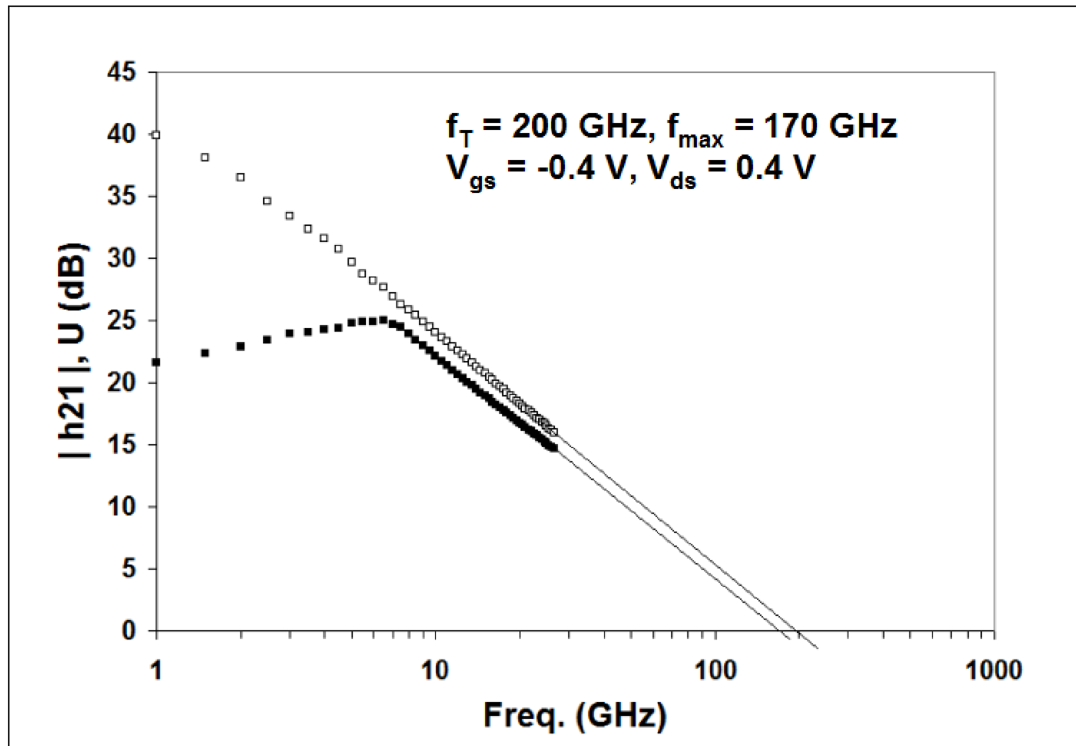

Figure 39. Peak f_T and f_{max} extracted from $|h_{21}|$ and U extracted from s-parameters measured on a 2 × 20 HEMT with 100 nm gate length and L_{ds} = 2 μm. Bias conditions for peak transition and osscilation frequencies are V_{ds} = 0.4 V and V_{gs} = -0.4 V.

7.3 Device Degradation Under Hot Carrier Stress

Fig. 40 shows the degradation in short circuit current gain $|h_{21}|$ calculated from measured s-parameters for a 2 × 20 μm HEMT with 100 nm gate length and 2 μm source-drain (S-D) spacing. The device is operated at $V_{gs} = -0.3$ V and $V_{ds} = 0.4$ V for 3 hours. From the I_g-V_{gs} plot, this gate voltage corresponds to maximum impact ionization in the channel. Extrapolation of $|h_{21}|$ beyond 26.5 GHz shows f_T decreases by 20 GHz following stress. Devices with gate lengths 100, 250, 500, and 700 nm and L_{ds} = 2 μm were tested (Fig. 41). Although f_T decreased between 5 and 25%, DC currents decreased less than 0.5% in all cases (Fig. 40).

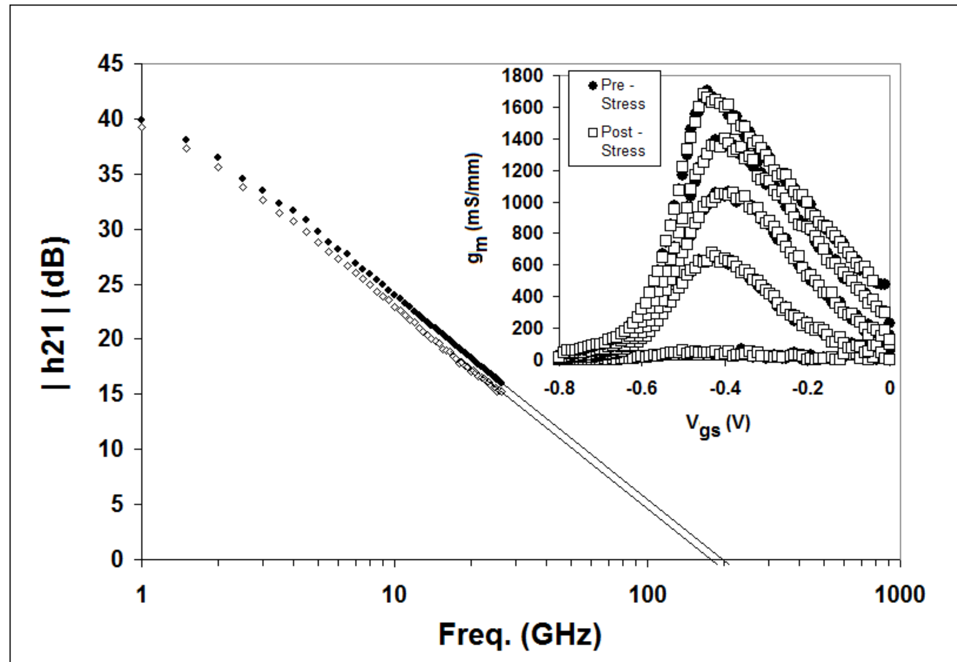

Figure 40. Pre and post-stress (V_{gs} = -0.3 V, V_{ds} = 0.4 V, 3hrs.) $|h_{21}|^2$, calculated from s-parameter measurements for a 2 × 20 μm InAs - AlSb HEMT with 100 nm gate length, at f_T peak (V_{gs} = -0.4 V, V_{ds} = 0.45 V). Post stress peak f_T degrades from 200 to 180 GHz. The panel inside shows pre and post DC g_m. There is no perceptible DC degradation.

Since all devices reported in Fig. 41 have 2 μm L_{ds}, the access region is shorter in devices with longer gate lengths. The gate bias is relatively small and only a fraction of the bias is dropped vertically across the InAs channel (the rest being dropped across the cap and upper and lower buffer layers). Therefore, the gate edge to drain field in the channel, which is the major source of hot carriers, is controlled more strongly by the drain bias and the gate-to-drain edge spacing than the gate length. Thus, the highest hot carrier generation rate occurs in devices with long gate lengths and, hence, short access regions. Fig. 42 shows f_T degradation results for 250 and 500 nm gate length devices for S-D spacings of 2, 2.5, and 3.5 μm. Degradation decreases steadily with increasing S-D spacing for all devices.

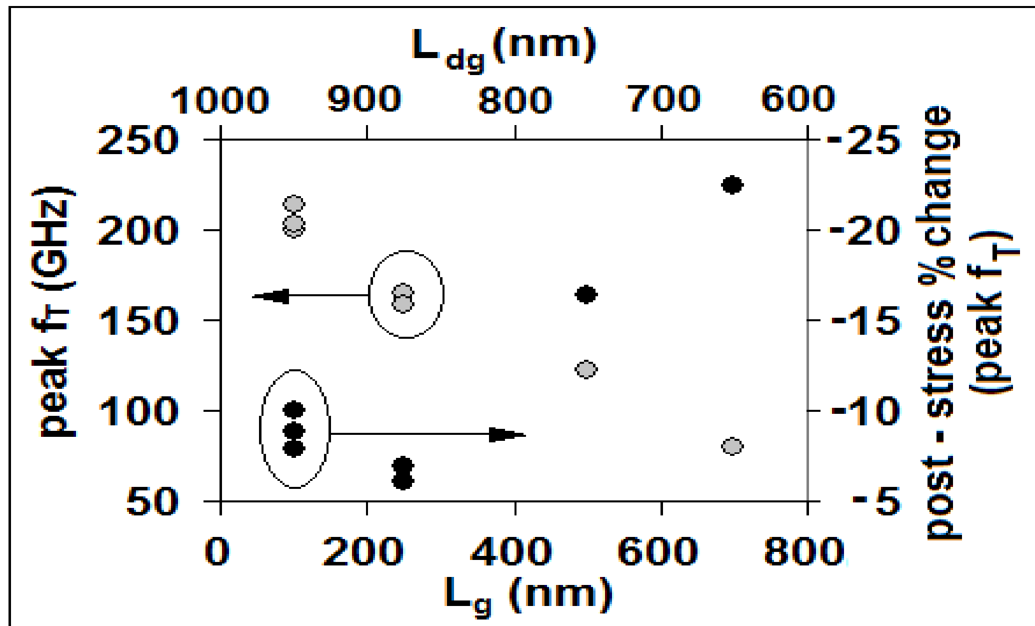

Figure 41. Starting peak f_T (left y-axis) and post stress percentage reduction in peak f_T (right y-axis) in 7 HEMTs of different gate lengths (100, 250, 500 and 700 nm). All devices are stressed for 3 h at V_{gs} = -0.3 V, V_{ds} = 0.4 V. For all devices, source-drain spacing is 2 μm, so longer gate length implies shorter gate edge to drain edge spacing (top x-axis). These devices show greater peak f_T degradation. The negative sign in % change implies reduction.

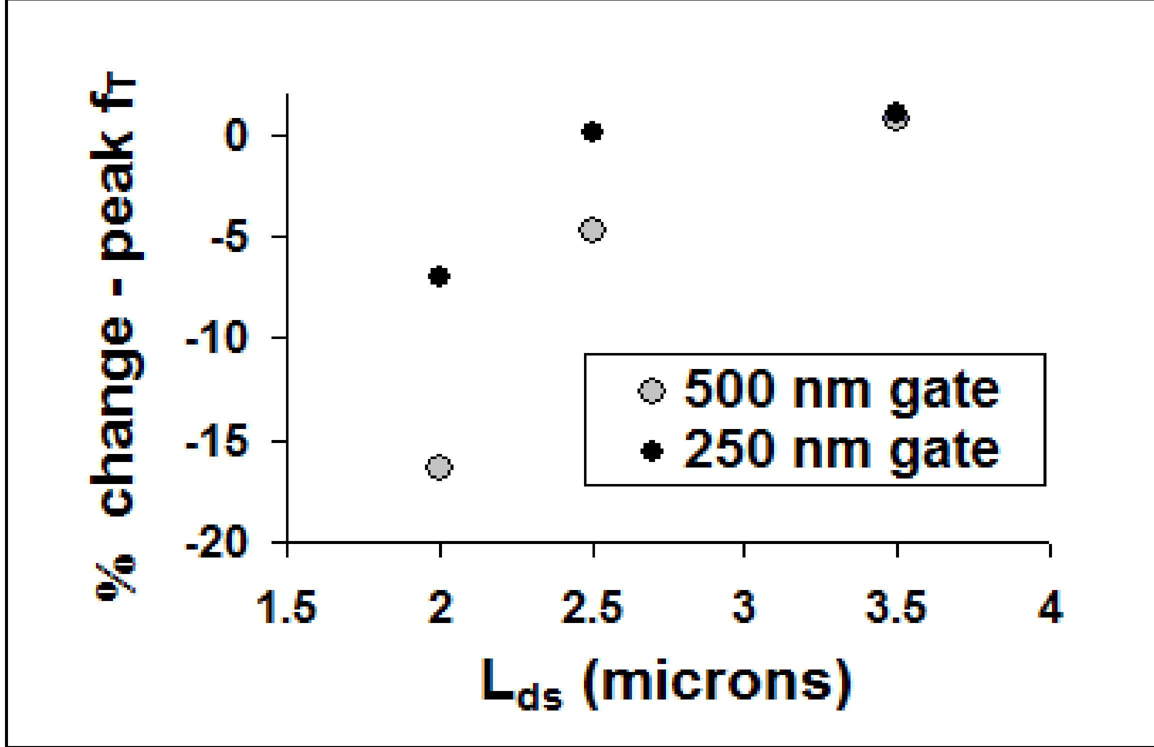

Figure 42. Post stress percentage change in peak f_T (negative sign in % change implies reduction) in HEMTs with gate lengths 250 and 500 nm for S-D spacing 2, 2.5 and 3 μm. All devices are stressed for 3 hrs. at V_{gs} = -0.3 V, V_{ds} = 0.4 V.

Devices with long access spacings are more resistant to f_T degradation. The transition frequency of the depletion mode HFET is given by the expression [48,49]

$$f_T = g_m/2\pi\ [(C_{gs} + C_{gd})[1 + (R_d + R_s)/R_{ds}] + C_{gd}g_m(R_d + R_s)]^{-1} \qquad \text{-(3)}$$

Since the DC characteristics of the device show almost no degradation, it is unlikely that the frequency independent components like R_d, R_s or R_{ds} play a significant role in the small signal degradation. This implies that either g_m or the parasitic capacitances could explain the change in transition frequency post stress. For this, it is necessary to

understand in detail the extraction of the small signal equivalent circuit parameters of the field effect transistor.

7.4 Modeling Active FET

A number of small-signal equivalent circuit topologies exist for microwave FETs [49-55]. The main differences between them lie in the locations of the parasitic elements, which depend on the transistor geometry and on the transistor-embedding medium. Independently of topology, equivalent circuit elements can be grouped in two categories:

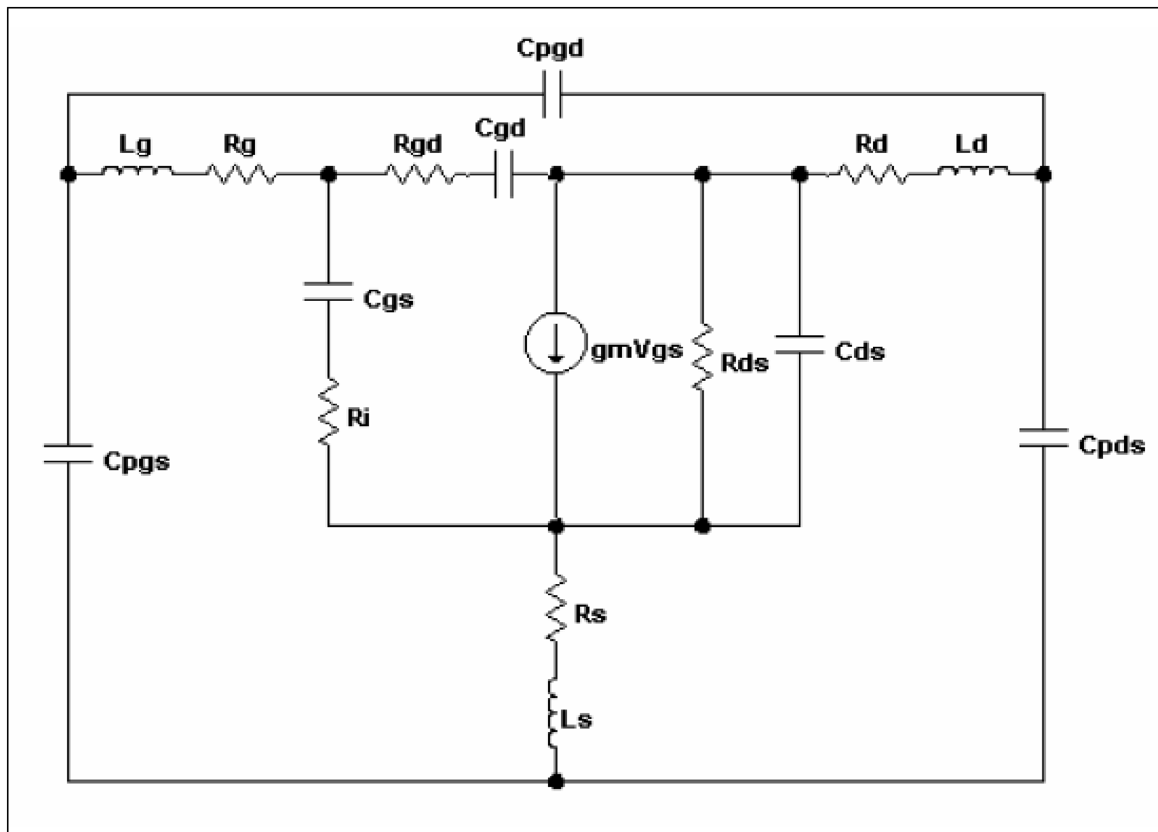

Figure 43. Small-Signal equivalent circuit for gate-drain resistor model [56].

extrinsic or parasitic parameters, which are bias independent (R_s, R_d, R_g, L_s, L_d, L_g, C_{pgs}, C_{pgd}, and C_{pds}), and intrinsic parameters, which are bias dependent (C_{gd}, C_{gs}, C_{ds}, R_i, g_m, R_{ds}) (Fig. 43). De-embedding of pad capacitances becomes an important issue for millimeter wave applications.

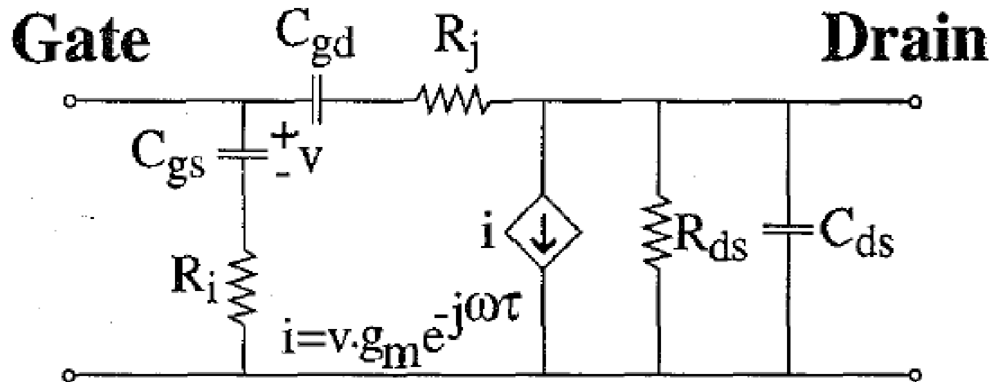

Figure 44. The intrinsic equivalent circuit of the HFET [57].

However, this involves methods of biasing the gate that tend to cause destructive damage to the HFET gate. For this reason the extraction of equivalent circuit parameters was done using the extrinsically measured s-parameters. While this would result in some of the parasitic pad capacitances, pad resistance and inductances being embedded in the active device model extraction, these are unlikely to be important factors in device degradation for two reasons. First, all these quantities are small and do not introduce first order errors in impedance at the frequencies at which s-parameters were measured. Second, all of these quantities depend on details of the device and pad structure, which are very unlikely to be affected by stress. For this reason, we shall use the Y-parameters

of the intrinsic device synonymously with Y-parameters extracted from s-parameter measurements on the extrinsic device. Fig. 43 shows the small signal equivalent circuit including all extrinsic parasitic elements like pad capacitances, contact resistances and inductances. Fig. 44 shows the equivalent model for the intrinsic device. The Y-parameters are given by

$$Y_{11} = Y_{gs} + Y_{gd} \quad -(4)$$

$$Y_{12} = - Y_{gd} \quad -(5)$$

$$Y_{21} = - Y_{gd} - \text{Im}\,(Y_{gs})/(Y_{gs}^{*}).g_m.e^{j(\pi/2 - \omega\tau)}, \quad -(6)$$

$$Y_{22} = Y_{ds} + Y_{gd} \quad -(7)$$

where Y_{gd}, Y_{gs} and Y_{ds} represent the gate-drain, gate-source, and drain-source admittances, respectively. Usually $\text{Re}(Y_{12})$ is neglected, but the nonzero $\text{Re}(Y_{12})$ can be accounted for by introducing a gate-drain series resistance R_j. The exact solution of the equivalent circuit parameters from the Y-parameters is

$$R_j = -\text{Re}(1/Y_{12}) \quad -(8)$$

$$C_{gd} = [\omega \text{Im}(1/Y_{12})]^{-1} \quad -(9)$$

$$R_i = 1/(Y_{11} + Y_{12}) \quad -(10)$$

$$C_{gs} = [\omega \text{Im}(1/(Y_{11} + Y_{12})]^{-1} \quad -(11)$$

$$R_{ds} = 1/\text{Re}(Y_{12} + Y_{22}) \quad -(12)$$

$$C_{ds} = \text{Im}(Y_{12} + Y_{22})/\omega \quad -(13)$$

$$g_m = |(Y_{12} - Y_{21})(Y_{11} + Y_{12})/\text{Im}(Y_{11} + Y_{12})| \quad -(14)$$

7.5. Degradation Mechanism

The largest contribution to f_T degradation was found to come from a decrease in the peak RF g_m. The degradation worsens with frequency and reaches a maximum value at ~ 10 GHz.

In the InAs - AlSb system, a component of the DC g_m and ac g_m at low frequencies comes from the feedback of the impact ionization generated holes moving slowly through AlSb [9]. Fig. 48a shows the I_g-V_{gs} plot for a 100 nm gate length HEMT (V_{th} ~ −0.55 V). For

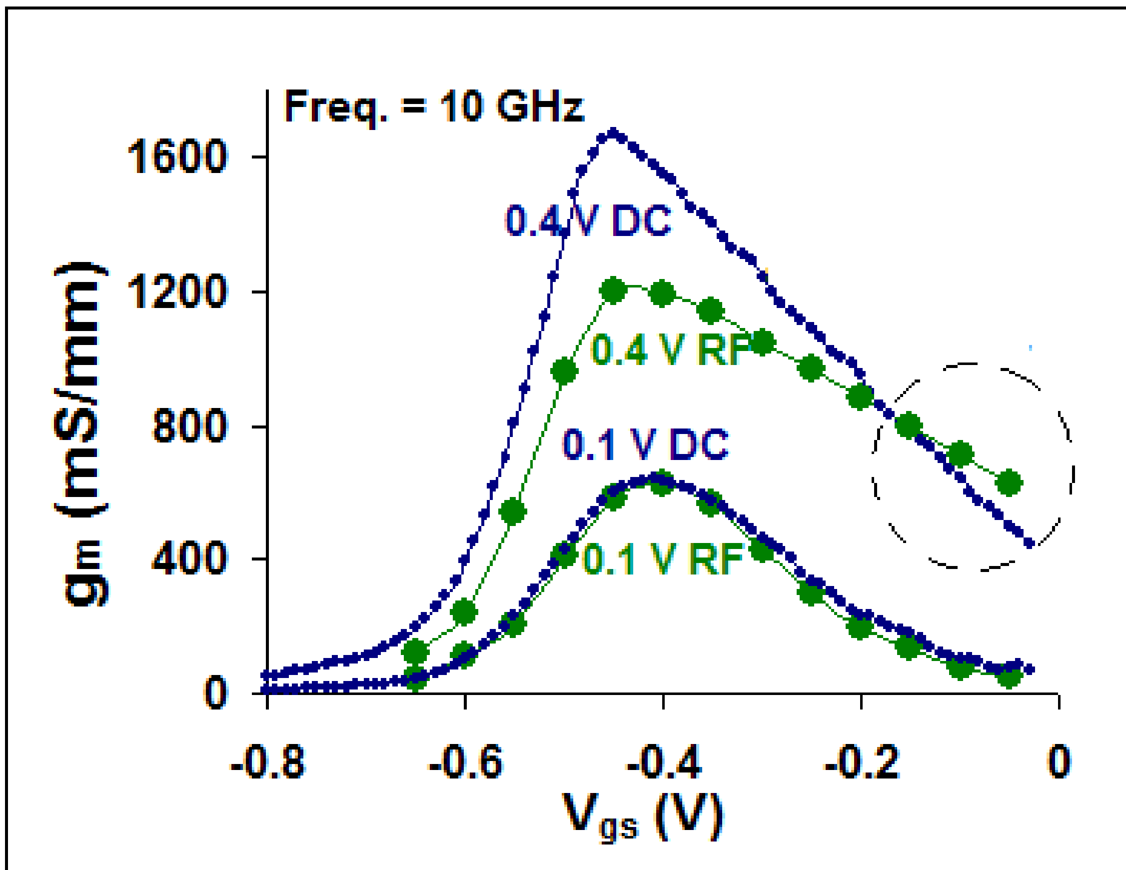

Figure 45. DC and RF g_m at 10 GHz. The effect of impact ionization adding to DC g_m up to peak impact ionization, and then reducing g_m, is evident. At high frequencies, generated holes fail to fully compete with the fast changing signal. The RF g_m is much less than the DC g_m for the increasing impact ionization regime. At less negative V_{gs}, the RF g_m approaches the DC g_m, and finally increases above it at V_{gs} ~ 0.2 V (dotted circle). At low V_{ds} (0.1 V), with negligible avalanche, this effect is absent.

most of the operating range of V_{gs}, holes in I_g are primarily derived from the channel impact ionization. For increasing negative V_{gs}, the vertical field under the channel increases, while the number of carriers in channel decreases. From $V_{gs} = V_{th}$ to ~ −0.3 V, the gate current increases as the impact ionization rate increases, due to a rise in the 2DEG density. Here impact ionization works in favor of gate control, increasing the DC g_m. From V_{gs} ~ -0.3 V to 0 V, I_g decreases as impact ionization in the channel drops due to smaller vertical fields in the channel under the gate. So, in this range, impact ionization works against gate control, decreasing the DC g_m [58,59].

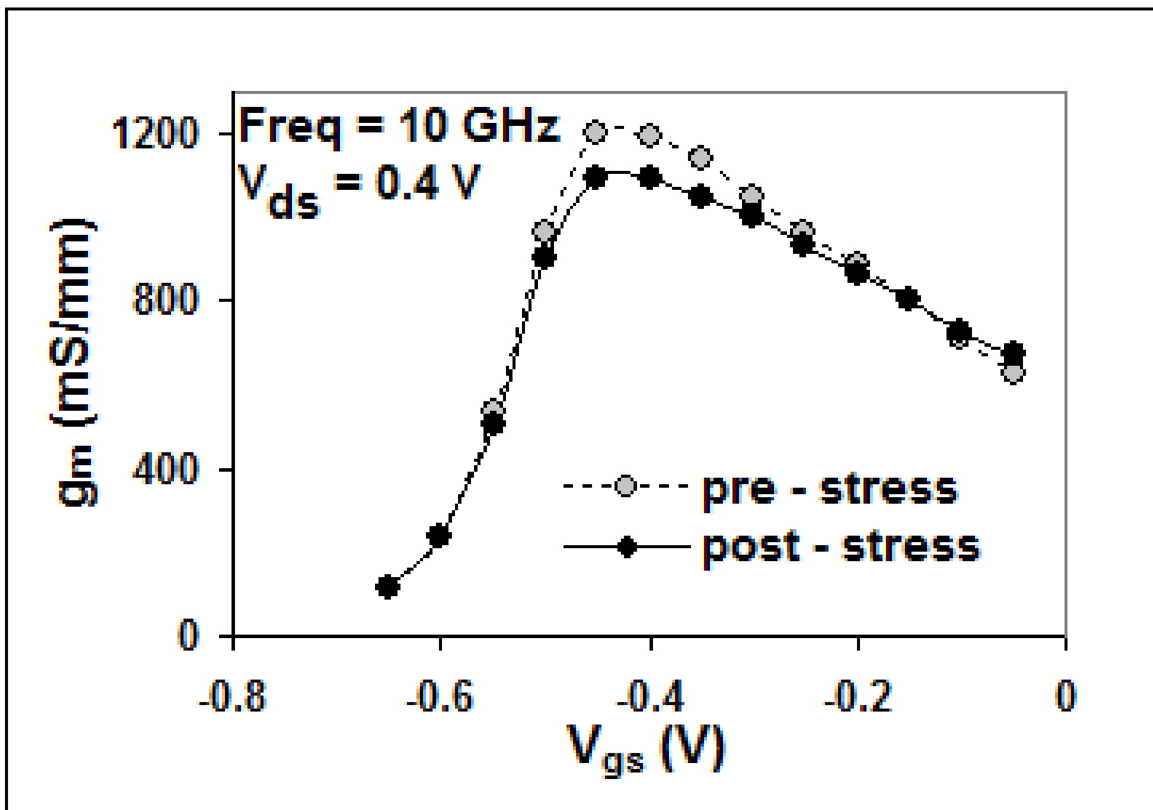

Figure 46. Pre and post-stress RF g_m, at 10 GHz. 'Flattening" of the RF g_m curve post-stress (similar to comparison between DC and RF in Fig. 45) indicates increased difficulty of removal of impact ionization generated holes.

In high frequency operation, the contribution of impact ionization is lost as the generated holes fail to keep up with the rapidly modulating gate signal. This leads to reduced RF g_m near the g_m peak. At less negative V_{gs}, the RF g_m approaches the DC g_m and finally increases above it at $V_{gs} \sim -0.2$ V, for high V_{ds}, as shown in Fig. 45 (region of increase marked with dotted circle). At low V_{ds} (0.1 V), with negligible avalanche, this effect is absent [10,59].

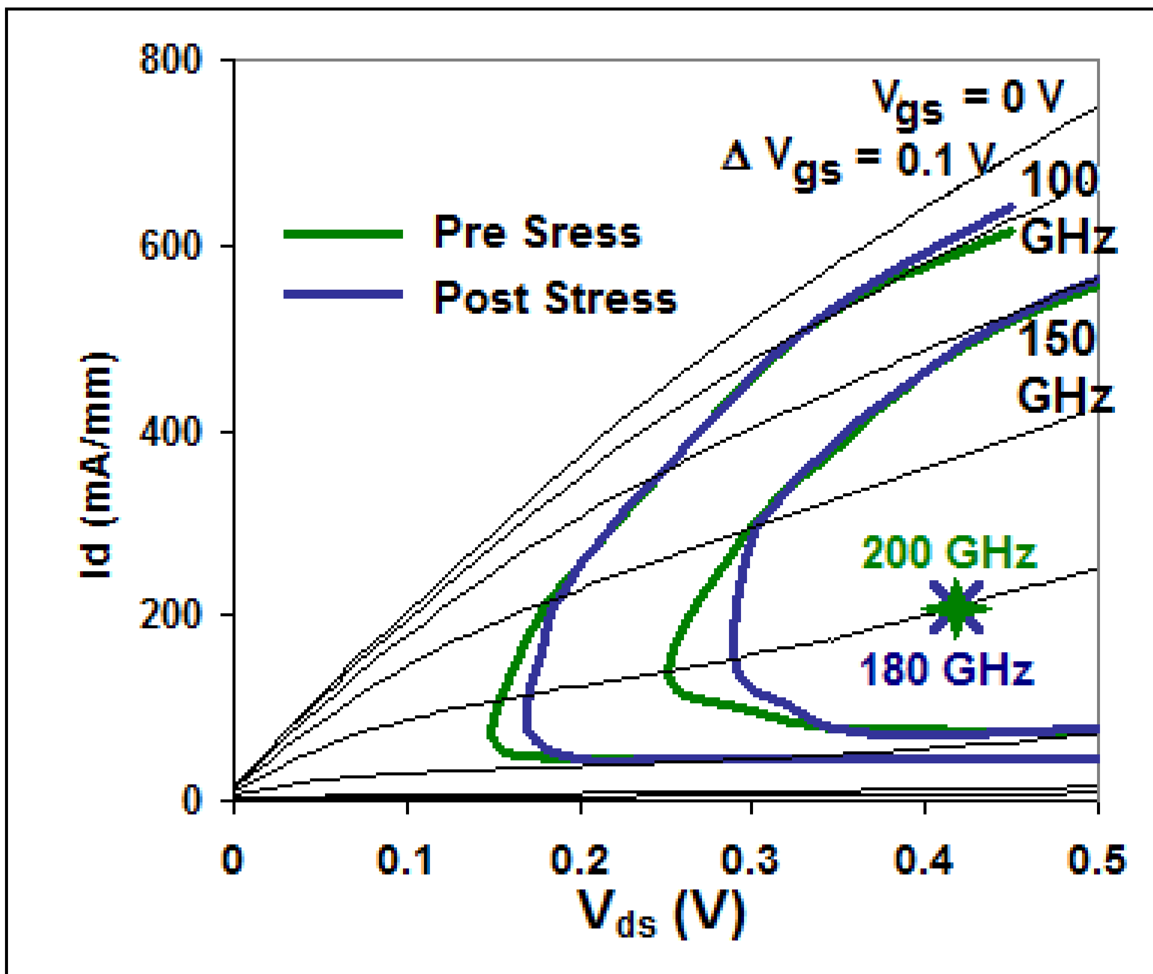

Figure 47. Pre and post-stress f_T contours for 100 and 150 GHz. The peak f_T shows trends consistent with the RF g_m degradation pattern. The gain decreases at high negative V_{gs} and high V_{ds}, leading to reduction in f_T . The increase in gain from RF g_m overtaking DC g_m is observed at high V_{ds} and $V_{gs} \sim -0.1$ V.

Fig. 46 shows pre and post-stress RF g_m at 10 GHz and $V_{ds} = 0.4$ V. The post-stress peak g_m decreases by about 10%. More importantly, the overall inductive “flattening” of the curve, similar to a transition from DC to RF operation, indicates the increased difficulty of avalanche generated holes in keeping up with the gate signal. This is also shown in the pre- and post-stress f_T contours for 100 and 150 GHz in Fig. 47. The gain decreases at large, negative V_{gs} and high V_{ds}, leading to a reduction in f_T. The increase in gain from the RF g_m overtaking the DC g_m is observed at high V_{ds} and $V_{gs} \sim -0.1$ V.

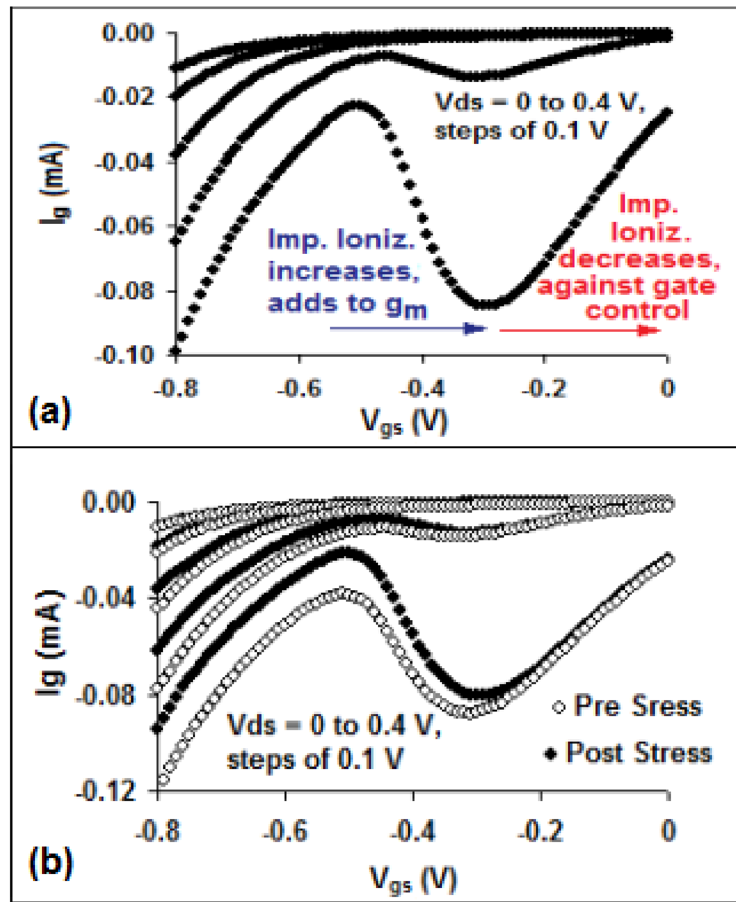

Figure 48. I_g of a 100 nm L_g shows the condition of maximum avalanche or hot carrier generation rate. From $V_{gs} \sim -0.5$ V to -0.3 V, increasing impact ionization helps to increase DC g_m. From -0.3 V to 0 V, decreasing impact ionization works against gate control to reduce DC g_m. b) Pre- and post-stress gate current. A reduction in gate current indicates poor hole removal.

The slowing down of avalanche-generated holes is supported further by a decrease in $|I_g|$. (Fig. 48b) The “flattening” of RF g_m and I_g reduction may be related to increased scattering of impact ionization generated holes. Fig. 49 shows pre and post-stress RF g_m variation with frequency at $V_{gs} = -0.4$ V, $V_{ds} = 0.45$ V. The degradation increases with frequency up to ~10 GHz. Stress-induced changes in phonon-assisted processes affecting energy relaxation times [25] could also be responsible for the observed slowness of the impact ionization process relative to the gate signal. Another possibility is the trapping of impact ionization generated holes at the cap-passivation interface on the source side – which would not affect DC charge control significantly – but inhibit the flow of holes to the gate or source considerably.

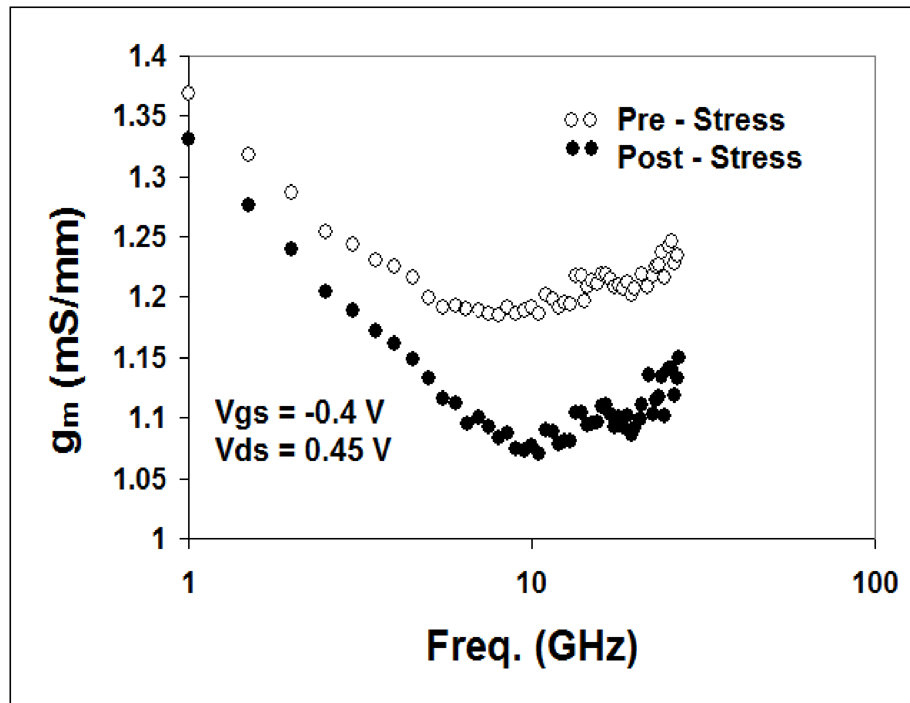

Figure 49. Pre and post-stress RF g_m variation with frequency at V_{gs} = -0.4 V, V_{ds} = 0.45 V. The degradation increases with frequency up to ~10 GHz. A post stress decrease in hole mobility in AlSb or increase in relaxation times associated with the InAs - AlSb quantum could potentially explain this behavior .

7.6. Post Stress Increase in Parasitic Capacitances

A comparison of the post-stress reduction in peak f_T and peak RF g_m at 10 GHz for all devices (Fig. 50) shows that f_T decreases more than g_m (as a percentage of the pre-stress value). While the reductions in f_T and g_m are almost the same (~ 9%) for a device with L_g = 100 nm and L_{dg} = 950 nm (L_{ds} = 2 μm), they are significantly different (f_T - 23 %, g_m - 15 %) for a device with L_g = 700 nm and L_{dg} = 650 nm (L_{ds} = 2 μm). Since $f_T = (1/2\pi)g_m / (C_{gs} + C_{gd})$ holds true for a first order approximation, this suggests some post-stress increase in C_{gs} or C_{gd} in devices with short access regions.

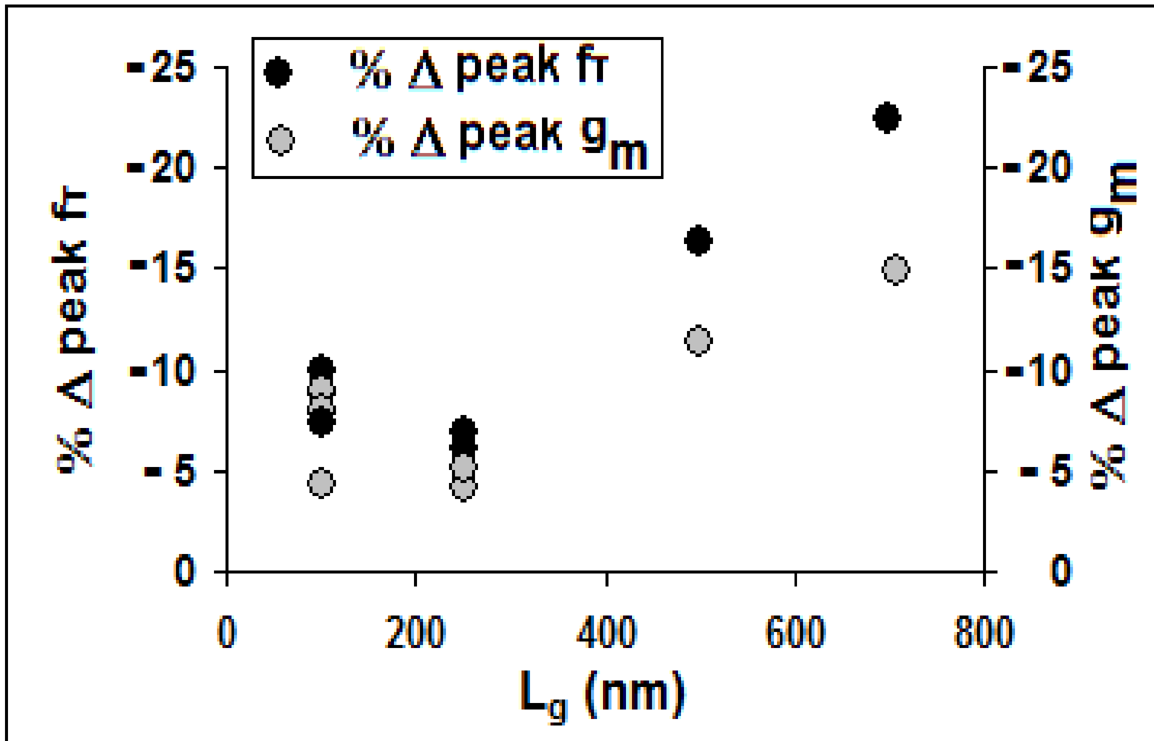

Figure 50. Post stress percentage reduction in peak f_T and peak RF g_m at 10 GHz. The decrease in f_T is more than the decrease in g_m, indicating some post stress increase in C_{gs} or C_{gd}, especially in devices with short access regions. L_{ds} = 2 μm for all devices.

7.7. Parasitic Capacitance Measurement

As mentioned earlier, pad capacitances and parasitic inductances from contacts were not de-embedded from our measurements. For this reason, the capacitance extracted from equations (9) and (11) will have some error from the pad capacitances. To consider how this error affects the capacitance measurement with frequency, let us consider a device with an intrinsic $y_{12} = a + jb$, measured Y_{12} and pad capacitance = C_{pgd}. The measured value Y_{12} will differ from the real value y_{12} by

$$y_{12} - Y_{12} = j\omega C_{pgd} \qquad -(15)$$

or,

$$Y_{12} = y_{12} - j\omega C_{pgd} = a + j(b - \omega C_{pgd}) \qquad -(16)$$

So by (9), the real value of $C_{gd} = [\omega \mathrm{Im}(1/ Y_{12})]^{-1} = -(a^2 + b^2)/b\omega = -(b/\omega + a^2/b\omega)$,

and the measured value from Y_{12} is given by $-[(b - \omega C_{pgd})/ \omega + a^2/(b - \omega C_{pgd})\omega]$

$$\text{or, } C_{gd,meas} = -[b/\omega - C_{pgd} + a^2/(b - \omega C_{pgd})\omega] \qquad -(17)$$

Thus, we find that an error equal to C_{pgd} is introduced as when capacitances are extracted using Y_{12}. However, this error is relatively small and has no frequency dependence. The

major frequency dependence of Y_{12} on C_{pgd} is introduced by the term $a^2/(b - \omega C_{pgd})\omega$, which differs from the real value $a^2/b\omega$.

It is important to understand the relative values of a and b over a range of frequencies. The value of a ($Re(Y_{12})$), the real part of gate to drain admittance, is significant at low frequencies, and much smaller at high frequencies. The value of b ($Im(Y_{12})$) follows the opposite of this trend, going from low values at low frequencies to high values at high frequencies. Thus, in a range of frequencies where the frequency is high enough such that b/ω is much greater than $a^2/b\omega$ or $a^2/(b - \omega C_{pgd})\omega$, the error in determining C_{gd} or C_{gs} is limited to C_{pgd}. Thus, our estimate of capacitances will be based on extraction of y-parameters from the measured s-parameter values at high frequencies.

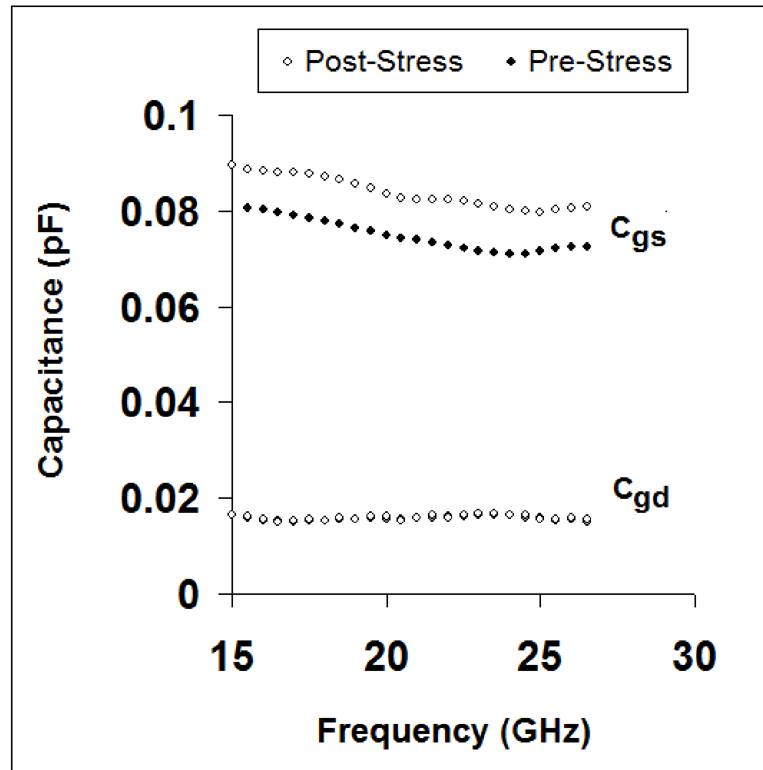

Figure 51. Extracted capacitances (C_{gs} and C_{gd}) pre and post-stress at the bias condition of peak f_T for a device with gate length 500 nm and S-D spacing of 2 microns. C_{gd} stays practically unchanged post-stress – unlike C_{gs}.

7.8 Pre- and Post-Stress C_{gs} and C_{gd}

Fig. 51 shows the extracted capacitances pre and post-stress at the bias condition of peak f_T for a device with gate length 500 nm and S-D spacing of 2 µm. Because of the bias conditions, C_{gd} is much smaller than C_{gs}. However, the comparison of pre- and post-stress values of C_{gd} and C_{gs} show that the increase in net parasitic capacitance comes almost entirely from C_{gs} rather than C_{gd}. Under the stress conditions, there are significant potential gradients to provide holes some extra energy towards the source side.

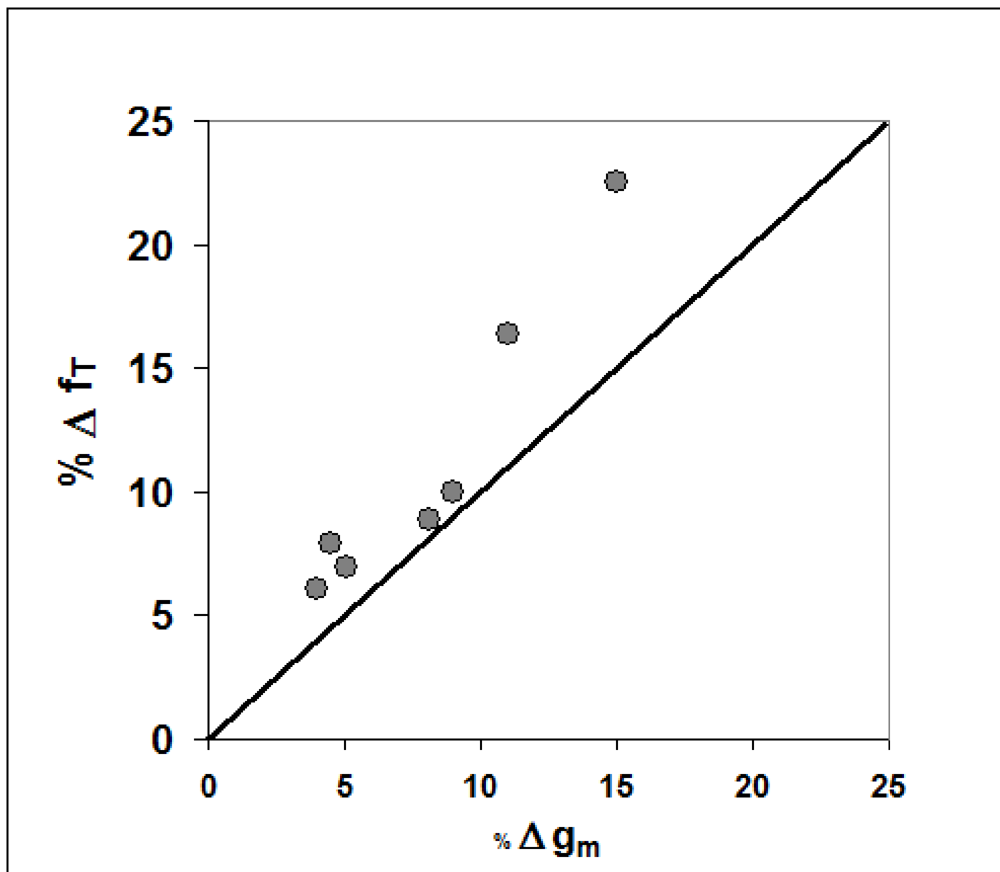

Figure 52. Percentage change in peak f_T plotted vs percentage change in g_m for the tested devices with 2 micron S-D spacing. The proximity of points to unit slope line gives the extent of correlation between the two quantities.

The increase in post-stress gate-to-source capacitance can be explained by the trapping of holes that escape from the channel and get trapped at the passivation-cap interface over the source-gate access region. Such traps would be expected to have some electrostatic effect on the access resistances if present anywhere in layers near the channel. Since the DC degradation is minimal, even at zero gate bias, the presence of these traps at the passivation-cap interface provides greater consistency with the experimental results.

7.9 Relative Contributions of g_m Reduction and Parasitic Capacitance Increase to Reduction of f_T

The relative contributions of fractional change in g_m and parasitic capacitances to the net f_T change are compared. The net reduction in transition frequency is clearly dominated by the reduction in RF g_m. The results in Fig. 50 show this to first order. Considering a simplified expression of f_T,

$$f_T = g_m/2\pi\ [(C_{gs} + C_{gd})^{-1} \qquad \text{-(18)}$$

one would expect that nearly equal percentage changes in f_T and g_m would imply negligible increase in $C_{gs} + C_{gd}$. The full delay expression of f_T , as shown in eqn. (3) is

$$f_T = g_m/2\pi\ [(C_{gs} + C_{gd})[1 + (R_d + R_s)/R_{ds}] + C_{gd}g_m(R_d + R_s)]^{-1} \qquad \text{-(3)}$$

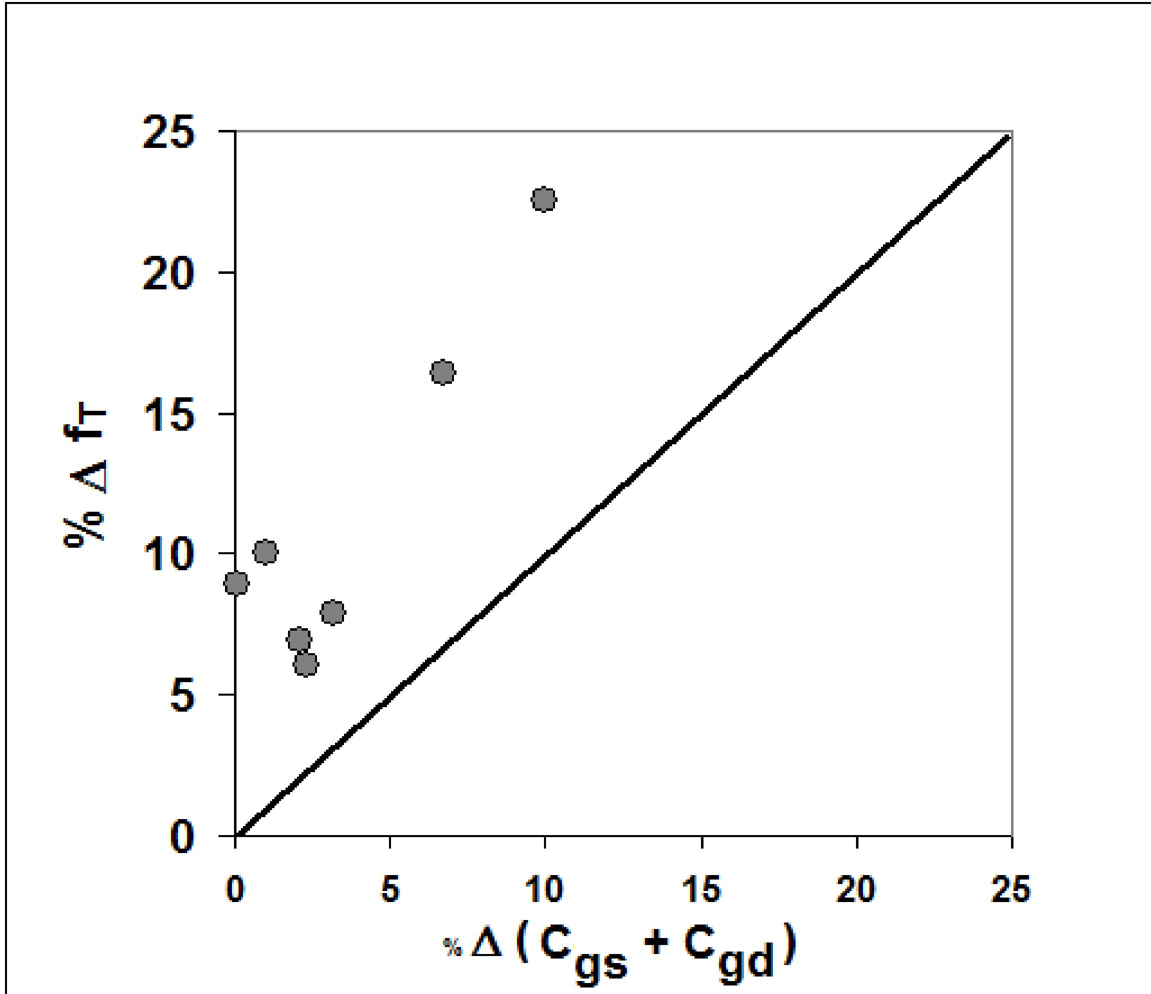

Figure 53. Percentage change in peak f_T plotted vs percentage change in (C_{gs} + C_{gd}) for the tested devices with 2 micron S-D spacing. Proximity of points to unit slope line gives the extent of correlation between the two quantities.

This would seem to imply that a reduction in peak g_m would tend to reduce the peak f_T, but not proportionally. A decreasing g_m would effectively reduce the coefficient of C_{gd} in the 2nd term of the denominator – effectively acting like reduced capacitance, tending to restore some of the reduction in the numerator of the expression. However, when the actual numbers are considered for an InAs - AlSb HEMT, the contribution of a 10 - 20% change in g_m introduces a change in the coefficient to C_{gd} that is only 1 - 10%. The smallness of C_{gd} compared to C_{gs} makes this an even smaller restoring factor to the

transition frequency. Fig 52 shows the relative changes in f_T and g_m. Fig 53 shows the same relative changes in f_T and the net capacitance $C_{gs} + C_{gd}$.

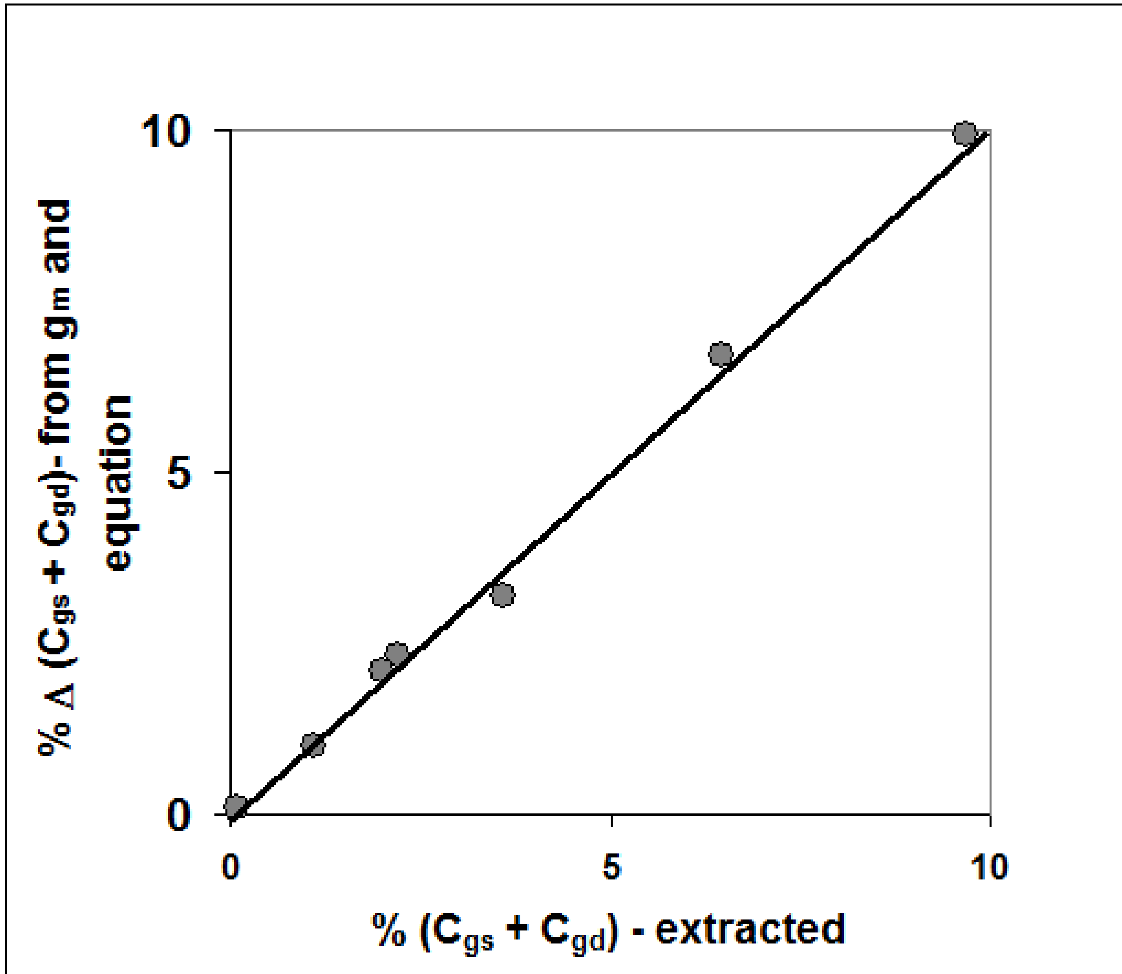

Figure 54. % change in ($C_{gs} + C_{gd}$) based on g_m degradation and eqn. (18) vs % change in ($C_{gs} + C_{gd}$) extracted from s-parameters for the tested devices with 2 micron S-D spacing. The proximity of points to a line of unity slope shows that eqn. (18) is fairly accurate for these HEMTs.

The straight line in Fig. 52 or 53 represents a unit slope. The aggregation of points much closer to the unit slope line for Fig. 52 than for Fig.53 shows the g_m degradation to have a much stronger correlation to the f_T degradation than the parasitic capacitance increase. Fig. 54 gives a similar comparison between the extracted capacitance and capacitance

measured by using g_m degradation and the first order expression of f_T. The closeness of the points to the unit slope line (especially for devices with short gate lengths) shows that the first order expression of f_T holds for the highly scaled InAs - AlSb HEMT up to a high degree of accuracy. This is consistent with the analysis in [21].

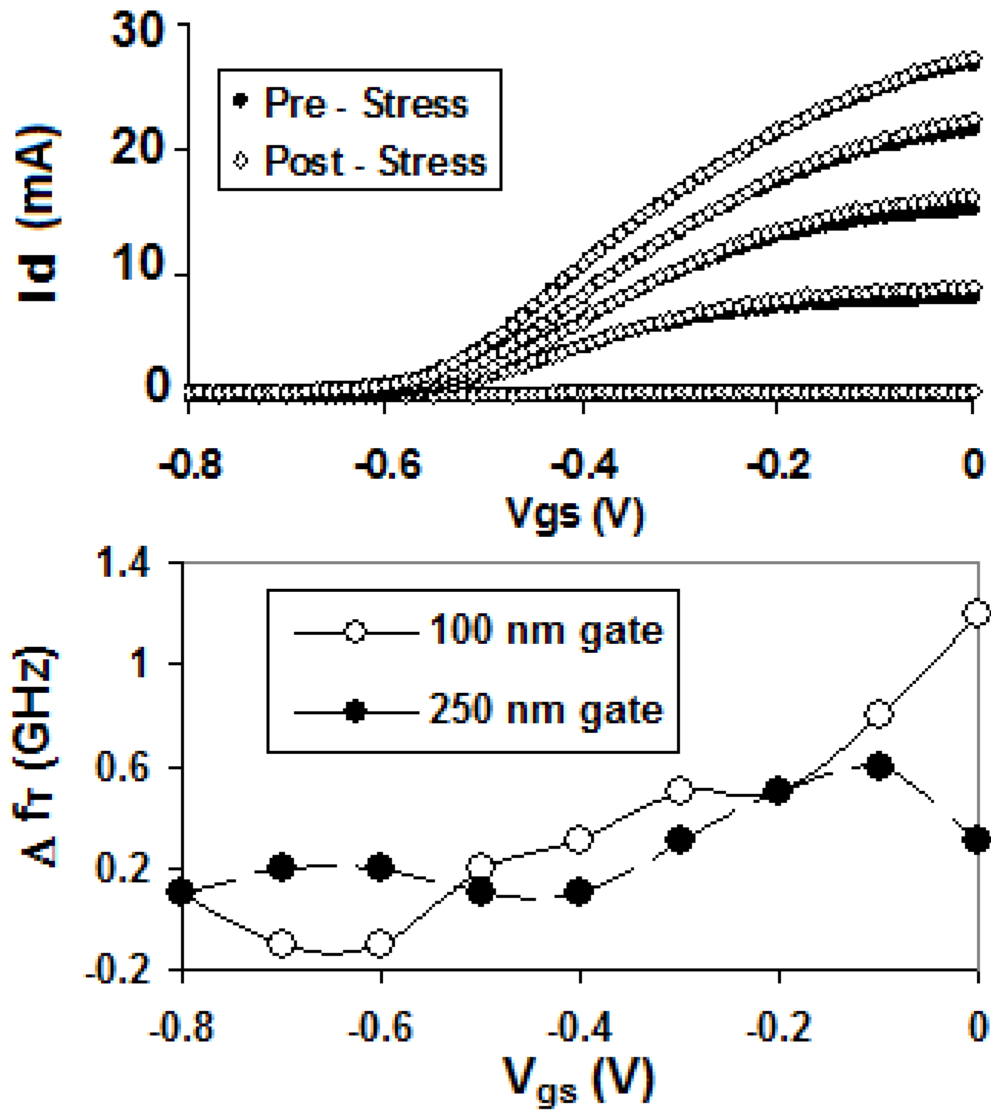

Figure 55. 2 × 20 μm HEMT with 100 nm gate length, stressed at high current (V_{gs} = 0, V_{ds} = 0.5 V, 3 h) showing a slight increase in drive current. Devices with 100 and 250 nm gates stressed similarly show very small increase in f_T.

7.10 High Current Stress and Small Signal Performance

To assess the effects of high current stress on small signal performance, some devices were stressed at zero gate bias and V_{ds} = 0.5 V for 5 hours. At the end of the 5 hour stress period, the devices showed a very slight improvement in drive current at the low gate biases, while the drain current at more negative gate biases stayed more or less the same. Fig 55 shows a slight post stress increase in the drain current near zero gate bias. As expected, the increased drive current results in a slight increase in f_T at low gate biases. However, the peak f_T, which happens near the transconductance peak, stays more or less unchanged, since there is no significant increase of drive current at the more negative gate biases.

7.11. Conclusion

InAs - AlSb HEMTs stressed with hot carriers exhibit negligible change in DC characteristics, but more than 20% degradation in peak f_T. Short access region lengths exacerbate the degradation. The degradation is related to various components of the small signal equivalent circuit of the HEMT, which is extracted from the measured s-parameters. The degradation is attributed primarily to a reduction in peak RF g_m, as well as post-stress increase in parasitic capacitances. RF g_m degradation increases with frequency, reaching a maximum value at ~ 10 GHz. The RF g_m reduction is investigated further as a function of gate and drain bias. This shows a post-stress slowness of the impact ionization process relative to the gate signal to be the major cause of g_m

degradation. The g_m reduction almost entirely explains the f_T degradation in the shorter gate length devices. The devices with longer gate lengths and short access region lengths, in addition to the g_m reduction, show a significant increase in gate-to-source capacitance after stress, while the gate-to-stress capacitance remains almost unchanged. The increase in gate-to-source capacitance could potentially be explained by trapping of holes in the passivation or at the cap-passsivation interface over the gate-source access regions.

Devices are also stressed at high current conditions. At high currents, devices exhibit some increase in the current near zero gate bias, but negligible changes in small signal performance.

CONCLUSION

InAs - AlSb HEMTs, which are strong candidates for extremely power efficient high-speed RF technologies, are studied for reliability under hot carrier or high impact ionization conditions. A significant fraction of HEMTs exhibit degradation under hot carrier stress. Degradation is manifested as a shift in the transconductance peak toward more negative gate voltages, with no mobility degradation, indicating the activation of new donor defects or deactivation of existing acceptors in the AlSb layers flanking the channels. Devices with large-magnitude threshold voltages and those with long gate lengths exhibit very little degradation, indicating the role of hot carriers. The defects anneal out within a few days. The I_d-V_{ds} trends and gate current magnitudes point to the existence of a metastable deep acceptor state that is modified by hot carriers. Density Functional Theory calculations of the energetics of substitutional and interstitial oxygen show metastable states consistent with the degradation trends. The defects satisfy the basic trends of threshold voltage shifts towards more negative voltages under stress. The calculated defect energies are also consistent with the strong dependence of degradation on the threshold voltage of the unstressed devices. Other physically abundant impurities like carbon and tellurium forming defects with metastable configurations as well as known native defects with metastable states are considered. The energies of these defects show that they are unlikely candidates for the observed degradation. The analysis can be considered as part of a general method to estimate the importance of a given defect in the reliability of a device under stress.

While a majority of HEMTs exhibit no measurable DC degradation under hot carrier stress within a short period of time, almost all HEMTs show significant degradation in small signal performance – in some cases more than 20% degradation in peak f_T. The degradation is related to various components of the small signal equivalent circuit of the HEMT, which is extracted from the measured s-parameters. The degradation is attributed primarily to a reduction in peak RF g_m, as well as a post-stress increase in parasitic capacitances. RF g_m degradation increases with frequency, reaching a maximum value at ~ 10 GHz. The RF g_m reduction is investigated further as a function of gate and drain bias. This shows a post-stress slowness of the impact ionization process relative to the gate signal to be the major cause of g_m degradation. The g_m reduction almost entirely explains the f_T degradation in the shorter gate length devices. The devices with longer gate lengths and shorter access region lengths show a significant increase in gate to source capacitance after stress, in addition to the g_m reduction, while the gate-to-source capacitance remains almost unchanged. The increase in gate-to-source capacitance could potentially be explained by trapping of holes in the passivation or at the cap-passivation interface over the gate-source access regions.

APPENDIX

A1. Effect of Operation at High AC Power

For any RF device – meant to be used as an amplifier component – the large signal response and operational stress are metrics of primary importance. A large signal setup delivering power at a low enough noise level in the range required to drive a single low power HEMT is difficult to achieve. Earlier large signal studies on the InAs - AlSb HEMTs have been limited to measurements where multiple amplifier stages are cascaded to increase the power requirement to levels that could be delivered by the available large signal setup [60]. Even after cascading stages – the presence of noise is evident in the measurements (Fig.A1).

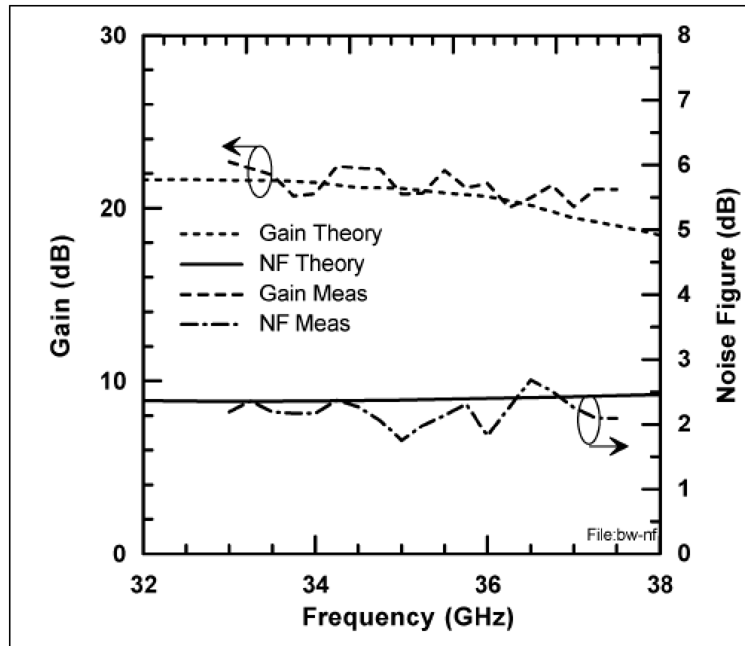

Figure A1. Measured noise figure and associated gain of the ABCS LP-LNA compared with the theoretical prediction from circuit model [60].

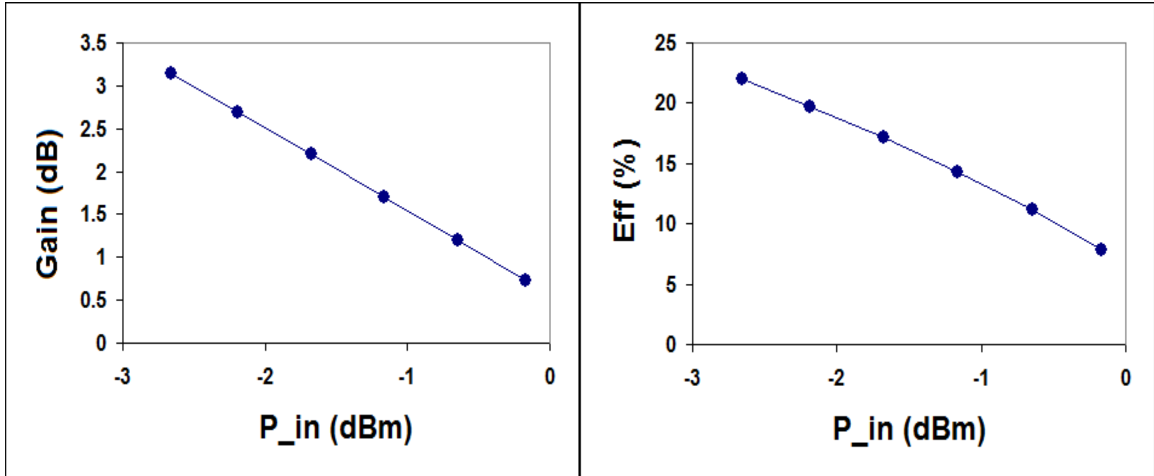

Figure A2. Gain and power added efficiency for a 2 × 20 micron InAs - AlSb HEMTs (100 nm gate length). A 50 Ohm loadline at V_{ds} = 0.35 V and V_{gs} = -0.4 V was chosen.

Some AC power sweeps were performed on the InAs - AlSb HEMTs described in this thesis. There being no definite knee voltage point within the usable range of the HEMT, a 50 Ohm load line was chosen. This quiescent point was chosen at V_{ds} = 0.35 V and V_{gs} = -0.4 V. This gate voltage was chosen to increase gate power dissipation – so as to maximize the chances of finding the peak efficiency input power level. For the same reason – we chose a device with very high starting gate leakage (peak I_g ~ 55 mA/mm at V_{ds} = 0.4 V).

Fig. A2 shows the results from the power seeps –which were performed between –2.6 to 0 dBm. As expected – there is a steady reduction in gain – which indicates that the device was in heavy gain compression at the -3 dBm point. Based on gain and peak P_{AE} conditions in [60], individual InAs - AlSb HEMTs could be expected to have peak P_{AE} at roughly -12 dBm (or even less for devices with good current drive) – so the heavy gain compression of the measured range is entirely expected. The power sweep was employed only once.

Heavy degradation of the device (and possibly faliure) was expected due to driving the gate at such high power. Very surprisingly – the sweepat high power greatly improved device characteritics. The peak gate current was reduced by more than a factorof 4. In the cases explained earlier – where gate current decreases following stress – the reduction is small – typically not more than 10 - 20 %. This was by far the biggest reduction in gate current post stress for any of the experiments performed by us. The peak transconductance also improved by ~ 10%.

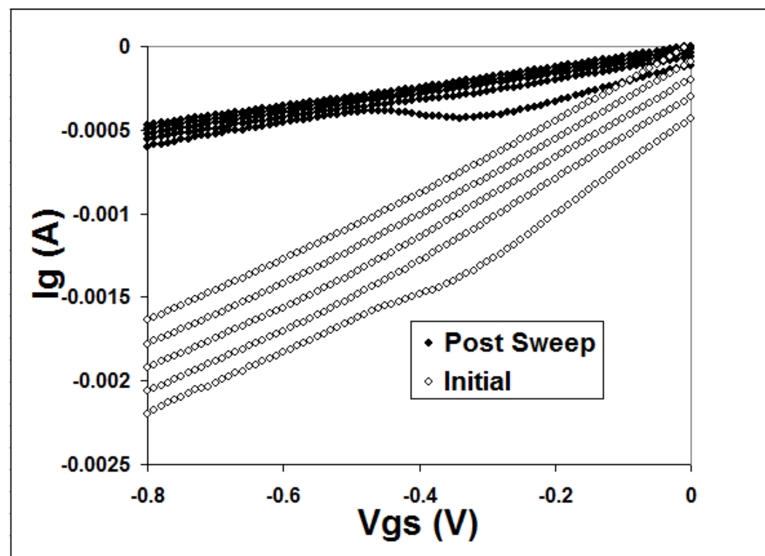

Figure A3. Large reduction in gate current for devices in Fig. A2 after power sweep.

The study could not be completed due to time and equipment constraints. However – the improvement in performance under high AC power conditions is very significant and is worth a detailed and complete investigation. Earlier studies have suggested significant defect passivation in AlGaN/GaN HEMTs driven into AC power compression [61]. This could potentially be a method of improving some devices with poor starting characteristics.

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