CHARACTERIZATION OF PROMPT DOSE- AND PULSED-LASER-INDUCED TRANSIENT PHOTOCURRENT FROM INTEGRATED CIRCUITS USING THE ON-CHIP PHOTOCURRENT MEASUREMENT CIRCUIT

By

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CHAPTER 1

Introduction

The impact of radiation on semiconductor microelectronics has been studied for over 50-years, with some of the first reported space radiation effects in metal-oxide-silicon (MOS) transistors appearing in nuclear science literature from 1964 [1]. This discovery transpired during the apex of the 20th century *Space Race*, which drove incredibly coordinated efforts to characterize the radiation response of microelectronic circuits for use in space [2] [3]. These efforts determined that radiation-induced failure mechanisms in microelectronics were diverse and multivariate. The earliest findings indicated that semiconductors were vulnerable to high-energy, high-speed ionizing energy sources that induce transistor-level perturbations at the sub-microsecond-scale [2] [3] [4] [5] [6] [7] [8] [9]. Semiconductors were also found to be vulnerable to accumulation effects that degraded the integrity of silicon and oxides through trap impurity build-up and damage to crystalline lattice structures [2] [3] [10] [11] [12] [13] [14]. Over many decades, these radiation effects were classified and standardized by the radiation effects community, which has enabled coordinated radiation testing procedures and heightened specificity for analysis of sub-categorical effects [15] [16] [17].

In tandem with the discovery of radiation vulnerabilities was the conception of radiation-hardening efforts [18] [19] [20] [21] [22] [23], which sought to protect microelectronics from both transient ionizing radiation and accumulation effects through improvements to technology processes or use of complex circuit elements. Early efforts to harden microelectronics in the 1960's has advanced significantly and is known as Radiation-Hardening-by-Design (RHBD). Over these many decades, RHBD models and techniques have closely followed technology and process-

dependent radiation effects. The majority of these effects are driven by Moore's law scaling of integrated circuits [17] [24]. Driven by industry, Moore's law has been observed since 1971, stating that the number of transistors on an IC will double every two years. ICs in the 1960's housed transistors in the thousands; today, ICs house transistors in the tens-of-billions [17] [24]. In addition to device scaling, which significantly impacts radiation-sensitive volumes and dimensions, various topological innovations of device structures have introduced intrinsic weaknesses and resiliencies to radiation effects that were not relevant in older generations of transistors. As such, the demand for RHBD is invariably present, and RHBD efforts are continuously following the next generation of ICs.

Apace with Moore's law scaling comes the development of radiation detection techniques so that the response of any particular technology or circuit is well-understood. This critical understanding of radiation effects supplies RHBD engineers the necessary information to assess probability of failure and estimated survival time in several applications, such as space, military, or even terrestrial radiation environments. In addition, insight into error rates and failure probability enables designers to either verify or update both physics-based radiation simulation tools [25] [26] [27] [28] and compact circuit simulation models [29] [30] that are used in conjunction with advanced circuit simulation software [31] [32] [33] to mimic radiation environments. The ability to perform such reliability checks with data-verified models is especially attractive since it is often a speedy and inexpensive solution to determine the reliability of a design before significant commitment to silicon fabrication. RHBD modelling efforts have even been shown to predict the radiation response of future technologies that were still under development, potentially closing the gap to the next generation of ICs. However, verifying the radiation response of a particular technology is unconditionally necessary. If the radiation response of a particular

technology or circuit is not documented, RHBD efforts become challenging, if not impossible, as simulation results are not based on verifiable data and could be incomplete or inaccurate.

Pertaining to prompt dose-induced photocurrent, characterization has been performed in the past to much success [8] [9] [23] [34]. Traditionally, P-Intrinsic-N (PIN) diodes are placed in line of sight to the radiation source in order to monitor the transient photocurrent response and keep a record of each radiation event. At the same time, a device under test (DUT) is placed in-line of the PIN diode such that the response of the DUT is recorded in parallel. While the photocurrent response of the PIN diode is simple to monitor with devices such as an oscilloscope, the response from the DUT varies from technology to technology, often requiring current-transformer (CT) probes or voltage measurement across sense resistors in order to isolate photocurrent from noise. Such a setup has enabled characterization of transient photocurrent generated in MOS transistors and the ability to identify radiation thresholds which induce failure in particular devices. In addition, it has supplied researchers the ability to form accurate transient photocurrent models [29] [34] [35] [36].

However, characterization of photocurrent has become increasingly more difficult as these technology feature sizes decrease. Prompt dose-induced photocurrent transients manifest in transistors at a timescale that is proportional to the duration of irradiation, which is often a sub-microsecond period [8] [9] [29] [34]. Transients with sufficiently low amplitude within such a period are unmeasurable off-chip due to a combination of signal-to-noise (SNR) ratio limitations and intrinsic impedance of on-chip transmission lines (See **Appendix IV)**. In sub-50nm silicon-on-insulator (SOI) technologies, this problem is more apparent; depletion regions are isolated from the substrate by a buried oxide, which significantly reduces the amplitude of drift photocurrent [34] [37] [38] [39] [40]. Because of this limitation, there is a noticeable absence of transient

photocurrent measurement data from modern integrated circuit transistors. Recent radiation test vehicles have focused on survivability, characterization of rail span collapse [41] [42] [43], and the response from electrostatic discharge (ESD) diodes [44] [45] [46] [47]. While a "pass or fail" experiment is useful for chip-by-chip reliability assurance, and current transients from power supplies and ESD diodes provide some insight, lack of data regarding device-level failure mechanisms is problematic for RHBD. Such testing would require all candidate technology nodes and designs to be irradiated in a prompt dose environment, and little-to-no insight into device-level photocurrent models could be created.

Work performed in [48] [49] [50] [51] has determined a method to resolve this limitation through on-chip measurement of current transients with high-speed mixed-signal circuitry, dubbed the photocurrent measurement circuit (PMC). The PMC is an on-chip integrated circuit, designed for technology-agnostic portability, and is capable of converting leakage-level photocurrent transients into digital data that contains the transient information of the signal. The PMC is also resistant to prompt dose and total-ionizing-dose (TID) effects to ensure both the transient response and degradation of measurement circuitry will minimally impact recorded data.

The PMC has been designed and fabricated in two technologies nodes: 22nm fully-depleted SOI (FD-SOI) and 45nm partially-depleted SOI (PD-SOI). Additionally, the PMCs have been tested at several radiation test facilities, including a linear accelerator (LINAC), flash x-ray (FXR), and a neodymium-doped yttrium lithium fluoride (Nd:YLF) diode-pumped Q-switched laser that is used to simulate the prompt dose radiation environment. Data acquisition at these test facilities was successful and shows the efficacy of the PMC design.

Dissertation Organization

Chapter II of this dissertation begins with an overview of primary and secondary photocurrent generation mechanisms and makes a comparison between these mechanisms in bulk, PD-SOI, and FD-SOI technology nodes. Additionally, discussion of the various transistor targets in the PMCs from both technology nodes is included. **Chapter III** details the technology-agnostic design of the PMC, how on-chip data collection is performed, and what considerations were made when integrating the PMC in both 22nm FD-SOI and 45nm PD-SOI. This chapter also includes self-test results in the form of recorded data, which demonstrates the linearity of the on-chip design. **Chapter IV** describes the various test facilities that the PMCs were experimented at and covers the infrastructure and experimental setup of the PMC. Data recorded at the various test facilities is presented in **Chapter V**, where results are discussed and compared. 3D technology-computer-aided-design (TCAD) results are shown in **Chapter VI**, where the unique effects observed in **Chapter V** were able to be corroborated with physics-based simulation. Schematic-level simulation is performed **Chapter VII**. 45nm PD-SOI designs in this work were created in Cadence Virtuoso, where simulations of applicable sections of the PMC are performed. Conclusions are covered in **Chapter VIII,** where the significance, implications, and potential use cases of the novel PMC design are discussed. The appendices document supporting information and significant findings from this work. **Appendix I** details the target arrays and target array variants available in both 22nm FD-SOI and 45nm PD-SOI implementations of the PMC. The results of in-house operational self-tests performed on both PMC variants are included in **Appendix II**. A summary of all tests performed at the ND:YLF pulsed laser and FXR is discussed in **Appendix III**. A summary of the tests performed at the LINAC are also included in this chapter for reference. However, these tests do not correspond to any transient photocurrent measurement

results in this work due to EMI effects. **Appendix IV** includes discussion and simulation results for the propagation and attenuation of transient photocurrent through on-chip transmission lines and parasitic-extracted structures. **Appendix V** covers EMI effects captured at the LINAC and FXR with discussion for potential obfuscation of data from these sources. **Appendix VI** details how the on-chip voltage sampler protects sensitive data from analog-to-voltage converter loss of operation during irradiation. Lastly, **Appendix VII** is a compilation of the layouts and schematics from designs utilized in the PMC.

CHAPTER 2

TRANSIENT PHOTOCURRENT AND TARGETS

Transient Photocurrent Generation Mechanisms

In all integrated circuits, photocurrents result from electron-hole pair (EHP) generation through energy deposition from photon-based radiation [6] [9] [34] [35]. Photocurrent is commonly associated with the low-amplitude current from photosensitive devices, such as solar panels. In this context, the intended radiation source is natural sunlight. In the context of radiation effects, radiation sources are high power, and undesirable photocurrents are generated in devices not intended to be photosensitive. Such radiation sources include x-ray sources, gamma ray sources, and sub-ultraviolet (UV) laser systems. For ionizing radiation such as gamma rays, on average, every 3.6 electron-volts (eV) of energy will produce a single EHP in silicon [6] [9] [34]. This mechanism is different for non-ionizing sub-UV lasers. Deposited energy must only surpass the bandgap of silicon (1.08 eV) to generate an EHP [6] [52] [53]; the pulsed infrared laser in this work creates photons with energies of 1.17 eV and generates EHPs close to 100% quantum efficiency, i.e., one EHP per photon [6] [46] [52] [53] [54].

Device-level photocurrent resulting from EHP generation is a combination of both drift and diffusion current, often referred to as primary photocurrent [9] [34] [37] [38], and activation of parasitic devices that enhance primary photocurrent, known as secondary photocurrent [9] [34] [37] [38]. In addition, transient threshold voltage shifts from back-gate diode perturbations are possible. Although transient threshold voltage shift is not a primary or secondary photocurrent effect, the resulting current is comparable to transient photocurrent.

In diodes, bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), the electric field is within the depletion region of the device, where EHPs manifest at the circuit-level as drift current [9] [34] [37] [38]. The sensitive drift current volumes of an integrated circuit diode, NPN BJT, and NMOS, are shown in Figure 1(a) and (b) and Figure 2(a). Outside the depletion region, EHPs will diffuse [9] [34] [37] [38]. In positively-doped regions, minority carrier electrons spread out until they enter a region of conduction to form diffusion current, unless the carrier lifetime expires, in which case they recombine [34]. The same is true for holes in negatively-doped regions. The average distance electrons or holes will travel before recombination is known as a diffusion length, which is the square root of the diffusion current coefficient in n- or p-type silicon multiplied by the minority carrier lifetime [34]. This distance is typically tens of microns long. For bulk devices such as the transistor in Figure 2(a), diffusion current from the substrate is significant and may dominate the primary photocurrent response. However, SOI devices [55] have a buried oxide (BOX) between the substrate and channel, eliminating diffusion current from the substrate. Because of the structural differences between bulk and SOI, their transient photocurrent responses are distinct [34] [37] [38].

Two version of sub-50nm SOI are featured in this work. One version is 45nm partially-depleted SOI (PD-SOI), shown in Figure 2(b). In PD-SOI, some of the doped silicon above the BOX remains undepleted, forming a quasi-neutral (QN) region. If this QN region is left floating, secondary photocurrent may be generated through parasitic BJT current amplification [56] [9] [34] [37] [38]. The N-QN-N region of Figure 2(b) forms a parasitic BJT with a floating base. EHPs generated in the base is equivalent to a base current, which will be amplified if voltage on the base activates the parasitic BJT. 45nm PD-SOI allows for body-ties in some of its transistors, which is an effective way to prevent such parasitic BJT activation.

Another technology featured in this work is 22nm fully-depleted SOI (FD-SOI), shown in Figure 2(c). The channel in FD-SOI is thin enough that the entire channel is depleted. Theoretically, FD-SOI is dominated by the drift current portion of primary photocurrent, as there is no region for a parasitic BJT to form and diffusion current from the substrate is isolated. However, 22nm FD-SOI features an optional, conventional-well back-gate that allows designers to modulate the threshold voltage of transistors by applying back-gate voltage bias to an isolated p-well. This design is seen in Figure 2(d). The wells under the transistor form a diode that is comparable to the structure in Figure 1(a), and diodes such as these are highly susceptible to photocurrent effects. Any positive voltage on the isolated p-well will consequently decrease the threshold voltage of the n-type MOS (NMOS) above, increasing leakage current or even activating the device.

Photocurrent Targets

The transistor variants in this work are grouped together in large parallel arrays and referred to as transistor "targets." Each target exists to investigate the impact of primary and secondary photocurrent effects based on device dimension (width and length), type (NMOS or PMOS), and variant (with or without back-gate or body-tie). The number of parallel arrays within a target can be varied through transmission-gating, which enables scaling of the transient photocurrent response. Careful circuit design analysis was performed to ensure that the transmission gates tied to these targets have minimal impact on transient photocurrent measured from the transistors. A complete list of the transistor targets in both the 22nm FD-SOI and 45nm PD-SOI PMCs is provided in Table A-1 and Table A-2 in **Appendix I**, and layouts of targets in both technologies are shown in **Appendix VII**. How transient photocurrents from these targets are isolated and measured will be shown in the next section.

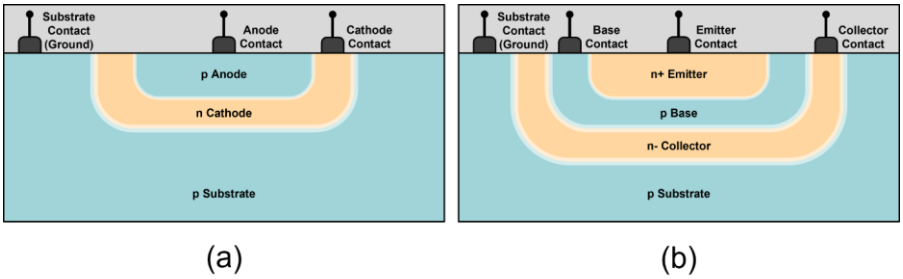

Figure 1 – Illustration of an integrated circuit diode (a) and NPN bipolar junction transistor (b). Depletion regions are represented by the brightened spaces between n-wells and p-wells. Dopants are laid upon a p-type substrate, which creates an additional depletion region between the bottom-most n-well and substrate.

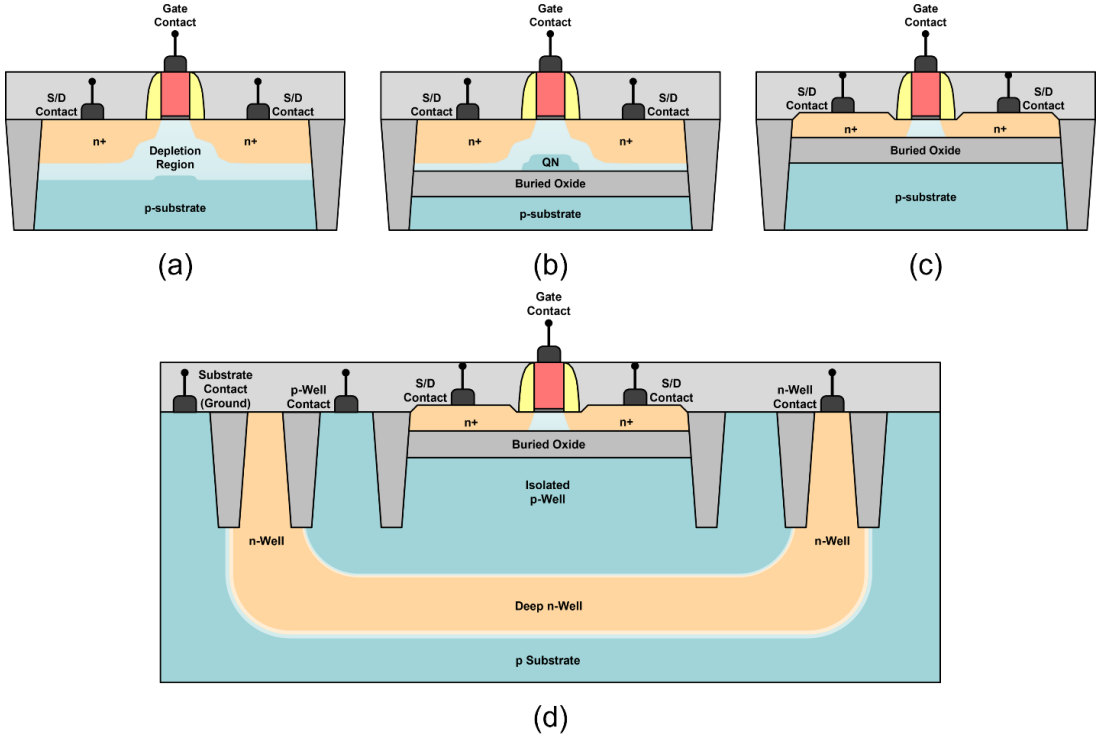

Figure 2 – Illustration of an integrated circuit bulk NMOS (a), partially-depleted SOI NMOS (b), fully-depleted SOI NMOS without a conventional well back-gate (c), and fully-depleted SOI NMOS with a conventional well back-gate (d). Depletion regions are represented by the brightened spaces between n-wells and p-wells. Isolation of the substrate from the channel produces a quasi-neutral (QN) region that is not depleted (b). In (c), the channel is thin enough that this QN region does not exist. The conventional well back-gate enables threshold voltage adjustment through application of a voltage to the p-well contact. Voltages on the conventional well must not forward-bias the diodes produced by the back-gate n- and p-wells.

CHAPTER 3

PMC DESIGN AND SELF-TESTS

Assumptions for On-Chip Measurement

The measurement techniques employed in this work operate under several assumptions when used in the on-chip transient photocurrent environment. The first of these assumptions is that transient photocurrent generated in the transistor targets have a sufficient magnitude such that photocurrents generated in the measurement circuitry are negligible. This assumption is key to operation of the PMC, as the measurement circuitry itself is a photocurrent "target" and will inevitably generate some level of unwanted photocurrent. For this reason, the targets in Table A-1 and Table A-2 allow transistor parallelization in the thousands of transistors. Photocurrent collection volumes in the measurement circuitry are at most equivalent to tens of transistors in these targets, which ensures minimal measurement error. The second assumption is that measurement circuitry, including both digital and analog subcircuits, will not lose operation during irradiation. For digital circuitry, if transistor-level photocurrents are capable of inducing digital errors, the PMC will fail. The level at which digital circuits fail, which is determined by technology node and transient energy, sets the upper bound for which the PMC can operate as a viable on-chip measurement technique. Analog circuitry, such as current mirrors and operational amplifiers (op amps), is a weaker link than digital circuitry. The PMC heavily utilizes current mirroring and op amp-buffering techniques in order to replicate currents and voltages to various nodes of the circuit for measurement. For this reason, analog components are designed over-specification to ensure linearity while transient photocurrents are generated within the circuits. Additionally, radiation-aware hardening techniques are employed to reduce sensitive depletion regions in analog

circuitry. Transient photocurrent simulations are run on these analog devices to verify survivability even in the harshest radiation environments. The third and final assumption is that indirect measurement of transient photocurrent is sufficient for characterization. It is preferrable to directly measure the continuous photocurrent, such as the transient from a CT probe, yet the low-amplitude nature of transient photocurrent in SOI eliminates this possibility. Instead, a compromise is made with the PMC: the linear nature of metal capacitors is leveraged to extract current from fundamental capacitor equations. The integral of current, which is the voltage on the capacitor, is the signal that the PMC directly measures. The equations that represent this measurement are covered in "PMC Data Acquisition."

Design of the PMC

The technology-agnostic design of the PMC is sectioned into isolated functional blocks, each of which has standardized inputs and outputs. The high-level view of this design is shown in Figure 3, which is comparable in both the 22nm FD-SOI and 45nm PD-SOI implementations of the PMC. As discussed previously in this section, the **Photocurrent Arrays** within the **Photocurrent Target** are used to scale the amplitude of transient photocurrent to levels which minimize the effects of the measurement circuitry. In addition to scaling photocurrent, this section of the PMC also scales leakage current, enabling self-testing. After the **Amplification Stage**, leakage and photocurrent is mirrored into the **Integration Stage**, where the **Integrator** converts total current into a periodic and continuous voltage waveform. Two variants of this waveform exist based on the specific **Integrator** variant, where current is converted into either a sawtooth or

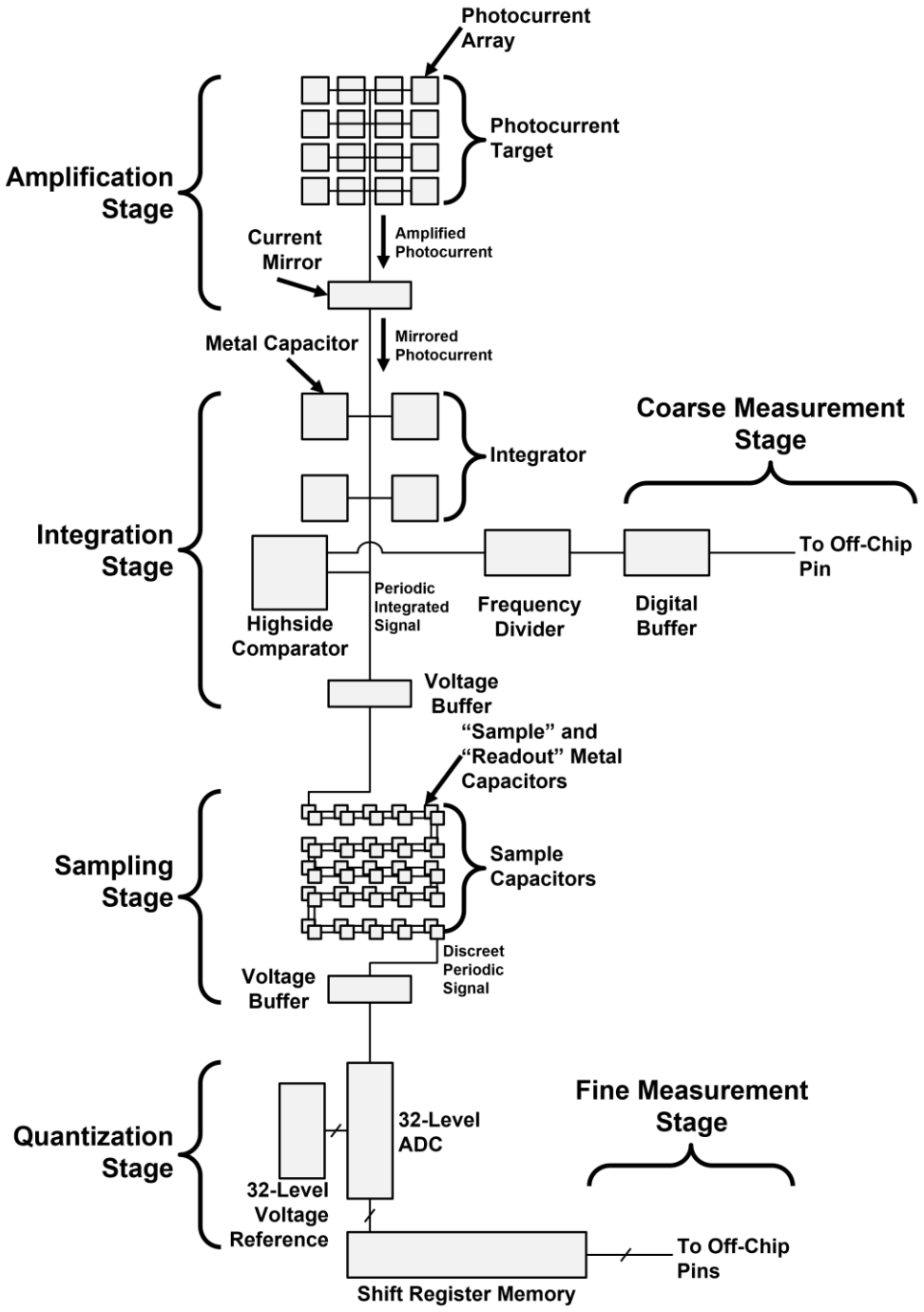

Figure 3 – Illustration of the high-level infrastructure of the on-chip photocurrent measurement circuit. Transient photocurrent is amplified by transmission-gated transistor arrays, integrated by a novel metal capacitor integrator into a periodic signal, sampled by a novel voltage sampler to protect data during irradiation, and quantized by a 32-level ADC. Stored quantized data is the fine output of the system, and the frequency of the periodic signal is the coarse output of the system.

triangle wave. The **Coarse Measurement Stage** digitally buffers the frequency of the sawtooth or triangle wave off-chip. Next, the integrator voltage is buffered into the **Sampling Stage**, where sampled analog voltages are stored on metal capacitors at a rate determined by an on-chip ring oscillator (RO) or phase-locked loop (PLL). The **Sampling Stage** exists to protect the highly-sensitive **Quantization Stage** from transient photocurrent effects that could compromise the integrity of the on-chip analog-to-digital converter (ADC). Finally, the quantized data from the **Quantization Stage** is stored in the **Fine Measurement Stage**, where digital data representing ADC thermometer code can be read after irradiation.

There are several intricacies of this design that are not apparent in the high-level view, such as optimization of transistor array size, the high-speed current mirror, and integrator capacitor sizing. Such intricacies are determined by technology node and can be accounted for within each functional block without changing the inputs or outputs. The high-level design is portable to various technology nodes; for example, the 22nm FD-SOI implementation of the PMC was created first, and the 45nm PD-SOI implementation of the PMC was created at a later date with no alterations to the high-level design.

PMC Data Acquisition – Coarse Measurement Stage

The Fine and Coarse Measurement Stages serve purposes akin to their name. The Fine Measurement Stage serves to capture peak photocurrent I_{PP} and primary photocurrent effects over a brief period, which requires high-speed sampling (nanosecond-scale), and the Coarse Measurement Stage serves to capture secondary photocurrent effects over an extended period, which often requires slower sampling speed (microsecond-scale).

The Coarse Measurement Stage reports a running frequency that is directly proportional to the period of the sawtooth or triangle wave when in linear option. This period is also proportional to the average current from the transistor targets, seen in **Equation 1**.

$$I_{Coarse} = C_{int} V_{range} f_{out} \quad (1)$$

where I_{avg} is the average current per period (i.e., $1/f_{out}$), C_{int} is the capacitance within the integrator, V_{range} is the voltage range of the integrator, and f_{out} is the off-chip frequency in the Coarse Measurement Stage. This frequency is captured in real-time by off-chip equipment and is best recorded by a frequency-detector or oscilloscope. This frequency is modulated by input current and is dynamic.

Error for I_{Coarse} is determined by the uncertainty of C_{int} and V_{range}. Even though C_{int} is determined by design, process variance and parasitic elements require that post-fabrication capacitance be measured. Robust built-in self-test (BIST) capabilities within the PMC ensure that C_{int} is easily determined and characterized across a wide range of input current magnitudes. The greatest source of uncertainty stems from V_{range}, which is determined by high-side and low-side comparators. Simulations of the comparators reveal a switching speed dependence that, in the context of the PMC, is most readily correlated to f_{out}. At high switching frequencies, the response of the comparators is delayed and results in a larger V_{range}. For example: the user defines V_{MAX} for a high-side comparator and a V_{MIN} for the low-side comparator with off-chip pins to bound V_{range}. These values are typically 750 mV and 250 mV, respectively. Simulations performed in Cadence Virtuoso [32] show that these voltages can extend past their desired value at high frequencies by as much as 25 mV each. At these typical bounds assuming a worst-case scenario, $V_{range} = 500\ mV \pm 50\ mV$. Though 10% error is tolerable, it is best to operate the PMC outside

of high-frequency regions. It will be shown at the end of this section that the PMC must operate within a linear region in order to report reliable values, so error originating from V_{range} is likely to be significantly less than the worst-case scenario of 10%.

In addition to traditional uncertainty quantification, the Coarse Measurement Stage is unable to track current waveforms with high-frequency components. If it is assumed that I_{Photo} is the input photocurrent to the Coarse Measurement Stage, then the following limitations may be imposed: For I_{Photo} with frequency components greater than half the maximum linear f_{out} value or I_{Photo} with frequency components greater than half the lowest of two consecutive f_{out} values, I_{Coarse} from **Equation (1)** strictly defines a lower bound of I_{Photo}. Otherwise, traditional uncertainty values may bound I_{Photo} to I_{Coarse}. A straightforward way to view this formal definition is to consider that I_{Coarse} represents a moving average of every two integration periods.

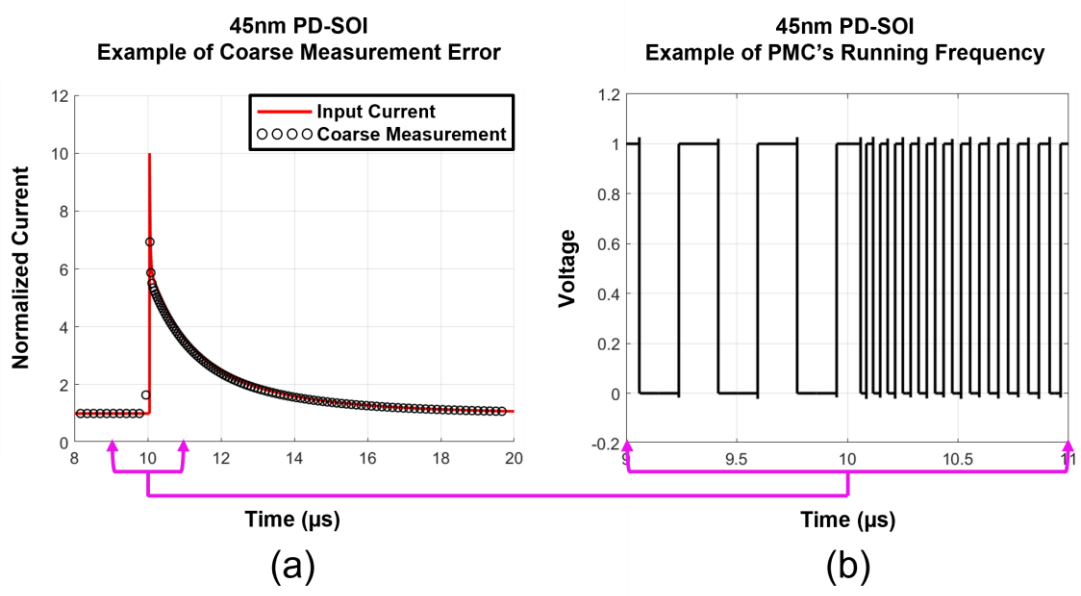

Figure 4 – (a) Obfuscation of peak photocurrent due to averaging in the Coarse Measurement Stage and (b) zoom-in of the PMC's frequency corresponding to this Stage. The impulse of photocurrent occurs in the middle of a running frequency period, averaging the impulse over two separate data points. This separation leads to an observed 25% error. Past this impulse, measurement error is negligible.

Current transients that resolve within these two integration periods will be obfuscated. An example of transient photocurrent obfuscation is shown in Figure 4, where peak photocurrent I_{PP} is averaged. Due to this limitation, coarse measurements are best suited for recording effects that lack high-speed components, such as effects that occur post-irradiation.

PMC Data Acquisition – Fine Measurement Stage

It was shown in the previous section that high-speed transient effects will be obfuscated by a moving average. This limitation is motivation for a more accurate form of on-chip measurement and led to the creation of the Fine Measurement Stage. In this stage, the voltage on the integrator is quantized, which enables the interpretation shown in **Equation 2**.

$$I_{Fine} = C_{int} \frac{dV}{dT_{samp}} \tag{2}$$

where I_{Fine} is the continuous current from the targets, C_{int} is the capacitance within the integrator, dV is the voltage differential from the sampled voltages, and dT_{samp} is the time differential from the period of samples. The integrator periodically charges and discharges, and to recover this continuous current from the integrator voltage, the sawtooth or triangle wave is "unwrapped" by inserting offsets to the samples such that the system virtually implements a larger capacitor. In the sawtooth case, this process involves adding a DC offset at each negative slope and zeroing out any samples taken during the "reset" period. An example of unwrapping of data from a sawtooth integrator is shown in Figure 5(a) and (b). Once unwrapped, data is interpolated, shown in Figure 5(c), then the interpolation is differentiated with respect to dV and dT_{samp}, shown in Figure 5(d). In order to correlate slope to known current, the DC response of the Coarse Measurement Stage is related to the slope from the integrator in a DC state, forming the following equality:

$$S_{DC} \propto I_{Fine_{DC}} = I_{Coarse_{DC}} \tag{3}$$

Though extensive self-testing, it was confirmed that ΔS_{DC} is linearly proportional to change of $\Delta I_{Coarse_{DC}}$, which provides the basis for the following assertion:

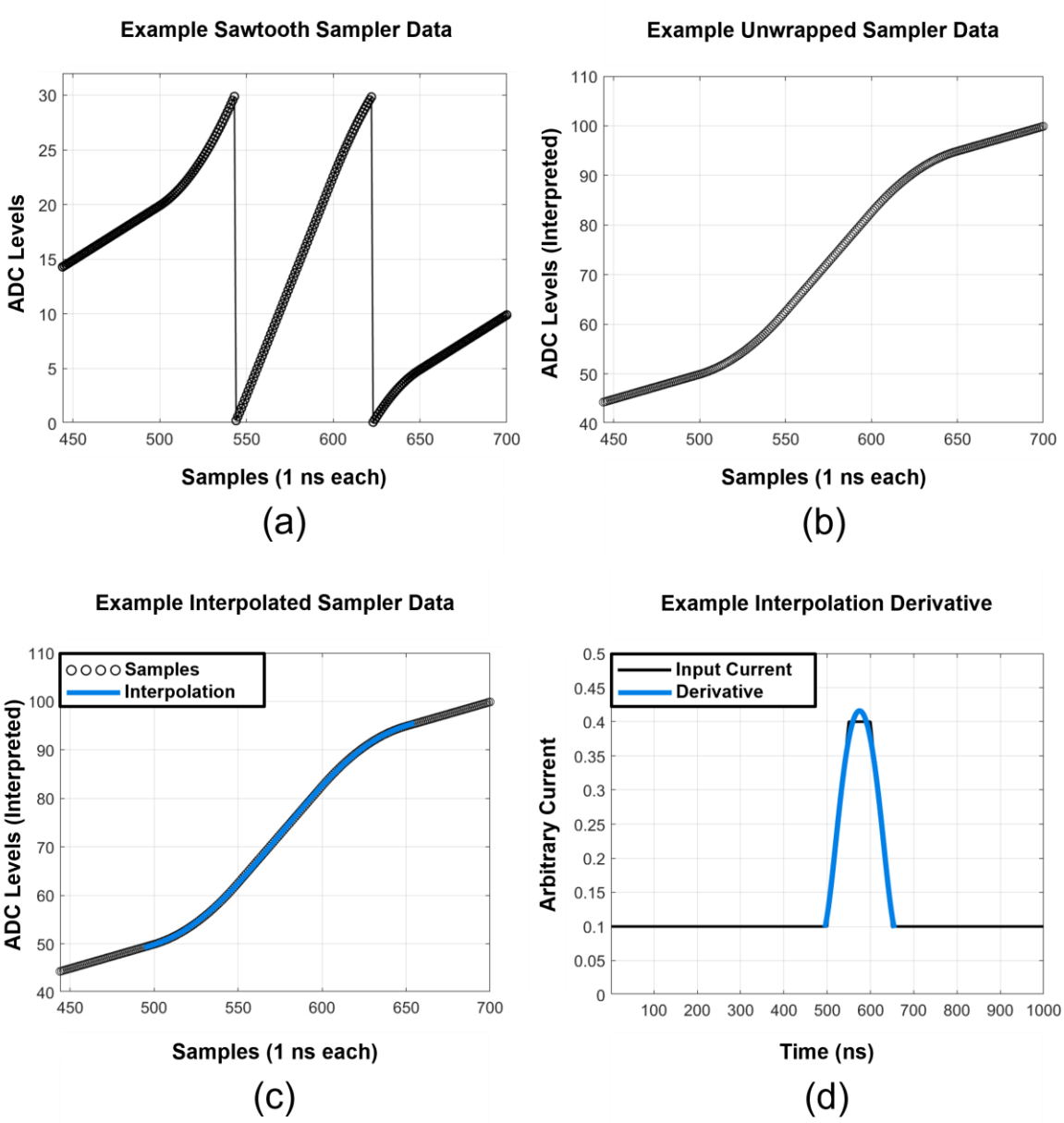

Figure 5 – Example simulation of the Fine Measurement Stage data interpretation process. (a) Raw ADC data from output of sampler with valid data bit (b) "unwrapping" of ADC data at each reset in sawtooth wave by applying a DC offset to each sawtooth reset (c) best-fit polynomial interpolation of ADC data. Data during resets are ignored in the interpolation. (d) derivative of interpolation according to Equation (2).

$$\frac{S_{I_{PP}}}{S_{DC}} = \frac{I_{PP}}{I_{Coarse_{DC}}},\ or\ I_{PP} = I_{Coarse_{DC}} \frac{S_{I_{PP}}}{S_{DC}} \tag{4}$$

where $S_{I_{PP}}$ is the maximum slope from the sampler interpolation and I_{PP} is peak current induced by transient photocurrent. A combination of **Equation 3** and **Equation 4** enables detection of I_{PP}. Error contributing to **Equation 4** originates from $I_{Coarse_{DC}}$ and $S_{I_{PP}}$. $I_{Coarse_{DC}}$ has been previously defined, and $S_{I_{PP}}$ error is bound by the maximum and minimum slopes encountered the period of irradiation, which is detected by an increase in slope from pre-irradiation slope. An example of the minimum and maximum slope that define this error is provided in Figure 6.

In some cases, transitionary information is lost due to aliasing. However, since samples are taken at a nanosecond timescale, the likelihood of such aliasing is incredibly low; such error would

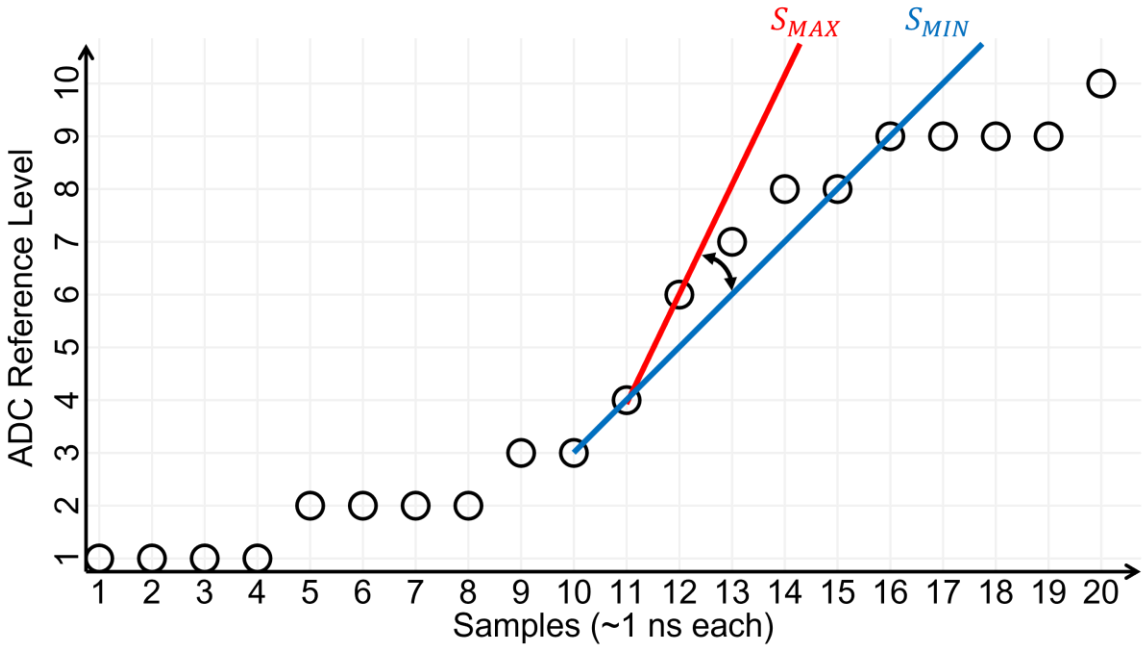

Figure 6 – Example of extracting maximum and minimum slope from sampler data for error bounding of I_{PP}.

require currents large enough to fully charge the integrating capacitor within a single sample. Further, such an effect cannot go undetected by the PMC, as the Coarse Measurement Stage reports the period of the sawtooth and triangle integral. In combination, the Fine and Coarse Measurement Stages enable the PMC to characterize the full transient photocurrent response of the targets. The efficacy of these indirect measurement techniques will be shown in the following chapters.

PMC Self-Tests

Extensive self-tests have been performed on both the 22nm FD-SOI and 45nm PD-SOI variants of the PMC. All basic operational self-tests pass and are included in Table A-3. The self-tests of interest in this section focus on linearity of the PMC. These measurements are performed by varying the number of parallel arrays in the targets and capturing leakage current with the Coarse Measurement Stage. Off-chip measurement of internal DC current sources is also available,

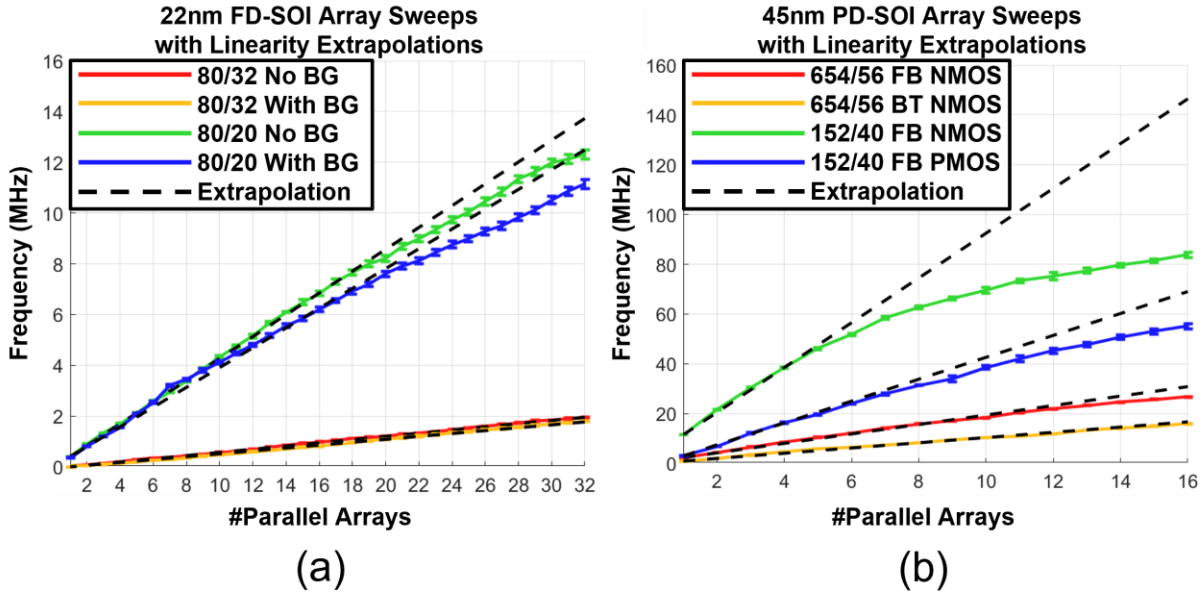

Figure 7 – Target linearity sweeps for (a) 22nm FD-SOI and (b) 45nm PD-SOI. Data is reported as frequency from the Coarse Measurement Stage. Dotted lines extrapolate the first 4 arrays in each dataset to show loss of linearity in the PMC at high currents.

which enables calculation of C_{int} from equations (1) and (2); these DC current sources replace the transistor targets and are mirrored into the PMC. The results of the linearity sweeps for 22nm FD-SOI are shown in Figure 7(a), and the results of the linearity sweeps for 45nm PD-SOI are shown in Figure 7(b).

Dotted lines in Figure 7(a) and (b) are extrapolated from the first 4 targets in each dataset. This extrapolation is made to show that the PMCs will lose linearity if the frequency of the integrator, and consequently, the current entering the integrator, is too great. This loss of linearity is expected; on-chip current mirrors are designed to operate within a region of linearity that is calibrated to each technology node. The 80nm / 20nm targets in 22nm FD-SOI and 152nm / 40nm targets in 45nm PD-SOI exhibit the most leakage current and enter this region of non-linearity when too many arrays are in parallel. Presented data in this work were captured with the number of parallel arrays such that pre-irradiation leakage is within the linear region of operation; however, photocurrent transients of sufficient magnitude will cause the PMC to enter the region of non-linearity at the apex of the current transient. For the majority of data presented in this work, this potential issue is not a concern. Linearity will be addressed when applicable.

CHAPTER 4

RADIATION TEST FACILITIES AND PMC INFRASTRUCTURE

Radiation Test Facilities

The PMC has been tested at four different radiation test facilities. The first testing evaluation took place in the Naval Surface Warfare Center (NSWC) Crane Linear Accelerator (LINAC). At this time, only the 22nm FD-SOI variant of the PMC was ready for experimentation. Additionally, electromagnetic interference (EMI) effects dominated at the LINAC, which obfuscated transient photocurrent. EMI effects from the LINAC are significant to this work and will be discussed in **Appendix V**.

The second of these testing evaluations was held at the Vanderbilt University ARACOR. The purpose of this testing evaluation was to measure TID-induced leakage current increase with the PMC, as prompt dose effects induce TID and impact photocurrent measurement efforts. Only the 22nm FD-SOI version of the PMC was available for testing in the fall of 2021. These TID results have already been published in radiation effects literature [48] [51] and confirm the tolerance of the PMC in a total dose environment.

The third testing evaluation took place at the U.S. Naval Research Laboratory (NRL). This testing facility implemented a Nd:YLF diode-pumped Q-switched laser with the capability to mimic a prompt-dose environment [6] [40] [46] [54] if laser light can reach active silicon unimpeded. The beam is a 5.6-nanoseconds full-width half-max (FWHM) pulse with a Gaussian profile. The beam was manipulated with optical elements to distribute the laser light over a rectangular region, a design which evenly irradiates DUTs [54]. The wavelength of the infrared

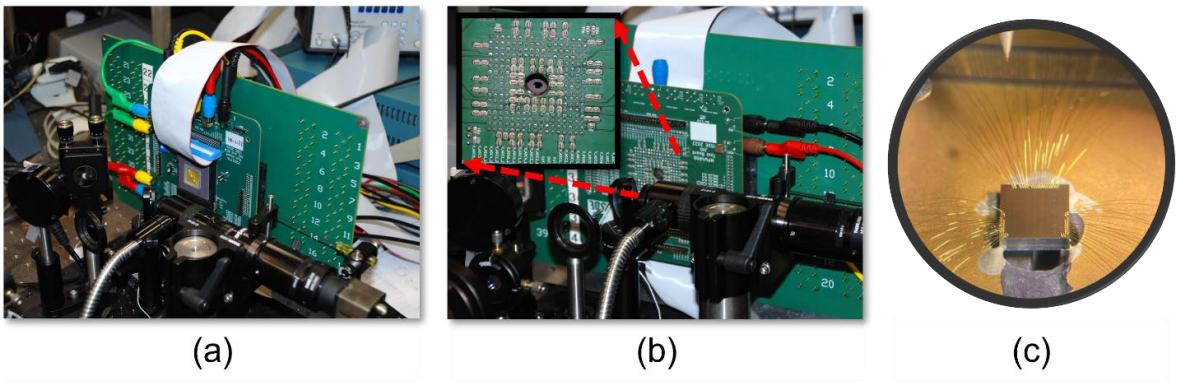

Figure 8 – Front-side view of the photocurrent measurement circuit test setup at NRL (a), back-side view (b), and custom-bonded 45nm PD-SOI die (c). Back-side lasing required the socket to be drilled, and the die was custom-bonded over the drilled hole.

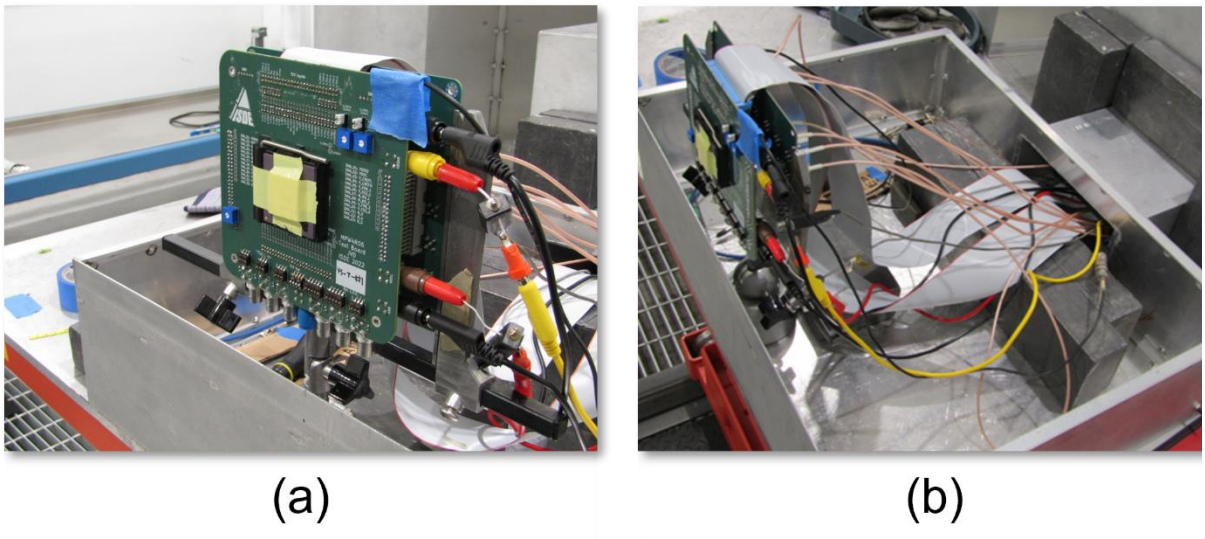

Figure 9 – Front (a) and side view (b) of the photocurrent measurement circuit test setup at the FXR.

laser is 1053-nanometers, which is sufficient to penetrate the back-side of silicon wafers used in this work. Both front-side and back-side irradiation of the DUTs were performed. Back-side irradiation is only available in the 45nm PD-SOI variant of the PMC, which features custom-bonded die which hangs over a drilled hole in the socket, shown in Figure 8(c). A full summary of the experiments performed at NRL are included in **Appendix III**. The test setup for front-side and back-side irradiation at NRL is shown in Figure 8(a) and (b).

The fourth and last testing evaluation took place at a Flash X-Ray (FXR). The FXR produces high-energy x-rays with a 20-nanosecond FWHM profile. These x-rays can penetrate metal, which enables a setup where the DUTs are fully enclosed in a Faraday cage, eliminating most EMI effects. The test setup at the FXR is shown in Figure 9(a) and (b). A full summary of the experiments performed at the FXR are included in **Appendix III**. Even with the aluminum Faraday cage, EMI results are comparable to that at the LINAC, but the temporal characteristics of noise from this source enabled isolation and measurement of transient photocurrent. EMI tests at the FXR are grouped with the EMI tests at the LINAC in **Appendix V**.

PMC Infrastructure

The 22nm FD-SOI and 45nm PD-SOI DUTs are wire-bonded onto 208-pin packages. These packages are mounted onto 21 x 21 pin sockets that enable speedy swapping of various DUTs. Sockets connect to printed circuit boards (PCBs) that are part of a custom infrastructure designed specifically for communication with the PMCs. This infrastructure is detailed in Figure 10. Like the on-chip PMC, this infrastructure is separated into several stages. The first of these is the **DUT and Socket Stage**, which was described previously. The socket is soldered onto a PCB named the "**DUT Board**," which is shown in Figure 11(a). The second is the Header Pin Stage, where high-speed signals from the **DUT Board** are connected to a PCB named the "SMA Board," shown in Figure 11(b). There are no active components on the **DUT Board** aside from the DUT, so these signals are driven by DUT itself. The SMA Board enables connection via SMA to BNC cables which can plug directly into an oscilloscope. These header pins also serve as a method to horizontally mount the **DUT Board**. The SMA Board can be mounted in open-air by fixating the board with clamps or by other means. These 40-pin header connectors are standardized, with multiple radiation test facilities employing their own version of the SMA Board. Since the DUT

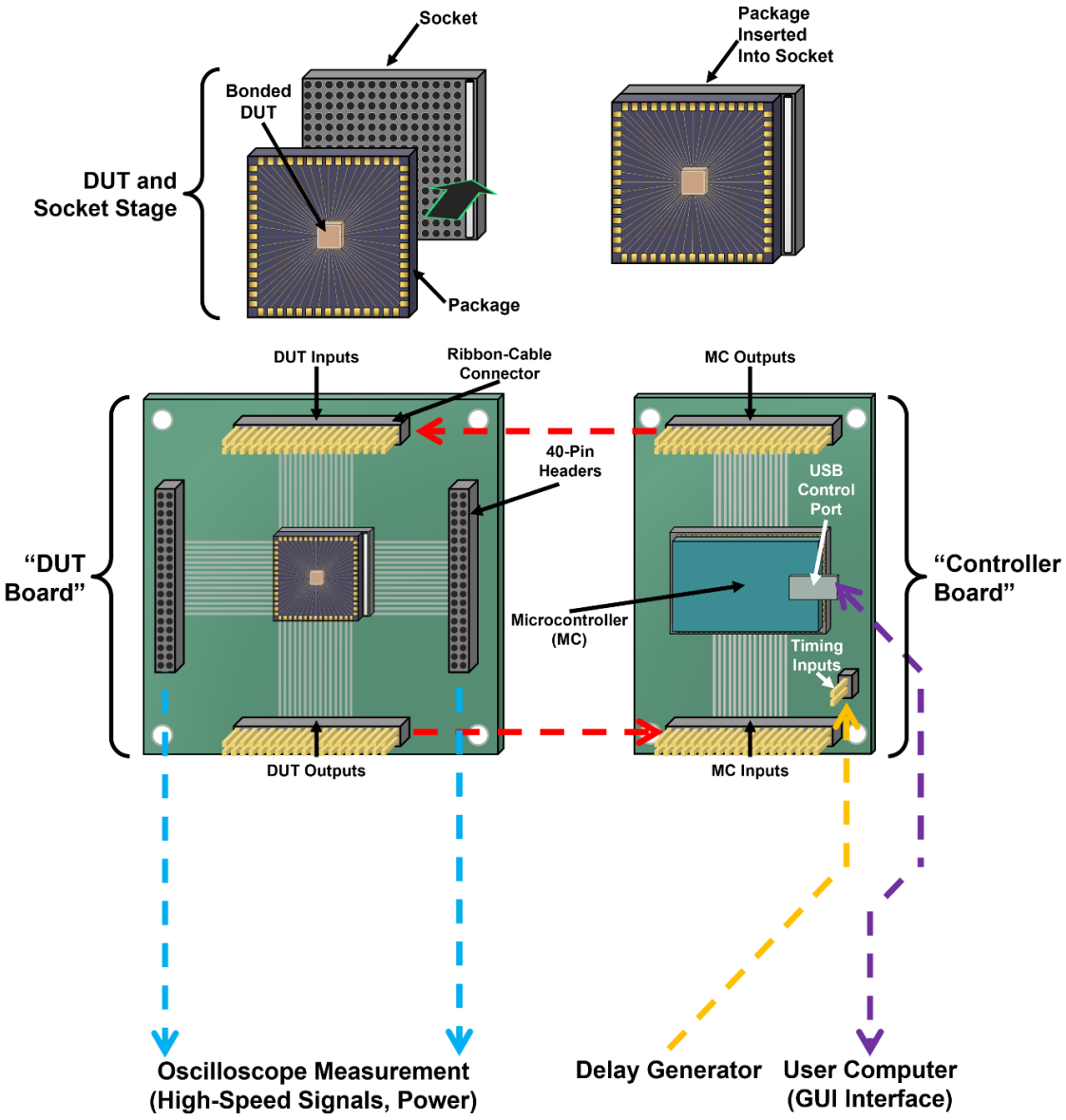

Figure 10 – Illustration of the photocurrent measurement circuit test setup infrastructure. The DUT is bonded to a package that is inserted into a socket. The socket is soldered onto the "DUT Board," which routes high-frequency signals and power to 40-pin headers and digital inputs and outputs to ribbon-cable connectors. The 40-pin headers mount onto an SMA board (not shown), and the signals are monitored by oscilloscopes. The "Controller Board" connects to the "DUT Board" via ribbon cables and is controlled through USB by a user computer that runs custom GUI software. A delay generator synchronizes to a facility signal and triggers the microcontroller with timing inputs.

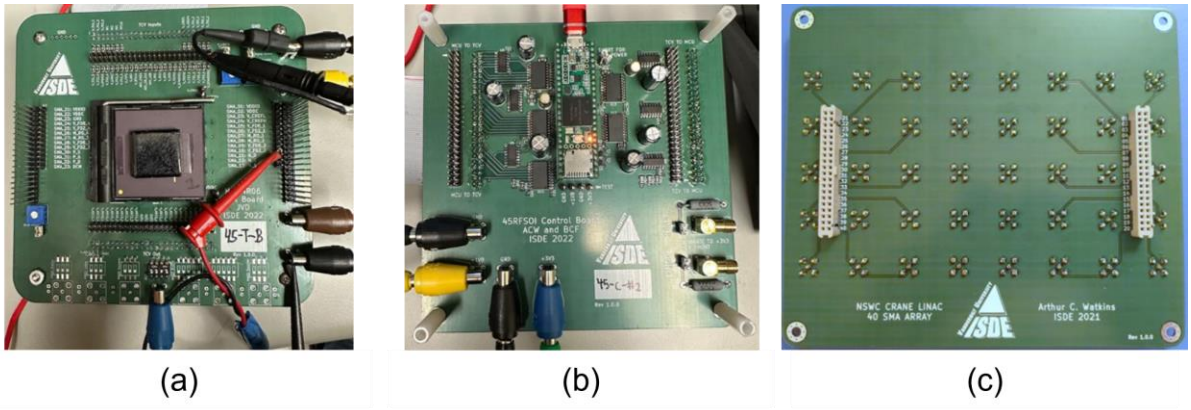

Figure 11 – (a) DUT board (b) Controller Board (c) SMA board.

Board contains no active components other than the DUT, digital control is achieved through the ribbon cables, which connects digital inputs and outputs of the DUT to an external PCB. This PCB is named the "**Controller Board**" as it houses a microcontroller that interprets commands that control the PMC. It is shown in Figure 11(c). The microcontroller is connected via USB to a user laptop or computer. Custom graphical user interfaces (GUIs) were written for this infrastructure that enable streamlined control and data collection. A timing input is in place that allows experimenters to utilize a delay generator that connects to the **Controller Board** and oscilloscope. This signal is synchronized such that PMC sampling begins before irradiation and that the oscilloscope captures data in the correct time window. Power is achieved through banana cable connectors on both the **DUT Board** and **Controller Board**, and power may also be sent through coaxial cable to the **DUT board**.

CT probes may be placed in-line with the banana cables in order to sense induced photocurrent on the power supplies. Additionally, current sense on the ground plane may be achieved with the "Sense Board," which is identical to the DUT Board except that sense resistors

are in series with the DUT's local ground and true ground. The decision to separate these PCBs was made to ensure sufficient ground-plane conductance for the DUT under normal operation.

CHAPTER 5

EXPERIMENTAL RESULTS

Summary of Presented Data

The data presented in this section is a compilation from the tests performed in **Appendix III**, which includes measurements made at the pulsed laser and FXR. Each dataset serves to investigate a specific variable in the design, such as varying the number of parallel arrays in the target, varying the W/L ratio of the devices, and isolating primary and secondary photocurrent by investigating the impact of the back-gate or body-tie. Photocurrent plots will be interpreted from the outputs of the Fine and Coarse Measurement Stages detailed in **Chapter III**. Plots from the Fine Measurement Stage will include the final result of the interpolation process, which is the current waveform resulting from the derivative of the interpolation. It is important to note that facility delay is not always consistent, especially at the FXR, where a few hundred nanoseconds of variance in the trigger signal was present. Because of this variance, data from the ADC will shift in time from plot-to-plot. This variance also causes the system to "miss," so data from the Fine Measurement Stage is limited. Data from the Coarse Measurement Stage is extensive, with frequency interpretations of transient photocurrent available for every shot. Prolonged secondary effects are shown to be significant in both 22nm FD-SOI and 45nm PD-SOI, so this data will be prominently featured.

Data from both measurement stages is normalized to pre-irradiation leakage, with the "1" value on each y-axis representing this leakage current. Normalization is self-consistent in each plot such that transient photocurrent is represented on the same scale. It is also important to recognize that DC offsets are applied to account for TID-induced leakage current. Some exceptions to this

normalization standard exist and will be detailed when they occur. Radiation levels are obfuscated in this work. Energy from the pulsed laser is represented on a scale of "PLE 0.01 to 20.0" and levels from the FXR is represented on a scale of "PDR 1 to 3000." These scales are arbitrary and are not directly comparable.

45nm PD-SOI Results

Figure 12(a) and (b) is a comparison of the four on-chip targets variants with irradiation energies and levels that produced a similar response at both test facilities. In order to achieve a comparable response at the pulsed-laser, back-side lasing was required. Figure 13(a) and (b) is comparison between radiation energy sweeps at both test facilities for the 654/56 floating-body target, and Figure 14(a) and (b) is the same comparison but with the 654/56 body-tied target. Similarly, Figure 15(a) and (b) is a comparison between radiation energy sweeps at both test facilities for the 152/40 floating-body NMOS target, and Figure 16(a) and (b) is the same comparison but with the 152/40 floating-body PMOS target. A comparison between front-side and back-side lasing at NRL is shown in Figure 17(a) and (b).

Linearity sweeps were also performed to ensure transient photocurrent scales with the number of parallel arrays in the target. Time allowed for a full sweep of parallel arrays at the pulsed laser, but only four arrays could be swept at the FXR. These linearity sweeps for the 654/56 floating-body target are shown in Figure 18(a) and (b). Fine Measurement Stage data in 45nm PD-SOI reveals no interpretable transient shape. In all recorded datasets from both the FXR and pulsed-laser, slope appears to instantaneously transition from pre-irradiation leakage to peak photocurrent I_{PP}. Instead of displaying each of these linear interpolations, I_{PP} from both the Fine and Coarse Measurement stages are compared in Figure 19(a) and (b). One example of the Fine Measurement Stage data extraction is shown in Figure 20(a)-(d).

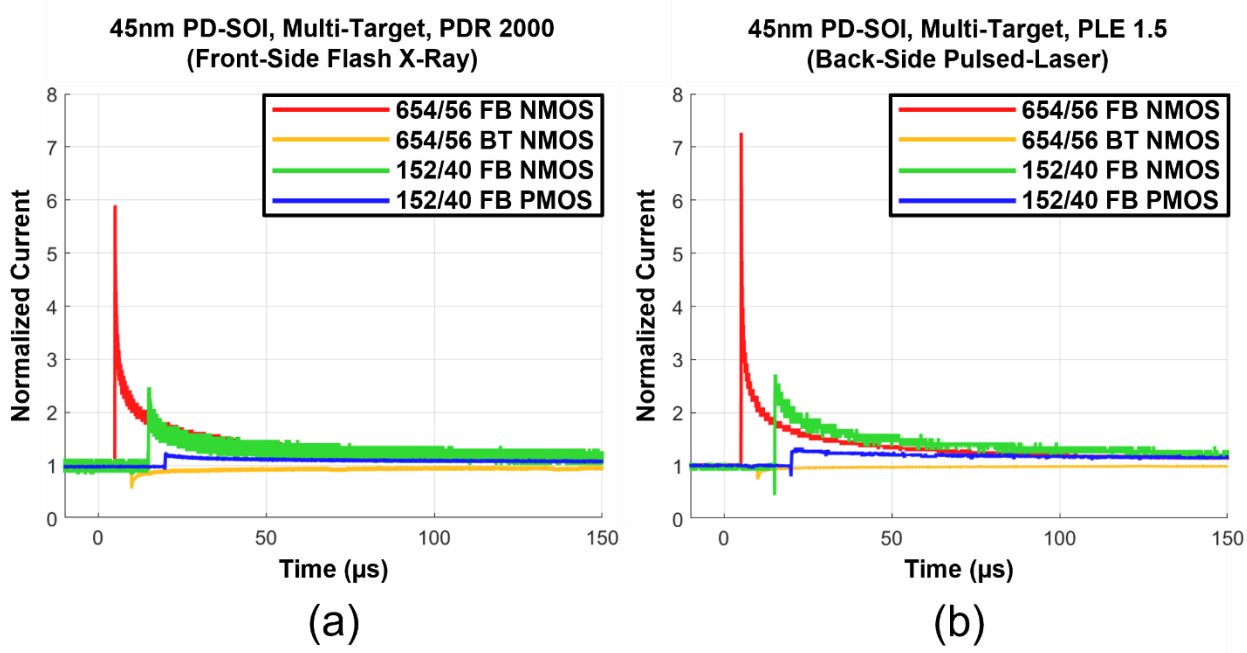

Figure 12 – Comparison of the 45nm PD-SOI target variants at the flash x-ray and pulsed laser. Each data set in both plots are offset by 5-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

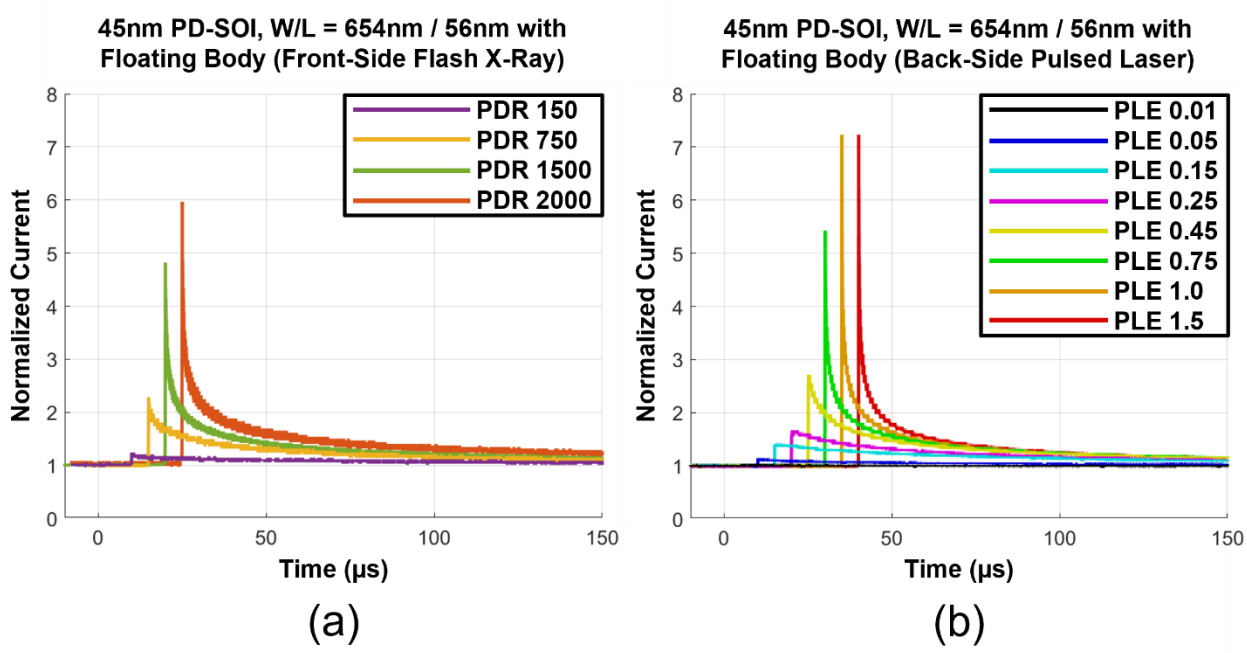

Figure 13 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the analog floating-body devices. Each data set in both plots are offset by 5-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

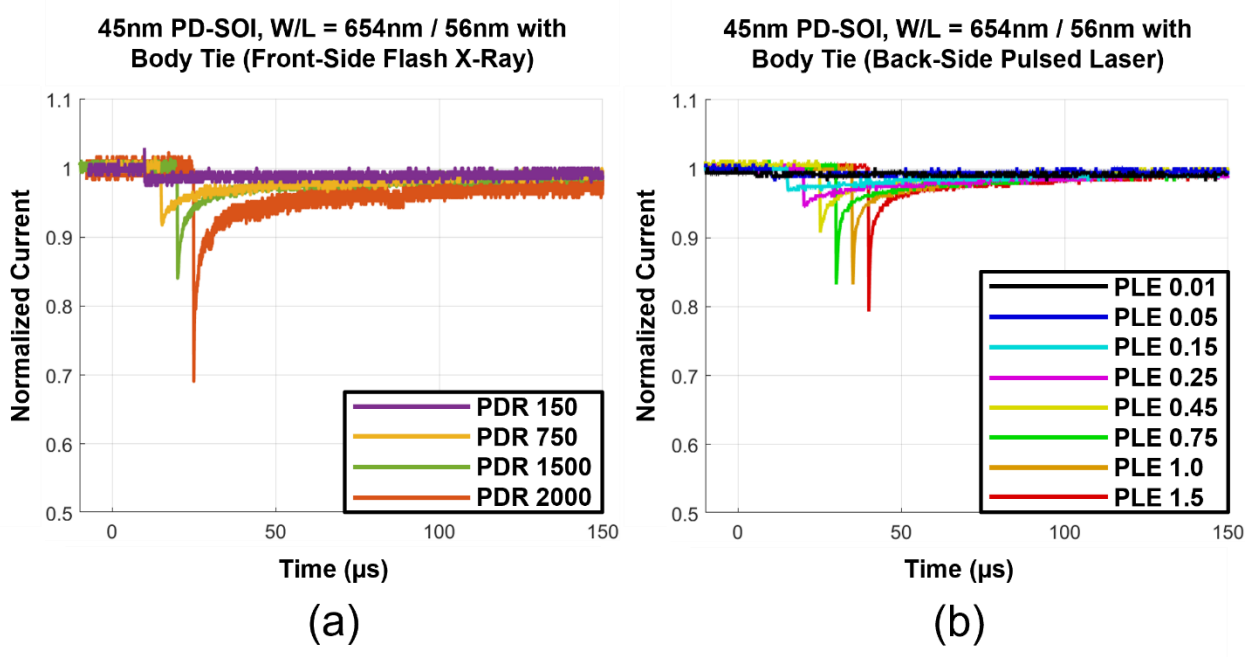

Figure 14 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the analog body-tied NMOS devices. The body is tied to ground. Each data set in both plots are offset by 5-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

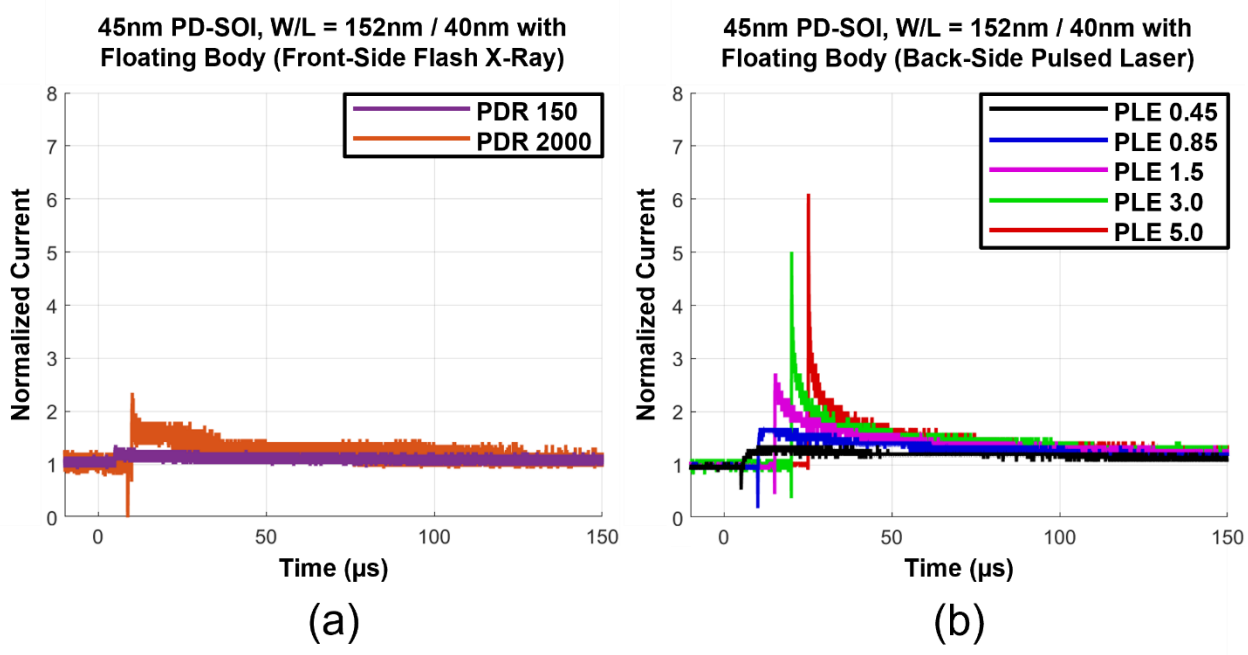

Figure 15 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the digital floating body NMOS devices. Limited data is available in (a). Each data set in both plots are offset by 5-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

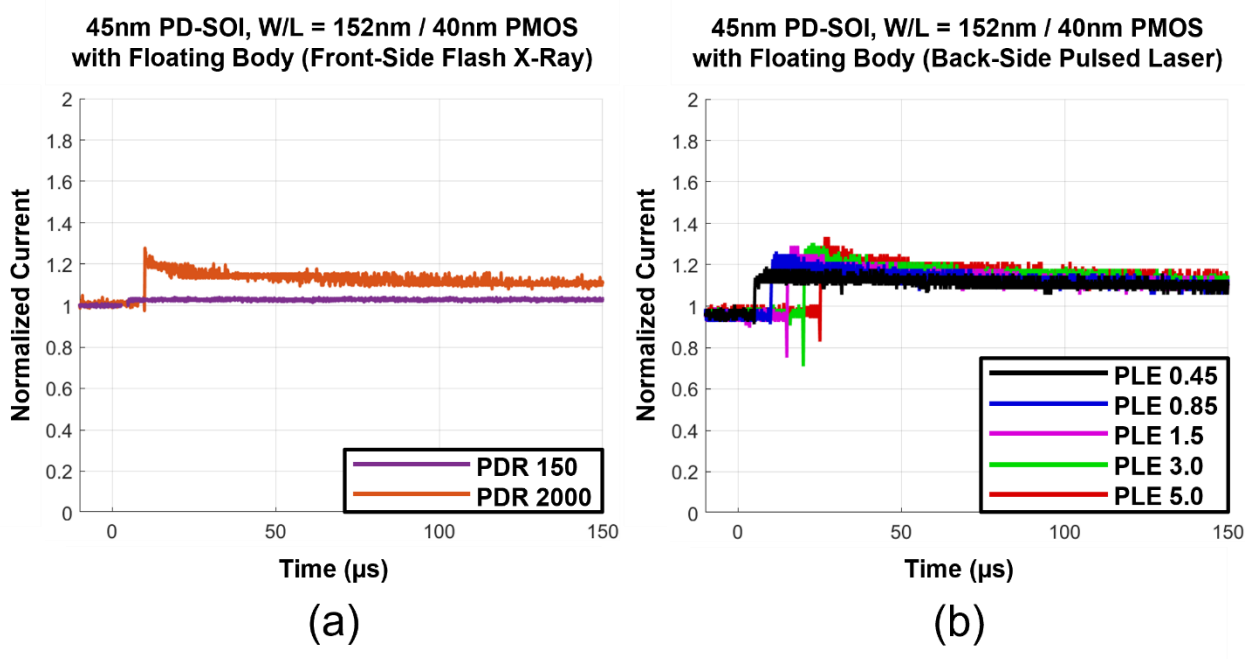

Figure 16 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the digital floating body PMOS devices. Limited data is available in (a). Each data set in both plots are offset by 5-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

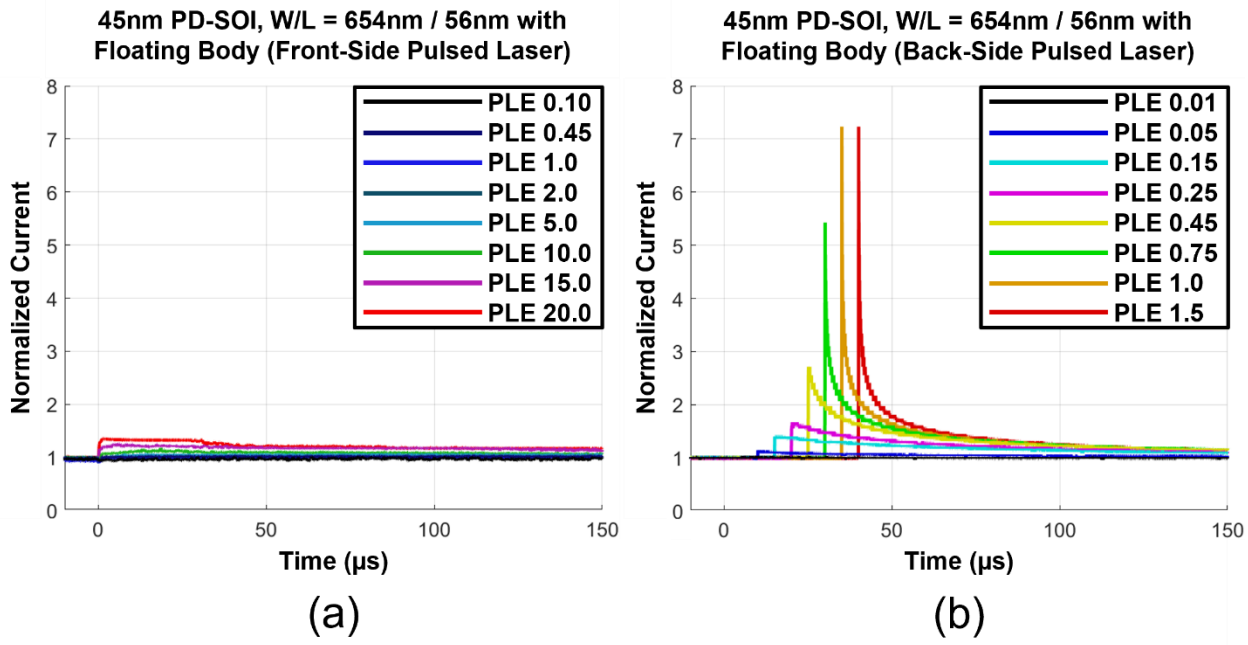

Figure 17 – Front-side pulsed-laser energy (a) and back-side pulsed laser energy sweeps (b) from the analog floating body NMOS devices. Each data set in both plots are offset by 5-µs for plot clarity. PLE 20.0 is facility maximum energy.

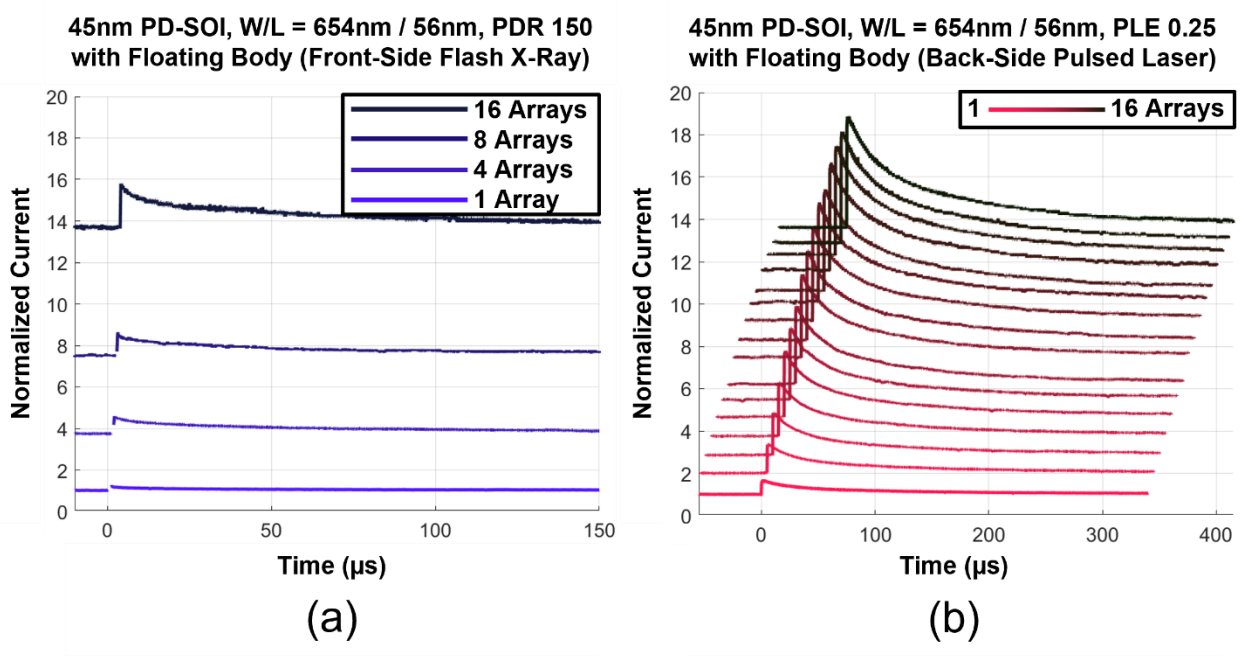

Figure 18 – Flash x-ray (a) and pulsed-laser (b) parallel array sweeps. EMI pulses in (a) are removed for plot clarity. Each data set in (b) is offset by 5-µs for plot clarity.

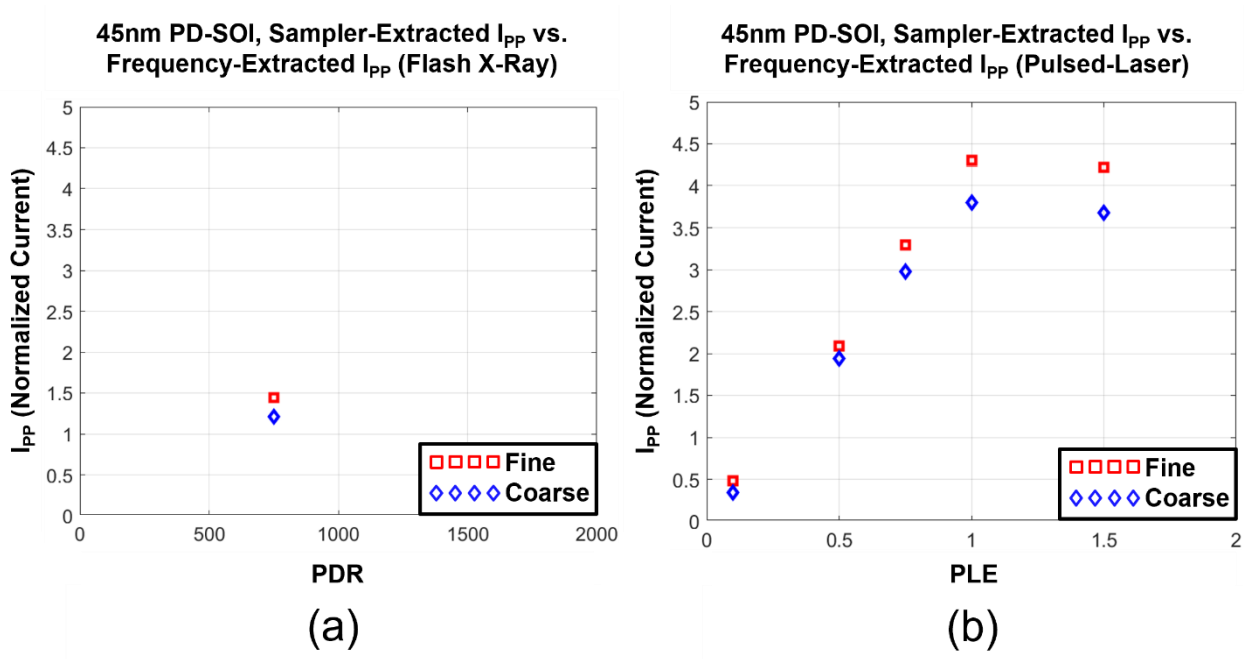

Figure 19 – Extracted I_{PP} with the Fine and Coarse Measurement Stages at the (a) flash x-ray and (b) pulsed-laser. Data from flash x-ray is limited due to facility timing constraints.

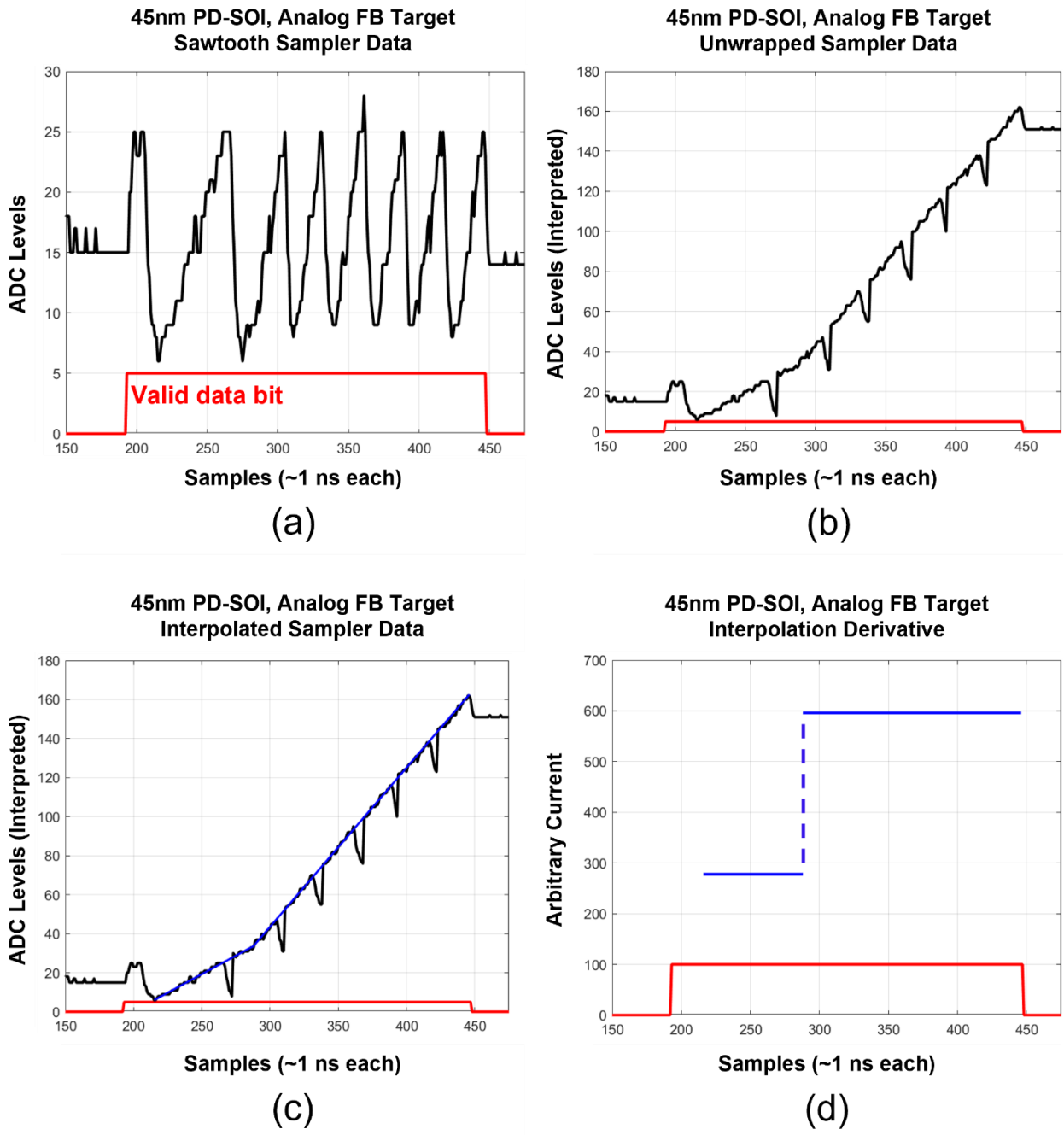

Figure 20 – Fine Measurement Stage data from 45nm PD-SOI at the FXR (a) raw ADC data from output of sampler with valid data bit (b) "unwrapping" of ADC data at each reset in sawtooth wave by applying a DC offset (c) best-fit interpolation of ADC data. Data during resets are ignored in the interpolation. (d) derivative of interpolation according to Equation (2). Red lines indicates the valid data bit. In all 45nm PD-SOI Fine Measurement Stage datasets, samples indicate an instantaneous transition from pre-irradiation slope to post-irradiation slope. Insufficient resolution is available for best-fit polynomial interpolation; all interpolations are the joining of two lines.

22nm FD-SOI Results

Only front-side lasing was available in 22nm FD-SOI, and laser energies past PLE 10 induced digital failures in this technology. There is a drastic increase in photocurrent amplitude from PLE 5 to PLE 10 – this jump in current is so large that the photocurrent responses cannot be plotted on the same linear scale without data obfuscation. Data is presented up to PLE 5 first, then data with PLE 10 will be shown. These failure mechanisms also induced temporary loss of operation in the on-chip ring oscillator, so data from the Fine Measurement Stage is limited in 22nm FD-SOI. Figure 21(a) and (b) is a comparison of four on-chip targets variants with irradiation energies that produced a similar response at both test facilities. Figure 22(a) and (b) is a comparison between radiation energy sweeps at both test facilities for the 80/20 target without back-gate. Figure 23(a) and (b) is a comparison between radiation energy sweeps at both test facilities for the 80/32 target without back-gate, and Figure 24(a) and (b) is the same comparison with the back-gate. Unless otherwise stated, both the n-well and p-well are grounded in these tests. Figure 25(a) and (b) is comparison between radiation energy sweeps at both test facilities for the 160/40 target without back-gate. Linearity sweeps were also performed to ensure transient photocurrent scales with the number of parallel arrays in the target. These linearity sweeps were performed in increments of 8, 16, 24, and 32 parallel arrays. The linearity sweeps for the 80/32 target with back-gate is shown in Figure 26(a) and (b). Figure 27 and Figure 28 include the PLE 10 energy data point for the various targets

Irradiation with applied back-gate bias was also performed. Negative back-gate bias on the p-well will increase transistor threshold voltage and consequently decrease leakage current in the targets. Similarly, positive back-gate bias on the p-well can significantly increase the leakage current in the targets. To keep the PMC operating in a linear region during these back-gate bias

tests, the number of parallel targets was set to both extremes: 32-parallel arrays for negatively biased p-well, and 2 arrays for positively biased p-well.

Figure 29(a) and (b) is a negative p-well back-gate bias sweep for the 80/32 targets, and Figure 30(a) and (b) is a positive p-well back-gate bias sweep for the same target. Because other tests were higher priority, only one datapoint exists for this testing configuration from the pulsed laser. TID effects in Figure 30(a) shifted the PDR 750 dataset by several times pre-irradiation leakage current and is visible due to the extreme threshold voltage shift induced by the positive p-well voltage. Fine Measurement Stage data in 22nm PD-SOI reveals a distinct transient shape. However, due to ring-oscillator loss of operation at medium-to-high PDRs and pulsed-laser energy, there is limited data from the Fine Measurement Stage, and meaningful peak I_{PP} comparisons cannot be made. One example of the Fine Measurement Stage data extraction is shown in Figure 31(a)-(d).

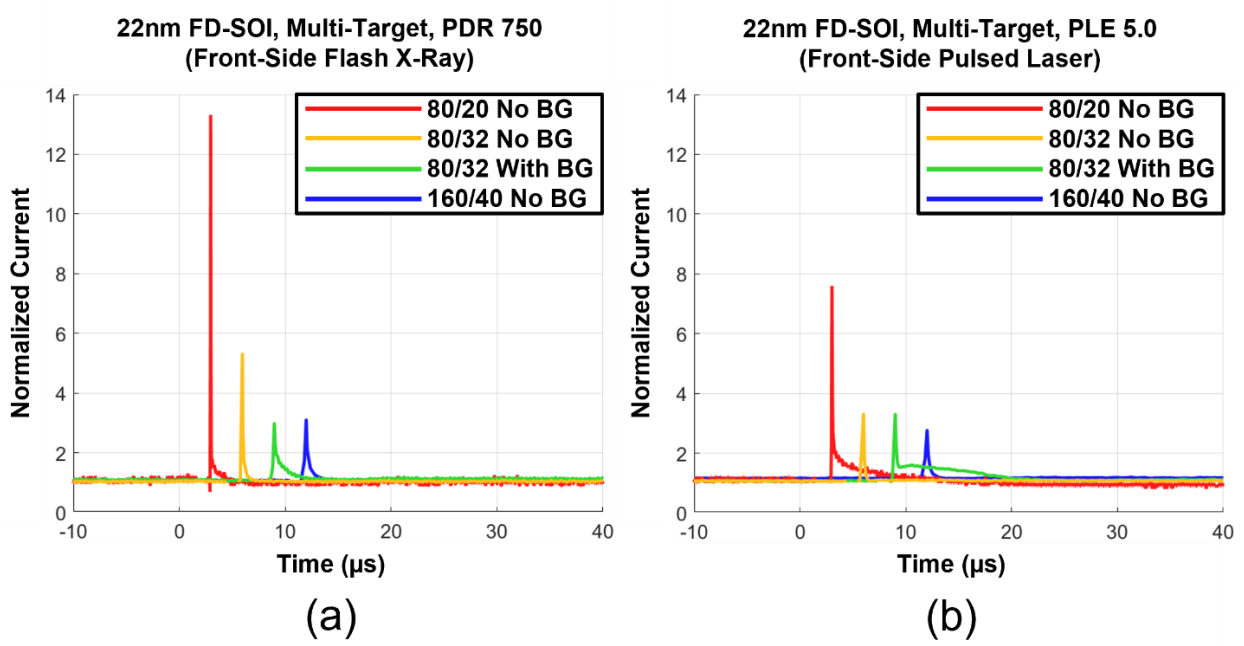

Figure 21 - Comparison of the 22nm FD-SOI target variants at the flash x-ray and pulsed laser. Each data set in both plots are offset by 3-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

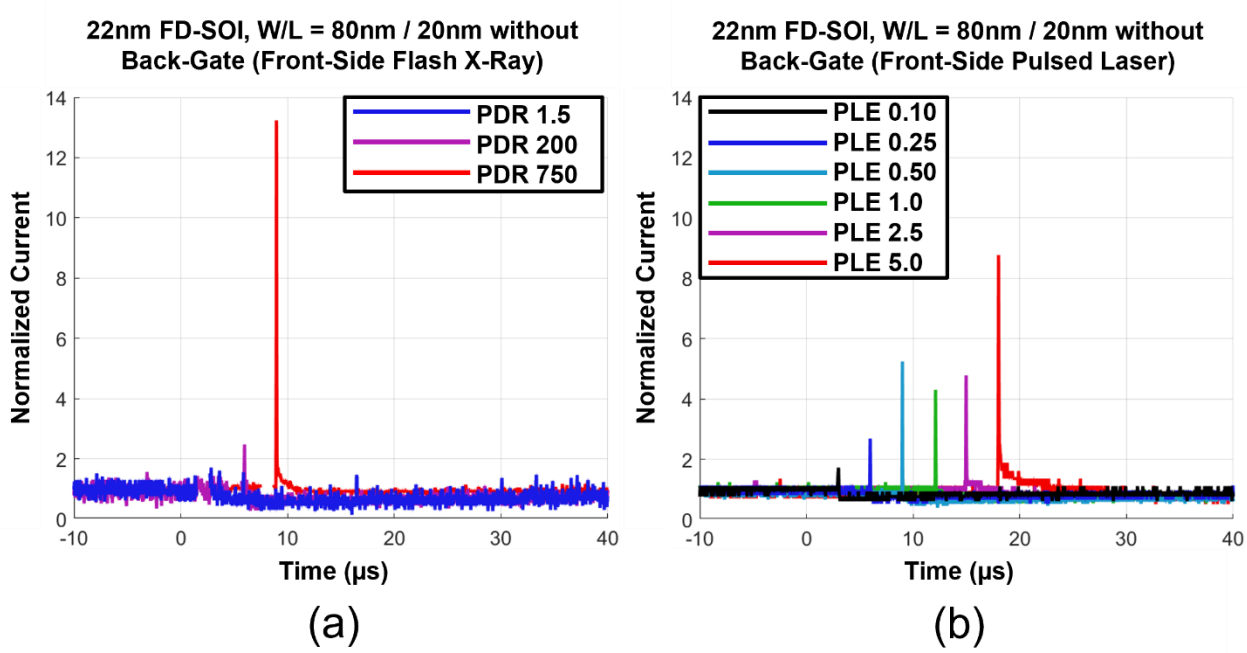

Figure 22 Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the 80nm / 20nm devices without back-gate. Each data set in both plots are offset by 3-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

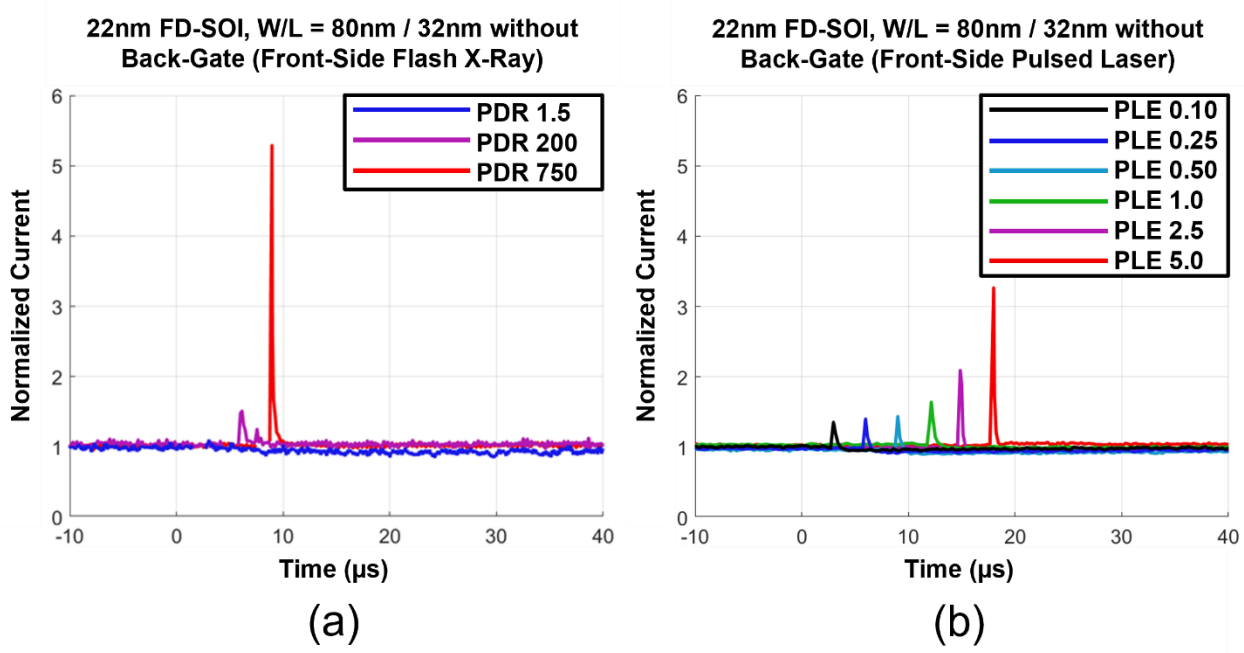

Figure 23 - Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the 80nm / 32nm devices without back-gate. Each data set in both plots are offset by 3-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

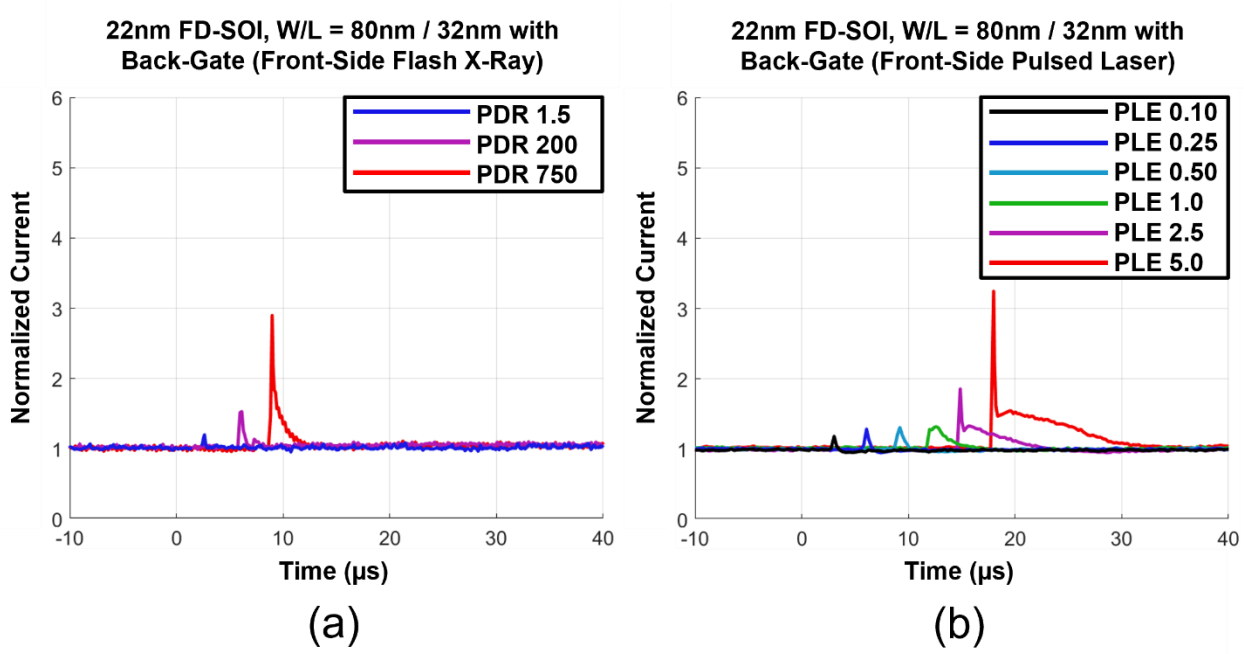

Figure 24 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the 80nm / 32nm devices with back-gate. The back-gate wells are grounded. Each data set in both plots are offset by 3-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

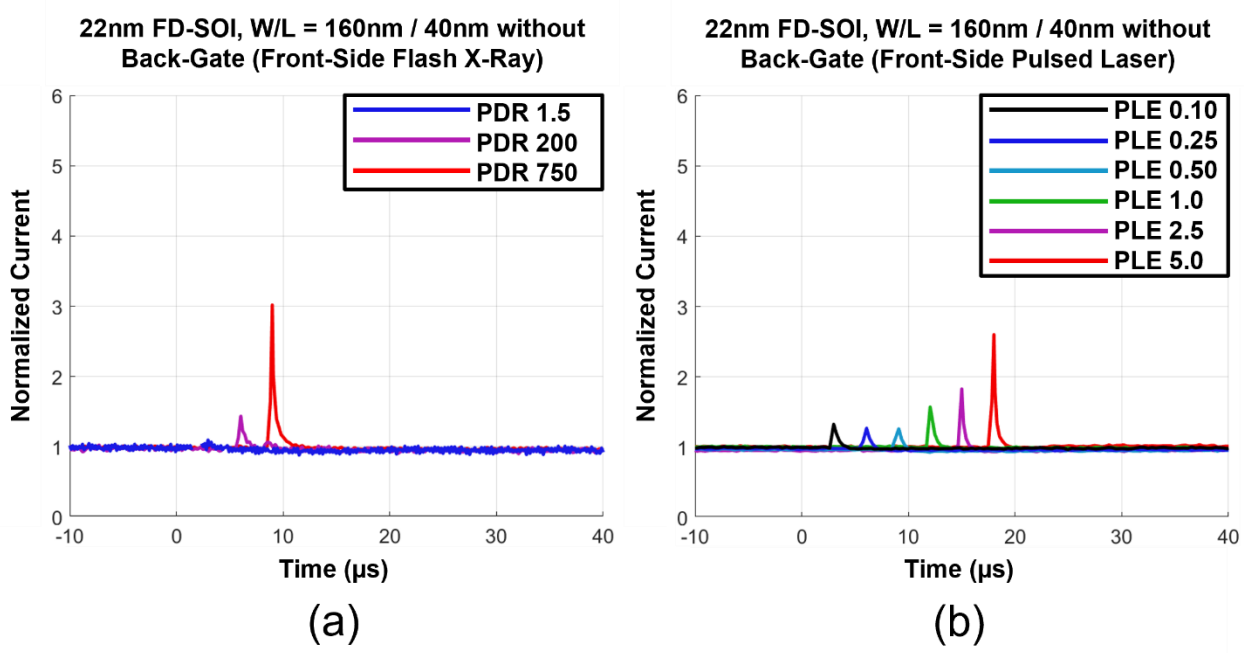

Figure 25 – Flash x-ray level (a) and pulsed-laser energy sweeps (b) from the 160nm / 40nm devices without back-gate. Each data set in both plots are offset by 3-µs for plot clarity. EMI pulses in (a) are removed for plot clarity.

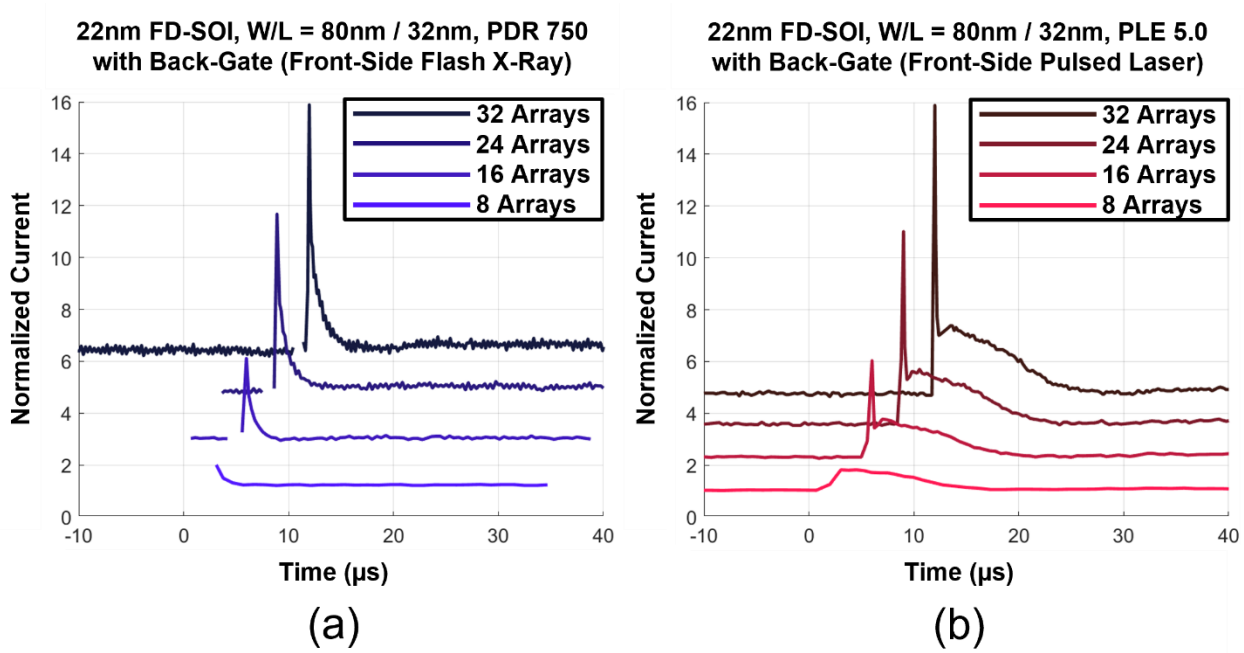

Figure 26 – Flash x-ray (a) and pulsed-laser (b) parallel array sweeps. EMI pulses in (a) are removed for plot clarity. Each data set in (b) is offset by 3-µs for plot clarity.

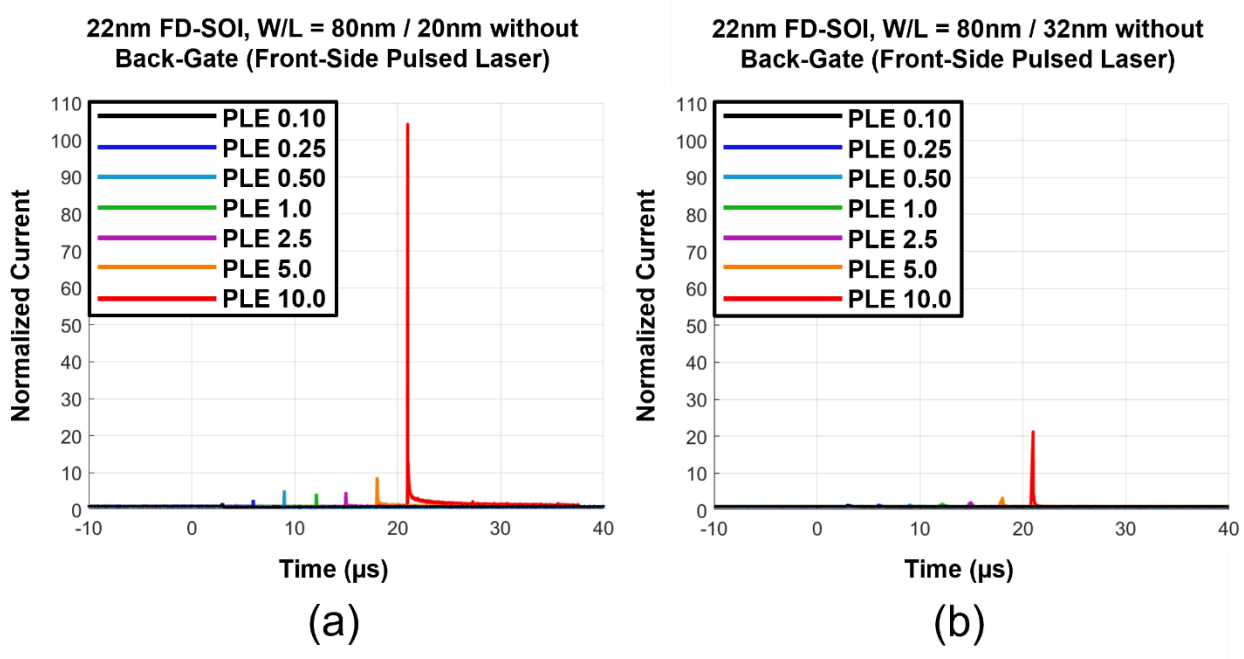

Figure 27 – Pulsed-laser energy sweeps from the 80nm / 20nm (a) and 80nm / 32nm (b) targets without back-gate up to PLE of 10.0. Each data set in both plots are offset by 3-µs for plot clarity.

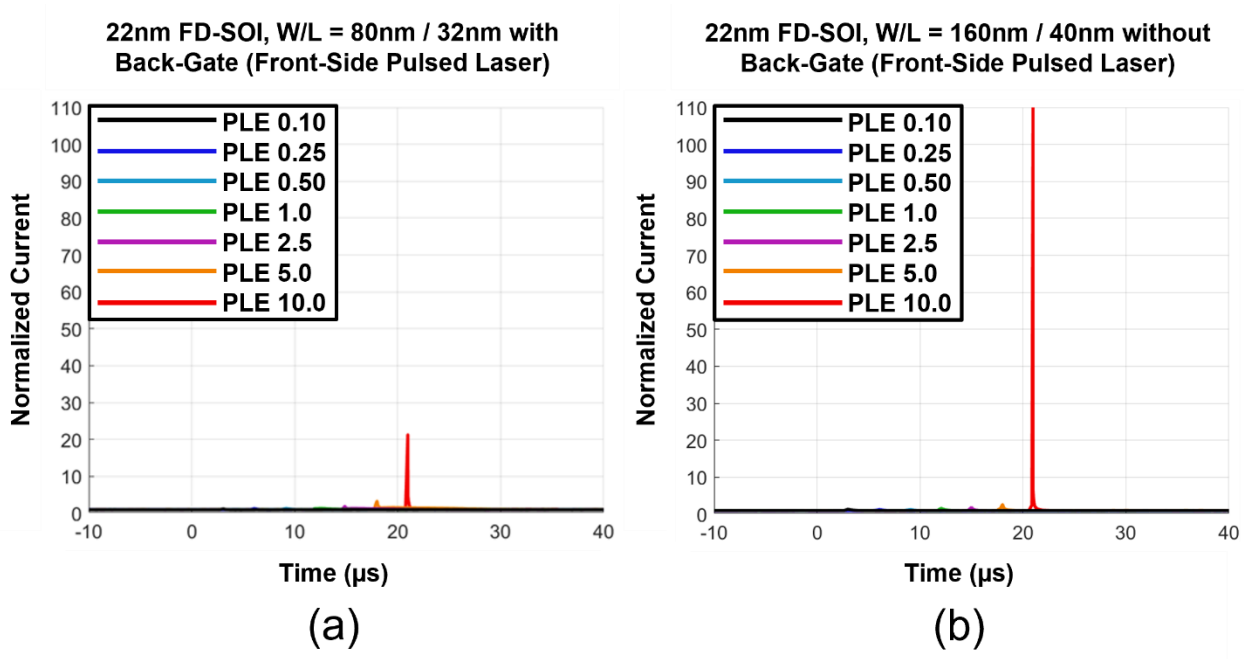

Figure 28 – Pulsed-laser energy sweeps from the 80nm / 32nm target with back-gate (a) and 160nm / 40nm without back-gate (b) up to PLE of 10.0. The back-gate wells are grounded. Each data set in both plots are offset by 3-µs for plot clarity.

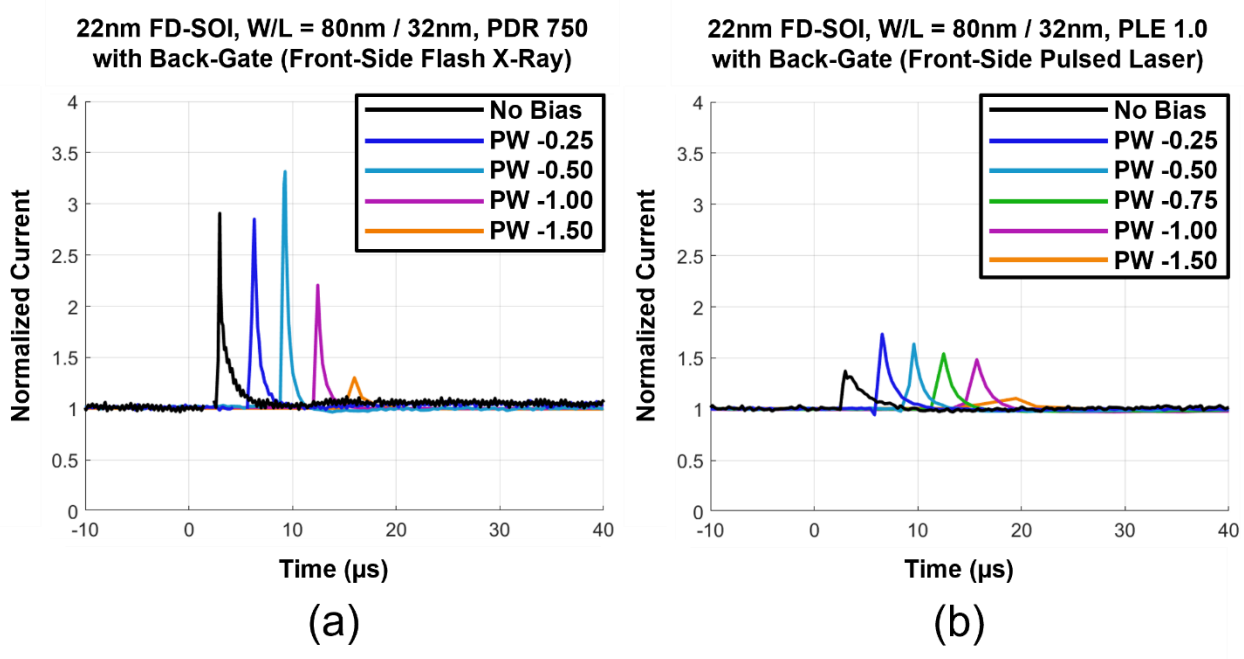

Figure 29 – Flash x-ray (a) and pulsed-laser (b) negative back-gate bias sweeps. N-well voltage is equal to the p-well voltage but positive. Offsets are applied to equalize leakage current in both plots. EMI pulses in (a) are removed for plot clarity. Each data set is offset by 3-µs for plot clarity.

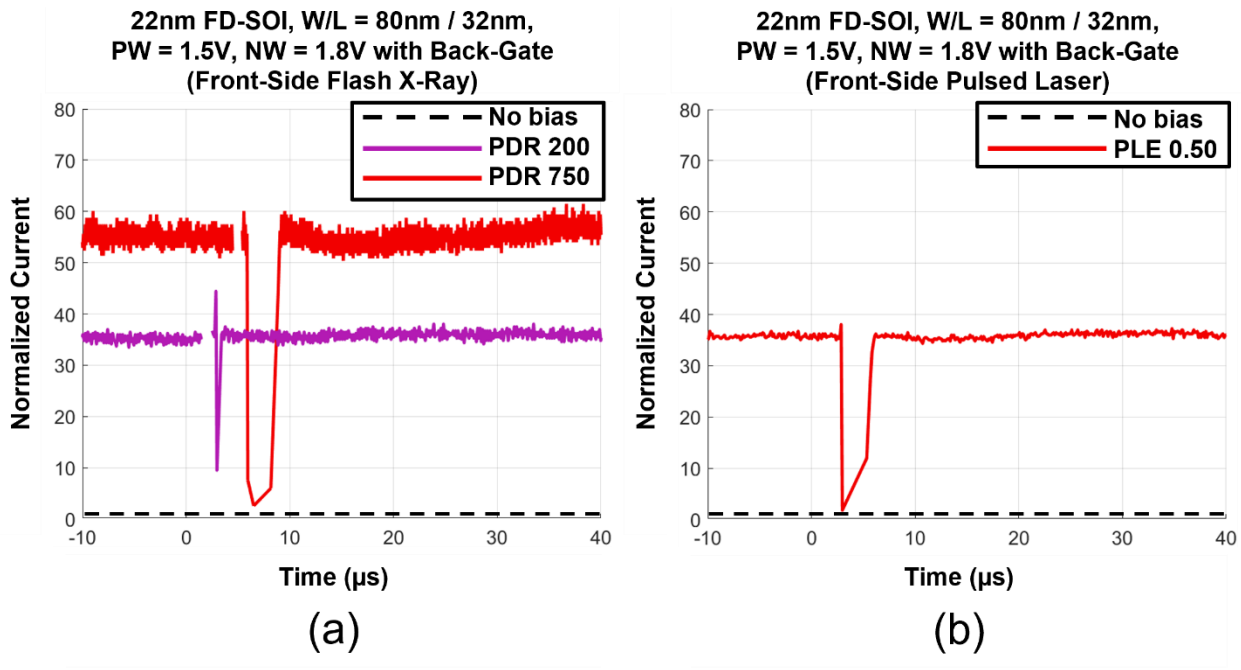

Figure 30 – Flash x-ray level (a) and pulsed-laser energy (b) sweeps with positive back-gate bias. Data in this configuration was only captured at a single energy from the pulsed laser. Current is normalized to leakage current with no bias and is represented with a dotted line in each plot. TID effects in (a) induced a significant threshold voltage shift that increased pre-irradiation leakage current in the PDR 750 case. EMI pulses in (a) are removed for plot clarity. Data sets in (a) are offset by 3-µs for plot clarity.

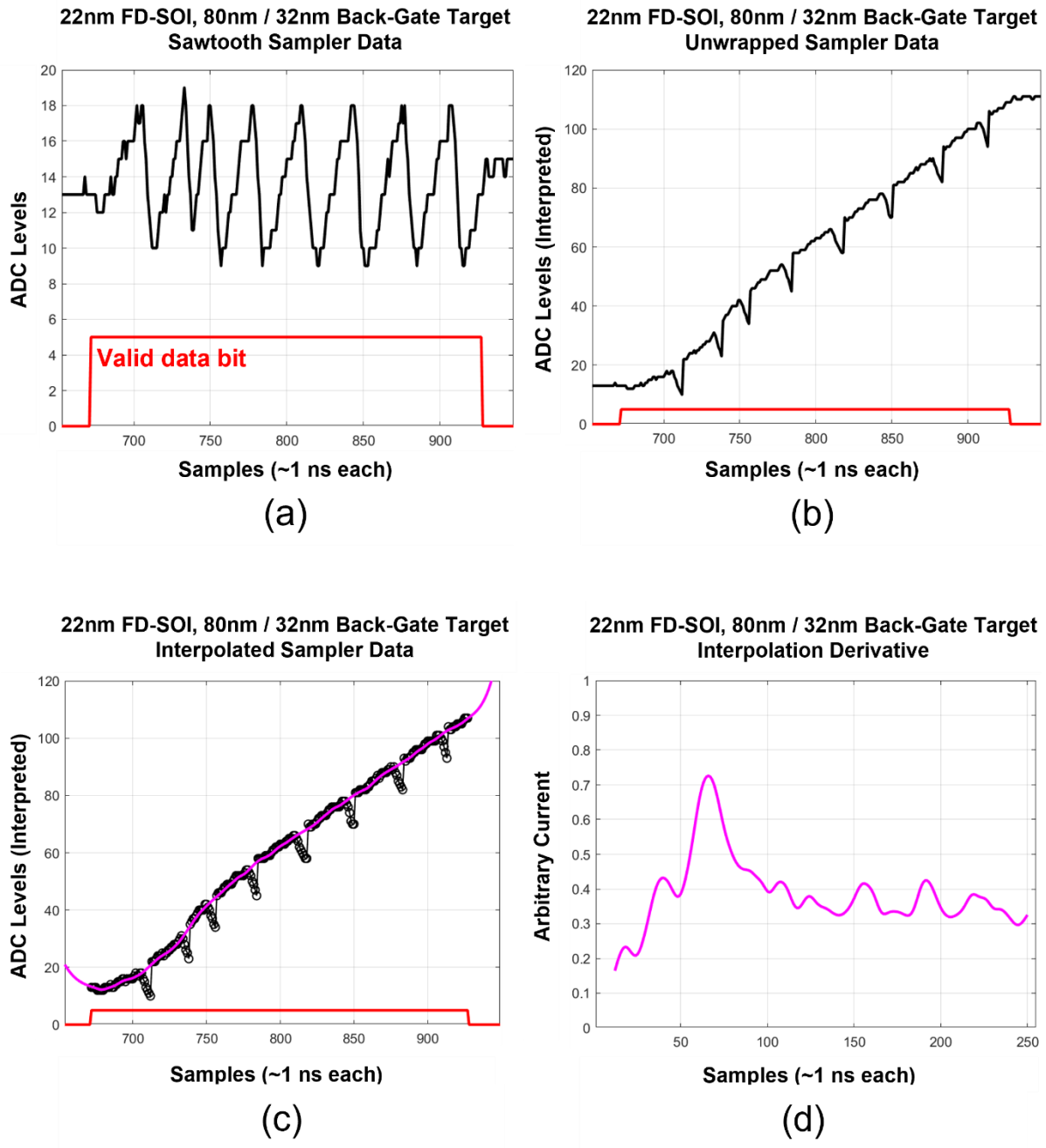

Figure 31 – Fine Measurement Stage data from 22nm FD-SOI at the FXR (a) raw ADC data from output of sampler with valid data bit (b) "unwrapping" of ADC data at each reset in sawtooth wave by applying a DC offset (c) smoothing spline interpolant of ADC data. Data during resets are ignored in the interpolation. (d) derivative of interpolation according to Equation (2).

Discussion

45nm PD-SOI – Parasitic BJT and Body-Tie

Results from both 22nm FD-SOI and 45nm PD-SOI indicate that secondary photocurrent effects and threshold voltage shifting dominate the transient response. This agrees with historical findings for SOI technologies [34] [37] [38]. In 45nm PD-SOI, there is evidence for the activation of a parasitic BJT [34] [56], as there is a consistent amplification mechanism at specific PDR and PLE thresholds. Also agreeing with historical findings, inclusion of a body-tie is extraordinarily effective at eliminating this parasitic BJT [34] [38], reducing peak photocurrent to nearly a tenth its floating-body counterpart. Peculiarly, the body-tie alters the response such that a slight negative current is measured. It is possible that the transient response of the PMC is responsible for this negative current, with perturbed input voltages to comparators in the Integration Stage modulating V_{range} from Equation (1). A parasitic BJT is still visible in the body-tied target, which supports that the source of this perturbation is from exterior circuitry. It should be noted that the prolonged response is not a circuit-level effect; built-in self-test (BIST) current transients do not produce any prolonged currents, and clear differences between the four target variants show that effects are originating from the targets.

45nm PD-SOI – EHP Generation and Saturation

Peak transient photocurrent from front-side lasing in 45nm PD-SOI is insignificant, with max energy of PLE 20 generating peak current less than leakage current. Peak photocurrent from back-side lasing saturates in some of the targets. Data from Figure 17(b) validates the notion that an upper bound exists for much drift current can manifest from EHP generation within a transistor. This is most likely the result of drain-loading in the targets; as current in the NMOS target increases, the drain voltage decreases, creating a stable feedback path. A detailed analysis of drain-

loading effects in photocurrent targets is investigated through 3D TCAD simulation in **Chapter V** and parasitic-extracted netlist simulations in **Appendix IV**. It is noteworthy that the analog floating-body NMOS targets appear to saturate between PLE of 1.0 and 2.0 and the digital floating-body NMOS targets are not saturated even at PLE of 5.0. Since peak photocurrent magnitude at the worst conditions never surpasses 8-times leakage current, a minimal circuit-level effect, and the FXR near facility max level was not saturating the photocurrent response of the devices, the 45nm PD-SOI process is likely inherently hardened to a prompt-dose radiation environment.

45nm PD-SOI – Linearity

The 45nm PD-SOI targets show excellent linearity with the number of parallel targets. Data from Figure 18(a) and (b) show that the transient photocurrent response will scale with the number of targets in an expected way, and this scaling is also evidence that transient photocurrent is generated in the targets and can be controlled.

45nm PD-SOI – Fine Measurement Stage Data

Though no interpretable shape could be extracted from Fine Measurement Stage data other than an instantaneous transition from pre-irradiation leakage to post-irradiation I_{PP}, these I_{PP} values corroborate peak current from the Coarse Measurement Stage, with the Coarse I_{PP} being less than 10% than the Fine I_{PP}. It will be seen in **Chapter 6** that these results match circuit simulations. Additionally, considering that the sampler is quantizing data at a frequency of approximately 1 GHz in these datasets, and that the FWHM profiles of both the pulsed-laser and FXR are 5.6 ns and 20 ns respectively, it is probable that the true photocurrent response is impulse-like. An explanation for this impulse-like behavior is buildup of charge for activation of the parasitic BJT. It will be shown in **Chapter 5** through 3D TCAD simulation of 45nm PD-SOI that the transient photocurrent response is most dependent on total EHPs generated and EHP generation rate; it is

almost independent of pulse width. Additionally, secondary photocurrent rises sharply over the course of a few nanoseconds. This finding supports the notion that thresholding is present for activation of this parasitic BJT and that measured data from the Fine Measurement Stage is accurate. Though not covered in detail in this work, it is notable that the 45nm PD-SOI Fine Measurement Stage is capable of recovering any arbitrary waveform loaded at 1 GHz, a feature achieved through inclusion of an on-chip high-speed arbitrary current waveform generator. This arbitrary current waveform generator enables exhaustive BIST procedures that confirmed proper operation of the Fine Measurement Stage prior to irradiation.

22nm FD-SOI – Parasitic BJT

Secondary photocurrent also heavily dominates in 22nm FD-SOI, but the source of these secondary effects are diverse and potentially indistinguishable without device-level simulation. The fully-depleted channel lacks the capacity to form a significant parasitic BJT and does not exhibit a prolonged transient response. However, secondary photocurrent effects lasting a few microseconds in targets without a back-gate are seen in Figure 22(a) and (b). If it is assumed that targets without the back-gate will not experience transient threshold voltage shifts from a perturbed substrate, then this secondary photocurrent is most likely activation of a parasitic BJT in the fully-depleted channel. It is also possible that this effect it not a parasitic BJT and results from n-well to substrate diode perturbations, discussed in the next sections.

22nm FD-SOI – With and Without Back-Gate

A clear lasting secondary photocurrent effect is observed in devices with the back-gate, while devices without the back-gate to not exhibit this response. It is important to recognize that these targets are otherwise identical. Data from Figure 24 indicates that the reversed-bias back-gate diode from Figure 2 is generating enough charge to perturb the isolated p-well voltage, which

in turn modulates the threshold voltage of the NMOS above the isolated p-well. Increase in NMOS leakage current corresponds to a decrease in threshold voltage, which corresponds to a positive transient voltage on the isolated p-well.

22nm FD-SOI – Back-Gate Effects from FXR and Pulsed-Laser

Back-gate targets respond differently at the FXR and pulsed-laser. The prolonged secondary photocurrent effects imply that the pulsed-laser is generating more EHPs in the back-gate than at the FXR, which is unsurprising given that front-side lasing is not uniform across the die. Metal stacks will reflect and diffuse laser light; the depletion regions in transistors are small in comparison to these metal stacks and may be easily blocked, while the depletion regions of the back-gates span hundreds of transistors and are not so easily blocked. Analysis of the optical absorption efficiency for front-side irradiation is complex as it requires calculation of optical trajectories and on-chip diffraction patterns accounting for all twelve metal stacks. Such analysis is beyond the scope of this work but may be relevant for the future if front-side lasing is ever to be considered.

22nm FD-SOI – Correlation to Drive Current

Peak photocurrent also appears correlated to drive current instead of depletion region volume. The 80nm / 20nm targets exhibit the largest peak photocurrent response, while the 80nm / 32nm and 160nm / 40nm targets exhibit a comparable response. This is further evidenced by data from Figure 29, where application of a negative voltage on the isolated p-well, increasing the threshold voltage of the NMOS and in turn decreasing drive current, significantly attenuated the transient photocurrent response. This effect could indicate that most of, if not all, transient photocurrent in 22nm FD-SOI is due to transient threshold voltage shift.

22nm FD-SOI – Non-Linear Current Increase and Device Failure

In Figure 22(a) and Figure 23(a), a sharp increase in photocurrent is observed. From a PDR level of 200 to 750, the increase in current is drastic. Little data past PDR of 750 is available in 22nm FD-SOI due to an unavoidable gap between the DUT and the FXR faceplate, so it is currently unknown if higher energies at the FXR would have induced failure. However, data from the pulsed-laser is available in Figure 27 and Figure 28. The jump from PLE 5 to 10 is extreme – some targets experience currents 100x that of leakage current, from less than 10x leakage current at PLE 5. Device failure was observed at PLE 15, and permanent damage to the die was sustained via shorted n-well voltages to ground and inability to control digital inputs. Investigation of the die and bond-wires revealed no external damage, so damage occurred on-chip. Determining the source of this failure mechanism is difficult without further study, but a likely source of failure is forward biasing of the n-well-substrate diode during irradiation. This is evidenced by three observations: first, the n-well was connected to ground via an unknown resistive element after irradiation at PLE 15. The substrate is grounded and is the only adjacent source to the n-well for ground, which renders damage between the two interfaces likely. Second, the targets experience an immense transient photocurrent response. If the substrate is debiased and takes on a transient voltage, this will lead to a significant threshold voltage shift in the devices which will appear as secondary photocurrent. The third and last observation which supports this hypothesis is from results from the 45nm PD-SOI DUT. The 45nm PD-SOI die contains only a p-substrate – there are no back-gate diodes in the technology. Even at PLE 20 with irradiation from the back, no damage to the die or additional transient photocurrent effects were observed.

If the source of this failure mechanism is indeed the back-gate diode, then SOI technology processes possess a unique radiation-hardening technique in transient photocurrent environments

by fully eliminating n-wells and in turn the back-gate diode. The n-wells in 22nm FD-SOI exist to provide low-power or high-performance operation through threshold shifting with back-gate voltages, but such convenience is not necessary for many applications. Simply removing the n-wells and implementing a chip-wide p-substrate could significantly harden 22nm FD-SOI and indeed other SOI processes that feature n-wells under the BOX.

22nm FD-SOI – Linearity

The 22nm FD-SOI targets show excellent linearity with the number of parallel targets. Data from Figure 26(a) and (b) show that the transient photocurrent response will scale with the number of targets in an expected way, and this scaling is also evidence that transient photocurrent is generated in the targets and can be controlled.

22nm FD-SOI – Well Debiasing

In a unique biasing condition, where the n-well and isolated p-well are both positively biased in such a way as to never forward-bias the diode between them, a positive voltage may be attained on the isolated p-well that significantly reduces the threshold voltage of the NMOS above. As seen in Figure 30, this positive p-well voltage can increase leakage current by over 30-times. At both the FXR and pulsed-laser, there is unambiguous evidence for the isolated p-well debiasing during irradiation, shown by the decrease in leakage current to near zero back-gate bias levels. This debiasing lasts for several microseconds and appears to be dependent on PDR level or PLE.

22nm PD-SOI – Sampler

Unlike data from the 45nm PD-SOI Fine Measurement Stage, where rise to I_{PP} appears instantaneous, there is a clear transient shape achieved through interpolation of 22nm PD-SOI sampler data. This result is significant, as it confirms that transient photocurrent data acquired in

45nm PD-SOI is impulse-like. Almost a polar opposite to this result, the rise-time for the 22nm FD-SOI dataset in Figure 31 takes place over a period of 100 ns. As it was previously determined that photocurrent effects in 22nm FD-SOI are produced by back-gate induced threshold voltage shift, this result is not surprising. The back-gates are weakly contacted; voltage transients on this back-gate diode will not be instantaneous.

45nm PD-SOI and 22nm FD-SOI Data Summary

Though the purpose of this work is not to specifically identify and model each transient photocurrent mechanism in these sub-50nm technology nodes, the PMC has made such analysis and modelling possible. Data from various targets in two different technologies nodes, all input to an identical on-chip measurement systems, shows the ability to isolate specific transient photocurrent mechanisms. Analysis of the data is straightforward; data from the Coarse Measurement Stage is presented as a lower bound, or moving average of current, and data from the Fine Measurement Stage is the interpolation of an integral. Both measurements leverage fundamental linear capacitor equations and require minimal interpretation. The radiation hardness of the PMC is highlighted, maintaining operation and linearity at remarkably high EHP generation rates.

CHAPTER 6

3D TCAD SIMULATION

Overview

Corroboration of on-chip transient photocurrent data captured by the PMC is critical for validation of the novel measurement techniques presented in this work. In order to accomplish this, 45nm PD-SOI transistor structures were modelled and simulated in 3D technology computer-aided design (TCAD) [26] software. The analog floating-body transistors were chosen for these simulations. These structures correspond to array 2 in Table A-1. However, simulation of targets this size is intractable in 3D TCAD; instead, a single device is simulated, and the photocurrent response is scaled appropriately. Other discrepancies are present when comparing physical and simulated test structures. The most significant of these is that photocurrent targets in the PMC are attached to a current mirror - the drain voltage is dynamic. In 3D TCAD, mimicking this current mirror exponentially increases simulation time and complexity. To simply this simulation, the drain voltage was characterized through Cadence Simulation of the PMC [32]. Both fixed-voltage and dynamic voltage simulations were performed in 3D TCAD. Fixed voltage simulations are accomplished by setting the drain voltages to values determined from pre-irradiation leakage current simulations in Cadence. The dynamic voltage simulations were performed by placing megaohm-level resistors between the drain and the power rail. These resistors attempt to bound the drain-voltage droop induced in PMOS current mirrors when input current increases. An example of targets in the PMC and 3D TCAD is illustrated in Figure 32. It will be shown in this

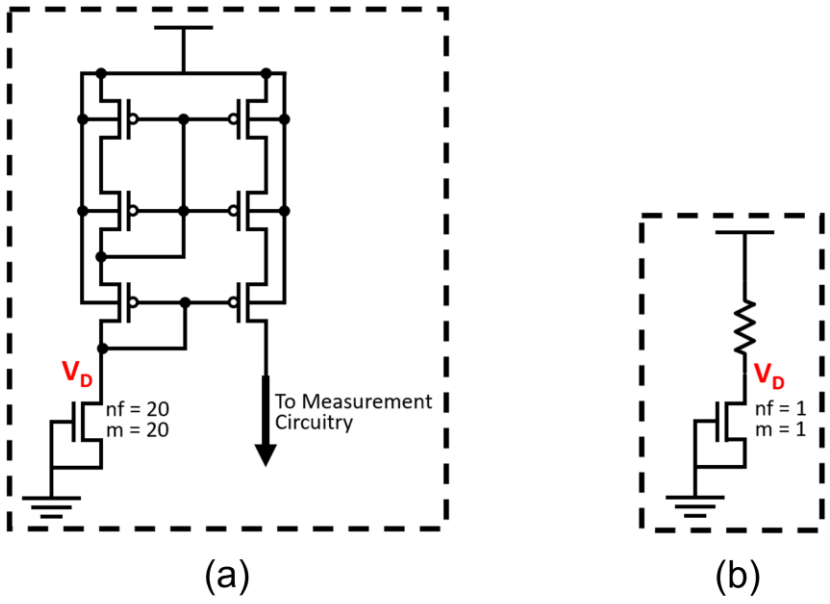

Figure 32 – Example schematic-level differences between (a) photocurrent target in the PMC and (b) modelled 3D TCAD target. In (a), the drain is connected to the input of a cascode current mirror and has a dynamic voltage. In (b), the current mirror is modelled with a megaohm-level resistor to mimic the high-impedance of the mirror. The number of fingers and parallel transistors in (a) is scaled while a single device is used in (b).

section that accurately modelling drain voltage is critical for recreation of data captured by the PMC, and the photocurrent attenuation caused by drain-loading is significant.

EHP generation rates (EHPGR) were set in 3D TCAD simulation to match FXR generation rates between PDR 100 and PDR 10000. Additionally, simulations were performed varying the pulse width to investigate the impact between the 20 ns FWHM profile of the FXR and the 5.6 ns FWHM gaussian profile of the pulsed-laser.

Results

Since simulated secondary photocurrent mechanisms from 3D TCAD simulation show excellent agreement with data, both FXR and pulsed-laser data are shown again in Figure 33(a) and (b) for reference. 3D TCAD EHPGR sweeps from level 100 to 10000 with a 5 MΩ drain load

resistance are shown in Figure 33(c) and (d), where the pulse width is varied from 20 ns to 6 ns respectively. Figure 34 details the impact of the drain load resistance swept from 0 Ω to 5 MΩ varying pulse width and EHPGR. The correlation of pulse width, total EHPs generated, and I_{PP} from 3D TCAD simulation is shown in Figure 35(a), and a similar comparison to FXR and pulsed-laser data is made in Figure 35(b). Finally, the pulse width dependence at equivalent EHPGR levels is investigated Figure 36 with detailed zoom-ins of 3D TCAD simulations from Figure 33(c) and (d).

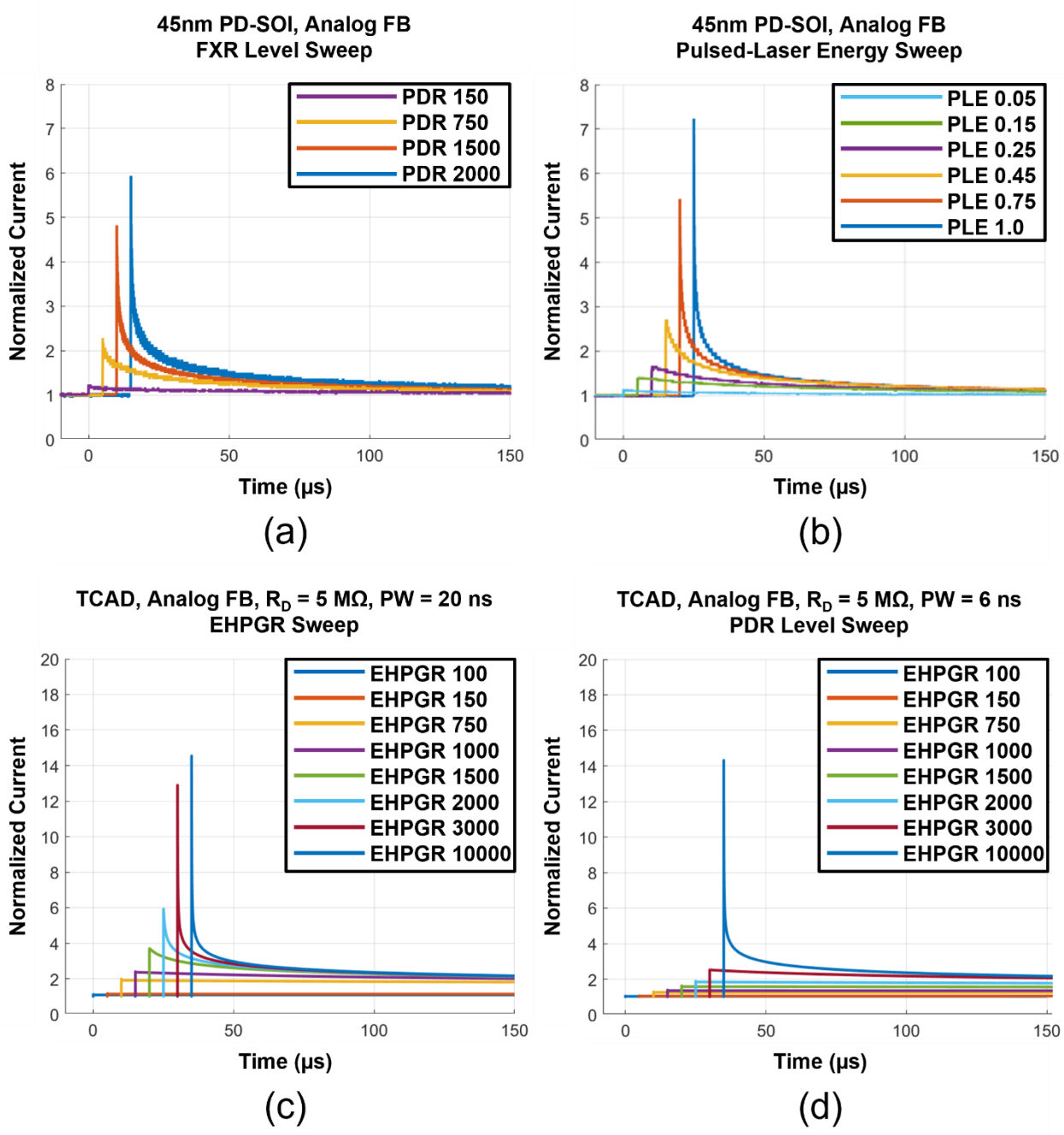

Figure 33– Comparison of FXR and pulsed-laser data from 45nm PD-SOI to 3D TCAD simulations (a) FXR level sweep data at a 20 ns FWHM irradiation profile (b) pulsed-laser energy sweep data at a 5.6 ns FWHM beam profile (c) TCAD EHPGR sweep at a 20 ns pulse width with a 5 MΩ load (d) 3D TCAD EHPGR sweep at a 6 ns pulse width with a 5 MΩ load

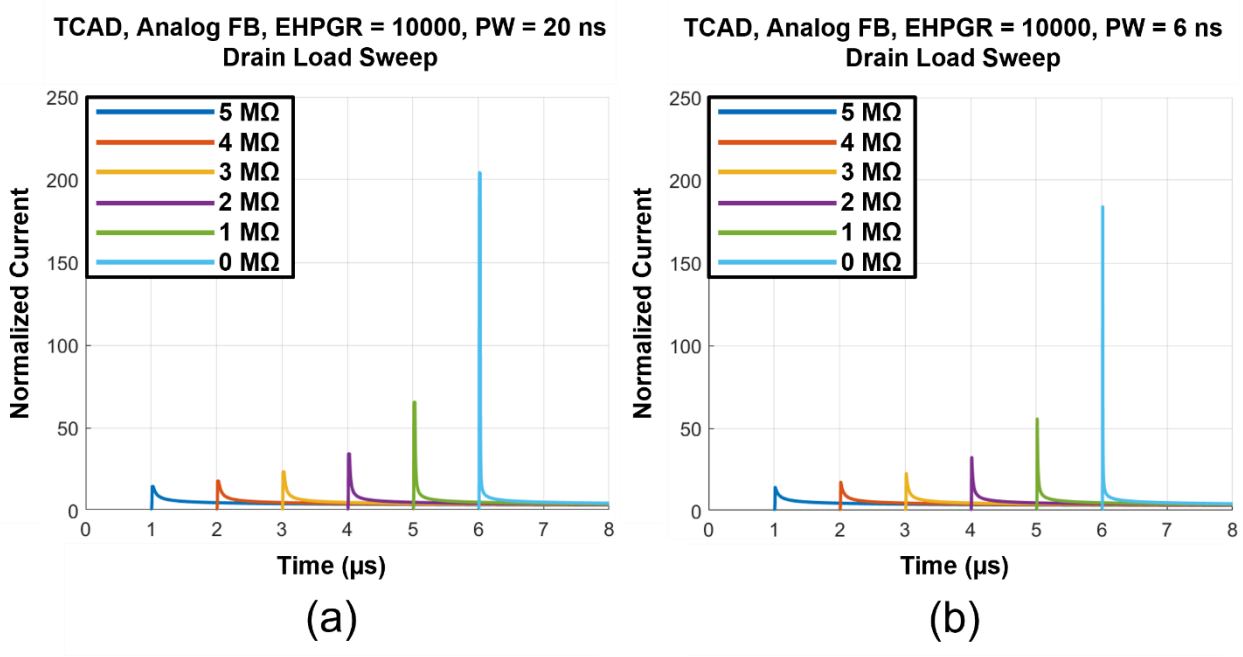

Figure 34 – 3D TCAD simulation of drain load resistance sweeps at (a) EHPGR of 10000 and PW of 20 ns (b) EHPGR of 10000 and PW of 6.

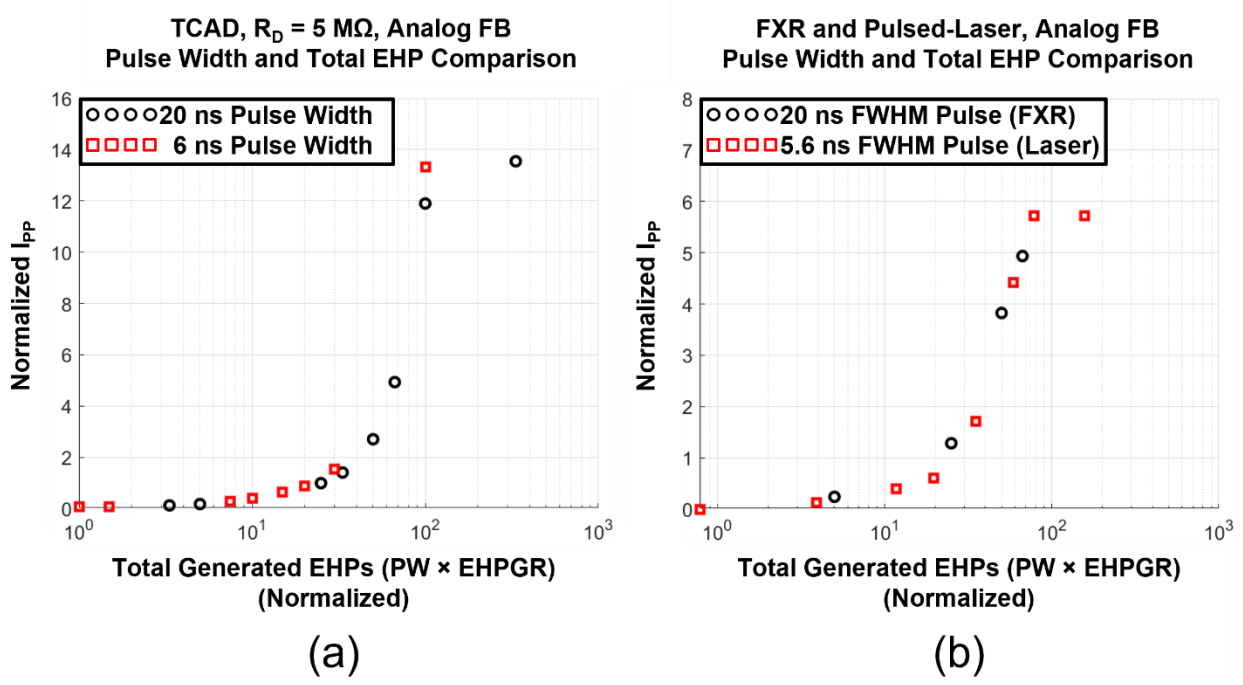

Figure 35 – Comparison of pulse width dependence from (a) 3D TCAD and (b) measured data from the FXR and pulsed-laser. Total EHPs are found in (a) by multiplying the pulse width by EHPGR. In (b), methods from [54] are utilized to correlate FXR and pulsed-laser EHP generation mechanisms.

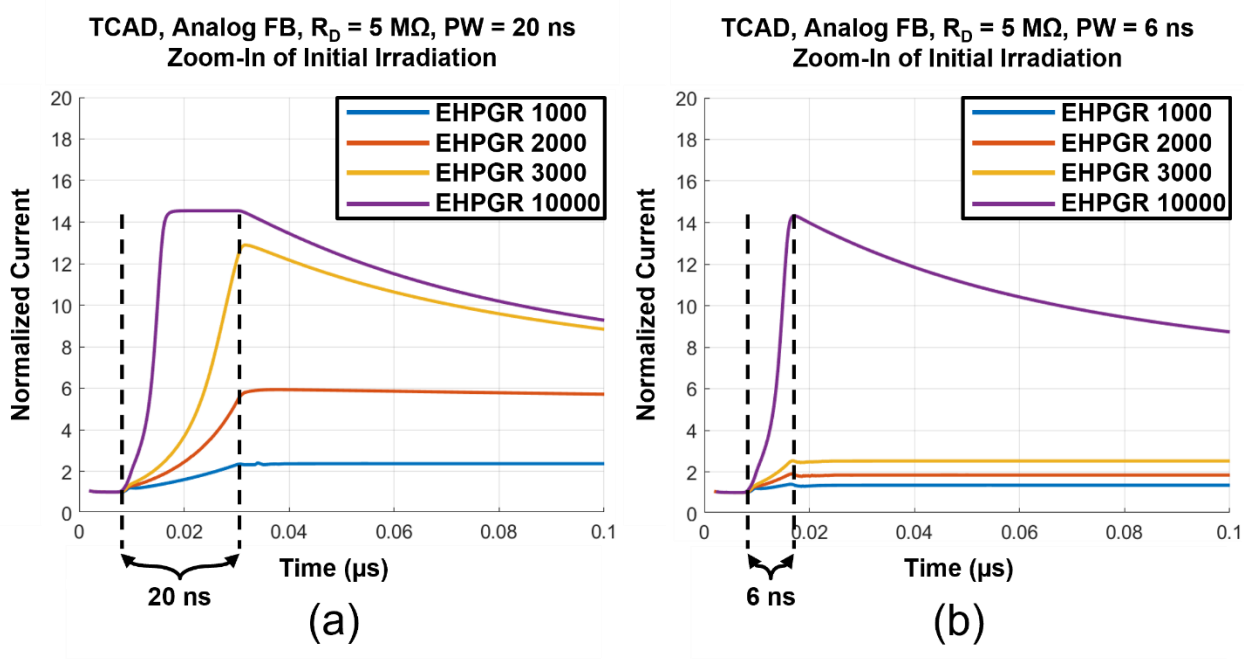

Figure 36 – 3D TCAD zoom-in of the initial irradiation at (a) 20 ns pulse width and (b) 6 ns pulse width. The period of irradiation is highlight in both plots.

Discussion

Activation of the Parasitic BJT and Impact of Drain Loading

3D TCAD simulations reveal that measurements made with the PMC are reasonable; comparable secondary photocurrent mechanisms are present in both data and 3D TCAD simulations. Data from Figure 33(a-c) details a similar trend seen from both the FXR and pulsed laser to 3D TCAD simulation. Though transient magnitude is off by a factor of two, activation of a parasitic BJT occurs in similar fashion; a negligible transient photocurrent response is followed by a sharp increase that saturates within the span of a tenth an order of EHPGR. The magnitude of current produced from this parasitic BJT is heavily dependent upon the drain load. In Figure 34, it is seen that a simulation without a drain load reaches current over 200-times pre-irradiation leakage current, an I_{PP} that may be more representative of devices with very little drain impedance. Both data from the pulsed-laser and 3D TCAD simulations indicate that drain-loading effects provide a

feedback path that attenuates maximum achievable peak photocurrent I_{PP}. Though the dynamic voltage produced at the input of a current mirror and the linear response from a resistor are vastly different, the principle behind drain-loading remains the same; if the potential difference between the source and the drain decreases, current must also decrease. As photocurrent magnitude rises, this drain voltage decreases – this is a stable feedback system. Further discussion of drain-loading effects and their impact of photocurrent measurement in the past is discussed in **Appendix IV**.

This result highlights the necessity for RHBD modelling efforts and device simulation in advanced physics-based software – assumption that I_{PP} measured in a target will match I_{PP} generated in devices without similar drain-loading may lead to unexpected failures. Such high currents are responsible for chip-wide rail-span collapse [41] [42] [43], a state where stiffening capacitance on power rails can no longer supply chip-wide photocurrent produced from the drain of both NMOS and PMOS transistors, resulting in voltage droop of power rails and probable failure.

Total EHPs and Pulse Width Dependence

In Figure 35(a), it is clear that inclusion of a 5 MΩ load increased the time constant of the simulated device to a point where there is little pulse width dependence at the nanosecond-scale. By evaluating the total EHPs generated at both the 20 ns and 6 ns pulses, comparable I_{PP}s are achieved when total generated EHPs align. This result is significant for comparisons between FXR and pulsed-laser data, which have 20 ns and 5.6 ns FWHM beam profiles, respectively. By converting to total EHPs generated, it is clear that PMC-measured data also features a pulse width independence, which is an expected result considering that the target drain load in Figure 32(a) is a multi-megaohm current mirror gate.

I_{PP} Saturation

A close-up of data from Figure 33(c) and (d) is shown in Figure 36(a) and (b) to investigate saturation of I_{PP} observed in pulsed-laser data, which was recreated in 3D TCAD. In Figure 36(a) at EHPGR 10,000, I_{PP} is reached well before the end of the 20 ns irradiation period and saturates due to the photocurrent-drain voltage feedback mechanism discussed previously in this section. This result confirms that data from Figure 13(b), where increasing PLE from 1 through 20 had no effect, is indeed the result of drain-voltage loading in the target.

Utilizing 3D TCAD for Circuit Design

3D TCAD simulation was an invaluable resource for gauging design choices in the PMC. Prior to this work, device-level transient photocurrent data was unavailable, which made design decisions regarding target selection and sizing challenging. Structures were created in 3D TCAD to mimic the targets in this work and were simulated at expected EHPGRs, producing waveforms that could be imported into circuit-level simulation. Based on these simulated waveforms, target sizing and current mirror optimization was possible. As detailed in Figure 7, the PMC operates within a defined region of linearity – this region of operation was partially guided based on these 3D TCAD simulations. PMC data closely following 3D TCAD results is an extraordinary result, not only for the PMC's ability to verify device-level models, but for effectiveness of 3D TCAD-based design guidance.

CHAPTER 7

CIRCUIT SIMULATION

Overview

Simulations in this chapter are performed in Cadence Virtuoso [32] upon circuits schematics that are incorporated in the final design of the 45nm PD-SOI implementations of the PMC. The purpose of this chapter is to verify recorded data at the FXR and pulsed-laser through simulation by recreating data via modelled primary and secondary photocurrent mechanisms. Simulations from the PMC in both technology nodes were performed prior to fabrication, yet simulations with inputs that follow real data will validate the efficacy of the PMC for use in RHBD model research. Outputs of these simulations exclusively originate from the Coarse Measurement Stage, where integrator frequency divided by two is the system output. Simulated current will be presented alongside the Coarse Measurement Stage interpretation from Equation 1.

Modelling

Basic modelling efforts are employed to recreate measured data by isolating photocurrent mechanisms and summing each modelled mechanism. From prior discussion in Chapter IV, these mechanisms in 45nm PD-SOI are: 1) Drift photocurrent proportional to depletion region size and 2) Secondary photocurrent from an activated parasitic BJT. Both are modelled in simulation by summing multiple exponential functions with varying damping coefficients. It is important to note that these models are not intended to be a perfect representation of the transient photocurrent mechanisms generated in the targets; creating usable transient photocurrent models is outside the scope of this work. These models are aimed to compare the simulation response of the PMC with known input waveforms. However, it is noteworthy how analysis of primary and secondary

photocurrent mechanisms utilizing the PMC enabled the production of first-pass models that follow measured data very closely. In conjunction with 3D TCAD analysis, it is likely that Cadence-usable models based on dynamic drain voltages discussed in **Chapter V** could be produced.

45nm PD-SOI Circuit Simulation

Simulation of the PMC while monitoring only the Coarse Measurement Stage is straightforward. The PMC reports a continuous modulated frequency that is proportional to the input current. In the state prior to irradiation, the PMC is recording only leakage current from the targets and reports a constant frequency. Post irradiation, this frequency fluctuates. During experimentation, an oscilloscope monitored this frequency for a period of 160 µs (150 µs post-trigger, 10 µs pre-trigger). To mimic this in simulation, the simulation ran for 160 µs, with irradiation occurring at 10 µs. Figure 37(a) is a simulation of the 45nm PD-SOI PMC with a transient photocurrent model from LVL 0 (no irradiation) to LVL 7 (transistor saturated) input from the targets. The dotted lines represent the current entering the PMC, while the solid lines are the Coarse interpretation of current after applying values from Equation 1. The model was calibrated to data from Figure 37(b).

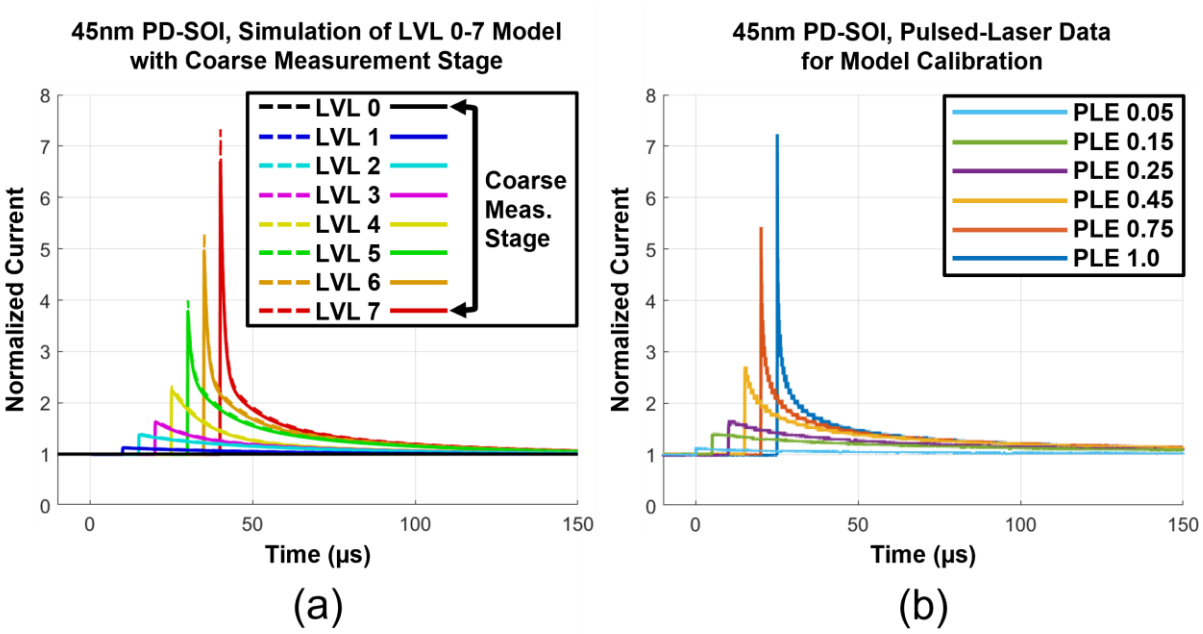

Figure 37 – Comparison of basic 45nm PD-SOI prompt dose model in simulation (a) versus pulsed laser data (b). Data in (b) is equivalent to data from Figure 13. Dotted lines in (a) are simulated current entering the Coarse Measurement Stage of the PMC. Solid lines in (a) are created from Equation (1) utilizing the integrator frequency.

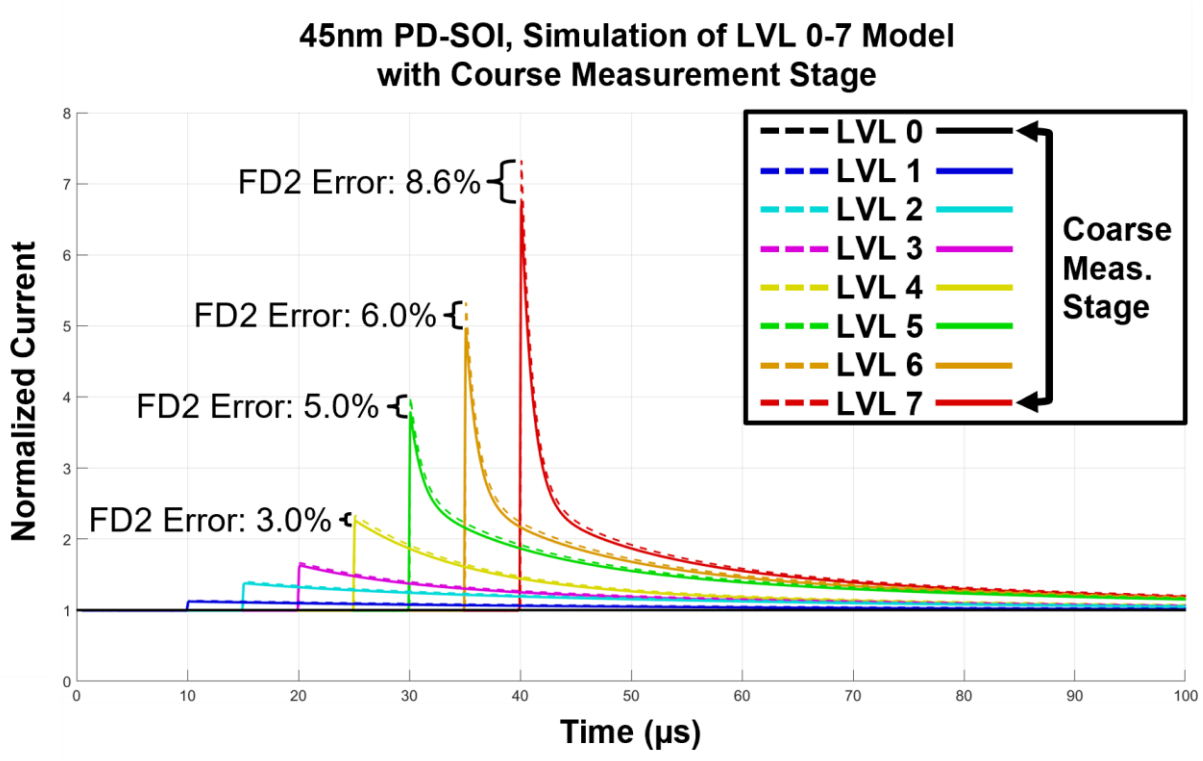

Figure 38 – Zoom in of Figure 37(a). Coarse Measurement Stage error (FD2) is shown at the peak of each current waveform past LVL 4.

Data from Figure 37(a) reveals that the Coarse Measurement Stage interpretation follows the input current closely. A zoom-in of Figure 37(a) is provided in Figure 38 for clarity, and the maximum error is provided for LVL 4-7. It was discussed in Chapter 4 that the Coarse Measurement Stage interpretation defines a lower bound for measured photocurrent provided that photocurrent is positive, which is clearly shown in Figure 38**.** Coarse Measurement Stage error is greatest at the apex of irradiation, where current changes most rapidly. At LVL 7 where primary photocurrent is greatest, the Coarse Measurement Stage error in simulation is less than 10%. These simulation results build confidence for data acquisition with the PMC and indicate that results from the Coarse Measurement Stage are valid for evaluating the transient photocurrent response.

CHAPTER 8

CONCLUSIONS

This dissertation presents the method, design, implementation, measurement results, and simulation verification of a novel on-chip transient photocurrent measurement circuit (PMC). Motivated by diminishing transient photocurrent amplitudes generated in integrated circuits transistors, which closely following Moore's law scaling, the PMC circumvents current attenuation and signal-to-noise ratio limitations by performing measurement on-chip. This on-chip measurement is made possible by leveraging the current-voltage proportionally of linear metal capacitors. This capacitor voltage is recorded as a continuous coarse measurement and a discreet fine measurement through specialized mixed-signal circuitry, each carefully constructed with technology-agnostic circuit elements to ensure design portability across multiple technology processes. The first implementation of the PMC is in the 22nm FD-SOI process and was later ported to the 45nm PD-SOI process with minimal alterations to the technology-agnostic design. Fabricated die are evaluated at a linear accelerator, flash x-ray, and infrared pulsed-laser source utilizing a facility-agnostic, open-air experimental setup designed to optimize experimentation efficiency. Successful data acquisition was achieved at both the flash-x ray and pulsed-laser source, and a myriad of transistor level effects across twelve different sub-50nm SOI targets were detected. Though the intrinsic hardness of sub-50nm SOI process was confirmed with these measurements, specific, unexpected weaknesses were identified that can result in device failure. Without the PMC's ability to characterize leakage-level currents, identifying the source of failure may have been impossible. Additionally, the linearity in the photocurrent measurement circuit was demonstrated, featuring the intrinsic ability to scale transient photocurrent magnitude through

addition of transmission-gated parallel target arrays. The radiation-hardness is also highlighted; the PMC maintained operation when transient photocurrent magnitudes were below transistor drive-current. In addition to capturing leakage-level transient photocurrents, these measurements results were corroborated through 3D technology computer-aided design (TCAD) and circuit-level simulations. In 3D TCAD simulations, comparable bipolar amplification mechanisms were recreated that closely follow data recorded with the PMC. This result is critical, as first-time measurements of on-chip photocurrents are able to confirm the reliability of such 3D TCAD simulations and models. Finally, the entire photocurrent measure circuit was constructed in circuit simulation software, and modelled photocurrent transients matching recorded data was input into the PMC. The simulated Coarse Measurement Stage recorded data that corroborates experimental data, adding an additional layer of validity for the PMC design.

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APPENDIX I

TARGET ARRAYS AND VARIANTS

Table A-1 45nm PD-SOI Targets

Array	Type	W/L (nm/nm) (Per Finger)	Fingers	W/L (nm/nm) Total per Array	Parallel Fingers	Body-Tied?
1	NMOS	152/40	400	60800/40	400-6400	N
2	NMOS	654/56	120	78480/56	120-1920	N
3	NMOS	654/56	96	62784/56	96-1536	Y
4	PMOS	152/40	400	60800/40	400-6400	N

Table A-2 22nm FD-SOI Targets

Array	Type	W/L (nm/nm) (Per Device)	W/L (nm/nm) Total per Array	Parallel Devices	Back-Gate?
1	NMOS	80/20	15600/20	195-6240	N
2	NMOS	80/20	15600/20	195-6240	Y*****
3	NMOS	80/32	15600/32	195-6240	N
4	NMOS	80/32	15600/32	195-6240	Y
5	NMOS	160/40	31200/40	195-6240	N
6	NMOS	160/160	31200/160	195-6240	N
7	NMOS	800/160	62400/160	78-2496	N
8	NMOS	800/160	62400/160	78-2496	Y

*** Isolated p-well floating**

APPENDIX II

OPERATIONAL SELF-TESTS

Table A-3 List of Operational Self-Tests

Self-Test	22nm FD-SOI TCV	45nm PD-SOI TCV
Target array parallelization and scaling	Pass	Pass
Coarse Measurement Stage frequency capture	Pass	Pass
Coarse Measurement Stage frequency is proportional to parallel arrays	Yes, within linear region of operation	Yes, within linear region of operation
Direct measurement of on-chip current sources	Pass	Pass
Current sources are proportional to coarse measurement frequency	Yes	Yes
Extraction of on-chip capacitance from current and frequency values	Pass	Pass
Highside and lowside voltage control	Pass	Pass
High-speed ADC and voltage reference functionality	Pass	Pass
4GHz ring-oscillator frequency halving and tuning	Pass	Pass
Fine Measurement Stage data capture	Pass*	Pass*
Fine and Coarse Measurement Stage record comparable currents	Yes	Yes
Back-gate bias threshold voltage control (22nm only)	Pass	N/A

***There is a chance upon power cycling the ring oscillator that the sampler in the Fine Measurement Stage will receive no clock signal. This flaw originates outside the sampler design – whenever the sampler is receiving both clock signals, it works as intended with no known issues.**

APPENDIX III

SUMMARY OF PULSED-LASER, FXR, AND LINAC TESTS

Pulsed-Laser

A total of 329 test shots were recorded at the pulsed-laser over the course of three days. 161 of these shots were recorded with the 45nm PD-SOI DUTs, and 168 shots were recorded with the 22nm FD-SOI DUTs. A total of 3 DUTs from 45nm PD-SOI and 2 DUTs from 22nm FD-SOI were evaluated. Front-side irradiation was ineffective in 45nm PD-SOI, so only 8 shots were recorded from the front. Back-side irradiation in 45nm PD-SOI was effective, which accounts for the remaining shots. In 22nm FD-SOI, all shots were from the front by necessity. Laser energies for both DUTs varied between PLE 0.01 to PLE 20.0, with the majority of the shots taking place in the range of PLE 0.1 to 5.0. PLE and the number of parallel arrays were the primary variables swept throughout testing; that is, each time laser energy was changed, the number of parallel arrays was swept at that energy. Data acquisition was only limited by the speed of data collection, so linearity sweeps that included each array were performed on specific targets. In 22nm FD-SOI, back-gate voltage sweeps were performed, which included negatively and positive biasing the isolated p-well and n-well. Data from the Coarse Measurement Stage is available for each shot. In 45nm PD-SOI, data from the Fine Measurement Stage is available whenever the ring-oscillator was active, which was approximately 10% of the shots. In 22nm FD-SOI, the ring-oscillator lost operation immediately following irradiation at most energies. Because of this failure mechanism, Fine Measurement Stage data is limited in 22nm FD-SOI, with successful data capture only taking place at exceptionally low laser energies.

Flash X-Ray

A total of 255 test shots were recorded at the FXR over the course of five days. 92 of these shots were recorded with the 45nm PD-SOI DUTs, and 163 shots were recorded with the 22nm FD-SOI DUTs. A total of 3 DUTs from 45nm PD-SOI and 2 DUTs from 22nm FD-SOI were evaluated. PDR levels were swept by varying the distance to the DUTs and FXR's faceplate. Levels for both DUTs varied between PDR 1.0 to PDR 2000, with the majority of the shots taking place in the range of PDR 150 to 2000. PDR levels and the number of parallel arrays were the primary variables swept throughout testing; that is, each time PDR level was changed, the number of parallel arrays was swept at that level. Data acquisition was limited by FXR recharge rate, which was roughly 8 minutes per shot, so linearity sweeps included only a few parallel array configurations. In 22nm FD-SOI, back-gate voltage sweeps were performed, which included negatively and positive biasing the isolated p-well. CT-probe measurements are available for both technologies, and ground-sense measurement are available in 22nm FD-SOI, where CT probe measurement did not detect any clear photocurrent transients. Data from the Coarse Measurement Stage is available for each shot. Data from the Fine Measurement Stage requires timing within a period of approximately 100-nanoseconds in order to capture the entire photocurrent transient. At the FXR, incident irradiation timing was random, which required many wasted test shots. Fortunately, enough data was gathered from shots that landed within an acceptable irradiation period that data from both 45nm PD-SOI and 22nm FD-SOI is available. Ring-oscillator failure was recorded in 22nm FD-SOI at elevated levels, so Fine Measurement Stage data is limited for 22nm FD-SOI. EMI shots were also taken at the FXR by removing the aluminum Faraday cage that surrounded the test board.

Linear Accelerator

A total of 449 test shots were recorded at the LINAC over the course of five days. Only the 22nm FD-SOI PMC was available during testing. A total of 4 DUTs were evaluated. PDR levels were swept by varying the distance to the DUTs and LINAC's faceplate; however, it was discovered that data from both the Coarse and Fine Measurement Stages indicated transient photocurrent several hundred-to-thousand times larger than expected. This discovery steered data acquisition away from the test plan to discover the source of this effect. Placing several inches of lead in line-of-sight to the LINAC, an inclusion that should block the high-energy electrons and eliminate transient photocurrent, had no impact on recorded data. This discovery led to the construction of a complete Faraday cage surrounding the DUT, which fully eliminated the recorded response. However, once the lead bricks were removed with this full Faraday cage, the effect returned. It was determined that EMI effects induced by the electrons could not be eliminated at the LINAC with the available setup. It was likely that transient photocurrent effects were present during these tests, but EMI effects were concurrent with transient photocurrent, obfuscating them. Despite this, the number of parallel arrays and distance to the LINAC was swept, and back-gate biasing effects were explored. Data acquisition with the Fine and Coarse Measurement Stages were successful, and the EMI response was characterized. This EMI response is comparable to the EMI response measured at the FXR, which is discussed in **Appendix V**.

APPENDIX IV

ON-CHIP PROPAGATION OF TRANSIENT PHOTOCURRENT

It is claimed in this work that off-chip measurement of nanosecond-scale transient photocurrent generated in sub-50nm SOI IC transistor arrays is ineffective due to combination of current attenuation and SNR limitations. It is worth noting that direct measurement data is available in the 45nm PD-SOI variant of the PMC, and no current signal was detected at any irradiation level with the maximum number of parallel arrays (6400 transistors). However, the PMC was not optimized for direct measurement of high-speed signals, and it is possible that additional parallel transistors could generate a visible signal.

To confirm that such transient photocurrent cannot easily be detected, a complete, parasitic-extracted (PEX) on-chip to off-chip measurement setup was laid-out in Cadence Virtuoso, detailed in Figure A-1. Fill generation was performed on all structures, which is the difference between "**A**" and "**B**" in Figure A-1. This setup includes PEX netlists for each photocurrent target in increments of 4,000 NMOS transistors. The source and gate of these transistors are grounded, and the drains are connected to a single output, shown as $\mathbf{I_D}$. To assume a best-case scenario, arrays are shorted at the output of this drain when placed in parallel. This parallel drain is then connected to the highest metal layer, labelled as "**C**."

For simulations performed with this on-chip to off-chip PEX model, a best-case scenario is assumed. Off-chip current measurement is probed in simulation through a small load resistor, and it is assumed that current-transformer (CT) probing is ideal. In addition, noise on the load is kept to a minimum; 10 MHz to 1 GHz random noise with a 40 mV peak-to-peak is generated on the output. The magnitude of this noise is smaller than the noise detected on I/O pins from the

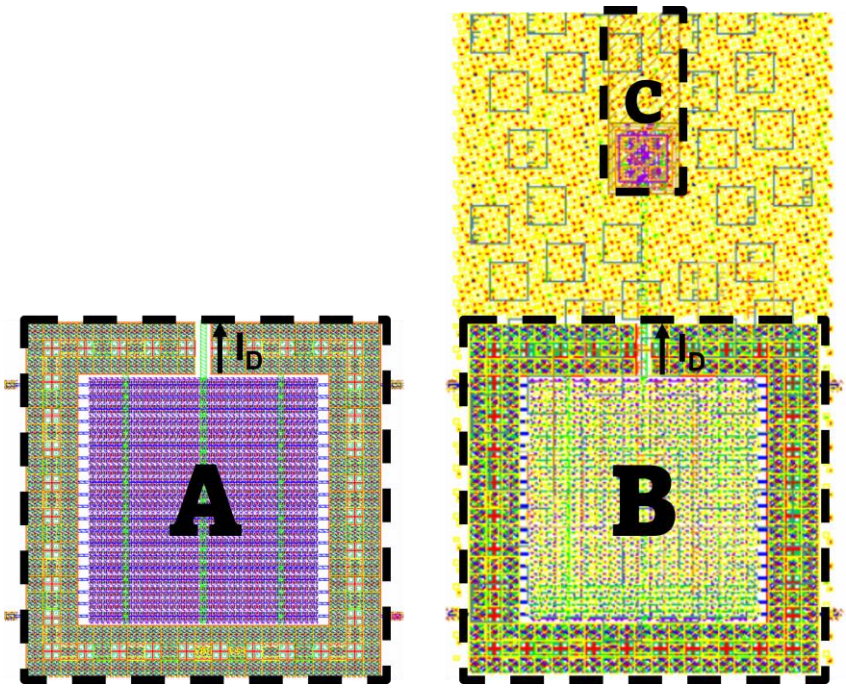
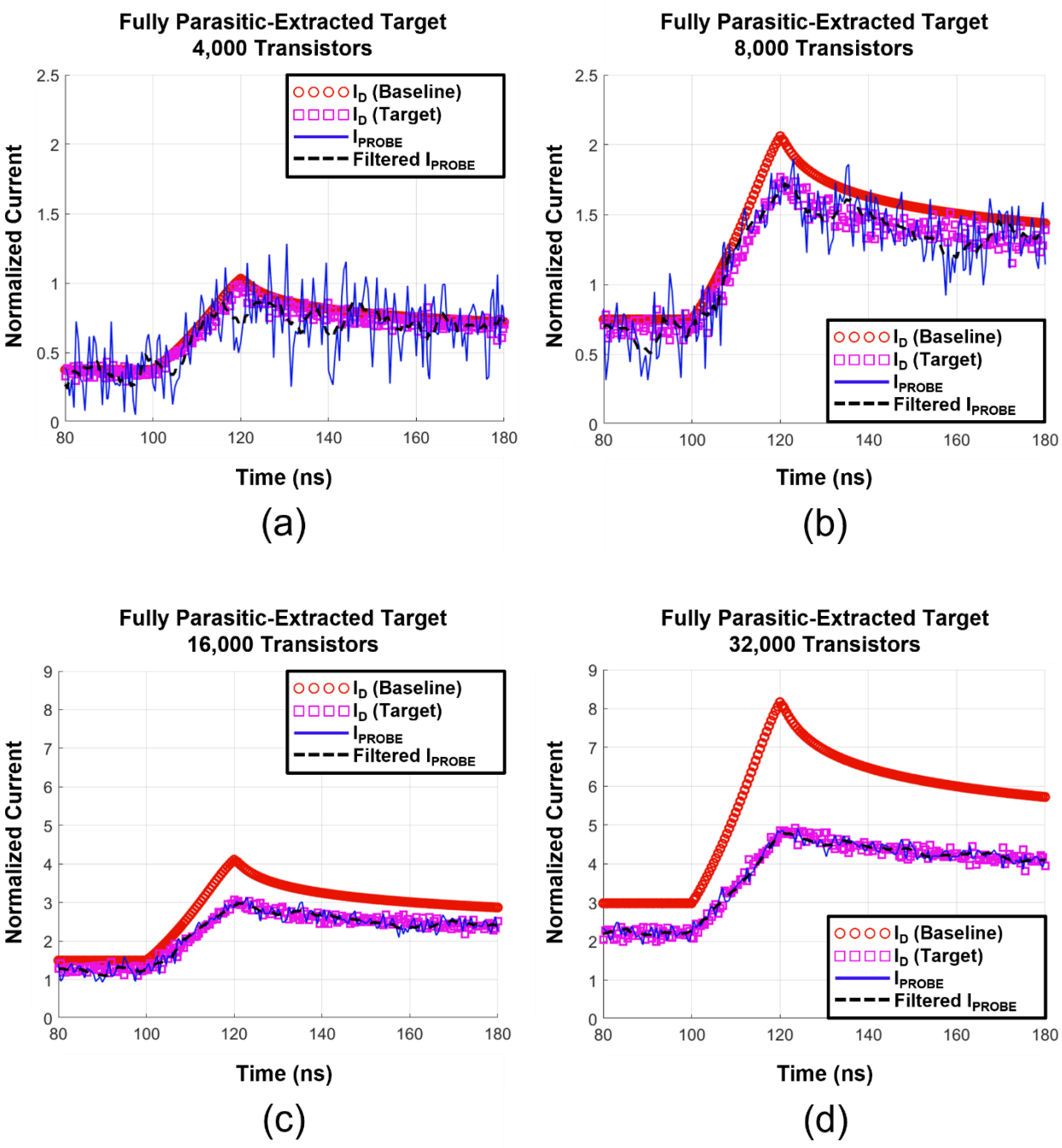


Figure A-1 Layout of transistor photocurrent target with and without PEX.
A) 4000-parallel NMOS transistor array. I_D is the output of the array.
B) 4000-parallel NMOS transistor array with complete fill generation.
C) Connection of array to top metal layer. Area surrounding is fill-generated.

TCV's shown in this work. Intrinsic on-chip noise is not modelled. In addition, powerful noise-inducing EMI effects detailed in **Appendix V** are not modelled.

In each simulation, transient photocurrent following characteristics from measured data in this work are generated in the targets. The magnitude of this transient photocurrent is calibrated to Array 1 from Table A-1 (digital floating-body targets) at PDRs close to FXR facility max. In each plot, a baseline transistor array drain current is shown as red circles. The drain of this transistor is connected to power. The drain current from the PEX modelled transistors is shown as purple squares. The current through the modelled load resistor, which would ideally match the drain current in purple, is shown as a blue line. A moving-average filtered version of this probed current is included in dotted black lines. The number of parallel

PEX-modelled transistors is scaled from 4,000 to 256,000 over 7 simulations, shown in Figure A-2(a)-(g). Simulation past 256,000 transistors was attempted but could not be performed due to limitations of dynamic memory in simulation software.



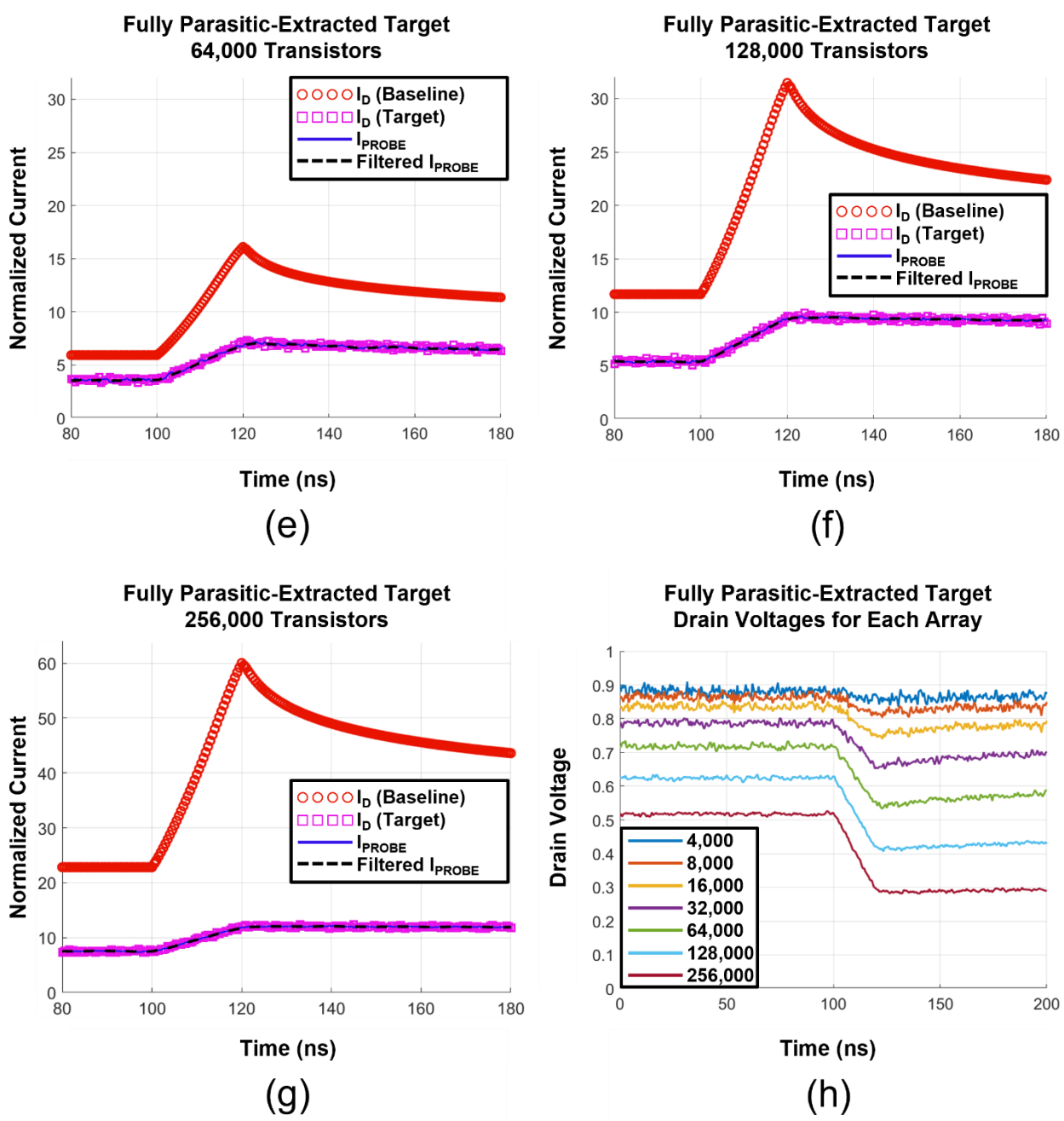


Figure A-2 Simulation results from fully-parasitic-extracted on-chip to off-chip direct measurement setup from Figure A-1. In (a-g), for "Baseline," the drain of parallel transistors is connected to power with no included parasitic structures. In "Target," the combined drain current from each target is probed at I_D in Figure A-1. I_{PROBE} is the ideal current of an off-chip current sense resistor. Filtered I_{PROBE} is a moving average filter of I_{PROBE}. In (h), the drain voltages from (a-g) are plotted.

Results from the simulation in Figure A-2 reveal two major effects resulting from inclusion of parasitic structures. The first of these is a significant decrease in peak photocurrent magnitude compared to the baseline. This attenuation results from loading of parasitic structures at the drain of the targets, shown in Figure A-2(h), which becomes a significant contribution to error past 8,000 parallel transistors (33% error). As more parallel transistors are added, this error increases. Additionally, pre-irradiation leakage current is observed to decrease per transistor due to drain-loading. It is possible that past direct measurement efforts have reported comparable results without accounting for this drain-loading effect. This possibility highlights the necessity for parasitic analysis of such structures to determine the impact of internal drain-loading prior to irradiation. For this work, this result concludes that adding additional parallel arrays to overpower SNR limitations is not a viable solution for an accurate emulation of baseline transistor-level photocurrents. However, additional transistors does increase peak photocurrent amplitude, which is eventually sufficient for signal detection.

Though these results indicate that direct measurement is possible in sub-50nm SOI, there are several significant disadvantages, which on-chip measurement with the PMC circumvents. Because measurement takes place locally in the PMC, requiring only hundreds of transistors opposed to tens-of-thousands, signal attenuation and SNR limitations are completely avoided.

APPENDIX V

EMI EFFECTS AT THE LINAC AND FXR

It was observed that EMI effects induced on-chip current transients in both 22nm FD-SOI and 45nm PD-SOI that were orders of magnitude greater than transient photocurrent. Initial testing at the LINAC was inconclusive, as EMI effects manifested within a time period that obfuscated transient photocurrent. These EMI effects at the LINAC persisted even with a full Faraday cage surrounding the DUT and ribbon cables, shown in Figure A-3(a). The EMI effects grew in magnitude with decreasing distance to the LINAC. All efforts to isolate the transient photocurrent response from EMI-induced current was unsuccessful.

Testing at the FXR induced EMI effects comparable to the LINAC, even with a full Faraday cage, shown in Figure A-3(b). However, these effects manifest approximately 400-

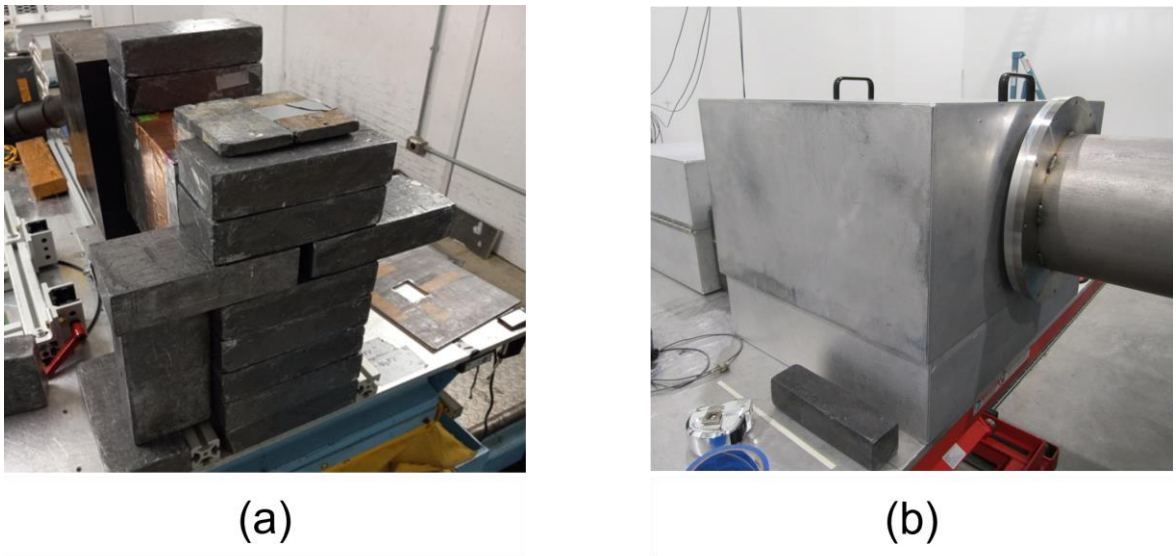


Figure A-3 Faraday cages at the (a) LINAC and (b) FXR. In (a), a small slit is made in direct path of the beam to allow electrons to penetrate the lead wall. Behind this slit, the DUT is sealed by aluminum tape.

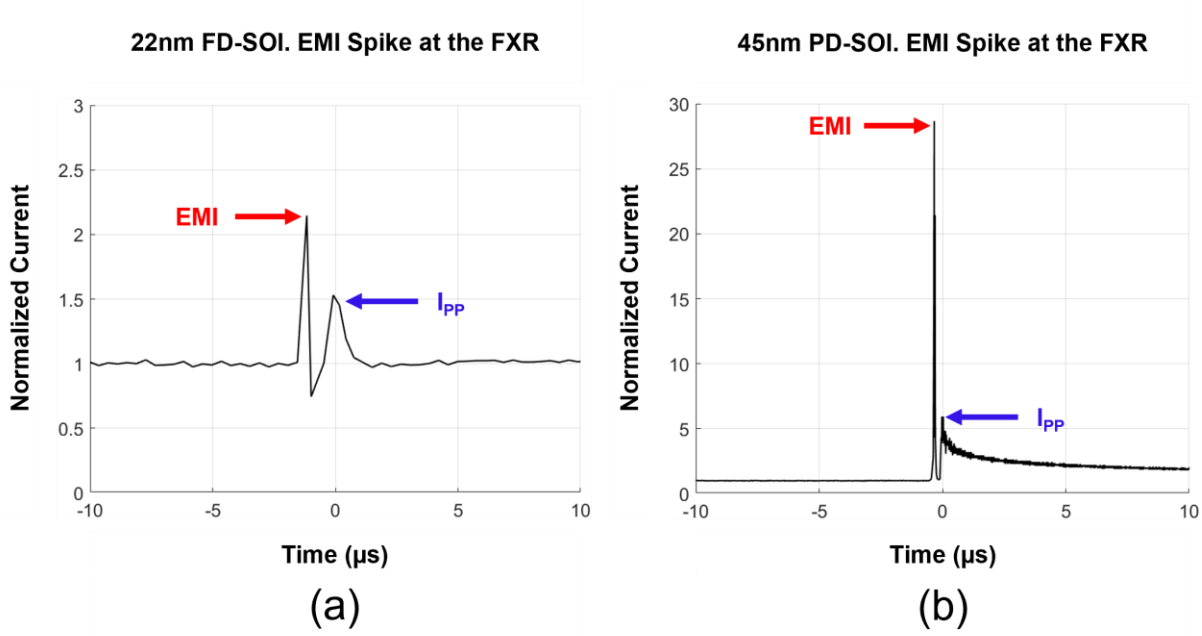


Figure A-4 EMI effects observed at the FXR in (a) 22nm FD-SOI and (b) 45nm PD-SOI. "EMI" refers to peak current manifesting approximately 400-ns before arrival of transient photocurrent and "I_{PP}" refers to peak current induced by transient photocurrent.

nanoseconds before irradiation occurs, so both EMI effects and transient photocurrent were captured separately at the FXR. An example of noise spikes for 22nm FD-SOI and 45nm PD-SOI is shown in Figure A-4(a) and (b).

For plot clarity, noise from the FXR was removed from trends and plots shown in this work by nullifying data within the known period of the EMI effect, which was consistent from dataset to dataset. The existence of such a current spike, however, is significant. Peak photocurrent I_{pp} is often analyzed as an important parameter in radiation effects literature because it may be compared to drive current in digital circuitry and determine failure thresholds. If a photocurrent detection circuit wrongfully conflates EMI-induced current with I_{pp}, false data could be reported. Indeed, EMI-induced current was initially conflated with photocurrent at the FXR and was isolated only after a thorough investigation of data. If this EMI-induced current at the FXR occurred less than a

microsecond later, no photocurrent data would have been measurable. Because of this EMI volatility, the pulsed laser is an excellent choice for fully isolating transient photocurrent mechanisms. The laser induces no observable noise or EMI effects and may be utilized prior to testing at a LINAC or FXR to confirm the transient photocurrent response of a system.

APPENDIX VI

DATA PRESERVATION IN THE SAMPLER

A critical design requirement for the Fine Measurement Stage is ensuring that sensitive ADC circuitry is protected during irradiation. However, designing a 32-level, multi-GHz speed flash ADC that is hardened to transient photocurrent effects is an intractable approach, especially for technology-agnostic design. Instead, an approach was implemented that completely avoided quantization during irradiation and postponed it until a much later time period. This was achieved using a 256-stage voltage sampler, which takes analog "snapshots" of the desired ADC input voltage and holds these voltages for post-irradiation quantization. With this approach, the radiation-hardening of the ADC is unnecessary, and design efforts were focused on high-

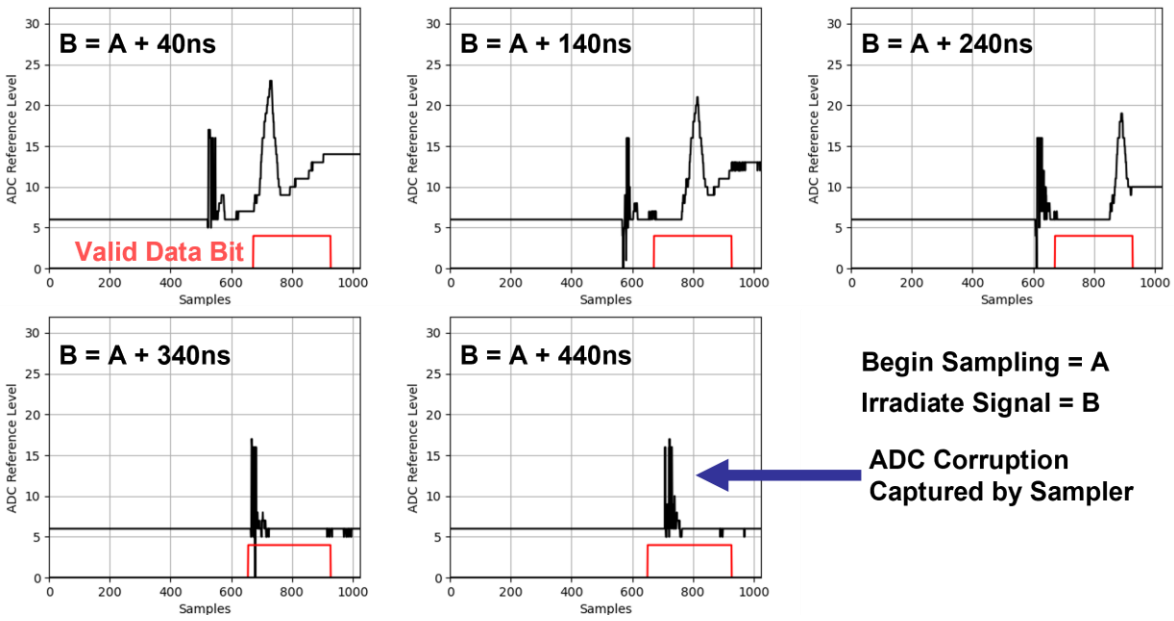


Figure A-5 Example datasets from the LINAC showing ADC corruption during irradiation. The begin irradiation signal is represented in time by "A," and the facility irradiate signal is represented by "B." The ADC fails when quantization is performed during irradiation.

performance. It can be seen that in Figure A-5, not only was the sampler effective at preserving data, the ADC would have also failed during irradiation. ADC corruption was able to be detected by timing the facility trigger signal to be aligned with the period of ADC quantization.

APPENDIX VII

CATALOGUE OF LAYOUTS AND SCHEMATICS FROM THE PMC

This section highlights layouts and schematics of the novel designs utilized in both the 45nm PD-SOI and 22nm FD-SOI variants of the PMC. Common layout structures or schematics required for chip functionality will not be covered.

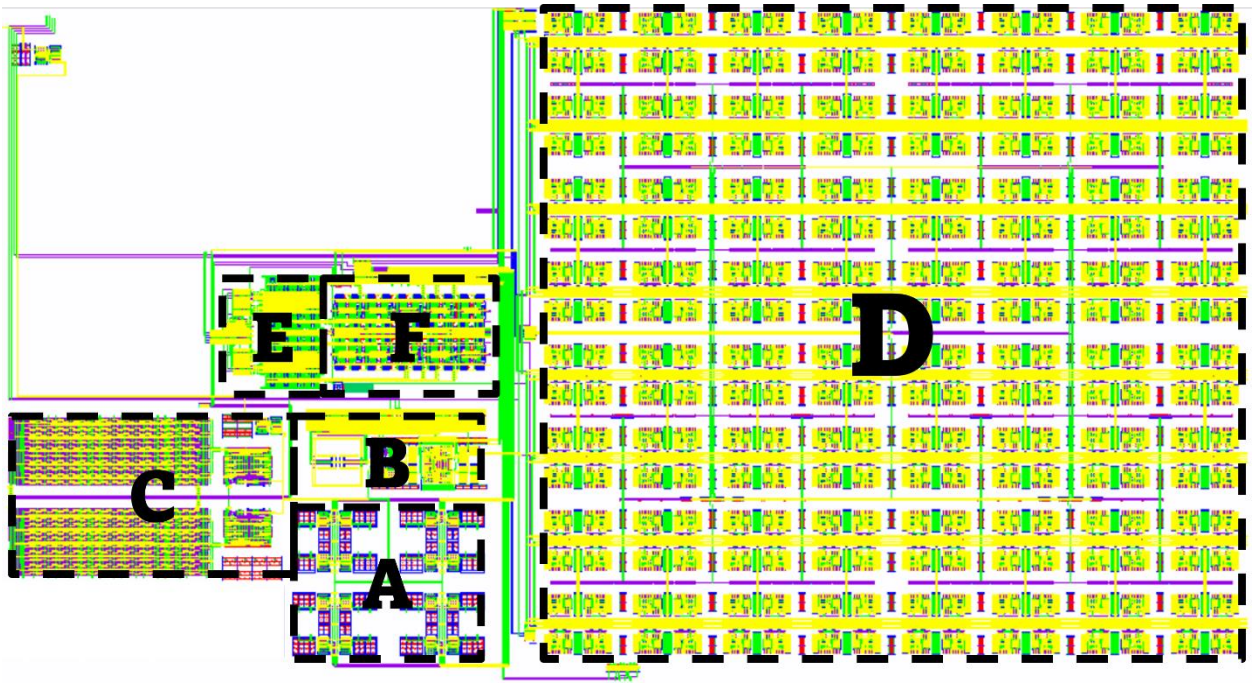


Figure A-6 Full layout of one 45nm PD-SOI variant of the PMC.
A) Photocurrent arrays – 16 total
B) Integrator, i.e., the Coarse Measurement Stage
C) Arbitrary Current Waveform Generator, i.e., the Built-In Self-Test
D) Sampler, i.e., the Fine Measurement Stage – 256 total sample cells
E) 32-Level Flash Analog-to-Digital Converter
F) 32-Level Switched Capacitor Voltage Reference

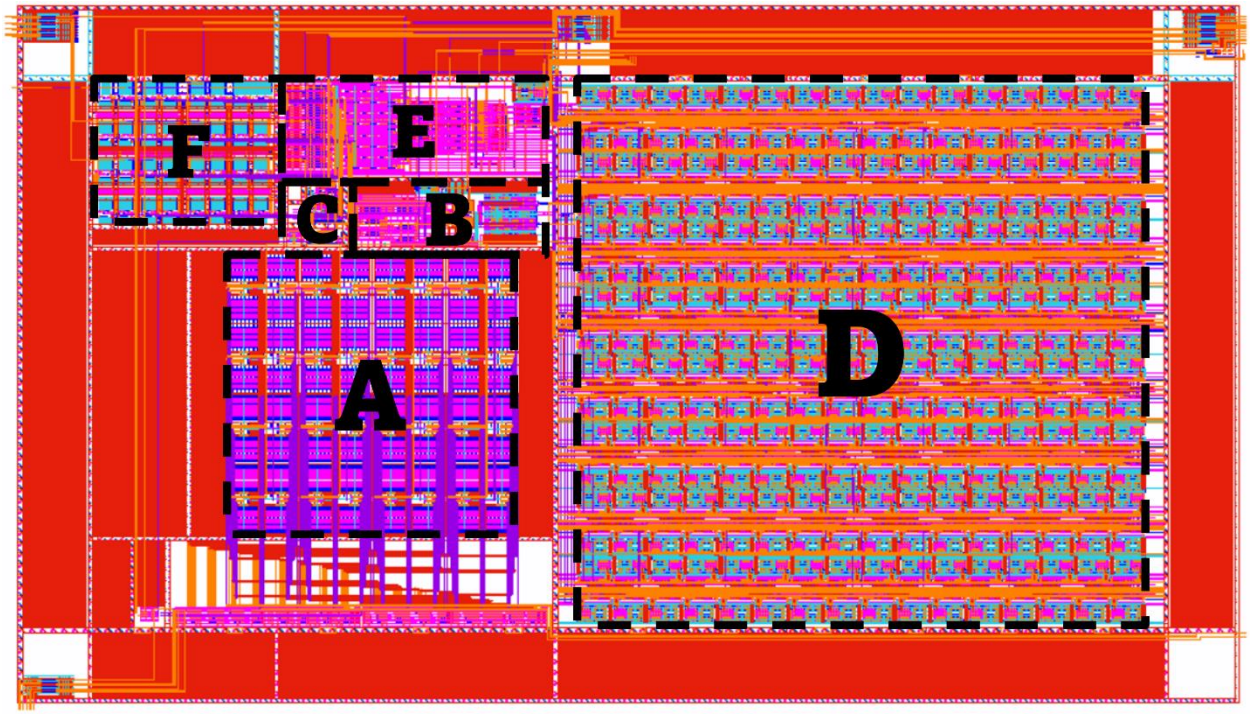


Figure A-7 Full layout of one 22nm FD-SOI variant of the PMC.
A) Photocurrent arrays – 32 total arrays per variant, 2 variants
B) Integrator, i.e., the Coarse Measurement Stage
C) 4-Level Built-In Self-Test
D) Sampler, i.e., the Fine Measurement Stage – 256 total sample cells
E) 32-Level Flash Analog-to-Digital Converter
F) 32-Level Switched Capacitor Voltage Reference

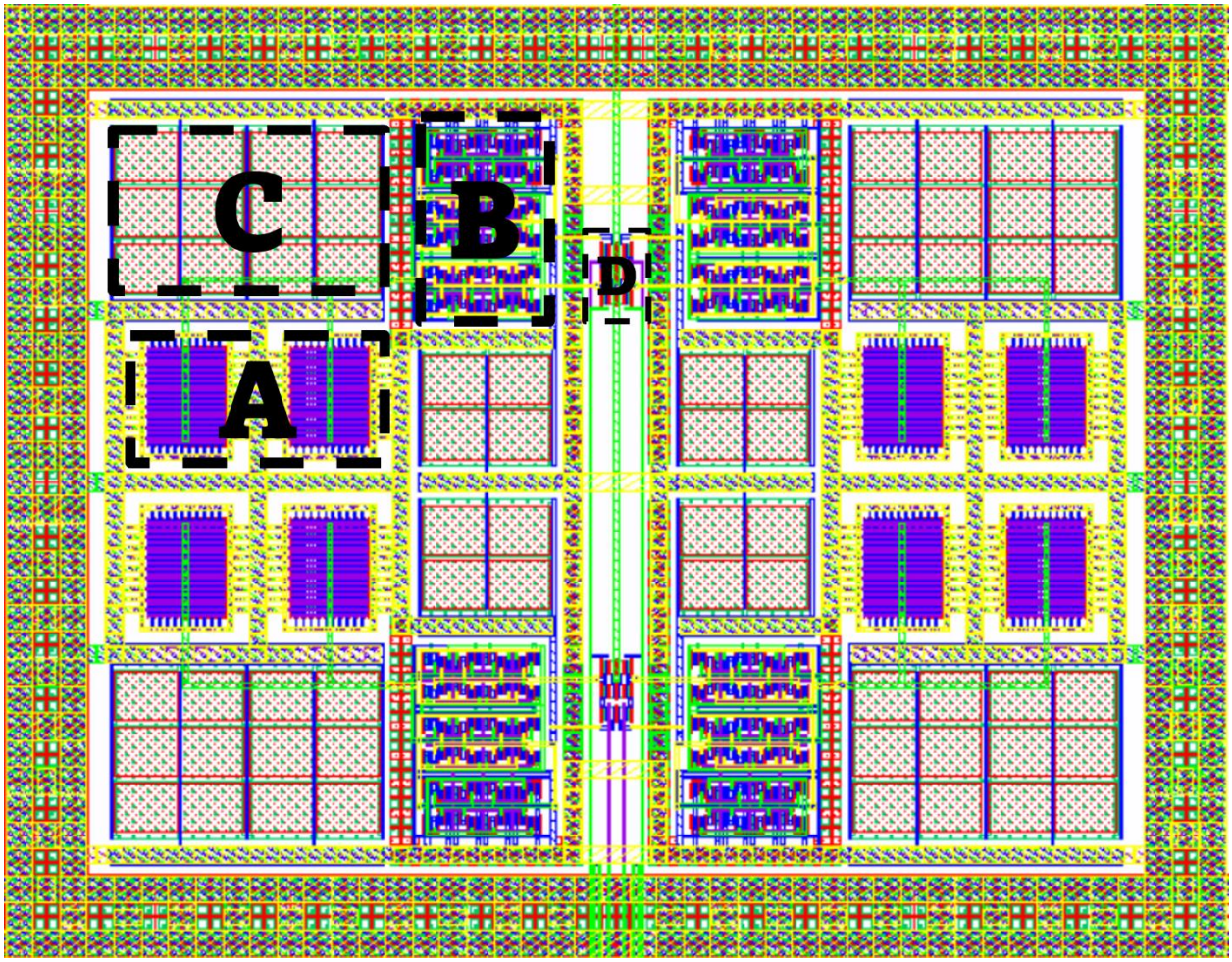


Figure A-8 Layout of four 45nm PD-SOI photocurrent arrays.
A) One photocurrent array with 400 parallel transistors
B) Photocurrent mirror
C) Decoupling capacitors
D) Transmission gating and logic

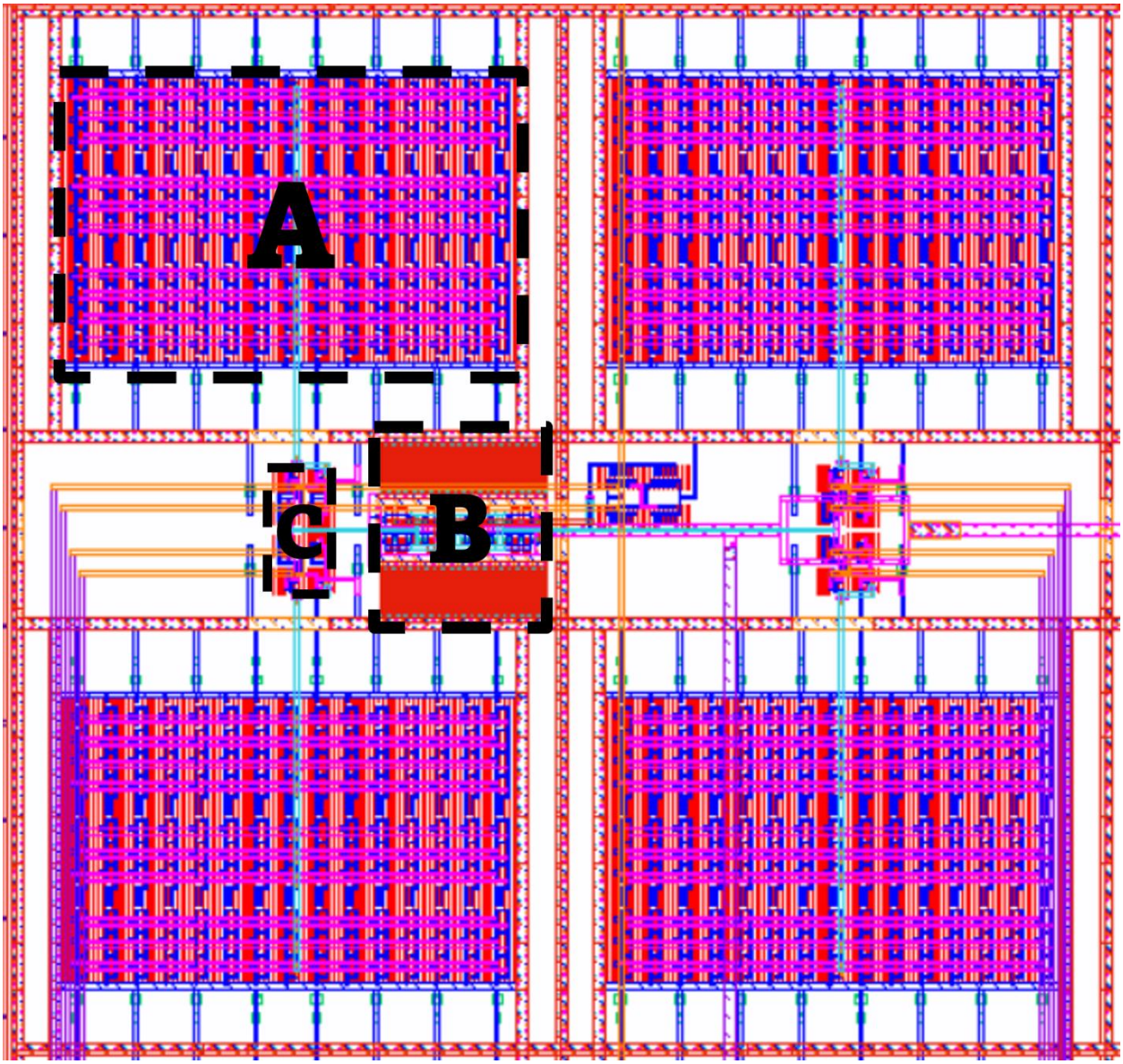


Figure A-9 Layout of four 22nm FD-SOI photocurrent arrays.
A) One photocurrent array with 195 parallel transistors
B) Photocurrent mirror
C) Transmission gating and logic

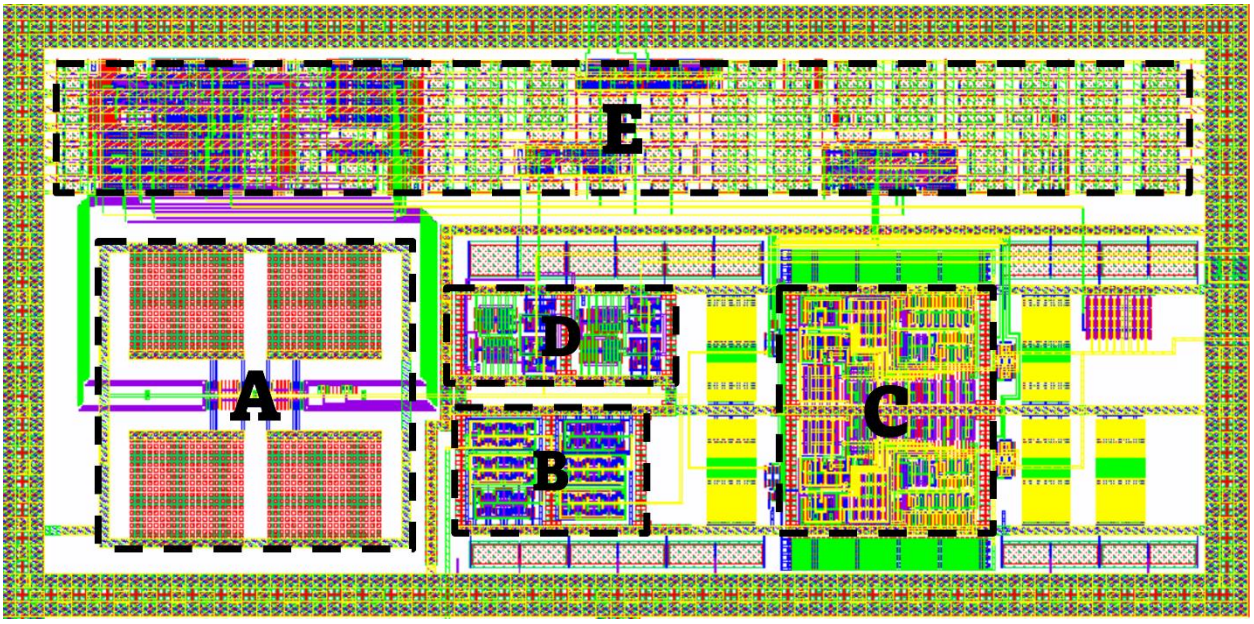


Figure A-10 Layout of the 45nm PD-SOI Coarse Measurement Stage
A) Sawtooth integrator
B) Input photocurrent mirrors
C) Sawtooth buffer pair
D) Highside and lowside comparators
E) Digital control logic

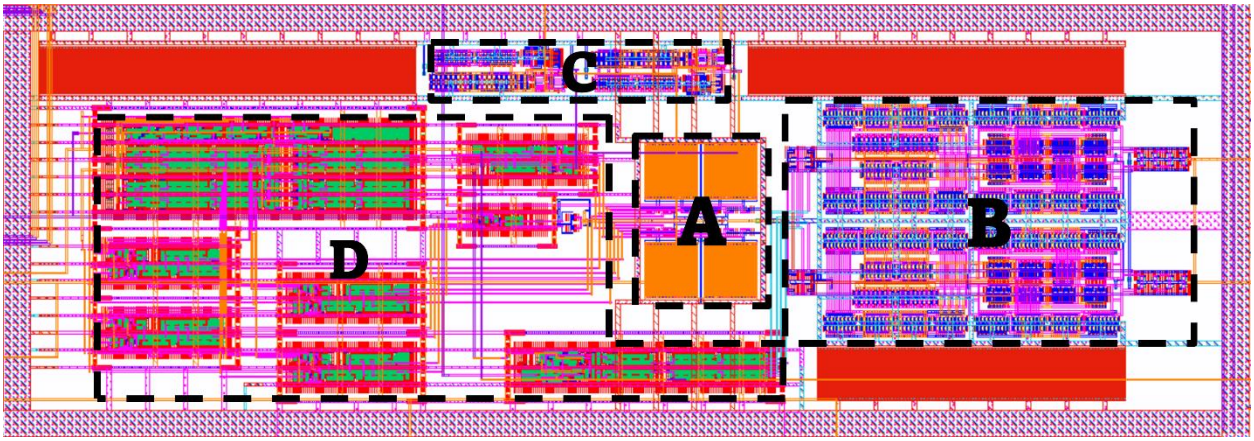


Figure A-11 Layout of the 22nm FD-SOI Coarse Measurement Stage
A) Sawtooth integrator
B) Sawtooth buffer pair
C) Highside and lowside comparators
D) Digital control logic

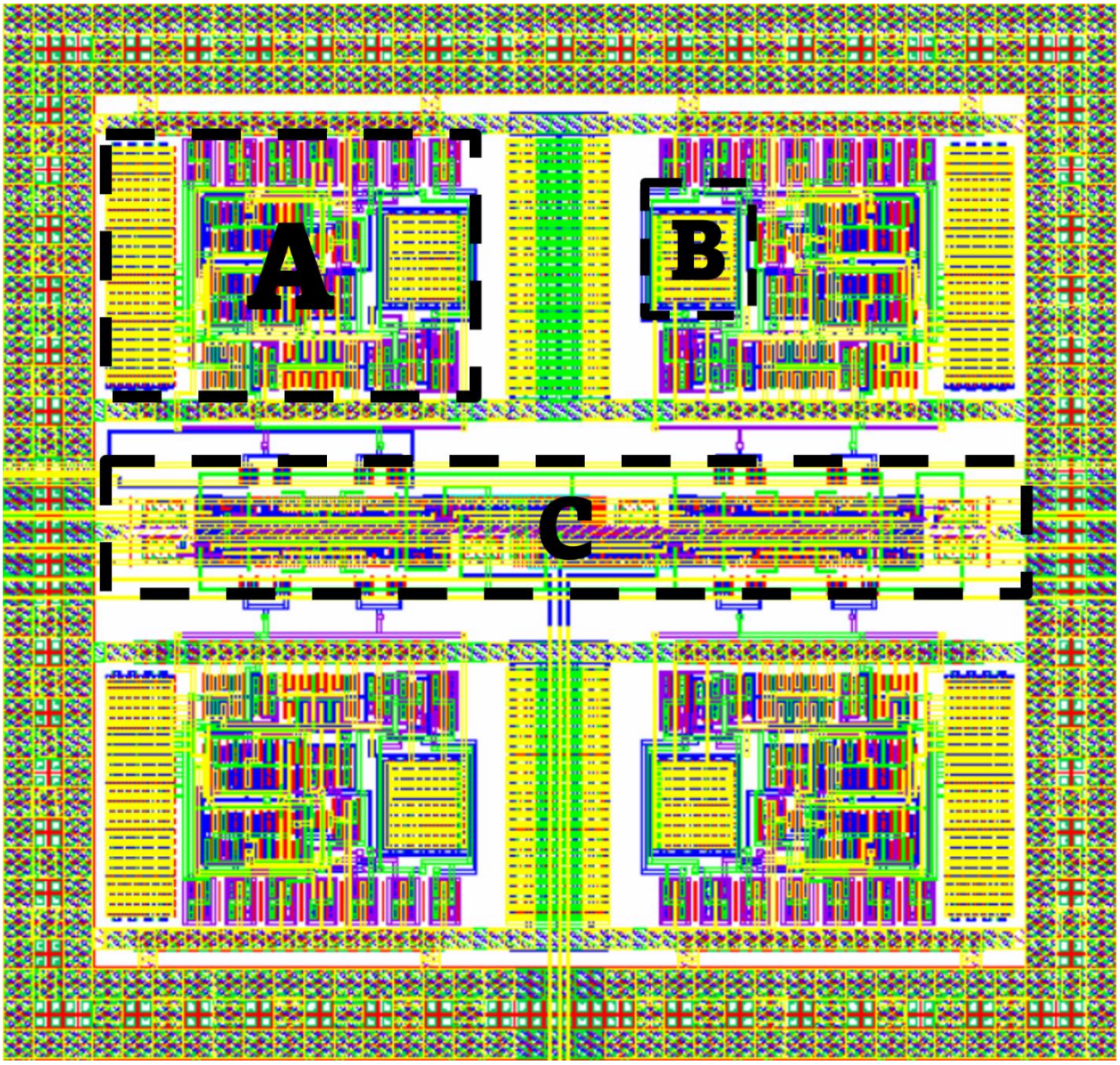


Figure A-12 Layout of four 45nm PD-SOI sample cells part of the Fine Measurement Stage
A) Sampler buffer
B) Storage capacitor
C) Digital control logic

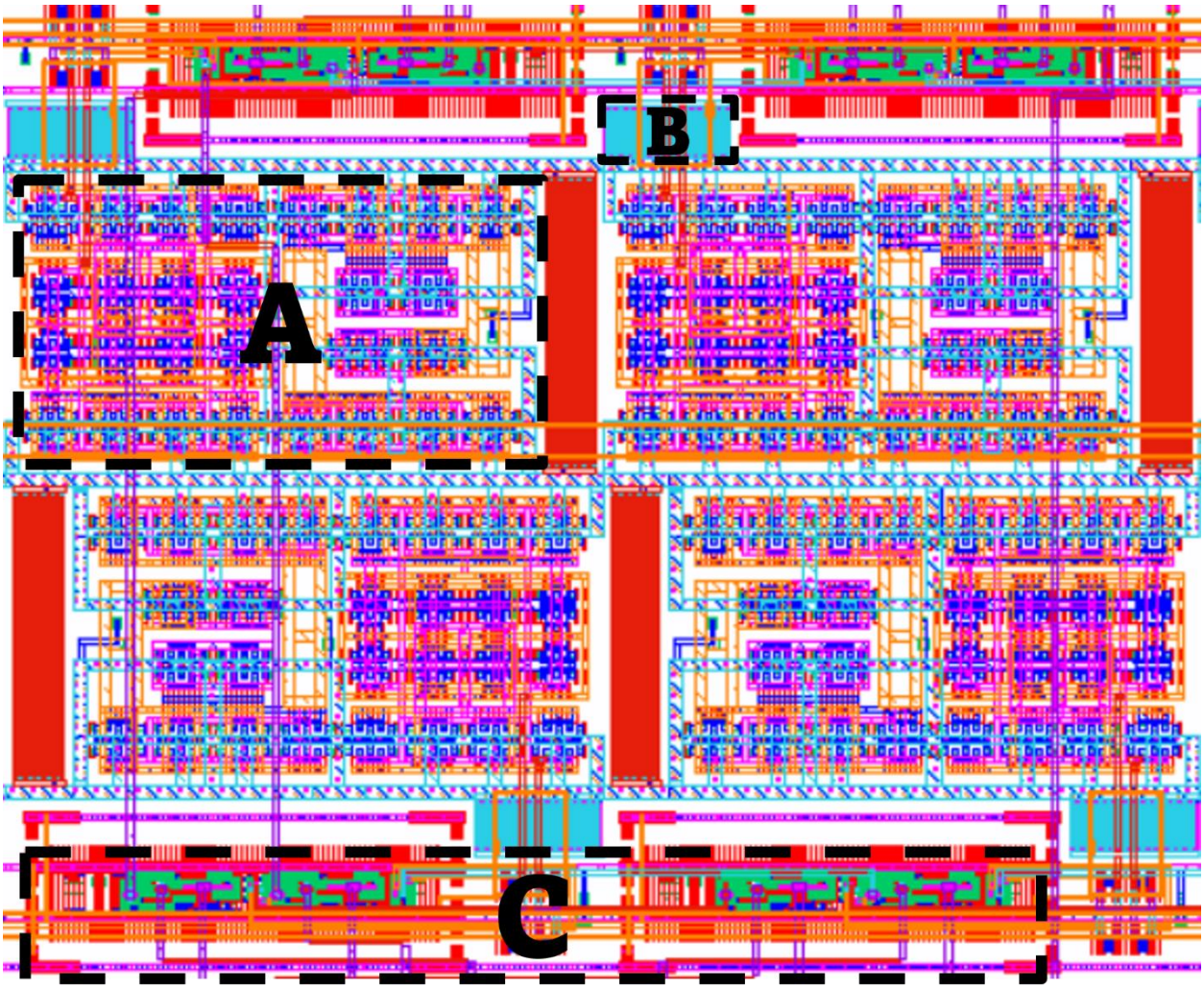


Figure A-13 Layout of four 22nm FD-SOI sample cells part of the Fine Measurement Stage
A) Sampler buffer
B) Storage capacitor
C) Digital control logic

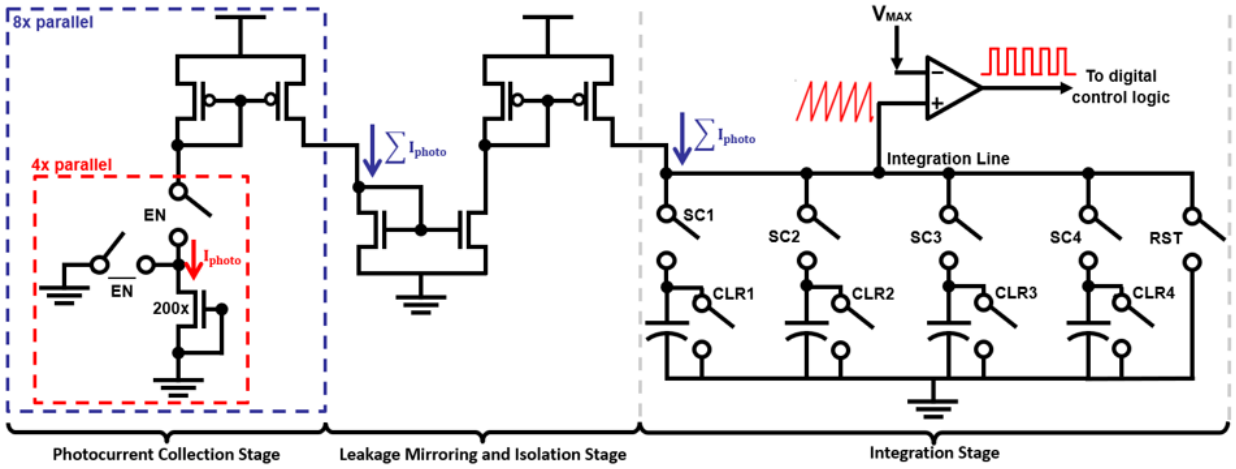


Figure A-14 High-level schematic of the Photocurrent Collection Stage, Leakage Mirroring and Isolation Stage, and Integration Stage in the 22nm FD-SOI implementation of the PMC. In the first stage, four target arrays may be placed in parallel with a current mirror by four switches, enabled with the "EN" bit, which is controlled off-chip. In the next stage, a pair of current mirrors are implemented to isolate to sensitive capacitors in the Integration Stage. In the final stage, the capacitors in the integrator charge, and when full, trigger a comparator that simultaneously discharges the Integration Line node and cycles the active capacitor to an empty one. V_{MAX} is controlled off-chip and may be adjusted to modulate the operating frequency of the integrator.

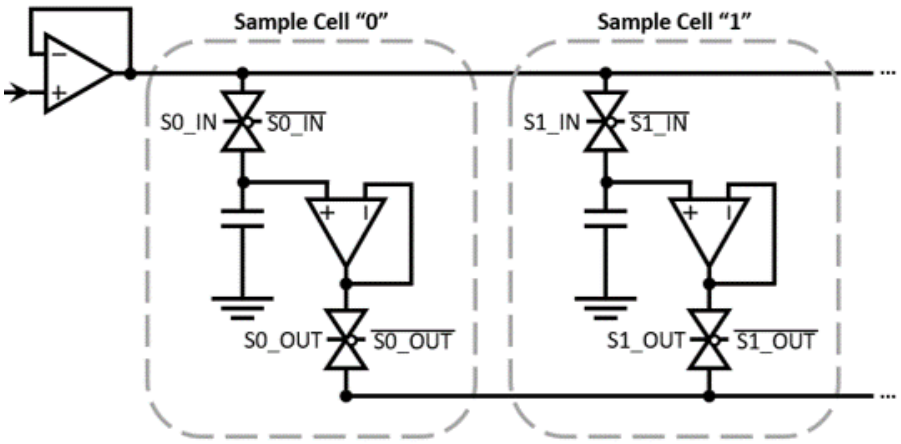


Figure A-15 High-level schematic of the sampler. The input op-amp buffers the Integration Line node from Figure A-14. Within each sample cell, a transmission gate controls a period of sampling, which charges a sample capacitor. Another transmission gate controls the output of an op-amp that buffers the stored capacitor voltage to an output line. Sequential logic controls the input and output transmission gates. Typically, a sampler is 256 sample cells in length.